Optical Digital Communication System Using LED and Photodiode

Project Report

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1. Abstract

A complete Free-Space Optical (FSO) communication link was designed and implemented for reliable ASCII-data transmission between microcontrollers. The system addresses the classical problem of photodiode saturation under ambient illumination by combining an AC-coupled analog front-end with a software-defined RZ-like modulation protocol. The receiver architecture includes a Transimpedance Amplifier (TIA), an AC-blocking stage, and an Active Low-Pass Filter to extract high-integrity data pulses from noisy optical environments. Bit detection and synchronization are fully implemented in software using dynamic baseline calibration, enabling stable operation across varying lighting conditions without hardware retuning.

The project demonstrates a low-cost, robust optical PHY suitable for academic and prototyping applications.

2. System Overview

The project implements a custom Physical Layer (PHY) over free-space visible-light propagation. The architecture applies a hybrid analog–digital co-design that shifts complexity from hardware to adaptive signal processing. The system consists of four main stages:

- **Transmitter:** High-brightness LED modulated via a controlled pulse pattern compatible with AC-coupled signal paths.
- **Channel:** Line-of-sight free-space optical propagation.
- **Receiver:** Multi-stage OpAmp AFE performing current-to-voltage conversion, AC-coupling, gain, and filtering.
- **Decoding Layer:** Dynamic thresholding and timing recovery handled by the microcontroller.

3. Hardware Design

3.1 Transmitter Stage

The transmitter uses a high-intensity LED driven by an NPN transistor for isolation and improved switching current.

Logic “1” is encoded using a short pulse rather than a sustained high level. This approach is essential for AC-coupled receivers: long static levels decay through coupling capacitors, while narrow pulses maintain integrity across multi-stage filtering. The selected RZ-like modulation ensures reliable decoding even through long bit sequences.

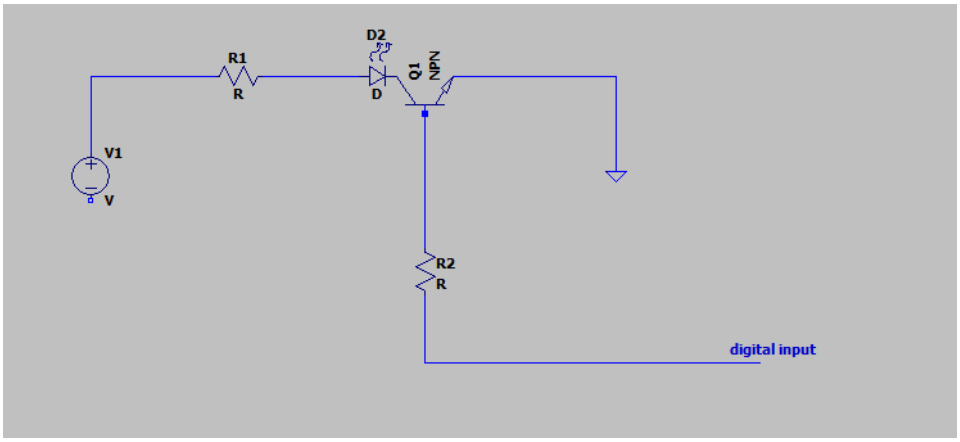

Figure 1: Transmitter Circuit Schematic

3.2 Receiver Analog Front-End (AFE)

The receiver was engineered to overcome the limitations of resistor-only photodiode circuits. It uses two cascaded OpAmp stages:

Stage A — Transimpedance Amplifier (TIA)

- Photodiode reverse-biased and connected to the inverting input.
- Feedback resistor: $100\,\mathrm{k}\Omega$, setting the transimpedance gain.
- Output represents total light intensity (signal + ambient).

This stage provides high sensitivity and excellent linearity.

Stage B — AC Coupling + Active Filtering

- **AC-Coupling Capacitor ($0.1\,\mu$F):** Blocks DC offsets from ambient illumination.
- **Active Gain / Low-Pass Filter:**
  - Gain $\approx 6.5\times$ using a $220\,\mathrm{k}\Omega/34\,\mathrm{k}\Omega$ network.
  - Feedback capacitor ($0.01\,\mu$F) forms an Active Low-Pass filter with cutoff frequency:

$$f_c = \frac{1}{2\pi R_5 C_3}$$

This stage suppresses high-frequency noise and improves SNR while preserving the data envelope.

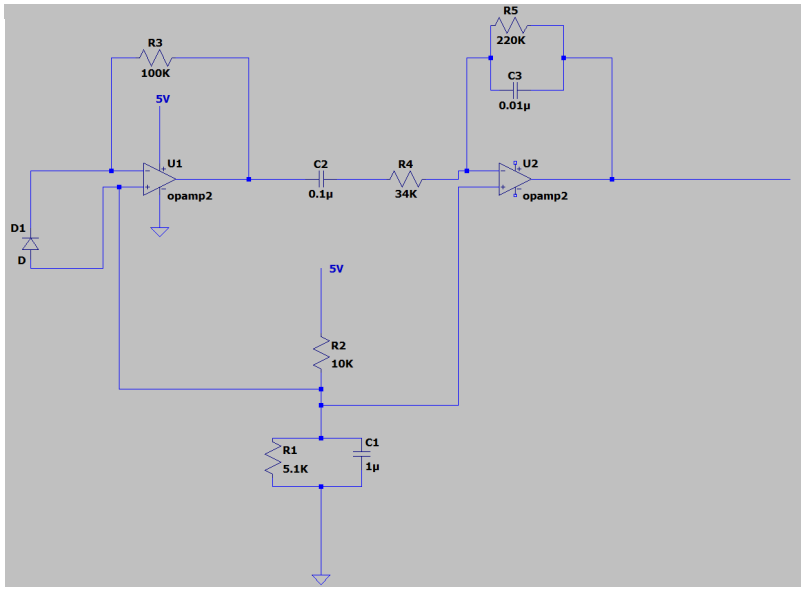

Figure 2: Receiver Circuit Schematic (TIA + Active Filter)

4. Software & Signal Processing

4.1 Modulation Protocol & Synchronization

A custom bit-banging protocol replaces UART timing to support the AC-coupled design:

- **Start Bit:** Wake-up pulse ensuring the receiver synchronizes to the incoming byte.
- **Data Bits:** Eight bits, sampled at each bit's midpoint.
- **Stop Bit:** Silent period.
- **Inter-Byte Guard Time (60 ms):** Prevents baseline drift and Inter-Symbol Interference (ISI) by allowing capacitors to discharge.

This creates a simple and predictable protocol optimized for optical transmission.

4.2 Receiver Signal Processing

Software-based bit discrimination replaces a hardware comparator:

1. **Baseline Calibration:** On boot, 100 samples are averaged to determine the ambient noise floor (`avg_val`).
2. **Adaptive Threshold:** Logical "1" is detected when:

$$\text{ADC} > \text{avg\_val} + \text{THRESHOLD}$$

3. **Timing Alignment:** After Start Bit detection, the receiver waits 1.5 bit periods to sample at the optimal point of the first data bit.

This adaptive approach provides robustness under widely varying lighting conditions.

5. Testing and Results

5.1 Experimental Setup

The system was implemented on breadboards using an Arduino Uno for both the transmitter and receiver. The physical setup allowed for easy adjustment of the alignment and distance between the LED and photodiode.

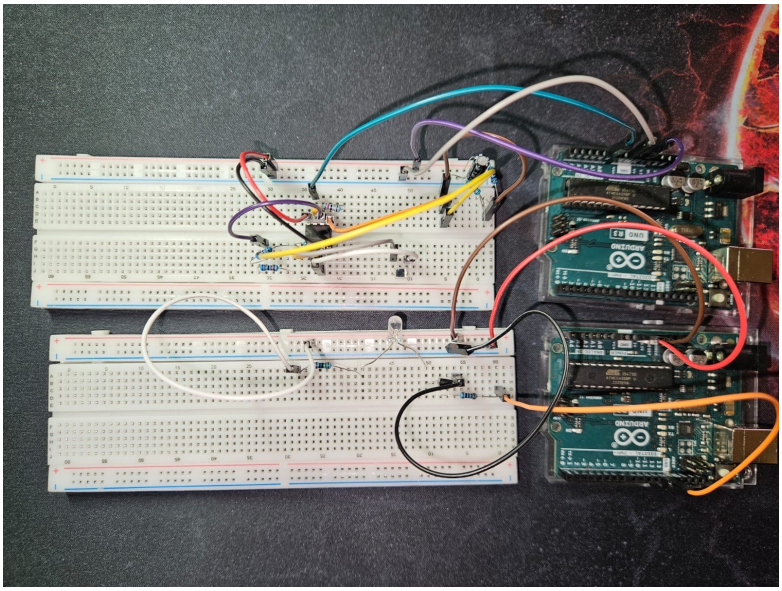

Figure 3: Physical Experimental Setup on Breadboards

5.2 Performance Metrics

- **Ambient Immunity:** The AC-coupled architecture successfully rejected slow-changing illumination, operating reliably in darkness, indoor lighting, and partial sunlight.
- **Noise Performance:** The active filter significantly reduced high-frequency interference, producing clean oscilloscopic signatures.
- **Data Integrity:** Reliable ASCII transmission achieved at 15 ms/bit (≈ 66 baud) with no observed drift or false triggers over extended sequences.

6. Conclusion

This project demonstrates a fully functional and efficient digital optical communication system integrating optoelectronics, analog filtering, and embedded software. The combined TIA, AC coupling, Active Filtering, and adaptive decoding pipeline establishes a highly robust communication link using low-cost components. The system highlights practical skills in mixed-signal circuit design, embedded C++, timing-critical protocols, and sensor-to-digital signal conditioning—core competencies in real-world communication and embedded systems engineering.