VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)
CHENNAI

Reg. Number:	

Continuous Assessment Test (CAT) – II - October 2024

Programme	:	B.Tech CSE, B.Tech CSE (Specializations) and B.Tech Electronics and Computer Engineering (BLC)	Semester	:	FALL 24-25
Course Code & Course Title	:	BCSE205L & Computer Architecture and Organization	Class Number	:	CH2024250101393 CH2024250101392 CH2024250102314 CH2024250102677
Faculty	:	Dr. Vaidehi Vijayakumar Dr. Kavitha J C Dr. Aswiga R V Dr. Arivarasi	Slot	:	F1 +TF1
Duration	:	1.30 Hrs	Max. Mark	:	50

Q. No.	Sub-division	Question Text	Marks

1		You are required to analyze the working of an architecture that makes use of a single internal processor bus and another that makes use of three buses. Illustrate which architecture is better by deriving the sequence of control steps required to execute the following instructions. List the data path components involved in the execution of the below 2 instructions
		
		MUL [R4], R5, R6 # The registers R5 and R6 have the source operands. The computed result is to be stored at a memory location held in Register R4.
		
		MOV [R4], R5 #The content residing at a memory location held in register R4 is to be moved to Register R5.
			10

2		Consider two different implementations of the same instruction set architecture with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 20% class A, 20% class B, 50% class C, and 10% class D with a clock rate of 3 GHz for P1 and clock rate of 2.5 GHz for P2. The instructions are divided into four classes according to their CPI as shown below.	

Instruction Class	CPI of Processor 1 (P1)	CPI of Processor 2 (P2)
A	1	1
B	2	2
C	3	3
D	3	2

i) Identify which implementation is faster? Why ? [4 Marks]
ii) What is the global CPI for each implementation? [3 Marks]
iii) Find the clock cycles required in both cases. [3 Marks]

10

3		Given a 4-way set associative cache with 256 blocks, using 4 bits to represent the offset and 8 bits for the tag and employ LRU (Least Recently Used) as the replacement policy. Using the given parameters for the following main memory addresses 184, 131, 075, 132, 197, 056, 189, 205, 222, 171, 153, and 076 i) Compute the cache line number [4 Marks] ii) The block number within the line, and [3 Marks] iii) Determine the offset within the block [3 Marks]	10
4		Illustrate the layout and organization of the 1MB x 16 RAM module using 64K x 8 DRAM chips. i) Calculate the number of chips, address bits, the size of the decoder. [6 Marks] ii) Create an address mapping table for the resulting 64K x 8 DRAM chips organized in the 4x4 grid. [4 Marks]	10
5		Comment on the trueness of the following statements and justify your answers. Use diagrams to elucidate your claim. i) In case of data transfer using DMA, both the CPU and the DMAC act as the bus masters at the same time. [5 marks] ii) The CPU uses polling to determine the source of the interrupt when a device generates a vectored address in case of Daisy chaining method. [5 marks]	10

********All the best**********