VIT
Vellore Institute of Technology

Reg. No. :

Final Assessment Test (FAT) - JUNE/JULY 2023

Programme	B.Tech.	Semester	Winter Semester 2022-23
Course Title	DIGITAL SYSTEMS DESIGN	Course Code	BECE102L
Faculty Name	Prof. Angalaeswari S	Slot	B2+TB2
		Class Nbr	CH2022232300556
Time	3 Hours	Max. Marks	100

Section 1 (10 X 10 Marks)
Answer All questions

01. A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations. [10]

(i) A is True , B is False

(ii) A is False, C is True

(iii) A, B, C are False

(iv) A, B, C are True

(a)Write the Truth table for F. Use the convention True=1 and False = 0.

(b) Write the simplified expression for F in SOP form.

(c) Write the simplified expression for F in POS form.

(d)Draw logic circuit using minimum number of 2-input NAND gates.

02. Determine a minimal SOP and POS expression for the following Boolean functions together with the don't care conditions d using four variable k map. Note that the don't care conditions have to be set to one value for the SOP solution and the other for the POS expression. [10]

$F(w,x,y,z) = \Sigma(1,9,10,11,12,13,14,15)$

$d(w,x,y,z) = \Sigma(3,5,8)$

03. Write the Verilog code for a parity generator circuit and draw its logic diagram. [10]

04. You wish to detect only the presence of the codes 1010,1100,0001 and 1011. An active HIGH output is required to indicate their presence. Develop the minimum decoding logic with a single output that will indicate when any one of these codes is on the inputs. For any other code, the output must be low. [10]

05. Discuss the concept of an adder whose carry propagation delays are eliminated. Draw its block diagram. [10]

06. Design a non- sequential synchronous counter using D Flip- Flops to count the sequence 6, 0, 7,1,3,6,0,7,1,3, -- so on. The loop for the undesired states must also be designed. [10]

07. (i) The initial contents of the 4-bit serial-in-parallel out, right-shift, Shift Register shown in the given Figure 1 is 0110. After six clock pulses are applied, contents of the Shift Register will be [10]

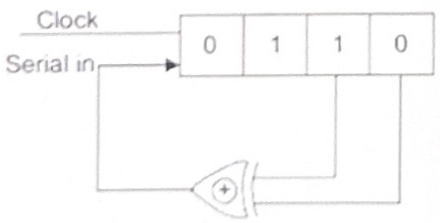

Figure 1

Explain and draw the necessary register diagram for every clock pulse. (5 marks)

(ii) Explain the working of a 3 bit Asynchronous up-counter. Write a Verilog HDL code for the same. (5 marks)

08. A sequence detector accepts as input a string of bits: either 0 or 1. Its output goes to 1 when a target sequence has been detected. Design a serial sequence detector which allows "overlapping" and detects the pattern "0101". Draw the respective state diagram, state table, transition table, derive the characteristic equations and implement the FSM using JK flip flop. [10]

09. Construct a Moore machine that prints 'a' whenever the sequence "1001" is encountered in any input binary string. Draw the respective state diagram, state table, transition table, derive the characteristic equations and implement the FSM using D flip flop. [10]

10. Implement the following boolean expression using Programmable Logic Array (PLA) [10]

$$F_1(x, y, z) = \sum_{m}(1,3,4,5,7)$$

$$F_2(x, y, z) = \sum_{m}(1,4,5,6)$$