CHENNAI

Continuous Assessment Test (CAT) – II – October 2024

Programme	:	B. TECH	Semester	:	FALL 2024-25
Course Code & Course Title	:	BCSE205L & Computer Architecture and Organization	Class Number	:	CH2024250101444 CH2024250102663 CH2024250100888 CH2024250100533
Faculty	:	Dr. R. M. Bhavadharini Dr. R. Madura Meenakshi Dr. Kaja Mohideen A Dr.A.R.Revathi	Slot	:	A2+TA2
Duration	:	90 Minutes	Max. Mark	:	50

Q. No.	Sub-division	Question Text	Marks
1		Consider an 8-way set associative mapped cache of size 512 KB with block size 1 KB. There are 7 bits in the tag. Find a) Number of Bits in Block Offset, Number of Lines in Cache (2 marks) b) Number of Sets in Cache (2 marks) c) Number of Bits in Physical Address (2 marks) d) Size of main memory (2 marks) e) Tag directory size (2 marks)	10
2		a) Analyse the following time steps, Explain the meaning line-by-line and identify to which instruction it belongs. (6 marks) 1 PCout, MARin, Read, Select4, Add, Zin 2 Zout, PCin, Yin, WMFC 3 MDRout, IRin 4 Address field of IRout, MARin 5 R1out, MDRin, Write 6 MDRoutE, WMFC, END. b) For the instruction identified, write down the control sequence steps for the multipath Control Unit. (4 marks)	10
3		A computer employs RAM chips of 1024 x 8 and ROM chips of 1024 x 8. The computer system needs 2k *8 bytes of RAM, 2k *8 bytes of ROM, and four interface units with four registers in each. A memory - mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers.	10

		a) How many RAM and ROM chips are needed? (2 marks) b) Draw a memory-address map for the system. (4 marks) c) Give the address range in hexadecimal for RAM, ROM, and interface. (2 marks) d) Develop a chip layout for the above said specifications. (2 marks)	
4		Write a combined micro routine that can implement that BGT (Branch if > 0), BPL (Branch if plus), and BR (Branch Unconditionally) instructions. The branch conditions, for the BGT and BPL instructions are Z + (N XOR V) = 0 and N = 0, respectively. What is the total number of micro instructions required?	10
5		In a real-time traffic control system, multiple events require the central processor to handle interrupts to ensure smooth traffic flow. The system uses a vectored interrupt structure with prioritized events: Emergency Vehicle Detection (highest priority), Pedestrian Crossing Request, and Traffic Light Timer Update (lowest priority). Each interrupt has an overhead of 5 microseconds for context switching, and handling the interrupt takes an additional 10 microseconds. Consider the following sequence of events: 1. At t = 0 µs, the Traffic Light Timer Update triggers an interrupt. 2. At t = 3 µs, an Emergency Vehicle is detected, triggering an interrupt. 3. At t = 5 µs, a Pedestrian Crossing Request triggers an interrupt. 4. At t = 10 µs, another Traffic Light Timer Update triggers an interrupt. a) Show how each interrupt is prioritized and handled by the system. (4 Marks) b) Discuss how the vectored and prioritized interrupt structure affects the response time of lower-priority events. (6 marks)	10

********All the best**********