VIT®

Vellore Institute of Technology

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Reg. No. :

## Final Assessment Test(FAT) - Nov/Dec 2024

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| Programme | B.Tech. | Semester | Fall Semester 2024-25 |
| Course Code | BCSE205L | Faculty Name | Prof. Linda Joseph |
| Course Title | Computer Architecture and Organization | Slot | E1+TE1 |
| | | Class Nbr | CH2024250100676 |
| Time | 3 hours | Max. Marks | 100 |

**General Instructions**

- Write only Register Number in the Question Paper where space is provided (right-side at the top of this) not write any other details.

**Course Outcomes**

1.Differentiate Von Neumann, Harvard, and CISC and RISC architectures. Analyze the performance of machine with different capabilities. Recognize different instruction formats and addressing modes. Validate efficient algorithm for fixed point and floating point arithmetic operations.

2.Explain the importance of hierarchical memory organization. Able to construct larger memories. Analyze and suggest efficient cache mapping technique and replacement algorithms for given design requirements. Demonstrate hamming code for error detection and correction.

3.Understand the need for an interface. Compare and contrast memory mapping and IO mapping techniques. Describe and Differentiate different modes of data transfer. Appraise the synchronous and asynchronous bus for performance and arbitration.

4.Assess the performance of IO and external storage systems. Classify parallel machine models. Analyze the pipeline hazards and solutions.

### Section - I

**Answer all Questions (10 × 10 Marks)** *M - Marks

| Q.No | Question | *M | CO | BL |
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| 01. | (i) Show the step by step transitions in different registers in an architecture that uses a shared memory unit. Assume that the instructions start at memory location 1000H. The assembly code is provided as follows: (4 marks)<br>LOAD A,[600]<br>LOAD R1,[601]<br>CMP A,R1<br>JMP LABEL1<br>MOV A,R1<br>ST R2,A<br>HLT<br>LABEL1: A holds the greater number<br>Assume the memory locations 600 and 601 to be containing 10 and 20 respectively.<br>(ii) Suggest and discuss a model that could improve the execution of the above instructions with a neat diagram. (4 marks)<br>(iii) Indicate the pros and cons of both the architectures.(2 marks) | 10 | 1 | 3 |

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| 02. | A data centre has 8 storage blocks with each storage block having 12 storage rows. From the given data, assume the highest number to be the multiplicand.<br>(i) Calculate the total storage capacity using the bit pair recoding method. (7 marks)<br>(ii) Enumerate the pros and cons of the recoding method with that of the booth's multiplication algorithm. (3 marks) | 10 | 1 | 3 |
| 03. | i) Identify the addressing mode used in the following instructions and provide a brief description of each. (5 marks)<br>ADD R1, #10;<br>MOV R1, R2;<br>MOV A, 0x0050;<br>MOV A, @R0;<br>MOV A, 0x2000[R1];<br>MOV A, [R1+R2];<br>JMP PC+4;<br>PUSH R1;<br>MOV A, @PTR;<br>MOV A, (R1) +<br>(ii) Determine the operand's address in memory, assuming an initial memory location of 2000H wherever relevant. Consider R0=5000H, R1and R2 to hold 200 and 1200H respectively, PC=2018H, PTR=3000H (5 marks) | 10 | 1 | 3 |
| 04. | (i) Design a multi bus Data path for computing the instruction MUL R1,R2,R3 with the following specifications: A register bank consisting of 8 registers, each register having a capacity to hold 32 bits, an ALU, a memory unit, and a MUX. Show the control signals that are needed by the multi bus. (4 marks)<br>(ii) Determine the control sequences for (6 marks)<br>LOAD R1, 4(R2);<br>ADD R1, R2, R3;<br>BEQ R3,R2 | 10 | 2 | 3 |
| 05. | Consider a 16 bytes direct mapped cache with a block size of 4 bytes. Assuming a byte addressable memory, the cache uses the following sequence of memory requests<br>0,1,2,3,4,5,6,7,0,1,4,5,8,9,12,13<br>(i) Determine the number of bits needed to specify the location of a byte within a cache block. ( 2 marks)<br>(II) Simulate the sequence of memory addresses and calculate the number of hits and misses. (4 marks)<br>(iii) If a fully associative cache is used and a LRU replacement policy to evict a cache block is utilized, analyze your results by determining the hit rate and the miss rate. (4 marks) | 10 | 2 | 3 |
| 06. | A system considers two 16 bit floating point numbers with 6-bit exponent and a 9-bit normalized fractional mantissa including the sign bit. The base of the scale factor is 2 and the exponent is represented in excess-31 format.<br>(i) Add the numbers A:30.0 and B:35.0 by converting the numbers to their floating point format. (3 marks)<br>(ii) Determine your results before and after normalization. (4 marks)<br>(iii)Show the status register updates. (3 marks) | 10 | 3 | 3 |

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| 07. | Three devices X, Y and Z are connected to a computers' bus and use the interrupt control for I/O transfers. Device X has the highest priority, device Y has a medium priority and device Z has the lowest priority. Interrupt nesting is allowed only for device Z, such that X and Y cannot interrupt each other but Z can interrupt both X and Y. Draw relevant diagrams wherever necessary.<br>(i) Suppose the computer has one interrupt request line shared by all the three devices. Implement a solution that respects the priority by satisfying the nesting rules. (5 marks)<br>(ii) if the computer has two interrupt request lines, INTR1 and INTR2, where INTR1has a higher priority than INTR2, Suggest how you would connect these devices to the interrupt lines and describe the conditions under which interrupts are enabled or disabled for each device. (5 marks) | 10 | 3 | 4 |
| 08. | A computer processor executes instructions with a 5-stage pipeline. Each stage takes 1 cycle to complete. For the given instructions, R1=R2+R3; R4=R1+R5; R6=R4+R7<br>(i) Identify how the processor will execute with and without pipelining concept, assuming there's no hazard or stall in this pipeline. Discuss with relevant answers. (4 marks)<br>(ii) Calculate the speedup gained by using pipelining. (3 marks)<br>(iii)If a 1 cycle stall (a data hazard) is inserted after the first instruction, how would it affect the total number of cycles and the speedup. (3 marks) | 10 | 4 | 4 |
| 09. | A bit stream 0110011100 is transmitted using the standard detection method,<br>(i) Apply the appropriate error detection method and determine the actual bit string transmitted. (5 marks)<br>(ii) Suppose the second bit from the left is inverted during the transmission, demonstrate how the receiver would detect this error. (5 marks) | 10 | 2 | 3 |
| 10. | A multimedia production company handles large volumes of video files and requires a storage solution to manage high-speed access and editing of these files. The company also needs to back up archived video projects that need less frequent access but must be stored safely and reliably.<br>(i) For the video editing storage system, recommend a suitable RAID level that ensures fast read/write access for editing purposes. Discuss the advantages and potential drawbacks of this RAID configuration in the context of high-speed, data-intensive operations. (5 Marks)<br>(ii) For the archival storage system that holds completed projects, recommend a suitable hybrid RAID level that offers a balance between redundancy, reliability, and storage capacity. Explain how this hybrid RAID configuration would provide data protection and the ability to recover from potential disk failures. (5 Marks) | 10 | 4 | 4 |

**BL-Bloom's Taxonomy Levels - (1.Remembering, 2.Understanding, 3.Applying, 4.Analysing, 5.Evaluating, 6.Creating)**

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