CHENNAI

Continuous Assessment Test (CAT) – I - JAN 2025

Programme	:	B.Tech CSE & B.Tech CSE all Specializations	Semester	:	Winter Sem 24-25
Course Code & Course Title	:	BCSE205L&Computer Architecture and Organization	Class Number	:	CH2024250502109 CH2024250502262 CH2024250502263 CH2024250502300
Faculty	:	MADURA MEENAKSHI R , SMRITHY, NIVEDITA M, and V.MANJULA	Slot	:	E1+TE1
Duration	:	90 minutes	Max. Mark		50

Answer all questions

Q. No	Sub Sec.	Description	Marks
1		Write an Assembly language program for the following expression using IAS computer Instruction set, A= (B-C). Consider that the data values are stored in memory location starting from 600 onwards and the program is stored from memory location 200 onwards. Assume that value of B is 5, C is 2. Interpret the flow of execution in IAS Computer for the above instructions using the following representation in a step by step manner. Also represent the register transfer code for each step. PC MAR MBR IR IBR	10
2	a)	A company is designing an embedded system for a real-time traffic monitoring device that collects data from sensors, processes it, and provides immediate feedback to traffic lights and alert systems. The system must handle simultaneous data acquisition and instruction execution efficiently without delays. Discuss the benefits of having separate memory for instructions and data in the context of real-time traffic monitoring. Illustrate the suitable architecture with a block diagram and describe its components. [5 Marks]	5
	b)	In a real-time application scenario, consider the deployment of a system that requires efficient processing of a large volume of sensor data from various IoT devices. The system aims to monitor and respond to environmental conditions in smart cities. Compare and contrast how RISC and CISC architectures would address the execution challenges and requirements of this real-time problem.[5 Marks]	5
	c)	Design the Register file which consists of 64 registers of size 8 bits each.	5

		Describe the process of given operation R3=R1+R5 using register file.	
3	a)	Consider you are an architect at AMS Computers and you are assigned with the task of designing an algorithm for two's complement multiplication which works for both unsigned and signed integers. Show the working of your algorithm for $(26)_{10}$ x $(-15)_{10}$ with all intermediate steps. a) Show the step-by-step process [5 Marks] b) Validate the correctness of the result. [2 Marks] c) Find the decimal equivalent of the content of the accumulator at the end of the third iteration.[3 Marks]	15
		Perform arithmetic operations of **Sign magnitude numbers** with eight bits to accommodate each number together with its sign. Determine if there is an overflow by checking its carry into and out of sign bit position. [5 Marks] a) $(-25)_{10} + (-45)_{10}$ b) $(-25)_{10} - (+45)_{10}$	
4		As an architect at MARS Computers, design an algorithm for performing given floating-point binary operations. Demonstrate the operation using the example $(105.25)_{10} - (50.5)_{10}$. Represent and carry out all calculations in IEEE single precision binary format.	10

**********All the best **********