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VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)
CHENNAI

Reg. Number:	

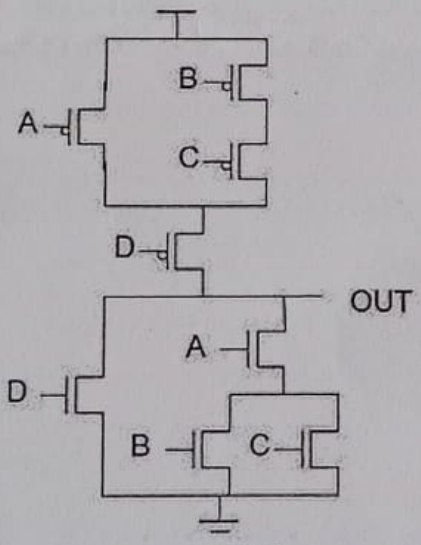
Continuous Assessment Test(CAT) – I /II - JAN 2024

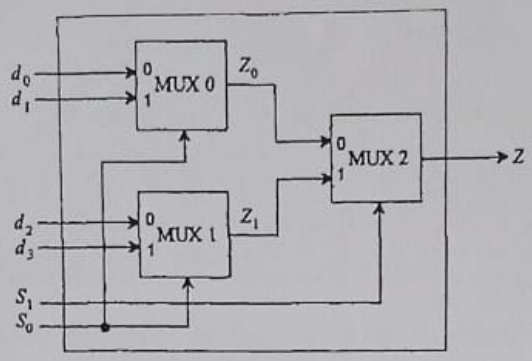
Programme	:	B.Tech (ECE/ECM/EVD)	Semester	:	WS 2023-24
Course Code & Course Title	:	BECE102L Digital System Design	Class Number	:	CH2023240501131 CH2023240501151
Faculty	:	Dr A Anita Angeline & Dr A Prathiba	Slot	:	D1 +TD1
Duration	:	90 Minutes	Max. Mark		50

General Instructions:

- Write only your registration number on the question paper in the box provided and do not write other information.
- Only non-programmable calculator without storage is permitted

Answer all questions

Q. No	Sub Sec.	Description	Marks
1.		a) For $F1 = x(\bar{y}\,\bar{z} + yz)$, determine $\overline{F1}$. b) Simplify $F2 = ABCD + \bar{A}\,BD + AB\bar{C}D$ c) Determine the functionality of the Static CMOS implementation depicted in Fig.1, and identify the path output for A=1; B=C=D=0  Fig.1	[10]
2.		Derive the circuit consisting only of two-input NAND gates for the function f (x1, x2, x3, x4) = ∑m(0, 1, 2, 3, 4, 6, 8, 9, 12). Assume that the input variables are available in both uncomplemented and complemented forms.	[10]

3.		Design the hardware depicted in Fig.2, using Verilog HDL code and write the testbench for the schematic (top module).  Fig.2	[10]
4.		a) Considering A0, A1, B0, B1 as single bit data, configure a circuit to implement F3 = (A1+B1) + (A0+B0) using appropriate adders and justify your design. b) Considering $W, X, Y. Z$ as single bit data, design a digital circuit to implement F4 = $\bar{W}\bar{X}\bar{Y}\bar{Z} + 1$ using appropriate gates and adder units and justify your design.	[10]
5.		Implement the Boolean function $F4 = \sum(0,2,5,7,11,14)$ using 8 X1 multiplexer.	[10]
		**********All the best **********	