VIT
Vellore Institute of Technology
CHENNAI

Reg. Number:	

Continuous Assessment Test (CAT) – I - August 2024

Programme	:	B.Tech CSE, B.Tech CSE (Specializations) and B.Tech Electronics and Computer Engineering (BLC)	Semester	:	FALL 24-25
Course Code & Course Title	:	BCSE205L & Computer Architecture and Organization	Class Number	:	CH2024250101393 CH2024250101392 CH2024250102314 CH2024250102677
Faculty	:	Dr. Vaidehi Vijayakumar Dr. Kavitha J C Dr. Aswiga R V Dr. Arivarasi	Slot	:	F1 +TF1
Duration	:	1.30 Hrs	Max. Mark	:	50

Q. No.	Sub-division	Question Text	Marks
1		Consider a real time scenario of developing a mobile application that requires efficient execution of multimedia tasks, such as video playback and image processing, on a smart phone. The application must run smoothly without draining the battery quickly.	
	a)	Which architecture would you prefer for the smart phone's processor, and why? [3 Marks]	
	b)	How does the chosen architecture influence the efficiency of multimedia processing and battery life? Explain with architecture diagram. [7 Marks]	10
2	a)	A simplified register file with 2 read ports and 1 write port has 9 registers (R0 to R8) with 8 bits each. Assuming that R0 = $(11001101)_2$ and R1= $(11010101)_2$, How the operations R2 =R1 X R0 and R3 = R1 +R0 is processed and stored. [6 Marks]	
	b)	Explain the above operation with appropriate architecture diagram.[4 Marks]	10
3	a)	Illustrate how the processor will perform multiplication of two numbers $(+27)_{10}$ and $(-11)_{10}$ through Modified Booth's algorithm method. [8 marks]	
	b)	Find the decimal equivalent of the accumulator at the end of second iteration [2 marks]	10
4	a)	Consider the numbers $(73.625)_{10}$ and $(22.75)_{10}$, Perform floating point addition and represent the result in single precision format. [5 Marks]	
	b)	Perform floating point subtraction and represent the result in half precision format. [5 Marks]	10

5		Identify the addressing modes and calculate the effective address of the operand R5 after executing each of the given instructions, considering the initial values R6 = 3000, SI = 3500 (Source Index Register), and PC = 1500, with the following memory address-value pairs
		
		Instructions:
		STA R5, #2000
		LDA R5, [1500]
		LDA R5, [R6]
		LDA R5, 500[SI]
		STA R5, 100[PC]
			10

Memory	Value
1500	4000
1600	9000
2000	10000
2500	11000
3000	12000
3500	13000
4000	13500

********All the best**********