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Vellore Institute of Technology

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Reg. No. : 23BLC1297

Final Assessment Test(FAT) - Nov/Dec 2024

Programme	B.Tech.	Semester	Fall Semester 2024-25
Course Code	BCSE205L	Faculty Name	Prof. Vaidehi Vijayakumar
Course Title	Computer Architecture and Organization	Slot	F2+TF2
		Class Nbr	CH2024250101399
Time	3 hours	Max. Marks	100

General Instructions

- Write only Register Number in the Question Paper where space is provided (right-side at the top) & do not write any other details.

Course Outcomes

1. Differentiate Von Neumann, Harvard, and CISC and RISC architectures. Analyze the performance of machine with different capabilities. Recognize different instruction formats and addressing modes. Validate efficient algorithm for fixed point and floating point arithmetic operations.
2. Explain the importance of hierarchical memory organization. Able to construct larger memories. Analyze and suggest efficient cache mapping technique and replacement algorithms for given design requirements. Demonstrate hamming code for error detection and correction.
3. Understand the need for an interface. Compare and contrast memory mapping and IO mapping techniques. Describe and Differentiate different modes of data transfer. Appraise the synchronous and asynchronous bus for performance and arbitration.
4. Assess the performance of IO and external storage systems. Classify parallel machine models. Analyze the pipeline hazards and solutions.

Section - I

Answer all Questions (10 × 10 Marks) *M - Marks

Q.No	Question	*M	CO	BL
01.	In a research lab using a Von Neumann architecture-based computer system, researchers are facing slow performance while analyzing large datasets. The system suffers from significant delays during data analytic algorithms that require frequent memory accesses and intensive computations, causing the CPU to remain idle for long periods while waiting for data retrieval (i) Identify the potential bottlenecks in the execution cycle contributing to this issue. Justify your answer with neat labelled diagram that impacts instruction fetching delays, and I/O operations (5 Marks) (ii) Propose specific optimizations for the above identified bottlenecks and describe the possible ways to enhance efficiency and caching mechanisms with a neat architecture (5 Marks)	10	1	3

02.	A digital signal processing system requires efficient multiplication of binary numbers to handle audio data in real time. (i) Implement Booth's Algorithm to multiply $A = -6_{10}$ (Multiplicand) and $B = -3_{10}$ (Multiplier) . Show each step of the algorithm, including partial products, shifts, and any necessary calculations. (6 Marks) (ii) Provide the final result of the multiplication in both binary and decimal form, and briefly explain how Booth's Algorithm optimizes the multiplication process for signed numbers. (4 Marks)	10	1	5
03.	A robotic device needs to distribute 7 packets evenly across 3 bins. (i) Using the Non restoring division algorithm, determine the quotient, or the number of packets that will go into each bin. Show each step of your calculation.(7 Marks) (ii) Using the same algorithm, calculate the remainder or the number of packets left over that do not fit into the bins. (3 Marks)	10	1	5

04.	A computer system is designed to execute the following simple assembly language program that performs basic arithmetic operations:
	LOAD R1, 0x1000
	LOAD R2, 0x1004
	ADD R3, R1, R2
	MUL R4, R1, R2
	STORE R3, 0x1008
	STORE R4, 0x100C
	OUTPUT R3
	(i) Sketch a simplified Datapath that includes the necessary components (such as registers, ALU, memory, and I/O interfaces) to support the operations in the assembly program. Label each component and indicate how data flows between them during execution. (3 Marks)
	(ii) Specify the control signals required for each step, detailing how the control unit coordinates the flow of data through the Datapath (7 Marks)
		10	1,2	4

05.	A system calculates the final amount for an order by first adding the prices of two items (₹8 and ₹4), then multiplying the result by a discount factor of 2. Finally, it adds a fixed processing fee of ₹5 to the discounted total. (i) Write the instructions to compute the final amount using three-address and Two-address instruction formats. (4 Marks) (ii) Write the instructions to compute the discounted total using one-address, and zero-address instruction formats (6 Marks)	10	1	3
06.	A direct-mapped cache consists of a total of 512 blocks. The main memory contains 16384 blocks, each consisting of 64 words. (i) How many bits are there in each of the TAG, INDEX, and WORD fields? (4 Marks) (ii) What is the size of the cache memory? (2 Marks) (iii) For the following main memory block requests: 15, 102, 20, 6, 33, 16, 250, 240, 520, 240, 128, 16, 96, 64, 146, 184, calculate the number of misses and the miss ratio if the replacement strategy is Least Recently Used (LRU). (4 Marks)	10	2	5

07.	In a smart home environment, a multi-device communication system is designed to manage various tasks such as lighting control, security monitoring, climate control, and entertainment management. Four devices—A, B, C, and D—are assigned unique IDs and generate specific interrupt signals to request access to a shared communication bus. Device A (ID 7) generates the interrupt signal 0111, Device B (ID 13) generates 1101, Device C (ID 9) generates 1001, and Device D (ID 14) generates 1110. (i) Discuss how the daisy chaining concept is used for gaining access to the bus if multiple devices attempt to transmit simultaneously. (5 Marks) (ii) If the system employs a polling strategy instead of daisy chaining, describe which device would be granted access first, and what are the advantages and disadvantages of using polling in this scenario? (5 Marks)	10	3	4
08.	In a data transmission system, a server needs to send a data packet of 8 bits: 11010101. To ensure data integrity, the server will use a cyclic redundancy check (CRC) with a generator polynomial of $x^3 + x + 1$ (i) Calculate the CRC code for the given data packet using generator polynomial. Show each step of your calculation, including the binary division process. (5 Marks) (ii)If the third bit from the left is corrupted in the received data packet , perform a CRC check to determine if any errors occurred during transmission. Explain your reasoning and what the result indicates about the integrity of the received data (5 Marks)	10	2	5
09.	A Company needs a storage system with at least 12 TB usable storage for video files, using 4 TB drives. They require high data availability and fast read speeds. The IT manager is considering RAID 5 or RAID 1+0. (i)How many drives are needed in each configuration (RAID 5 and RAID 1+0) to meet the 12 TB requirement? (4 Marks) (ii)Describe the RAID level that is most suitable for the company's needs, considering factors such as fault tolerance, performance, and storage efficiency. (6 Marks)	10	4	5
10.	The Design team of a high-performance processor for a mobile gaming console is focused on optimizing a pipelined architecture to enhance instruction throughput and minimize latency. The pipeline consists of five stages: Fetch (IF), Decode (ID), Execute (EX), Memory Access (MEM), and Write Back (WB). However, the team encounters significant pipeline hazards, including data hazards and control hazards which impact overall performance. (i) Given the following sequence of instructions, identify any data hazards present (5 Marks) 1. ADD R1, R2, R3 ; R1 = R2 + R3 2. SUB R4, R1, R5 ; R4 = R1 - R5 3. AND R6, R1, R7 ; R6 = R1 & R7 4. BEQ R4, R8, target ; If R4 == R8, branch to target 5. OR R9, R6, R10 ; R9 = R6 | R10 (ii) Explain how control hazards could occur due to the branch instruction in the sequence. What strategies could be employed to mitigate the impact of control hazards in the pipeline? (5 Marks)	10	4	5

BL-Bloom's Taxonomy Levels - (1.Remembering, 2.Understanding, 3.Applying, 4.Analysing, 5.Evaluating, 6.Creating)

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