Continuous Assessment Test - II – December - 2022

Programme	: B.Tech(EEE/ECE/ECM/Civil)	Semester	: Fall 2022-23
Course	: BEEE102L - Basic Electrical & Electronics Enggineering	Slot	: E1+TE1
Faculty	: Rani S (CH2022231701005)	Faculty	: Inayathullaah M A (CH2022231700039)
Faculty	: Meera P S (CH2022231700041)	Faculty	: Mohd Aneesh (CH2022231700047)
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Time	: $1\frac{1}{2}\,hours$	Max. Marks	: 50

Answer all the Questions

1. A Y-connected balanced three-phase generator with phase sequence abc is connected to a Δ-connected balanced load with an impedance of $(15 + j5)\Omega$ per phase. The voltage between phase-a and the neutral of the Y-connected source is $V_{an} = 230 \angle - 30°$ V. The neutral point of the Y connected source is connected to the ground.

   (a) Find the line voltages, line currents and phase currents, assuming a positive sequence for the source voltages.

   (b) Find the power absorbed by the load.

2. A magnetic circuit shown in Fig. 1 with an iron core is having a relative permeability of 950. A coil of 1000 turns is wound on the iron core. Find the current (i) in the exciting coil required to establish a magnetic flux density of $0.5T$ in the air gap. The cross section of the core has the dimension $3cm X 4cm$. Account for fringing effect in the airgap. Width of the core is uniformly $2cm$.
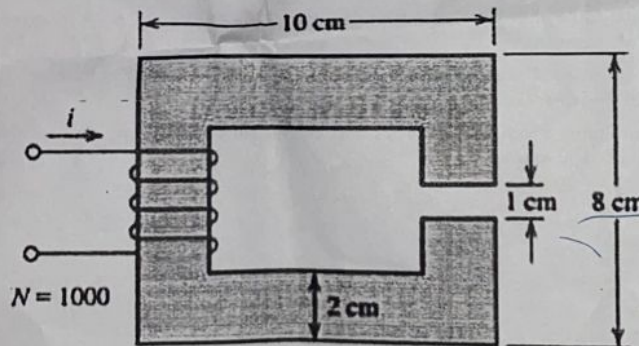

Fig. 1

3. An ideal transformer circuit is shown in Fig. 2. Given $V_s = 100\angle 0°V$. $R_{line} = 5\Omega$ and $R_L = 25\Omega$. Step up $\quad$ (10) transformer ratio is 1 : 20 and the step down transformer ratio is 10:1.

(a) Compute the power dissipated in the R_{line} and R_L.
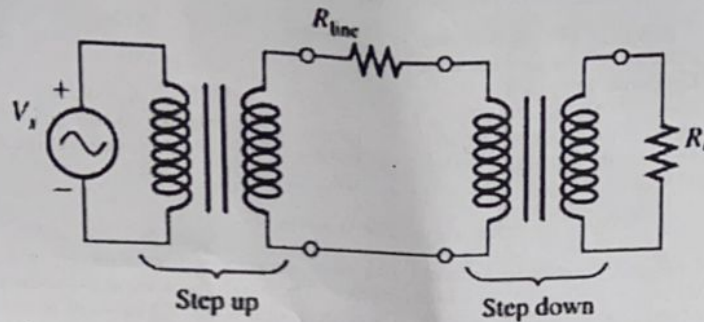
(b) Find the power supplied by the source.

Step up $\qquad\qquad\qquad$ Step down

Fig. 2

4. (a) Represent the unsigned decimal number $(10.75)_{10}$ in binary, octal and hexadecimal numbers systems. $\quad$ (10)

(b) Find the five bit signed magnitude two's complement representation for $A = (-15)_{10}$ and $B = (-2)_{10}$. Perform the binary arithmetic of (A+B) and (A-B). Specify if there is an overflow in the result.

5. Design a combinational circuit to realize the following expression $F(A, B, C) = \sum(m_1, m_3, m_5, m_7)$ $\quad$ (10)

(a) Draw the truth table showing the output function F and write the boolean expression in canonical form as sum of minterms.

Using Karnaugh map, obtain the minimum sum of product form (SOP) of the function (F) and realize the reduced SOP expression using logic gates.

btain the minimum product of sum form (POS) of the function (F) and realize the reduced POS xpression using logic gates.

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