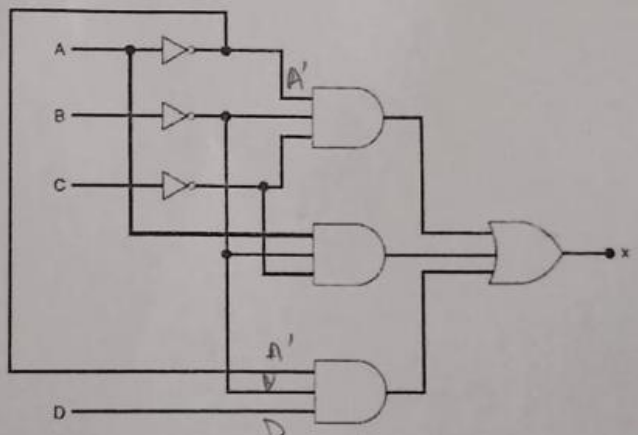
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test I – March 2023

Programme	:	B.Tech	Semester	:	WS 2022-23
Course	:	Digital System Design	Code	:	BECE102L
			Class Nbr	:	CH202223230013
Faculty	:	Prof. J. Divya	Slot	:	D1
Time	:	90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q.No.	Sub-division	Question Text	Marks
1.		A logic 'voter' circuit has 4 inputs ***a, b, c, d*** and one output ***v***. The output is to be logic 1 if any 3 or all 4 inputs are at logic 1. Draw a truth table map for each input and hence write down the simplified Boolean equations using K-Map method of reduction. Design a circuit using NOR gates to satisfy this requirement.	[10]
2.		Draw a CMOS logic circuit for the given expression. (Assume both true and complementary inputs are available) $F = (A + \overline{CD})(\bar{A} + B)$.	[5]
3.		Write the Boolean expression for output x in Figure 1. Determine the value of x for all possible input conditions in a truth table.  Figure 1	[5]
4.	i.	Simplify the given function F1=∑ (1, 5, 6, 7, 11, 12, 13, 15)	
	ii.	For the original and the simplified expression, write the Verilog HDL code using dataflow modelling.	[5] + [5]
5.		Write a gate level Verilog code for the schematic shown in Figure 2 and write a test bench for the same.	[10]

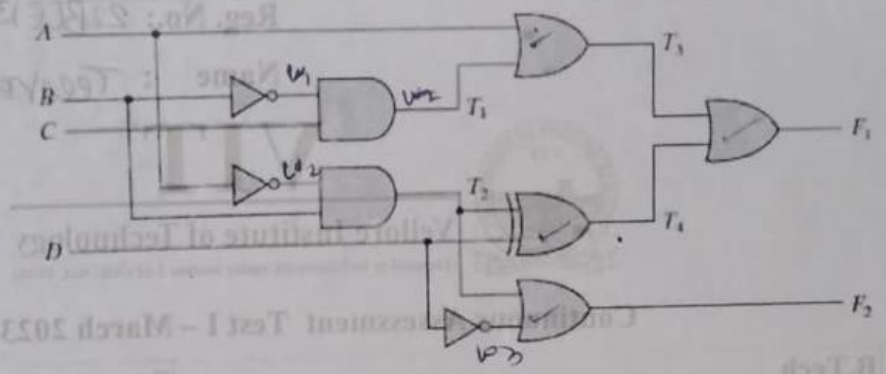


Figure 2

Design a 4:2 priority encoder. Also discuss the differences between encoder and priority encoder? **[10]**

Total Marks **[50]**

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