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Vellore Institute of Technology

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Reg. No. : 23MCE1460

Final Assessment Test(FAT) - Nov/Dec 2024

Programme	**B.Tech.**	Semester	**Fall Semester 2024-25**
Course Code	**BCSE205L**	Faculty Name	**Prof. Anusha K**
Course Title	**Computer Architecture and Organization**	Slot	**C1+TC1**
		Class Nbr	**CH2024250100951**
Time	**3 hours**	Max. Marks	**100**

General Instructions

- Write only Register Number in the Question Paper where space is provided (right-side at the top) & do not write any other details.

Course Outcomes

1. Differentiate Von Neumann, Harvard, and CISC and RISC architectures. Analyze the performance of machine with different capabilities. Recognize different instruction formats and addressing modes. Validate efficient algorithm for fixed point and floating point arithmetic operations.
2. Explain the importance of hierarchical memory organization. Able to construct larger memories. Analyze and suggest efficient cache mapping technique and replacement algorithms for given design requirements. Demonstrate hamming code for error detection and correction.
3. Understand the need for an interface. Compare and contrast memory mapping and IO mapping techniques. Describe and Differentiate different modes of data transfer. Appraise the synchronous and asynchronous bus for performance and arbitration.
4. Assess the performance of IO and external storage systems. Classify parallel machine models. Analyze the pipeline hazards and solutions.

Section - I

Answer all Questions (10 × 10 Marks)

*M - Marks

Q.No	Question	*M	CO	BL
01.	Draw the modified computer structure and describe the process that the CPU must undertake to read a value from memory and to write a value to memory adopting both the Harvard machine and von Neumann-based machine. Justify how the performance of your design is affected.	10	1	2
02.	Consider the following expression H = L * S. Let L = $-24_{(10)}$ and S = $7_{(10)}$. Perform the computation L * S using Booth's Algorithm. Identify the required number of iterations for the given input. Specify the iteration number if you have the same value of Q_0Q_{-1} separately. Display the accumulator value of each iteration and the final product.	10	1	3
03.	At memory address, 3227 H, "Mul R23, R44, R56" instruction is residing. Draw the single-cycle data path architecture and multi-cycle data path architecture for fetching and executing concerning "Mul R23, R44, R56" instruction with appropriate control sequence signals and also write the micro routine sequence for time (T1) for each architecture. Also, compare the architectures in terms of time.	10	1	3

04.	i) Consider a cache consisting of 512 blocks of 32 words each, for a total of 8192 (8k) words, and assume that the main memory is addressable by a 32-bit address and it consists of 8k blocks. How many bits exist for different mapping techniques in the Tag, Block / 4-way Set, and word fields? (5 Marks) ii) A computer employs RAM chips of 1024 x 8 and ROM chips of 2048 x 4. The computer system needs 2K bytes of RAM, 2K bytes of ROM, and an interface unit with 256 registers each. A memory-mapped I/O configuration is used. The two higher-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface. a) How many RAM and ROM chips are needed? How many address bus lines must be used to access Computer system memory? (2 marks) b) Draw a memory-address map for the system and give the address range in hexadecimal for RAM, and ROM. (3 marks)	10	2	5
05.	A base station BA1 transmits the hamming code to another base station BA2 through a color pattern as given in Figure 1. The data received by base station BA2 is given in Figure 2 where "G- Green color indicates 1" and "R-Red color indicates 0". Figure 1: Data transmitted  Figure 2: Data Received  Decode the pattern appropriately, then detect and correct the error that occurred during transmission and explain the complete process in detail.	10	2	2
06.	There are five devices D1, D2, D3, D4, and D5 waiting to have control over the single bus, at a time the bus controller can be active with one device. The device that gets control over the bus is called a master and others are called slaves. Elaborate the different techniques in which the master-ship of the bus can be granted to the devices. Justify your answers with neat diagrams.	10	3	1
07.	A company proposes to set up a RAID system for its servers. Design the most appropriate RAID architecture for the following. Justify your choice. (a) i) To store a replica of the data ii) To be able to correct errors on the fly(3 Marks) (b) i) For storing video data ii) Hybrid RAID that can sustain multiple disk failures(3 Marks) (c) i) For servers with high read access handling single disk failure, ii) RAID using block-level striping (4 Marks)	10	4	3

08.	A 5-stage pipelined processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX), and Write Operand (WO). The IF, ID, OF, and WO stages take 1 clock cycle each for any instruction. The EX stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction. Obtain the number of clock cycles needed to execute the following sequence of instructions. Compare the result without the pipelining concept.
	MUL R2,R10,R1
	DIV R5,R3,R4
	ADD R2,R5,R2
	SUB R5,R2,R6
		10	4	4

09.	You have bought an i6 Celeron processor, and you have been given a task to improvise your software for this processor. You will run 2 applications on this Celeron processor, but the resource requirements are not equal. The 1st application needs 60% of the resources, and the other only 10% of the resources. Assume that when you parallelize a portion of the program, the speedup for that portion is 3. Given that 35% of the first application is parallelizable, a. How much speedup would you achieve with the first application run in isolation? (5 Marks) b. How much overall system speedup would you observe if you parallelize it? (5 Marks)	10	3	4
10.	The processor receives three interrupts I1, I2, and I3 simultaneously with the priority values 2, 7, and 1 respectively during some I/O operations. Assume that the lowest number is used to represent the highest priority value. How does the processor handle these interrupts? Explain this in detail with the necessary diagrams.	10	3	1

BL-Bloom's Taxonomy Levels - (1.Remembering, 2.Understanding, 3.Applying, 4.Analysing, 5.Evaluating, 6.Creating)

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