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Vellore Institute of Technology

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Reg. No. :

Final Assessment Test (FAT) - May 2024

Programme	**B.Tech.**	Semester	**WINTER SEMESTER 2023 - 24**
Course Title	**COMPUTER ARCHITECTURE AND ORGANIZATION**	Course Code	**BCSE205L**
Faculty Name	**Prof. PAVITHRA S**	Slot	**C1+TC1**
		Class Nbr	**CH2023240502008**
Time	**3 Hours**	Max. Marks	**100**

General Instructions:

- Write only Register Number in the Question Paper where space is provided (right-side at the top) & do not write any other details.

Answer all questions (10 X 10 Marks = 100 Marks)

01. i) Illustrate the stored program concept on an accumulator-based machine that has same memory for storing instructions and data. Explain the operational steps involved to execute the given instructions with a suitable diagram. **[10]**

a) Load M(X)
b) Mul R3
c) Store M(X) (7 marks)

ii) Processor X has 32 general purpose registers and separate memory for storing instructions and data. Processor Y has 64 general purpose registers and a shared memory system for storing instructions and data. Identify which would be having a faster execution and justify your answer. (3 marks)

02. Consider implementing Booth's algorithm for the following number $(-41)_{10} * (9)_{10}$. **[10]**

i) Sketch the flowchart for implementing the Booth's algorithm to multiply two binary numbers. (2 marks)

ii) Illustrate the procedure involved in Booth's algorithm for the given numbers $(-41)_{10} * (9)_{10}$. Discuss how it efficiently multiplies two binary numbers by reducing the number of additions or subtractions (8 Marks)

03. Draw the architectural design of multi–Cycle Data Path to fetch and execute the following instructions. **[10]**

a) MOV (AX), R2
b) MUL R2, R3
c) MOV R3, (BX)

i. Write down the control sequence steps with respect to the given instructions which adhere to Opcode source, destination format. (8 marks)

ii. Suppose the processor employs micro programmed control for generating control signals, Write the micro routine for one of the above instructions. (2 marks)

04. Consider a cache of 32lines of 16 bytes each. The main memory is divided into blocks of 16 bytes each. That is, block 0 has bytes with addresses 0 through 15, and so on. The processor needs to access memory in the following sequence of addresses during program execution: [10]

a. $(58BF)_{16}$

b. $(3E3E)_{16}$

c. $(0F5A)_{16}$

i) Find the address configuration when the cache is Direct Mapped and 2-way Set Associative. (4 Marks)

ii) Identify the Cache block/Line to which the above addresses map to if direct mapped scheme is adopted. (6 marks)

05. Intel's chips are used in applications that have high I/O operations. Typically, an image is loaded from the disk and a face is detected. Then the next image is loaded and processed in a loop. [10]

i) Suggest and justify an I/O technique which will handle bulk transfer of data with minimum intervention by the processor. (5marks)

ii) Discuss the suggested I/O technique with suitable diagram and the registers involved in the operation. (5marks)

06. Draw a timing diagram for a machine that synchronizes the sequence of events with a common high-frequency clock for the following scenarios: [10]

i) When the CPU initiates a read operation to retrieve the data from memory. (5 Marks)

ii) When there is a write request to copy data into memory. (5 Marks)

07. A Banking application demands zero down time and maintains payment based sensitive data. How will you ensure reliability, availability and redundancy of data if the server crashes out? [10]

i) Identify and discuss hybrid RAID levels suitable for this application with appropriate diagram. (5 marks)

ii) A large-scale industry is looking for a high performance and fault-tolerance storage design. The response time is vital for the day-to-day operations of this industry and requires read operations to be fast. Discuss a suitable RAID level architecture that will meet the requirements. (5 marks)

08. Consider the transmitted word 001100110111 which consists of data bits and check bits and the syndrome word is 1110. The receiver has to search for appropriate parities to ascertain whether the code is correct. [10]

i. Identify the received word using the Hamming code algorithm when even parity is employed. (5 marks)

ii. Prove that the error bit is in the same position as the syndrome word. (5 marks)

09. Consider the following sequence of instructions is executed in a basic 5-stage pipelined processor ((Note: In all the instructions, the destination operand is given last) [10]

I1: Mul #20, R0, R1

I2: Add #3, R1, R3

I3: And R1, R2, R4

I4: Div R0, R4, R5,

instructions with an appropriate 5-stage pipeline diagram (5 marks)

ii. Propose the solutions to resolve these hazards and discuss their advantages and disadvantages (5 Marks)

10. i. Calculate the speedup achieved by pipelining compared to sequential execution when read operations take 110 nanoseconds, execute operations take 90 nanoseconds, and a register access time of 5 nanoseconds is used as the inter-stage buffer time. (5 marks) **[10]**

ii. Identify and discuss Flynn's classification that applies to parallelism of instructions only. Give some examples of where such models can be applied. (5 marks)

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