VIT

Reg. Number

Continuous Assessment Test (CAT) – II - OCTOBER 2024

Programme	:	B.Tech (CSE)	Semester	:	Fall Semester 2024-25
Course Code & Course Title	:	BCSE205L Computer Architecture and Organization	Class Number	:	
Faculty	:	Prof M. Nivedita, Dr. L Padma Dr. Surya Prakash Tiwari, Dr. M. Vidhya Lakshmi	Slot	:	C2+TC2
Duration	:	1 ½ hours	Max. Mark	:	50

General Instructions:

- Write only your registration number on the question paper in the box provided and do not write other information.

Answer all questions

Q. No	Sub Sec.	Description	Marks
1		Two processors, X1 and X2, execute the same set of instructions for a given program. X1 has a clock rate of 3.5 GHz, while X2 has a clock rate of 2.8 GHz. The instruction set can be broken down into three categories, as shown in the table below. Both processors execute the same number of instructions for each category. However, X1 has a lower CPI for arithmetic and logic instructions, while X2 has a lower CPI for memory-related operations.	10

Instruction Category	Instruction Count (%)	CPI of X1	CPI of X2
Arithmetic	40%	1	2
Logic	20%	1	1.5
Memory Access	40%	4	3

a. Analyze the performance of each processor in terms of execution time. Which processor completes the program faster, and why? Support your analysis with appropriate calculations. (5 marks)

b. If an optimization is applied to Processor X2, reducing the CPI for memory access instructions by 25%, would that change your conclusion? Recalculate and justify your answer. (5 marks)

2		Consider the following instruction LOAD R1, [R2] ; Load the value from memory at address in R2 into register R1 a. Write down the control sequence steps generated for the above instruction during both the **fetch** and **execute** phases in a **single-bus** organization. For each step, specify the necessary	10

			control signals and how data moves through the system.(5 Marks) b. Repeat part a. for a **multi-bus** organization (e.g. three-bus architecture). Explain how having multiple buses affects the control sequence and data flow compared to the single-bus organization.(5 Marks)	
	3		Design a **2046 × 256-bit memory chip** with the aim to optimize for both performance and efficiency a. Calculate the number of address lines required to access any word in the memory chip. (1 Mark) b. Given that the memory chip stores 256 bits per word, propose a suitable memory organization (such as row-column arrangement) that ensures efficient access to the data. Determine how many rows and columns you need, and explain how this design helps in minimizing access time. (4 Marks) c. Suppose you have the option to increase the memory size from **2046 × 256 bits** to **4092 × 128 bits**. Compare the advantages and disadvantages of this change in terms of memory addressing, bandwidth, access time, and overall performance. Which design would you recommend for a high-performance system, and why?(5 Marks)	10
	4		Consider a system with a main memory of 2 GB and a cache memory of 256 KB. The block size is 64 bytes. If the cache is organized as a direct mapped cache, a. Compute the number of blocks in the cache and determine the number of bits required for the tag, index, and block offset fields in the memory address. (4 Marks) b. Given that 20% of memory accesses are subject to cache misses in the direct-mapped configuration, analyze the potential performance impact if the system switches to a fully associative cache where the cache miss rate drops to 5%. Assume that accessing main memory takes 100 cycles and accessing the cache takes 5 cycles. Calculate the average memory access time for both configurations and discuss which setup provides better overall performance. (6 Marks)	10
	5		At some point in time 'N', the processor is accessing data from RAM. During the same time, a device R is in need of the processor's service. a) How will the processor handle the service requested by the device R? (4 Marks) b) Can the processor deny the service requested by the device R?(1 Mark) c) How will the processor handle multiple requests from other devices?(5 Marks) Justify your answer in detail.	10