VIT
Vellore Institute of Technology
CHENNAI

Reg. Number

Continuous Assessment Test (CAT) – II - October 2024

Programme	:	B. Tech CSE Specialization in BDS	Semester	:	Fall 24-25
Course Code & Course Title	:	BCSE205L & Computer Architecture and Organization	Class Number	:	CH2024250100676
Faculty	:	Dr. Linda Joseph	Slot	:	E1+TE1
Duration	:	1.30 Hrs	Max. Mark	:	50

Q. No.	Question Text	Marks
1.	Consider the execution of an object code with 200,000 instructions on a 40 GHz processor. The program consists of four major types of instructions. The mix of the instructions and their corresponding number of cycles per instruction are given below based on the result of the program trace experiment:	10

Instruction Type	CPI	Instructions (%)
ALU operations	1	60
Load/ Store with cache hit	2	18
Branch	4	12
Memory reference with cache miss	8	10

a. Calculate the average CPI when the program is executed with the above trace results. (4 marks)

b. Calculate the MIPS rate based on the CPI obtained in part (a). (3 marks)

c. Calculate the execution time. (3 marks)

2.	Design a datapath consisting of three buses, such that bus A is used to pass the contents of the register to the ALU or memory, bus B is used to pass the second operand to the ALU, and bus C is used to write the result back to the register. Also, include all the other essentials in the design to determine the control sequences for the given instructions a. ADD R4, (R3), R4 (5 Marks) b. JMP 16-bit memory address (5 Marks)	10

3	i) A hypothetical computer is designed to have a dynamic memory with an access time of 100 ns. It is also fitted with three static memories, out of which two are placed within the processor and one is placed on the motherboard. A data fetch was tested and assuming a hierarchical ordering, the success rate was found to be 0.95, 0.85 and 0.70 with an access time of 2 ns, 10 ns and 25ns respectively. Ignoring the search time, determine the average access time for the system. [5 Marks] ii) A computer system with two levels of cache as L1 and L2 use a 32-bit address space and each cache has the following characteristics: L1 cache: 32 KB, 64 blocks, 4-way set associative and L2 cache: 256 KB, 64-byte blocks, 8-way set associative. For each level of cache, compute a. Number of sets in the cache. [2 marks] b. Number of bits required for the tag, index and block offset. [3 marks]	10
4.	A computer system is designed to manage data transfer between a peripheral device such as a hard drive and the main memory. When a large file needs to be copied from the hard drive to RAM, the CPU has to oversee each byte of data that is moved. a. Determine how you will improve the efficiency of the CPU in terms of overall system performance. [5 marks] b. Describe the working principle of the CPU initiating such a technique. [5 marks]	10
5.	Imagine you are designing an embedded system for a smart home controller. This system has several components, including a temperature sensor, a motion detector, a smoke alarm and a button to reset the system. Each of the components needs to communicate with the processor according to their functionalities and priorities. a. Summarize the design strategy you would follow to handle each component's signal based on its urgency and importance? [5 marks] b. Examine the kind of mechanisms would you suggest for each of the above-mentioned components. Justify your answer. [5 marks]	10

********All the best**********