

Continuous Assessment Test (CAT) – II-OCTOBER 2024

Programme	:	B.Tech. Computer Science and Engineering	Semester	 Fall Semester 2024 - 25
Course Code & Course Title	:	BCSE205L Computer Architecture and Organization	Class Number	CH2024250101443 CH2024250100885 CH2024250100532
Faculty	:	Dr. M. Asha Jerlin Dr. Kaja Mohideen A Dr. M. Vidhya Lakshmi	Slot	 A1+TA1
Duration	:	90 Minutes	Max. Mark	50

Answer all questions

Q. No	Description	Marks
1	Consider Nivida MX600 processor assuming all references hit in the primary cache with a base CPI of 1.0, and Clock Rate 5 GHz. The main memory access time of 200 ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 4%. If we add a secondary cache, it takes 7 ns access time for a hit or a miss. The secondary cache reduces the miss rate to main memory to 0.4%.	10
	 a) Calculate the CPI for the processor with primary caching. (3 Marks) b) Calculate the CPI for the processor with secondary caching. (3 Marks) c) How much faster does the processor works effectively by adding secondary cache? (4 Marks) 	
2	Consider your Birth date (DD/MM/YYYY), now identify the value T=DD+MM. Write a program to identify whether the value of T is "ODD" or "EVEN". Using Single cycle Data path architecture a) Take the instruction which is used to identify "ODD" or "EVEN" number and write its operation sequence and Control sequence. (6 marks) b) Draw the single cycle data path architecture highlighting the flow of data along with essential components required for the instruction. (4 marks)	10
3	A computer employs RAM chips of 1024 x 8 and ROM chips of 2048 x 4. The computer system needs 2K bytes of RAM, and 2K bytes of ROM and an interface unit with 256 registers each. A memory -mapped I/O configuration is used. The two higher -order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface. a) How many RAM and ROM chips are needed? (2 marks)	10

	b) How many II	nes of the a	iddress bus	s must be	used to a	ccess Computer		
	And the second					common to all		
75	chips? (2 mar							
			1 1 1	Con abin o	alact? Spe	cify the size of	-	
	c) How many li	nes must be	e decoded	for emp s	elect: Spe	cerry the size of		
	the decoder.	S2						
	d) Draw a mem	ory-address	map for th	e system a	and give th	e address range		
	in hexadecim	nal for RAM	, ROM. (4	marks)				
4	Assume a 2-way set associative cache with 4 blocks. Solve the problem, as							
	demonstrated below on the address sequence "0, 1, 2, 3, 4."							
	Cantina of Casho Blocks after Reference							
		-	200	ro.	233	272		
	0	Miss	Mem[0]					
	1 2	Miss	Mem[0]	Mem(2)	Mem[1]	-		
	3	Miss	Mem[0]	Men(2)	Mem[1]	Mem(3)		
	4	Miss 0	Mem[4]	Men(2)	Mem[1]	Mem(3)		
	The following table shows address sequences.							
	Real Property Control Na							
	0.2 4.8 40 42 44 45 0							
	0 0 0 4 8 10 12	14 16 0						
	a. 0, 2, 4, 8, 10, 12.		ent policy	by flinnin	g a coin	For example.		
	Simulate a randor	n replaceme						
		n replaceme	t block in	a set and '	'tails" mea	ans to evict the		
5	Simulate a randor "heads" means to	n replaceme evict the firs et. How man	t block in a y hits does	a set and ' this addres	tails" mea	ans to evict the exhibit?	10	
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