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Vellore Institute of Technology

Reg. No. :

Final Assessment Test(FAT) - Nov/Dec 2024

Programme	B.Tech.	Semester	Fall Semester 2024-25
Course Code	BCSE205L	Faculty Name	Prof. Linda Joseph
Course Title	Computer Architecture and Organization	Slot	E2+TE2
		Class Nbr	CH2024250100678
Time	3 hours	Max. Marks	100

General Instructions

- Write only Register Number in the Question Paper where space is provided (right-side at the top) & do not write any other details.

Course Outcomes

1.Differentiate Von Neumann, Harvard, and CISC and RISC architectures. Analyze the performance of machine with different capabilities. Recognize different instruction formats and addressing modes. Validate efficient algorithm for fixed point and floating point arithmetic operations.

2.Explain the importance of hierarchical memory organization. Able to construct larger memories. Analyze and suggest efficient cache mapping technique and replacement algorithms for given design requirements. Demonstrate hamming code for error detection and correction.

3.Understand the need for an interface. Compare and contrast memory mapping and IO mapping techniques. Describe and Differentiate different modes of data transfer. Appraise the synchronous and asynchronous bus for performance and arbitration.

4.Assess the performance of IO and external storage systems. Classify parallel machine models. Analyze the pipeline hazards and solutions.

Section - I

Answer all Questions (10 × 10 Marks) *M - Marks

Q.No	Question	*M	CO	BL
01.	(i) Assume a RAM formulated as rows and columns, for the given CISC instruction, convert into its corresponding RISC instructions, the result being stored back in the location 2:1. MULT 2:1, 3:1 (4 marks) (ii) Determine the efficiency of the processors in terms of space and speed. (3 marks) (iii) If RISC-based ARM processors and CISC-based x86 processors are evaluated to deploy a mixed architecture environment to optimize performance and cost for different applications. What types of applications would benefit more from RISC processors, and which would benefit from CISC? (3 marks)	10	1	3
02.	A company has a total of 96 gigabytes (GB) of data that needs to be distributed across servers. Given if each server has 12 slots, (i) Calculate how many servers are needed to store the total data, show the step by step sequences in terms of restoring division method. (8 marks) 6 (ii) Summarize the benefits of the restoring division method. (2 marks)	10	1	3

03.	Considering the given snippet of memory, (i) Indicate the type of the addressing modes used by the instructions and calculate their effective addresses. (5 marks)
	ADD C, #10;
	ADD C, A;
	ADD C, (B);
	ADD C, (1000+IR);
	ADD C, (BR+2)
	(ii) Determine the values of register C after every execution of the given instructions.(5 marks)
		10	1	3

Memory Address	Memory Content
1000	15
1001	25
1002	35
1003	45
1004	55
1005	10

Registers	Contents of Registers
Base Register (BR)	1000
Index Register (IR)	5
Register A	10
Register B	1005
Register C	0

04.	(i) Design a shared bus architectural Datapath with components involving bank of registers, MUX-2 Numbers, ALU and their corresponding control signals. The Datapath can handle types of instructions such as Load and store instructions, Jump instructions and Arithmetic/ Logic instructions. Consider each instruction to be operating on a 32-bit registers and memory addresses. (5 marks) (ii) Determine the control sequences and the clock cycles required to execute the micro instructions for ADD (R3), R1 and Branch on Negative (Branch<0). (5 marks)	10	2	3

05.	Consider a 3-level Direct mapped cache system with the following properties:	10	2	4

L1 cache	Hit time: 1 ns, Miss rate: 10%	Modified Miss rate: 5%
L2 cache	Hit time: 5 ns, Miss rate: 20%	New L2 cache: Hit time-
L3 cache	Hit time: 10 ns, Miss rate: 30%	6 ns, Miss rate-5 %
Main Memory	Access time: 100 ns	

(i) Calculate the average access time for the given system, and if the same cache architecture is converted to a set associative cache having a reduction in the cache levels, say L2 and L3 are combined (new L2 cache), analyze the average access time required for such a scenario. (4 marks)

(ii) The main memory consists of a 32-bit address space, having the cache specifications of L1 cache: 32 KB, 64-byte blocks, 4-way set associative, L2 cache: 256 KB 64-byte blocks, 8-way set associative. Compute the number of sets in the cache, the number of bits required for the tag, index and block offset for each cache level. (6 marks)

06.	A server uses ECC (Error Correcting Code) memory to protect data integrity, relying on Hamming code to detect and correct single bit errors in a 6-bit data word. The 6-bit data word 110101 is transmitted along with the Hamming code parity bits. (i) Determine the required number of parity bits and generate the Hamming code for the data. (5 marks) (ii) Assume a single-bit error correction is performed in the received code by flipping the bit at position 6. Find out the data word, detect and correct the error. (5 marks)	10	2	3
07.	An audio processing device is connected to a computer via a DMA controller. This device continuously records audio data and transfers it to system memory in small packets (128 bytes) at regular intervals. The CPU needs to continue performing other tasks, such as processing user inputs and managing applications, with minimal interruptions. (i) Elaborate how the DMA controller can manage the transfer of audio data without heavily interrupting the CPU's operations. (5 marks) (ii) Discuss the trade-off in terms of CPU performance if multiple DMA controllers are trying to transfer data frequently? Describe with neat diagrams wherever necessary. (5 marks)	10	3	3
08.	A processor has a 5-stage pipeline (Fetch, Decode, Execute, Memory, Write back). If the ALU can only handle one operation per cycle, for the given instructions R1=R2+R3; R4=R5*R6; R7=R1÷R4, i) Determine the additional cycles needed to avoid the structural hazards. Illustrate with neat diagram.(5 marks) ii) Provide the solutions to overcome structural hazards with relevant diagrams. (5 marks)	10	4	3
09.	(i) A program has a portion that is 60% parallelizable and 40% serial. If the parallelizable portion is executed on 4 processors, what is the overall speedup according to Amdahl's law? (5 marks) (ii) If the program's parallelizable portion was increased from 60% to 80%, what would be the new speedup when using the same 4 processors? (5 marks)	10	4	4
10.	A team is designing a high-performance embedded system that requires frequent data transfers between multiple processors, memory modules and I/O devices. They plan to use a bus structure, but found that they are encountering issues as the system grows in complexity. (i) Suggest a bus mode to manage data transfers without facing issues related to scalability and timing constraints. Describe your answers with diagrams to illustrate both input and output operations of the bus. (6 Marks) (ii) Discuss the advantages of the proposed bus mode in terms of improving the scalability and overcoming the timing constraints. (4 marks)	10	3	3

BL-Bloom's Taxonomy Levels - (1.Remembering, 2.Understanding, 3.Applying, 4.Analysing, 5.Evaluating, 6.Creating)

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