Vellore Institute of Technology
CHENNAI

Continuous Assessment Test (CAT) – I - AUGUST 2024

Programme	:	B.Tech. Computer Science and Engineering	Semester	:	Fall Semester 2024 - 25
Course Code & Course Title	:	BCSE205L Computer Architecture and Organization	Class Number	:	CH20242501009517 CH20242501026857 CH20242501009477
Faculty	:	Dr. K. Anusha, Dr. R. Madura Meenakshi, Prof. M. Nivedita	Slot	:	C1+TC1
Duration	:	90 Minutes	Max. Mark		50

Answer all questions

Q. No	Description	Marks
1	The organization of an IAS computer has 4096-word memory space with 40-bit word data and 20-bit instruction length. Consider the following modifications in the IAS computer and discuss the architectural changes for each. a. How would the register architecture change if we expand the memory space with another 4096 words? (3 Marks) b. How would the instruction set change if we introduce two more data registers (R1 and R2) in the existing architecture? (3 Marks) c. What changes would allow us to specify more than one operand in an instruction? (2 Marks) d. If we reduce the word size to 20 bits, which register would be no longer required? Justify (2 Marks)	10
2	a. Compare and contrast the two different types of instruction set computers. (5 Marks) b. How could you solve the following arithmetic expression with both computers and write the assembly code for the same? (5 Marks) $Y = A + B * C - D * E$	10
3	Perform the arithmetic operation $X = 43 - 65$, with a. signed magnitude representation (3 Marks) b. 1's complement representation (3 Marks) c. 2's complement representation (3 Marks) d. Design a logic circuit to identify the overflow/underflow situation	10

	without using the XOR gate. (1 Mark)	
4	a. Draw the flowchart to illustrate the procedure for non-restoring division. (5 Marks) b. Solve the arithmetic operation $\frac{-11}{3}$ by following the same method. (5 Marks)	10
5	Consider the given sequence of zero-address instruction, which executes an arithmetic expression and stores the final result at the memory location X. You are asked to express the code in a. One address instruction(3 Marks) b. Two address instructions (3 Marks) c. Three address instructions (3 Marks) d. Among the three formats, identify the one which is more memory-efficient than the others. Justify. (1 Mark) **PUSH B** **PUSH C** **MUL** **PUSH A** **SUB** **PUSH E** **PUSH F** **DIV** **PUSH D** **ADD** **DIV** **POP X**	10

**********All the best **********