VIT
Vellore Institute of Technology
CHENNAI

Reg. Number:	

Continuous Assessment Test (CAT) – II-OCTOBER 2024

Programme	:	B.Tech. Computer Science and Engineering	Semester	:	Fall Semester 2024 - 25
Course Code & Course Title	:	BCSE205L Computer Architecture and Organization	Class Number	:	CH2024250101443 CH2024250100885 CH2024250100532
Faculty	:	Dr. M. Asha Jerlin Dr. Kaja Mohideen A Dr. M. Vidhya Lakshmi	Slot	:	A1+TA1
Duration	:	90 Minutes	Max. Mark		50

Answer all questions

Q. No	Description	Marks
1	Consider Nivida MX600 processor assuming all references hit in the primary cache with a base CPI of 1.0, and Clock Rate 5 GHz. The main memory access time of 200 ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 4%. If we add a secondary cache, it takes 7 ns access time for a hit or a miss. The secondary cache reduces the miss rate to main memory to 0.4%. a) Calculate the CPI for the processor with primary caching. (3 Marks) b) Calculate the CPI for the processor with secondary caching. (3 Marks) c) How much faster does the processor works effectively by adding secondary cache? (4 Marks)	10
2	Consider your Birth date (DD/MM/YYYY), now identify the value T=DD+MM. Write a program to identify whether the value of T is "ODD" or "EVEN". Using Single cycle Data path architecture a) Take the instruction which is used to identify "ODD" or "EVEN" number and write its operation sequence and Control sequence. (6 marks) b) Draw the single cycle data path architecture highlighting the flow of data along with essential components required for the instruction. (4 marks)	10
3	A computer employs RAM chips of 1024 x 8 and ROM chips of 2048 x 4. The computer system needs 2K bytes of RAM, and 2K bytes of ROM and an interface unit with 256 registers each. A memory -mapped I/O configuration is used. The two higher -order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface. a) How many RAM and ROM chips are needed? (2 marks)	10

	b) How many lines of the address bus must be used to access Computer system memory? How many of these lines will be common to all chips? (2 marks) c) How many lines must be decoded for chip select? Specify the size of the decoder. (2 marks) d) Draw a memory-address map for the system and give the address range in hexadecimal for RAM, ROM. (4 marks)	
4	Assume a 2-way set associative cache with 4 blocks. Solve the problem, as demonstrated below on the address sequence "0, 1, 2, 3, 4."	10

Address of Memory Block Accessed	Hit or Miss	Evicted Block	Contents of Cache Blocks after Reference			
			Set 0	Set 0	Set 1	Set 1
0	Miss		Mem[0]			
1	Miss		Mem[0]		Mem[1]	
2	Miss		Mem[0]	Mem[2]	Mem[1]	
3	Miss		Mem[0]	Mem[2]	Mem[1]	Mem[3]
4	Miss	0	Mem[4]	Mem[2]	Mem[1]	Mem[3]

The following table shows address sequences.

	Address Sequence
a.	0, 2, 4, 8, 10, 12, 14, 16, 0

Simulate a random replacement policy by flipping a coin. For example, "heads" means to evict the first block in a set and "tails" means to evict the second block in a set. How many hits does this address sequence exhibit?

5	Direct Memory Access (DMA) allows devices to access memory directly rather than working through the CPU. This can dramatically speed up the performance of peripherals but adds complexity to memory system implementations. Explore DMA implications by answering the questions about the following peripherals. • Mouse Controller • Ethernet Controller a) Does the CPU relinquish control of memory when DMA is active? For example, can a peripheral simply communicate with memory directly, avoiding the CPU completely? (5 marks) b) Of the peripherals listed above, which would benefit from DMA? What criteria determine if DMA is appropriate? (5 marks)	10

**********All the best **********