VIT

Vellore Institute of Technology

Reg. No. :

Final Assessment Test(FAT) - Nov/Dec 2024

Programme	B.Tech.	Semester	Fall Semester 2024-25
Course Code	BCSE205L	Faculty Name	Prof. Vidhya Lakshmi M
Course Title	Computer Architecture and Organization	Slot	A1+TA1
		Class Nbr	CH2024250100532
Time	3 hours	Max. Marks	100

General Instructions

- Write only Register Number in the Question Paper where space is provided (right-side at the top) & do not write any other details.

Course Outcomes

1. Differentiate Von Neumann, Harvard, and CISC and RISC architectures. Analyze the performance of machine with different capabilities. Recognize different instruction formats and addressing modes. Validate efficient algorithm for fixed point and floating point arithmetic operations.
2. Explain the importance of hierarchical memory organization. Able to construct larger memories. Analyze and suggest efficient cache mapping technique and replacement algorithms for given design requirements. Demonstrate hamming code for error detection and correction.
3. Understand the need for an interface. Compare and contrast memory mapping and IO mapping techniques. Describe and Differentiate different modes of data transfer. Appraise the synchronous and asynchronous bus for performance and arbitration.
4. Assess the performance of IO and external storage systems. Classify parallel machine models. Analyze the pipeline hazards and solutions.

Section - 1

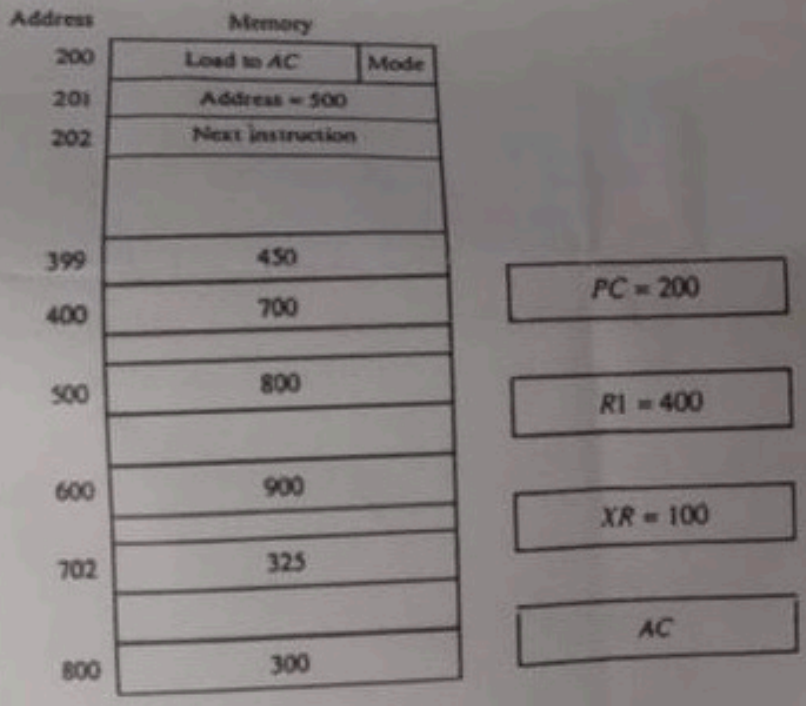
Answer all Questions (3 × 5 Marks) *M - Marks

Q.No	Question	*M	CO	BL
01.	Analyze the primary structural distinctions between Harvard and Von Neumann architectures and explain how these differences impact data processing and memory access.	5	1	2
02.	A processor has a 5-stage instruction pipeline (Fetch, Decode, Execute, Memory, Write-back). An arithmetic instruction requires 5 cycles to complete. Suppose a load instruction is followed immediately by an arithmetic operation using the loaded data. a) Identify the kind of hazard that might occur, and how could it affect the pipeline's performance? (3 marks) b) How can this hazard be resolved through techniques like data forwarding or pipeline stalls? (2 marks)	5	4	3
03.	Calculate and interpret the average memory access time for a processor with a 90% cache hit rate, given a cache access time of 5 ns and a main memory access time of 50 ns. How do these parameters affect overall performance?	5	2	5

Section - II

Answer all Questions (4 × 10 Marks)

Q.No	Question	*M	CO	BL
04.	Using Modified Booth's algorithm, multiply the 4-bit binary numbers **0110** (multiplicand) and **0011** (multiplier). Show the detailed step-by-step execution, including all intermediate values of the registers (**A, Q, Q-1, M, -M**) and the shifts performed at each stage. Finally, interpret the binary result and convert it back to decimal form.	10	1	5
05.	Evaluate the effective address and operand value for the following addressing mode a) Direct (2marks) b) Indirect (2marks) c) Index (2marks) d) Register indirect (2marks) e) Auto Decrement (2marks) from the following memory diagram	10	1	3



06.	a) A CPU accesses memory addresses in the following sequence: 0x1A4, 0x2B6, 0x1A4, 0x2B7, 0x2B6. Assume a direct-mapped cache with 4 blocks and each block size is 16 bytes. Determine whether each access results in a hit or a miss. (6 marks) b)A cache has 4 blocks, each of size 8 bytes, and the main memory size is 1KB. Calculate: i) The number of bits for memory address, tag, and block offset. (2 marks) ii) If the memory address is 0x0C7, which block will it be mapped to? (2 marks)	10	2	5
07.	A small business is looking to set up a storage solution for their server, with a focus on data redundancy to ensure their data is safe in case of a disk failure. They need a balance between performance, storage capacity, and redundancy. Compare the different RAID levels (RAID 1, RAID 5 and RAID 6) and recommend the most suitable RAID configuration for their needs, considering the pros and cons of each in terms of redundancy, storage efficiency, and cost.	10	4	4

Section - III
Answer all Questions (3 × 15 Marks)

*M - Marks

Q.No	Question	*M	CO	BL
08.	A computer system has multiple devices (CPU, DMA controller, and various I/O devices) that need access to the system bus to read or write data. The bus arbitration mechanism used to decide which device gets control of the bus can be either synchronous or asynchronous. The CPU has the highest priority, followed by the DMA controller and then the other I/O devices. The devices request access to the bus by sending signals to the bus controller, which in turn uses a certain arbitration technique to grant access. a) If the system switches to an asynchronous bus arbitration mechanism, where devices request access without relying on a clock signal, describe how the bus controller would handle multiple simultaneous requests from the CPU, DMA, and I/O devices. (7.5 marks) b) What challenges might arise in terms of timing, and how does the system ensure that higher-priority devices like the CPU get access over lower-priority devices? (7.5 marks)	15	3	4
09.	A processor uses a 5-stage instruction pipeline with the stages: IF (Instruction Fetch), ID (Instruction Decode), EX (Execute), MEM (Memory Access), and WB (Write Back). Each stage takes 1 clock cycle to complete, and the pipeline operates at a clock frequency of 2 GHz. However, due to data hazards, branch instructions, and cache misses, the following events occur: 1. A data hazard between two instructions causes a 2-cycle stall. 2. A branch instruction causes a 3-cycle penalty due to misprediction. 3. A cache miss during the MEM stage results in a 4-cycle delay. Given the following sequence of instructions: 1. Instruction A (no hazards) 2. Instruction B (data hazard with Instruction A) 3. Instruction C (branch instruction) 4. Instruction D (no hazards) 5. Instruction E (cache miss during MEM stage) a) Calculate the total time in clock cycles to execute the sequence of instructions, considering the stalls and delays. (5 marks) b) Determine the average CPI (Cycles Per Instruction) for this sequence. (5 marks) c) Analyze how the delays impact the overall pipeline performance and suggest strategies to mitigate the impact of each type of stall or delay. (5 marks)	15	4	5
10.	A communication system is transmitting data packets between two computers. To ensure data integrity during transmission, the system uses Hamming code for error detection and correction. Each data packet is 7 bits long, and the system adds parity bits to create a Hamming codeword. During transmission, the following 11-bit Hamming codeword is received: Received Codeword: 10110100101 a) Determine if there is an error in the received codeword using Hamming code. If an error exists, identify the erroneous bit position and provide the corrected codeword. (5 marks) b) Explain the steps you took to detect and correct the error in the received codeword. Why is Hamming code suitable for this error detection and correction? (5 marks) c) If the system switches to using a simple parity check instead of Hamming code, how many errors can it detect and correct? Compare the effectiveness of the simple parity check with that of Hamming code. (5 marks)	15	4	5

BL-Bloom's Taxonomy Levels - (1.Remembering, 2.Understanding, 3.Applying, 4.Analysing, 5.Evaluating,