Reg. No.:

Name :

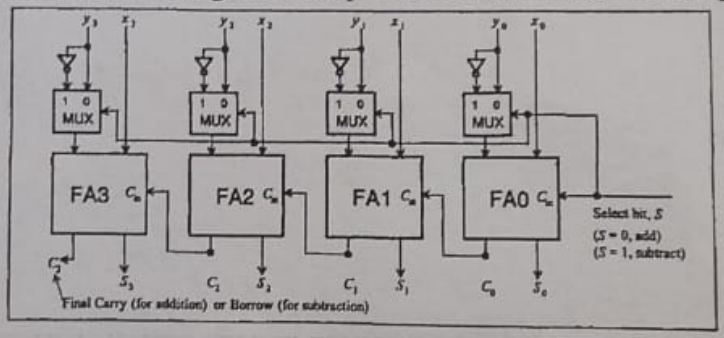
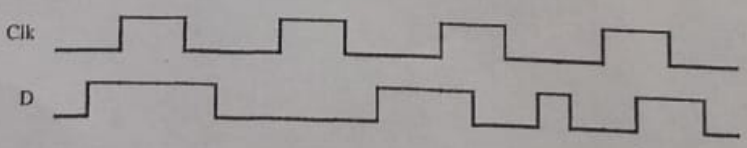
VIT

Vellore Institute of Technology

Continuous Assessment Test II – October 2023

Programme	:	B.Tech (ECE/ECM)	Semester	:	FS 2023-24
Course	:	Digital System Design	Code	:	BECE102L
			Class Nbr	:	CH2023240100538, CH2023240100368, CH2023240100369, CH2023240100535 CH2023240100365
Faculty	:	Dr Gargi Raina, Dr K Chitra, Dr B Lakshmi, Dr A Prathiba, Dr Jenifer	Slot	:	B1+TB1
Time	:	90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q.No.	Sub. Sec.	Questions	Marks
1.		Consider a simple digital lock system which has 2-bit digital inputs A and B. In order to unlock the system, all the bits of the two inputs should exactly match with each other. Design a secure circuit for this scenario by formulating a table with all possible combinations of the inputs A & B.	5
2.		Develop a Verilog HDL code for the schematic shown. All the submodules in the code should be in data flow modelling and the top module in structural modelling 	15
3.		Use an appropriate algorithm to determine the product of integers (13 X -9) and neatly tabulate each cycle with all operations mentioned	10
4.		Depict the output waveform for the following i) A positive level sensitive gated D latch for the input waveform shown 'D'  ii) A positive edge triggered clocked J-K flip flop for the given input waveform 'J&K'	5+5

(i). Design a sequential logic circuit using appropriate flip-flops which converts the incoming data from sensor into data that can be handled by the microcontroller as shown in Figure-1. [4 Marks]

(ii). Illustrate with a neat table, how serial input 1010 (D3D2D1D0) of sensor is get transferred to microcontroller. [3 marks]

(iii). Write a Verilog HDL code for the same in behavioural modelling [3 marks]

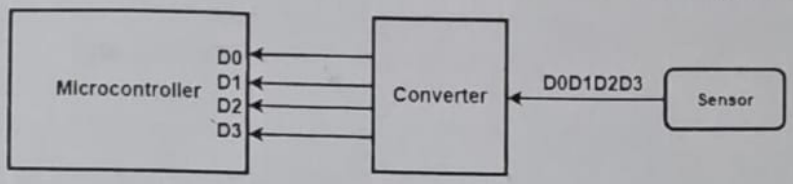


Figure-1

5. For the logic diagram shown in Figure-2, assume output of a D flip-flop is HIGH and output of the JK flip-flop LOW. Formulate a table as shown below representing the sequence of outputs produced from J-K flip flop for the next 5 clock pulses. **[10]**

CLK	D	Q_D	Q_{D+1}	J	K	Q_{JK}	Q_{JK+1}
1							
2							
3							
4							
5							

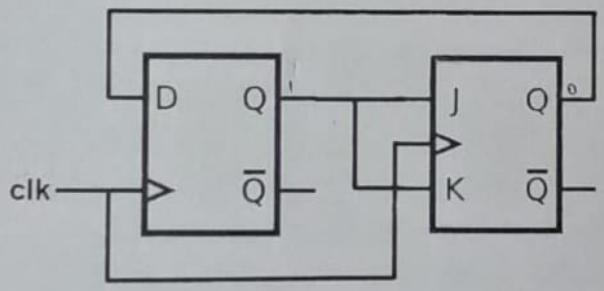


Figure-2

Total **[50]**

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