VIT

Vellore Institute of Technology
CHENNAI

Reg. Number	

Continuous Assessment Test (CAT) – II - OCTOBER 2024

Programme	:	B.Tech(CSE)	Semester	:	Fall Semester 2024-25
Course Code & Course Title	:	BCSE205L Computer Architecture and Organization	Class Number	:	CH2024250100951/ CH2024250102685/ CH2024250100947
Faculty	:	Dr. K. Anusha, Dr. R. Madura Meenakshi, Prof. M. Nivedita	Slot	:	C1+TC1
Duration	:	1 ½ hours	Max. Mark		50

General Instructions:

- Write only your registration number on the question paper in the box provided and do not write other information.

Answer all questions

Q. No	Sub Sec.	Description	Marks
1		Consider a simple single-bus datapath for a basic CPU. The instruction being executed is ADD R1, R2, R3, which adds the contents of register R2 to register R3 and stores the result in register R1. a) Identify the steps involved in executing this instruction on the single-bus datapath.(5 Marks) b) For each step, specify the control signals that must be activated, such as register read/write signals, ALU operation signals, and memory read/write signals.(5 Marks)	10
2		A processor executes three types of instructions: A, B, and C. The following table provides the information about each instruction type, its CPI (Cycles Per Instruction), and the percentage of instructions executed of that type: Instruction Type / CPI / Percentage of Instructions executed A / 4 / 40% B / 3 / 35% C / 2 / 25% a) Calculate the overall CPI of the processor. (3 Marks) b) Suppose optimizations are made to reduce the CPI of instruction type A by 25% and instruction type B by 20%. Calculate the new overall CPI after these optimizations. (4 Marks) c) Determine the percentage improvement in the overall CPI after optimization.(3 Marks)	10
3		Consider designing a ROM to store the firmware of a washing machine system manufactured in Coimbatore. The firmware size is 16KB (16,384 bytes). Available ROM chips have a size of 2048 × 8.	10

		a) How many ROM chips are needed to store the firmware?(4 Marks) b) How many address lines are required to access the entire memory?(2 Marks) c) Suggest a design for connecting the ROM chips and address lines.(4 Marks)	
4		A two-way set-associative cache consists of total of 256 blocks .The main memory contains 8192 blocks each consist of 128 words. a) How many bits are there in a main memory address? (1 Mark) b) How many bits are there in each of the TAG, SET and WORD field?(3 Marks) c) What is the size of the cache memory?(2 Marks) d) For the following main memory block requests: 10, 55, 11, 4, 13, 8, 132, 129, 212, 129, 64, 8, 48, 32, 73, 92 calculate the number of misses and the miss ratio if the replacement strategy is Least Recently Used (LRU). (4 Marks)	10
5		A CPU is interfacing with a peripheral device that needs to transfer 20 KB of data to memory using a DMA controller. The transfer occurs in two modes: block transfer mode and cycle stealing mode. Given: Transfer Size: 20 KB (20,480 bytes) Block Size: 1 KB (1,024 bytes) Data Transfer Rate of DMA: 1 MB/s (1,024,000 bytes per second) CPU Cycle Time: 200 ns (0.2 μs) Number of CPU Cycles per Memory Access: 4 cycles System Bus Bandwidth: 1 MB/s a) Calculate the total transfer time for DMA in block transfer mode.(2.5 marks) b) Calculate the total time the CPU remains in a blocked state during the transfer in block transfer mode.(2.5 marks) c) Calculate the total transfer time for DMA in cycle stealing mode.(2.5 marks) d) Calculate the total time the CPU remains in a blocked state during the transfer in cycle stealing mode.(2.5 marks)	10