VIT
Vellore Institute of Technology
CHENNAI

Reg. Number:	22BCE1423

Continuous Assessment Test (CAT) – I (January 2025)

Programme	:	B. Tech. Computer Science and Engineering	Semester	:	Winter Sem 24-25
Course Code & Course Title	:	BCSE412L Parallel Computing	Class Number	:	CH2024250502060 CH2024250502065
Faculty	:	**Dr. Christopher Columbus C Dr. Lakshmi Harika Palivela**	Slot	:	C1 + TC1
Duration	:	1½ Hours	Max. Mark		50

General Instructions:

- Write only your Reg. No. on the question paper in the box provided and do not write other information.
- Use statistical tables supplied from the exam cell as necessary
- Use graph sheets supplied from the exam cell as necessary
- Only non-programmable calculator without storage is permitted

Answer all questions

Q. No	Sub Sec.	Description	Marks
1		Three processor cores (C0, C1, and C2) are part of a multi-core system, each with a private cache. The following sequence of operations occurs on a shared variable x: • Core C0 reads variable x from memory, caches it, and stores the value 10 in its cache. • Core C1 reads x from memory, caches it, and also stores the value 10 in its cache. • Core C1 writes x = 20, updating both its cache and the memory value of x. • Core C0 reads x again from its cache, which still holds the value 10. • Core C2 reads x from memory, caches it, and stores the value 20. • Core C2 writes x = 30, updating both its cache and the memory value of x.	10
	a)	Based on the given scenario, identify the caching policy being used. Explain how this policy contributes to the observed inconsistency in the system. (5 Marks)	
	b)	Analyze the impact of the MESI protocol in resolving cache coherence issues in this situation. Evaluate the different cache states in the MESI protocol and justify their role in ensuring consistency across the cores'	

		caches. (5 Marks)	
2		A research team is exploring advanced computing architectures for specialized applications and has encountered MISD. They are seeking a detailed explanation of MISD, how it functions, and whether it has practical real-world applications. Furthermore, they would like to understand how this architecture could be utilized to align with and advance the cryptography application. Provide a comprehensive narrative in your response.	10

3		Given the following scalar code:
		int sum = 0;
		for (int i = 0; i < N; i++) {
		if (A[i] > 0) { // Mask: Only add positive values
		sum += A[i];
		} }
		Array A is given as: A = [3, -1, 4, 7, -2, 6, 5, -3]
		The vector processor can process four elements at a time. Convert the above scalar code into a vectorized form using vector instructions. Explain in detail how the system processes the array and computes the final sum.
			10

4	a)	Discuss the key differences between the 'parallel region' and 'work-sharing constructs' in terms of their application, scope, and impact on parallel performance. Illustrate your response with a conceptual code for each scenario to demonstrate the implementation of parallel regions and work-sharing constructs in OpenMP. (6 Marks)	10
	b)	Consider this example of PRIVATE, FIRSTPRIVATE and DEFAULT int A = 1, B = 1, C = 1; #pragma omp parallel default(none) private(B) firstprivate(C) (i) Is the code snippet correct? (1 Mark) (ii) Identify the data sharing attributes for B and C? (2 Mark) (iii) Provide the initial values of B and C inside and after the parallel region? (1 Mark)	

5	a)	Decode the output of the program. (6 Marks)
		#include <stdio.h>
		#include <omp.h>
		#include <time.h>
		int main() {
		clock_t start, end; // Variables for timing
		double cpu_time_used; // Variable to store execution time
		// Record the start time
		start = clock();
		// Initialize arrays
		int a[5] = {1, 2, 3, 4, 5};
		int b[5] = {6, 7, 8, 9, 10};
		int c[5];
		#pragma omp parallel for num_threads(4)
		for (int i = 0; i < 5; i++) {
		int td = omp_get_thread_num();
		c[i] = a[i] + b[i];
		printf("c[%d] = %d (Thread %d)\n", i, c[i], td);
		}
		end = clock();
		cpu_time_used = ((double)(end - start)) / CLOCKS_PER_SEC;
		printf("Execution time: %f seconds\n", cpu_time_used);
		return 0;
		}
			10

	b)	You are developing a deep learning model for real-time image recognition in an autonomous vehicle system. The model requires high-speed inference, low latency, and efficient power consumption. Critically assess whether a CPU, GPU, or TPU would be the most suitable choice for deployment. Justify your decision by analyzing computational efficiency, model complexity, and workload demands. (4 Marks)	

**********All the best **********