VIT Vellore Institute of Technology Reg. No. :

Final Assessment Test (FAT) – November/December 2022

Programme	B.Tech.	Semester	Fall Semester 2022-23
Course Title	COMPUTER ARCHITECTURE AND ORGANIZATION	Course Code	BCSE205L
Faculty Name	Prof. ANUSHIYA RACHEL	Slot	B1+TB1
		Class Nbr	CH2022231001489
Time	3 Hours	Max. Marks	100

Part A (10 X 10 Marks)
Answer All questions

1. Assume a RISC-based computer system. Illustrate the steps required to execute the sequence of instructions : [10]

Memory Address	Instruction
1010	Load A
1011	Add B
1100	Store C

Where, 1010, 1011, 1100 are the memory address of the instructions, A is the memory address of the first operand and the data value in A is 20 and location B has a data value of 30. Identify the contents of registers PC, MAR, MDR, and IR during the instruction fetch and execute phases. (10 marks)

2. Perform multiplication using Booth's Algorithm. [10]
   i. Show the step-by-step process for multiplying $(-23)_{10}$ and $(7)_{10}$. (7 Marks)
   ii. Write the re-coded value of the multiplier. How many passes have no Arithmetic operation? (3 Marks)

3. Perform the following Floating point operation on the numbers $(356.65)_{10}$ and $(222.75)_{10}$. [10]
   i. Convert the above numbers into the normalized notation of binary format. (3 marks)
   ii. Perform subtraction operation for the given numbers and write the normalized result in IEEE-754 double precision format.(7 marks)

4. i. Assume a stack-oriented processor that includes the stack operations PUSH and POP. Arithmetic operations automatically involve the top one or two stack elements. Begin with an empty stack and illustrate the contents of the stack after each instruction. (5 marks) [10]

   PUSH 5
   PUSH 16
   PUSH 2
   PUSH 6
   ADD
   DIV
   MUL
   PUSH 3
   DIV

ii. You are on the design team for a new processor. It is decided that this processor's clock must run at 2 GHz. Assume that the programs that would be executed on this processor would typically consist of 30% of load and store instructions, 60% of arithmetic and logical instructions, and 10% branching instructions. If each of these classes of instructions requires 6, 2, and 5 clock cycles, respectively, calculate the CPI and the MIPS rating of this processor. (5 marks)

5. A company needs to find out which of its two processors would require less time to execute the instruction, MUL R1, [R2], R3. The first processor has a single internal processor bus, while the second processor has three internal buses. Illustrate the architectural design of the two processors and provide the control steps involved in fetching and executing the above instruction with both processors. (10 marks) [10]

6. Consider a 2-way set associative cache with a total of 12 cache blocks. The main memory block requests are as follows: [10]

   10, 55, 11, 4, 13, 8, 132, 129, 212, 129, 64, 8, 48, 32, 73, 92

   Calculate the number of misses and the miss ratio if the replacement strategy is

   i. Least Recently Used (LRU) (5 marks)

   ii. First In First Out(FIFO) (5 marks)

7. In a DMA transfer, there are 2 devices placing bus requests. Device A has ID 5 and Device B has ID 8. Identify the device that becomes the bus master and Illustrate the distributed arbitration process with appropriate diagram. [10]

8. Consider an 8-bit word $(01111101)_2$ transmitted as $(0\dot{1}\dot{1}\dot{1}\dot{1}\dot{1}\dot{1}\dot{1})_2$. [10]

   i. Draw the layout of data bits and calculate the check bit for storing and retrieving the given data.(5 marks)

   ii. Using hamming code, show the steps involved in error detection and apply the correction if any for the same.(5 marks)

9. An E-Commerce application like Flip kart demands zero downtime and maintains payment-based sensitive data. How will you ensure the reliability, availability, and redundancy of the data if the server crashes out? Explain the Hybrid RAID level suitable for this application with an appropriate diagram. [10]

10. Consider the two instructions : [10]

    I1 : Add R1, R2, R3

    I2 : Shift left R3

    i. Draw the timing diagram for a 4-stage pipeline. (5 marks)

    ii. Identify the number of stalls due to data dependencies and show how they are handled using the operand forwarding scheme. (5 marks)

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