Reg. Number:

Vellore Institute of Technology
CHENNAI

Continuous Assessment Test (CAT) – I - August 2024

Programme	:	B. Tech CSE Specialization (BDS)	Semester	:	Fall 24-25
Course Code & Course Title	:	BCSE205L & Computer Architecture and Organization	Class Number	:	CH2024250100676
Faculty	:	Dr. Linda Joseph	Slot	:	E1+TE1
Duration	:	1.30 Hrs	Max. Mark	:	50

Q. No.	Sub-division	Question Text	Marks
1		An architecture involving an arithmetic unit with a shared memory is assigned to add two numbers stored in a memory location. The first number loaded into the accumulator is $(13)_{10}$ and the second numberloaded into one of the registers is $(6)_{10}$. (i) Formulate the sequence of operations that the control unit must perform to calculate the sum and store the result back into the memory. (7 Marks) (ii) Provide a brief justification on whether the architecture can be modified to handle the instructions and data? (3 marks)	10
2		(i) Identify the appropriate processor design for the provided instructions and discuss their advantages and disadvantages in detail.[8 marks] Note:The memory address is given in [row]:[col] wise as shown below. LOAD A,1:1 LOAD B,2:1 PROD A,B STOR 1:1,A (ii) Identify an alternative processor design capable of processing with fewer instructions, and discuss its advantages. [2 marks]	10
3		(i) Show the step-by-step computational steps for multiplying the given numbers $(-15)_{10}$ X $(6)_{10}$ with the bit pair recoding algorithm.[8 marks] (ii) Outline the challenges the algorithm addresses to enhance the multiplication accuracy of signed and unsigned numbers. [2 marks]	10

4		With a neat hardware implementation of binary division, (i) Provide a step-by-step sequence of how restoring algorithm divides a binary dividend $(11)_{10}$ by a binary divisor $(3)_{10}$ [6 marks] (ii) Discuss the advantages and disadvantages of the above algorithm. [4 marks]	10

5		i) Identify the addressing mode used in the following instructions and provide a brief description of each. (5 marks)
		
		Load R4,30(R1)
		Move R4,#2000
		Store R4, 50(R1,R2)
		Move R4,–(R2)
		Move R4,(R1)+
		
		ii) Determine the effective address of the memory operand for the above instructions. Note: The registers R1 and R2 contain decimal values 1400 and 5600 respectively. (5 marks)
			10

********All the best**********