VIT
Vellore Institute of Technology
CHENNAI

Reg. Number:	

Continuous Assessment Test (CAT) – II–October 2024

Programme	:	B.Tech Electronics and Computer Engineering (BLC)	Semester	:	FALL 24-25
Course Code & Course Title	:	BCSE205L &Computer Architecture and Organization	Class Number	:	CH2024250101399 CH2024250101395
Faculty	:	Dr. VAIDEHI VIJAYAKUMAR Dr. M. VIDHYALAKSHMI	Slot	:	F2+TF2
Duration	:	1.30 Hrs	Max. Mark	:	50

Q. No.	Sub-division	Question Text	Marks
1		Consider a multi cycle data path architecture system. Assume the processor wants to execute the following instructions in the given order ADD R1, R2 STORE (R2), R1 Explain the sequence of control operations involved in the execution of the above instructions with a neat process flow diagram.	10
2		In an agricultural automation system, the memory requirement is 64 KB RAM and 32 KB ROM. The system uses 8 KB RAM and ROM chips, and a 16-bit address bus (0000 to FFFF hex). RAM starts at 0000, and ROM follows. (i) How many RAM and ROM chips are needed? (2 marks) (ii) Provide a memory map with address ranges for each RAM and ROM chip. (4 marks) (iii) Design an address decoding circuit and list the required components. (4 marks)	10
3		An autonomous car's control unit uses a fully associative cache with 16 blocks (8 words/block) and a 65,536-word main memory. The cache is initially empty, with a 40 ns access time and 1 µs block transfer time. The car executes instructions from memory locations 20 to 45 and repeats the loop from locations 28 to 45 four times. (i) Calculate the cache hit ratio based on the instruction sequence. (3 marks) (ii)Compute the total execution time, considering cache hits, misses, and block transfer times. (3 marks) (iii)If the cache was instead 2-way set associative with the same block size, how would the hit ratio and total execution time change? (4 marks)	10
4		Consider a Direct Memory Access module needs 3×10^3 bits/second to transfer data into the Main Memory. The CPU fetches instructions from the main memory at the rate of 10^6 instructions per seconds. For a given module execution, the CPU and DMA need to access the Main Memory at the same time. i) Suggest an appropriate technique which would be allowing I/O controllers to read or write Main Memory without CPU intervention. (7 Marks)	

		ii) Justify how DMA can improve I/O Speed during data transfer? (3 Marks)	10
5		(i) Three network servers, X, Y, and Z, are connected to a central router. Servers Y and Z have the same priority, while server X has a higher priority. Illustrate pictorially how the servers will be arranged if the router has two data request lines and two data acknowledgment lines, and if requests from server Y must be processed before server Z. Justify your answer. (5 Marks). (ii) Assume that the processor is executing the following program: **Address** | 200 | Load X, 25 201 | Load Y, 15 202 | Mul X, Y 203 | Store 300, X 204 | Load Z, 5 205 | Div X, Z 206 | HLT When executing the instruction at address 202, the processor is interrupted by a device. List the subsequent steps the processor takes assuming the interrupt is a vectored interrupt. What would change if it were a non-vectored interrupt? (5 Marks)	10

********All the best**********