VIT®

Vellore Institute of Technology

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Reg. No. :

Final Assessment Test(FAT) - Nov/Dec 2024

Programme	B.Tech.	Semester	Fall Semester 2024-25
Course Code	BCSE205L	Faculty Name	Prof. Aswiga
Course Title	Computer Architecture and Organization	Slot	F1+TF1
		Class Nbr	CH2024250102314
Time	3 hours	Max. Marks	100

General Instructions

- Write only Register Number in the Question Paper where space is provided (right-side at the top) & do not write any other details.

Course Outcomes

1. Differentiate Von Neumann, Harvard, and CISC and RISC architectures. Analyze the performance of machine with different capabilities. Recognize different instruction formats and addressing modes. Validate efficient algorithm for fixed-point and floating-point arithmetic operations.
2. Explain the importance of hierarchical memory organization. Able to construct larger memories. Analyze and suggest efficient cache mapping technique and replacement algorithms for given design requirements. Demonstrate hamming code for error detection and correction.
3. Understand the need for an interface. Compare and contrast memory mapping and IO mapping techniques. Describe and Differentiate different modes of data transfer. Appraise the synchronous and asynchronous bus for performance and arbitration.
4. Assess the performance of IO and external storage systems. Classify parallel machine models. Analyze the pipeline hazards and solutions.

Section - I

Answer all Questions (10 × 10 Marks)

*M - Marks

Q.No	Question	*M	CO	BL
01.	Assume that the Program Counter (PC) is set to 4120 at the start of the execution process. The following instructions are stored in the system where the syntax consists of an opcode followed by the destination register followed by one or two source registers. At memory address 4120, Store R3, (R15) instruction is located. At memory address 4124, Add R2, R1, R4 instruction is stored. At memory address 4128, Sub R5, R7, R6 instruction is available. The initial values of the source registers are as follows: R1 is set to 5, R4 is set to 10, R6 is set to 5, R7 is set to 10, R15 contains 200 and, value 50 is stored at address 200. i) How will the processor fetch and execute the instructions using RISC architecture? After completing the execution, Specify the content of all registers involved. [5 Marks] ii) Design two distinct architectures for the above instruction execution. One design allowing concurrent access of instructions and data, and in contrast, the second should allow for sequential access. Identify the performance bottlenecks and the impact of execution flow in each architecture. [5 Marks]	10	1	4

02.	Perform restoring division method on the dividend $(50)_{10}$ and the divisor $(-15)_{10}$. i) Find out the values of accumulator A and register Q at the end of the last step. i.e When Step Count SC=1 ? [6 Marks] ii) How many restoring takes place during the division? [2 Marks] iii) State the quotient and the remainder in decimal with the inclusion of signs [2 Marks]	10	1	3
03.	i) In a hardware designing company, a manager assigned his team to perform Binary Floating-Point addition on $(26.25)_{10}$ and $(5.50)_{10}$. What are the various intermediate steps the team will consider to perform the addition operation to produce the result? [5 Marks] ii) Represent $(-145.50)_{10}$ in IEEE double precision format. [5 Marks]	10	1	3
04.	i) Identify the addressing mode used in each of the following instructions and comment on the pros and cons of these modes. [5 marks] a) STORE $[1000_H]$ b) SUB [R1] c) OR R1, R2, R3 d) CMA e) LOAD 4000_H ii) Write a step by step control sequence for the given instruction with a single data path architecture. [5 Marks] SUB R4, R1, R2 # performs subtraction and stores the result in R4.	10	2	4
05.	Consider a 2-way set associative mapped cache of with 16 lines. Which of the following memory blocks will be in the cache at the end of the sequence? 3, 5, 2, 8, 0, 6, 3, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24 i) Apply LRU as the replacement strategy. [6 Marks] ii) Calculate the hit ratio and miss rate.[4 Marks]	10	2	3
06.	i) Assume that you have a processor for performing an image classification task. The java code for this image processing task consists of different instruction types and its corresponding cycles per instruction is listed in the table below. Calculate the CPI for this image processing task? (4 Marks)	10	3	3

Type of Instruction	Frequency	Cycles
ALU	50%	4
Load	20%	5
Store	15%	3
Branch	15%	3

ii) Suppose you are asked to design two different systems that can perform image processing and classification together. If system A takes 3ns clock cycle time and CPI of 2 whereas system B takes 4 ns clock cycle time and CPI of 3, then identify which system is faster for this image classification task and by how much? (3 Marks)

iii) A computer programmer is trying to decide between two code sequences for a particular image classification task that has the following instruction counts and its corresponding CPI. Identify which code sequence executes the most instructions? (3 Marks)

	Instruction Count for each instruction class			
	A	B	C	D
System A	45	25	15	15
System B	55	15	10	10
CPI	1	2	3	4

07.	i) In terms of determining access to a shared resource, describe how a single authority controls the allocation process with a neat diagram. If a system where multiple entities with ID 10, 15, 8 and 12 participate in deciding the access to the resource, Identify which device will be given access in a step by step manner with a neat diagram. [6 Marks] ii) Imagine you are designing a processor system for a high-performance computing application. Your architecture needs to support various tasks like data processing, I/O operations, and real-time data analysis by implementing a synchronous or asynchronous bus for data transfer. Which communication model would you recommend for a system primarily focused on real-time data analysis, and why? [4 Marks]	10	3	4
08.	(a) A 12-bit odd parity Hamming code sent by sender A is received as $(101101010101)_2$ by the receiver B. The decoder's job at the receiver B is to test if the received code contains a single bit error or not. Trace the approach in which the decoder checks this code for an error. If an error is detected, find the location of the error bit and also the corrected Hamming code? (6 marks) (b) The data bits $(100110)_2$ are stored in the memory with check bits $(1001)_2$. When the data is retrieved from the memory, the check bits are derived to be $(1100)_2$. If an even parity is used, detect if there is an error in the retrieved data and give the retrieved data bits. (4 marks)	10	4	3
09.	A growing start-up is looking to implement a RAID system in its infrastructure to enhance data storage reliability and performance. As the consultant tasked with this project, how you will implement various RAID levels for the below tasks, Justify your answer with neat sketch. i) Design a RAID level that significantly speeds up read and write operations for storing large media files. Ensure that it does not provide any data redundancy. In contrast, identify the approach to access the lost data with minimum cost. [3 Marks] ii) Design a RAID that uses bit level, byte level and block level striping method for a research laboratory that requires data integrity for storing their critical science experiments. [3 Marks] iii) Design a RAID with distributed parity level for an e-commerce company that relies heavily on its database for inventory management and customer transactions. Ensure that the company's critical data remains safe even in the event of multiple drive failures. [4 Marks]	10	4	4

10.	Consider the following instructions where the syntax consists of an opcode followed by the destination register followed by one or two source registers.
	Sub R2, R1, R3
	And R12, R2, R5.
	Or R13, R6, R2.
	Add R14, R13, R2.
	Justify which type of dependency is present in the above instructions and also specify the possible solutions to overcome the hazard encountered.[10 marks]
		10	4	4

BL-Bloom's Taxonomy Levels - (1.Remembering, 2.Understanding, 3.Applying, 4.Analysing, 5.Evaluating, 6.Creating)