VIT

Vellore Institute of Technology
CHENNAI

Reg. Number:	

Continuous Assessment Test (CAT) – II - October 2024

Programme	:	B. Tech CSE Specialization in BDS	Semester	:	Fall 24-25
Course Code & Course Title	:	BCSE205L & Computer Architecture and Organization	Class Number	:	CH2024250100678
Faculty	:	Dr. Linda Joseph	Slot	:	E2+TE2
Duration	:	1.30 Hrs	Max. Mark	:	50

Q. No.	Question Text	Marks
1.	A subset of the MIPS instruction set consists of the {add, sub- Arithmetic Operations, lw, sw- load and store operations, beq, j- branch if equal and jump} (i) Design a single bus Datapath involving a register bank, CPU, ALU, MUX-2 Numbers, Data Memory, control lines and the corresponding control signals. (4 marks) (ii) Formulate the complete execution with the control sequence for R-type instructions. (4 marks) (iii) Show how unconditional branching instructions could be formulated with the control sequences. (2 marks)	10
2.	Consider a direct mapped cache with 4 cache blocks. The main memory consists of 16 blocks. Each block can hold 1 word. The cache uses the following sequence of memory requests (in decimal): 0,1,2,3,4,1,2,0,5,6,0,4,1,2,3,5 (i) Determine which cache block/line each memory block maps to. (3 marks) (ii) Simulate the sequence of memory accesses and calculate the number of hits and misses. (4 marks) (iii) Identify when replacement occurs based on the direct mapped cache policy. (3 marks)	10
3.	Consider a system with the following specifications: Main Memory Size: 64 MB x 16 Word Size: 16 bits Fully Associative Cache with a block size of 64 bytes: 32 KB 1000 1000000 $10^3 \times 10^3 = 10^6$ $10^3 \times 10^3$ $2^{10} \times 2^{10}$	10

	(i) Determine the total number of words that can be stored in the RAM. (2 marks) (ii) Determine the number of blocks in the cache and main memory. (4 marks) (iii) Determine the number of bits required for the tag, the index (line number) and the block offset. (4 marks)	
4.	You are a system architect designing a new embedded system for a digital camera. The camera is expected to capture high-resolution images and videos, which will require significant data transfer from the image sensor to the main memory. The main features of the camera include: High-resolution image sensor: Captures images at 24 MP (megapixels), Video recording capability: Supports 4K video recording at 30 frames per second (fps), Memory: 32 GB of RAM to temporarily store images and videos before processing, Processing Unit: A microcontroller with limited processing power, focusing on low power consumption. (i) How would implementing DMA benefit the data transfer from the image sensor to memory in this camera system? (5 marks) (ii) Indicate which mode of data transfers could be preferred for the DMA controller in this scenario. Discuss in brief with a neat diagram. (5 marks)	10
5	Imagine a computer system where multiple devices including a CPU, a GPU and a network interface card (NIC) need to communicate with the main memory through a shared bus. The system uses a priority-based bus arbitration scheme. The CPU has the highest priority, followed by the GPU and then the NIC. During heavy load, all three devices request access to the bus simultaneously to perform read/write operations. (i) Identify the device which will get the bus access first and why? (3 marks) (ii) Examine what happens to the other devices requests during this time? (3 marks) (iii) How does the arbitration change if the CPU is continuously requesting the bus while the GPU and NIC also have high-priority operations pending? Give remedial solutions. (4 marks)	10

********All the best**********