VIT®

Vellore Institute of Technology

(Deemed to be University under section 3 of the UGC Act, 1956)

Reg. No. :

Final Assessment Test (FAT) - May 2024

Programme	B.Tech.	Semester	WINTER SEMESTER 2023 - 24
Course Title	BASIC ELECTRICAL AND ELECTRONICS ENGINEERING	Course Code	BEEE102L
Faculty Name	Prof. Aravind C K	Slot	Y11+Y12+Y21
		Class Nbr	CH2023240503677
Time	3 Hours	Max. Marks	100

General Instructions:

- Write only Register Number in the Question Paper where space is provided (right-side at the top) & do not write any other details.

Answer all questions (10 X 10 Marks = 100 Marks)

01. Using node voltage analysis, estimate the voltages at various nodes and current through each branch in the circuit shown in Fig.1. [10]

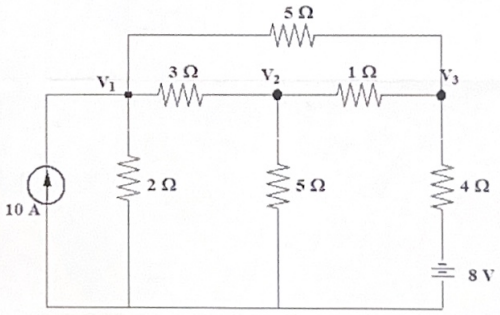

Fig. 1.

02. Calculate the equivalent resistance across terminals A and B shown in Fig.2. [10]

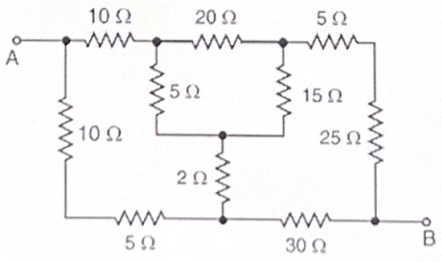

Fig.2.

03. Explain the distinct functions of grounding and earthing in Electrical installations. Elaborate on the critical role of earthing in ensuring electrical safety and how earthing specifically mitigates the risk of electric shock. [10]

04. In the circuit of Fig. 3 at a frequency of 500 Hz, the current lags the voltage by 50°. Find the resistor(R) and the voltage across each circuit element and also draw the phasor diagram. [10]

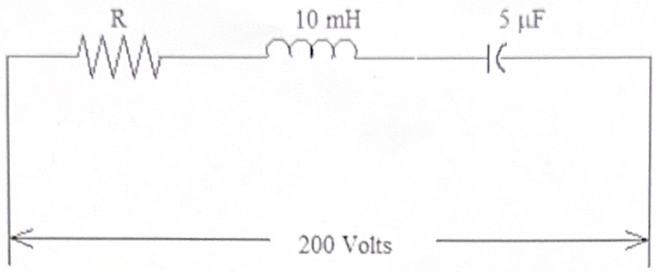

Fig. 3.

05. An iron rod of 1 cm radius is bent to a ring of mean diameter 30 cm and wound with 250 turns of wire as shown in Fig. 4. Assume the relative permeability of iron as 800. An air gap of 0.1 cm is cut across the bent ring. Calculate the current required to produce a useful magnetic flux of 20,000 lines. Neglect leakage. [10]

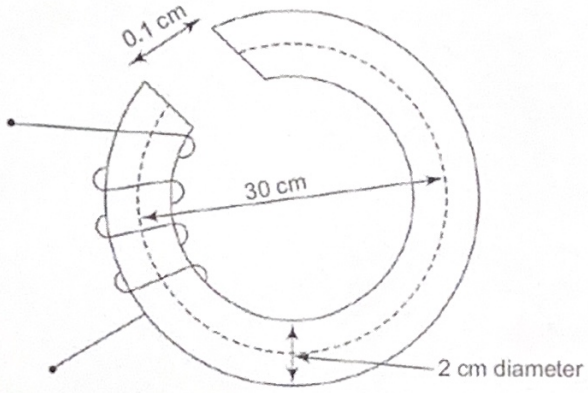

Fig. 4

06. With the aid of clear diagrams, explain the construction and working principle and operation of an electrical machine that converts DC electrical energy into mechanical energy. [10]

07. Draw a logic circuit, incorporating any gates of your choice, which will produce an output 1 when its two inputs are different. Also, draw the same logic circuit incorporating only NOR gates. [10]

08. Plot the logical expression on a four-variable Karnaugh map. Obtain the simplified expression and implement the real minimal expression in logic gates. [10]

$$F(A,B,C,D)=ABCD+A\overline{B}\,\overline{C}\,\overline{D}+A\overline{B}C+AB$$

09. Draw the circuit diagram of the basic inverting amplifier configuration. Give an expression for the closed-loop voltage gain of the circuit in terms of the resistances, assuming an ideal op amp. Give expressions for the input impedance and output impedance of the circuit. [10]

10. Explain the biasing conditions required for a BJT to operate in the common emitter configuration. How do these biasing conditions affect the transistor's operation? [10]