Reg. Number:

VIT

Vellore Institute of Technology
CHENNAI

Continuous Assessment Test (CAT) – I - AUGUST 2024

Programme	:	B.Tech CSE & CSE all Specializations	Semester	:	FALL 24-25
Course Code & Course Title	:	BCSE205L - Computer Architecture and Organization	Slot	:	C2+TC2
Faculty	:	Prof.M. Nivedita, Dr. J. Padma Dr. Smrithy, Dr. M. Vidhya Lakshmi	Class Number	:	CH2024250100949/ CH2024250100953/ CH2024250102441/ CH2024250100985
Duration	:	1 ½ hours	Max. Mark	:	50

Answer all questions

No	Sub Sec.	Description	Marks
1	a	A Computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has an operation code, a register code part to specify one of 64 registers, and an address part. i. How many bits are there in the operation code, the register code part, and the address part? (2 Marks) ii. Draw the instruction word format. (2 Marks) iii. How many bits are there in the data and address memory inputs? (1 Mark)	05
	b	Elaborate on the work of von Neumann architecture for the given code with a sketch of the IAS computer structure. LDA R1 MUL R2 ADD R3 STA 400 Assume R1, R2, R3 are general-purpose registers	05
2		Write an instruction cycle procedure for the assembly code of the IAS architecture using the instructions set found in the reference (Reference to Question No. 1.b).	10
3		Prove that the multiplication of two n-digit signed numbers in base 2 gives a product of a number more than 2n digits with (+11) * (-6)	10
4	a	Perform division for the dividend value 11 and divisor value 3 by using the restoring method (considering the number of bits as 5).	7
	b	Convert $(1259.125)_{10}$ to IEEE 754 single precision Floating point number	3

5		Evaluate the effective address and operand value for the following addressing mode (a) Direct (b) Indirect (c) Index (d) Register indirect (e) Auto Decrement from the following memory diagram [5 X2 =10]	10