



Continuous Assessment Test (CAT) – I - August 2024

Programme	: B. Tech CSE Specialization (BDS)	Semester	: Fall 24-25
Course Code & Course Title	: BCSE205L & Computer Architecture and Organization	Class Number	: CH2024250100678
Faculty	: Dr. Linda Joseph	Slot	: E2+TE2
Duration	: 1.30 Hrs	Max. Mark	: 50

Q. No.	Sub-division	Question Text	Marks																																				
1		<p>i) A typical processor processes each instruction cycle as two sub cycles and the size of each instruction being 40 bits in word length. For the given pseudocode:</p> <pre>BEGIN NUMBER s1, s2, sum INPUT s1, s2 sum=s1+s2 OUTPUT sum END</pre> <p>Trace the contents of different registers namely the Program counter, Memory address register, Memory buffer register, Instruction register, Instruction buffer register and Accumulator. [7 marks]</p> <p>ii) Provide valid justifications for why a memory buffer register may be necessary in this architecture. [3 Marks]</p>	10																																				
2		<p>The given diagram below depicts the storage scheme of a generic computer. Use the instructions LOAD, STORE, PROD and MULT to find out the product of two numbers and then store the result back in to a memory location.</p> <div style="text-align: center;"><table border="1" style="display: inline-table; margin-right: 20px;"><tr><td></td><td>1</td><td>2</td><td>3</td><td>4</td></tr><tr><td>1</td><td></td><td></td><td></td><td></td></tr><tr><td>2</td><td></td><td></td><td></td><td></td></tr><tr><td>3</td><td></td><td></td><td></td><td></td></tr><tr><td>4</td><td></td><td></td><td></td><td></td></tr><tr><td>5</td><td></td><td></td><td></td><td></td></tr></table><div style="display: inline-block; text-align: center; vertical-align: middle;">\longleftrightarrow<table border="1" style="display: inline-table; margin-right: 20px;"><tr><td>A</td><td>D</td></tr><tr><td>B</td><td>E</td></tr><tr><td>C</td><td>F</td></tr></table>\longleftrightarrow<div style="border: 1px solid black; width: 100px; height: 100px; display: inline-block;"></div></div><div style="display: flex; justify-content: space-around; margin-top: 10px;">Main MemoryRegistersExecution Unit</div></div>		1	2	3	4	1					2					3					4					5					A	D	B	E	C	F	10
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		simple and a complex instruction set with a neat architecture diagram. [7 marks]																							
		(ii) Differentiate the advantages and disadvantages of the above approaches. [3 marks]																							
3		(i) Using the floating-point arithmetic, sum up the numbers $(0.75)_{10}$ and $(-0.275)_{10}$ in binary and show how the output is stored using the IEEE single precision format. [8 Marks] (ii) Determine whether there is any overflow or underflow for the computed output. [2 Marks]	10																						
4		(i) Perform non-restoring binary division for computing the quotient and the remainder of Dividend: $(1011)_2$ and Divisor: $(0101)_2$. [7 Marks] (ii) List out the differences between the restoring and non-restoring division methods. [3 Marks]	10																						
5		<p>Calculate the Effective address and content of the accumulator for the instruction "Move to AC" given the following addressing modes: Immediate, Register Indirect, Direct, Indirect and Index Address.</p> <table border="1"><thead><tr><th>Memory Location</th><th>Memory Content</th></tr></thead><tbody><tr><td>1000</td><td>0200</td></tr><tr><td>1200</td><td>1800</td></tr><tr><td>1400</td><td>1234</td></tr><tr><td>1500</td><td>ADD AC, [1200]</td></tr><tr><td>1600</td><td>8500</td></tr><tr><td>1800</td><td>2720</td></tr><tr><td>1900</td><td>3000</td></tr><tr><td>2000</td><td>Move to AC</td></tr><tr><td>2002</td><td>INZ 1500</td></tr><tr><td>2004</td><td>MUL (1000)</td></tr></tbody></table> <p>Default Mode = Register</p> <p>R1 <input type="text" value="1900"/> PC <input type="text" value="2000"/> INDEX <input type="text" value="0200"/></p>	Memory Location	Memory Content	1000	0200	1200	1800	1400	1234	1500	ADD AC, [1200]	1600	8500	1800	2720	1900	3000	2000	Move to AC	2002	INZ 1500	2004	MUL (1000)	
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***** All the best*****