Lab A3

Tutorial Group TT01

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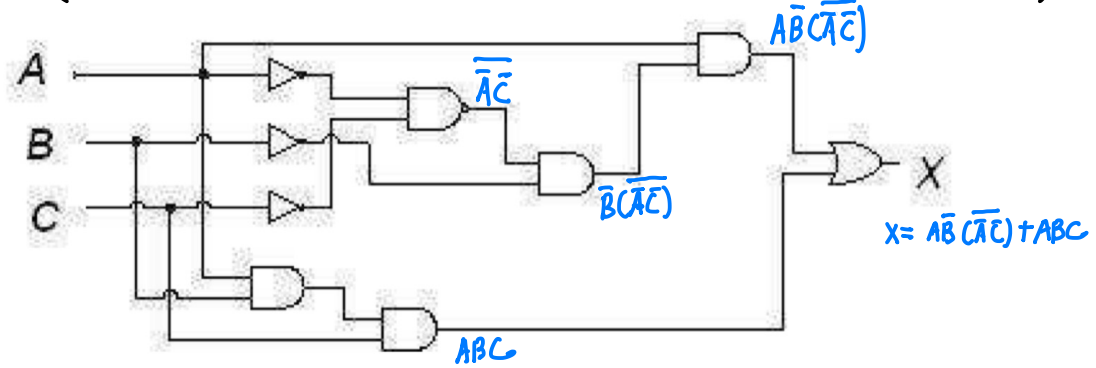
1. (i) Identify the Boolean expression for the given logic diagram and obtain the truth table



1)(i)

$X = A\bar{B}(\bar{A}\bar{C}) + ABC$

Inputs			Output					
A	B	C	ABC	$\bar{A}\bar{C}$	$\bar{A}\bar{C}$	$\bar{B}(\bar{A}\bar{C})$	$A\bar{B}(\bar{A}\bar{C})$	X
0	0	0	0	1	0	0	0	0
0	0	1	0	0	1	1	0	0
0	1	0	0	1	0	0	0	0
0	1	1	0	1	0	0	0	0
1	0	0	0	0	1	1	1	1
1	0	1	0	0	1	1	1	1
1	1	0	0	0	1	0	0	0
	1	1	1	0	1	0	0	1

(ii) Simplify the identified expression using the Boolean rules, laws and theorems. Draw the truth table for the simplified Boolean expression. **Construct the circuit only for the simplified expression and verify the truth table experimentally.**

(ii) $X = A\bar{B}(\bar{\bar{A}}\bar{\bar{C}}) + ABC$

$= A\bar{B}(\bar{A} + \bar{\bar{C}}) + ABC$

$= A\bar{B}(A + C) + ABC$

$= A\bar{B}A + A\bar{B}C + ABC$

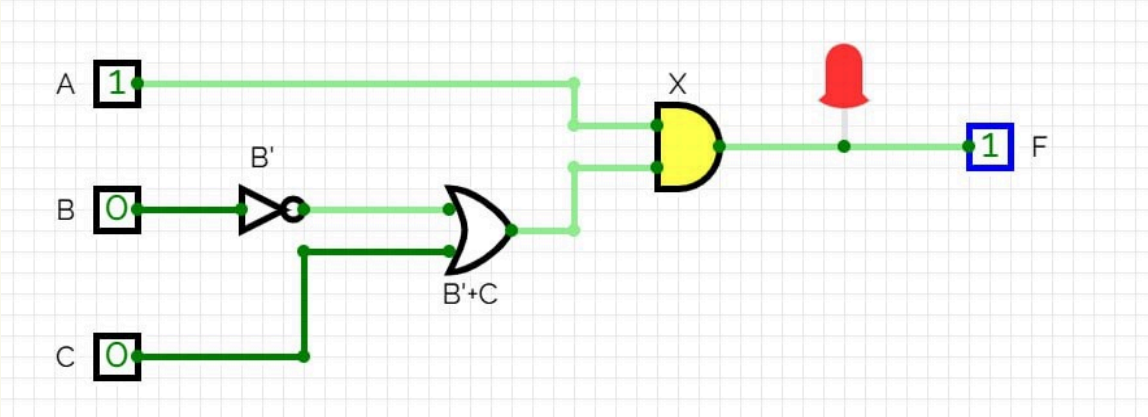
$= A\bar{B} + A(C\bar{B} + B)$

$= A\bar{B} + AC$

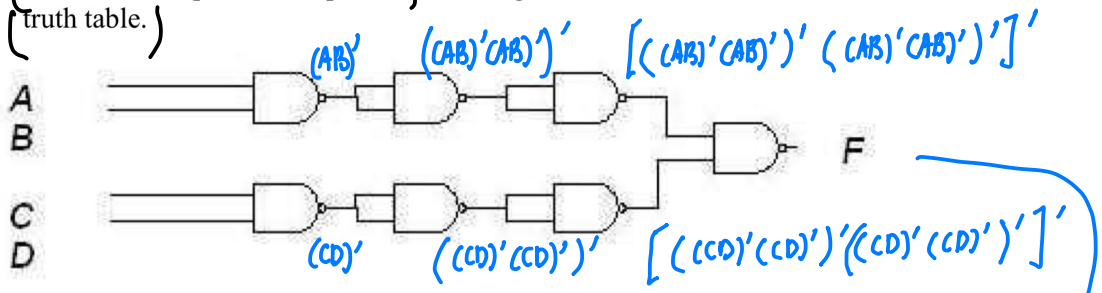
$X = A(\bar{B} + C)$

Inputs			Output		
A	B	C	$\bar{B}$	$\bar{B}+C$	X
0	0	0	1	1	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	1	0	1	0
1	0	0	1	1	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	1	0	1	1

$X = A(\bar{B} + C)$



2. (i) Obtain sum of products expression for the given NAND network and draw the truth table.



(ii) **Construct the logic diagram only by using AND/OR/NOT gates and verify the truth table experimentally**

$F=[[(AB)'(AB)')'(AB)'(AB)')']'$
$[(CD)'(CD)')'(CD)'(CD)')']']'$

2) (i)

$F=[[(AB)'(AB)')'(AB)'(AB)')']'[(CD)'(CD)')'(CD)'(CD)')']']'$

$=[[(AB)')'(AB)')']'[(CD)')'(CD)')']']$

$=[[(AB)''(AB)'']'[(CD)''(CD)'']']$

$=[[(AB)'']'[(CD)'']']'$

$=[(AB)'(CD)']'$

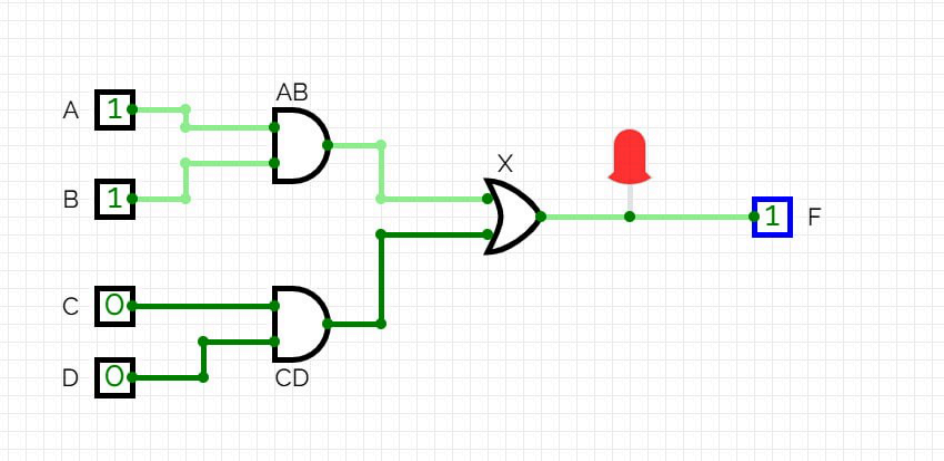
$=[(AB)']'+[(CD)']'$

$=(AB)''+(CD)''$

$F=AB+CD$ (SOP)

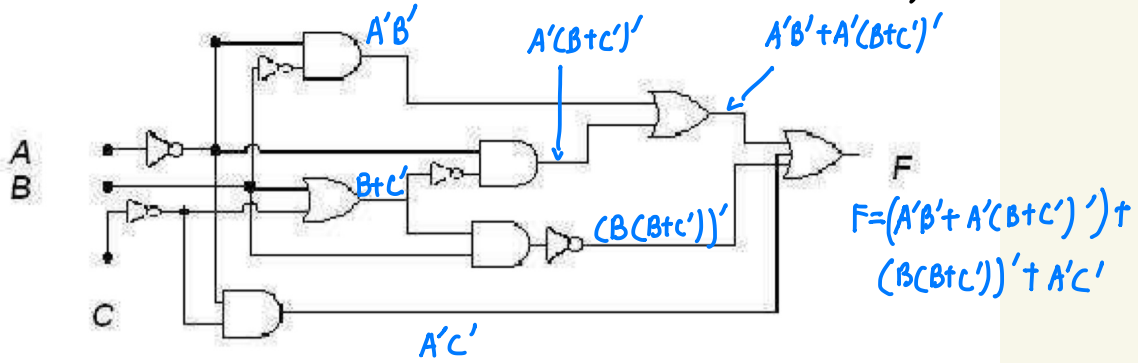
Input				Output
A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

(ii)



Input				Output
A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

3. (i) Identify the Boolean expression for the given logic diagram and obtain the truth table.



(ii) Simplify the identified expression using the Boolean rules, laws and theorems. Draw the truth table for the simplified Boolean expression. Construct the circuit for the simplified expression.

3)(i) $F = A'B' + A'(B+C')' + (B(B+C'))' + A'C'$

Inputs			Output
A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

(ii) $F = A'B' + A'CB+C')' + (BCB+C')' + A'C'$

$= A'B' + A'CB' \cdot C'') + (B' + CB+C')') + A'C'$

$= A'B' + A'B'C + (B' + (B'C'')) + A'C'$

$= A'B' + A'B'C + (B' + B'C) + A'C'$

$= A'B' + A'B'C + B' + B'C + A'C'$

$= B'(A' + A'C + 1 + C) + A'C'$

$= B'(1) + A'C'$

$F = A'C' + B'$

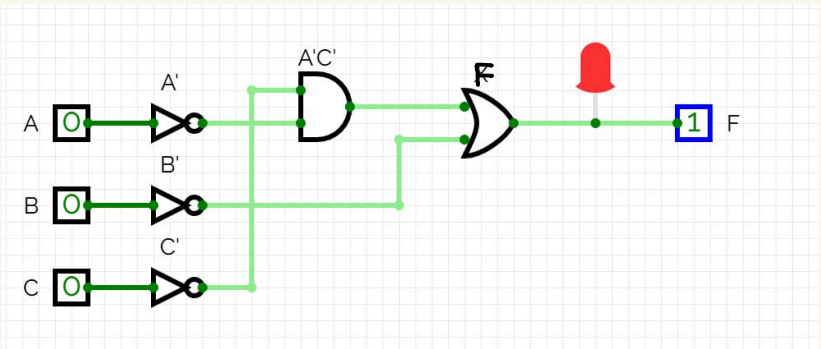
$(B+C)' = B'C'$

$(BC)' = B'+C'$

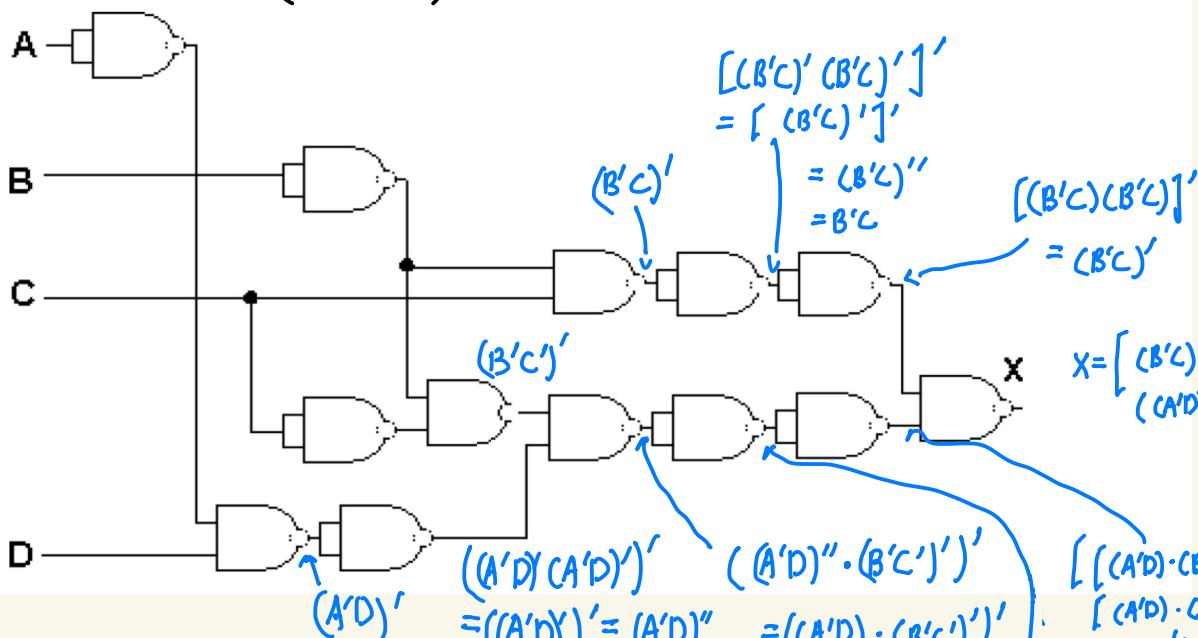
$1+A = 1$

$1(A) = A$

Inputs			Output
A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0



4. (i) Obtain sum of products expression for the given NAND network and draw the truth table
(ii) Construct the logic diagram using AND/OR/NOT gates.



4)(i) $F = \left(\left((A'D)\cdot(B'C')'\right)'\cdot(B'C)'\right)'$

$F = \left(\left((A'D)\cdot(B''+C'')\right)'\cdot(B''+C')\right)'$

$= \left((A'DB + A'DC)'\cdot(CB+C')\right)'$

$= (A'DB + A'DC)'' + (CB+C')'$

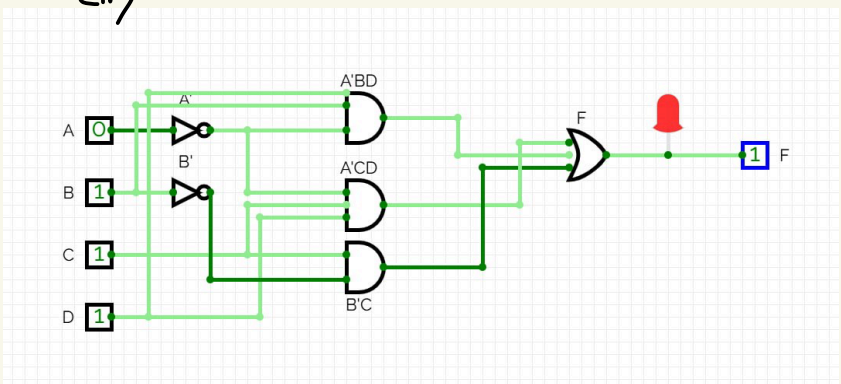
$= A'DB + A'DC + (B'C'')$

$= A'DB + A'DC + B'C$

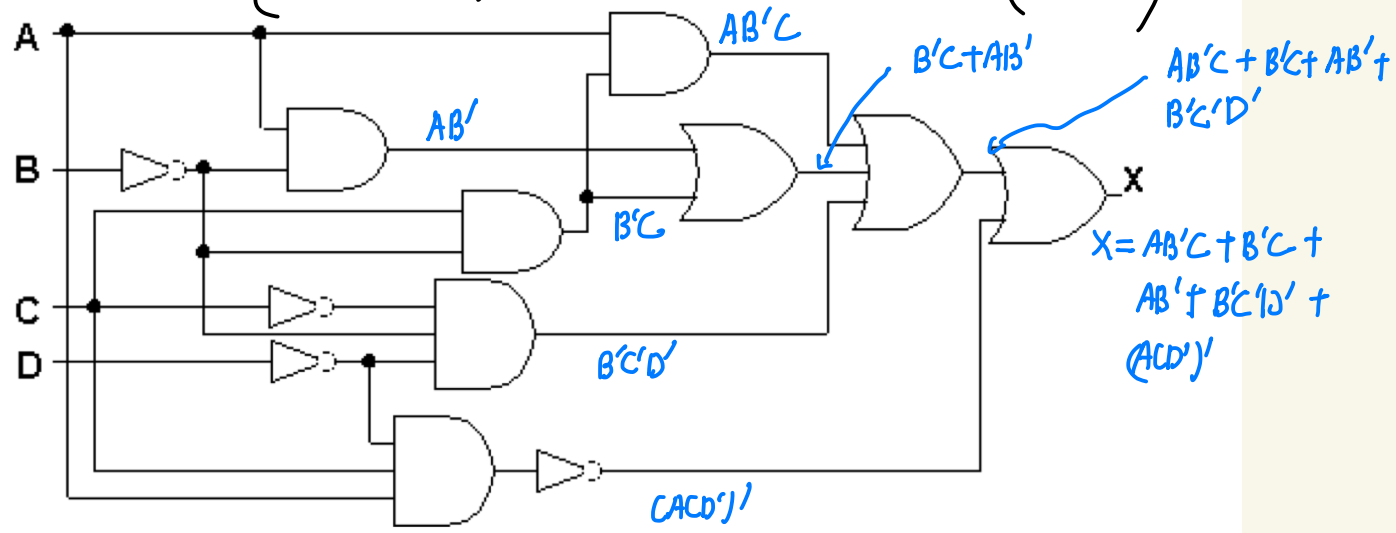
$F = A'BD + A'CD + B'C$ (SOP)

Input				Output
A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

(ii)



5. (i) Identify the Boolean expression for the given logic diagram and obtain the truth table.



(ii) Simplify the identified expression using the Boolean rules, laws and theorems. Draw the truth table for the simplified Boolean expression. Construct the circuit for the simplified expression.

5) (i) $X = AB'C + B'C + AB' + B'C'D' + (ACD')'$

Input				Output				✓ AB'C	✓ B'C	✓ AB'	✓ B'C'D'	ACD'	✓ (ACD')'	X
A	B	C	D	A'	B'	C'	D'							
0	0	0	0	1	1	1	1	0	0	0	1	0	1	1
0	0	0	1	1	1	1	0	0	0	0	0	0	1	1
0	0	1	0	1	1	0	1	0	1	0	0	0	1	1
0	0	1	1	1	1	0	0	0	1	0	0	0	1	1
0	1	0	0	1	0	1	1	0	0	0	0	0	1	1
0	1	0	1	1	0	1	0	0	0	0	0	0	1	1
0	1	1	0	1	0	0	1	0	0	0	0	0	1	1
0	1	1	1	1	0	0	0	0	0	0	0	0	1	1
1	0	0	0	0	1	1	1	0	0	1	1	0	1	1
1	0	0	1	0	1	1	0	0	0	1	0	0	1	1
1	0	1	0	0	1	0	1	1	1	1	0	1	0	1
1	0	1	1	0	1	0	0	1	1	1	0	0	1	1
1	1	0	0	0	0	1	1	0	0	0	0	0	1	1
1	1	0	1	0	0	1	0	0	0	0	0	0	1	1
1	1	1	0	0	0	0	1	0	0	0	0	1	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	1	1

$F = A' + B' + C' + D$

(ii) $X = AB'C + B'C + AB' + B'C'D' + (ACD')'$

$X = B'C(A+1) + AB' + B'C'D' + (A' + C' + D'')$

$= B'C + AB' + B'C'D' + A' + C' + D$

$= B'C + AB' + C'(B'D' + 1) + A' + D$

$= B'C + AB' + C' + A' + D$

$= B'C + C' + \underline{A'} + A\underline{B'} + D$ $\quad A + A'B = A + B$

$= B'C + C' + A' + B' + D$

$= B'(C+1) + C' + A' + D$

$= B' + C' + A' + D$

$= A' + B' + C' + D$

Input				Output			
A	B	C	D	A'	B'	C'	X
0	0	0	0	1	1	1	1
0	0	0	1	1	1	1	1
0	0	1	0	1	1	0	1
0	0	1	1	1	1	0	1
0	1	0	0	1	0	1	1
0	1	0	1	1	0	1	1
0	1	1	0	1	0	0	1
0	1	1	1	1	0	0	1
1	0	0	0	0	1	1	1
1	0	0	1	0	1	1	1
1	0	1	0	0	1	0	1
1	0	1	1	0	1	0	1
1	1	0	0	0	0	1	1
1	1	0	1	0	0	1	1
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	1