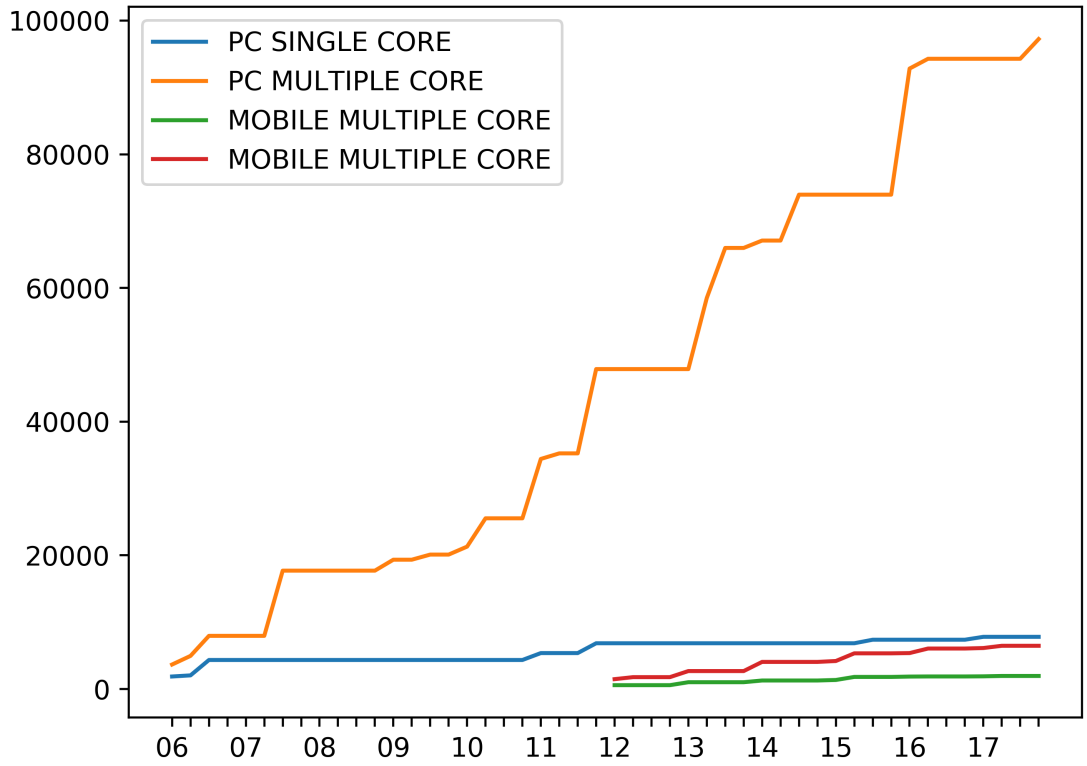
CMPE202 – HM1

NAME: Jianfeng Zhao, Email: jzhao65@ucsc.edu February 2, 2018

Qustion 1

Final Graphics:



How I get these data:

For PC:

1. first I get all CPU name from http://browser.geekbench.com/processor-benchmarks. Then get the release date from https://www.cpubenchmark.net/cpu.php?cpu=AMD+Phenom+II+X4+960T, and get the highest score of this particular CPU from http://browser.geekbench.com/geekbench3/search?dir=desc&sort=score&q= and http://browser.geekbench.com/geekbench3/search?dir=desc&sort=multicore_score&q=.
2. Get CPU name and release date from http://www.cpu-world.com/Releases/Desktop_CPU_releases_(2013).html then get highest score as above.
3. get all Intel and AMD cpu from http://browser.geekbench.com/geekbench3/search?&q=intel&page= and http://browser.geekbench.com/geekbench3/search?&q=AMD&page= then get release date from https://ark.intel.com/search?q= and https://www.cpubenchmark.net/cpu.php?cpu=AMD+Phenom+II+X4+960T

4. Totolly get millions data, then combine them together. But I realized some data is not good cause some user overclocking the CPU. Hence, I search the Score from http://browser.geekbench.com/geekbench3/search manually.

For Mobile:

1. Get CPU name and release date from http://www.cpu-world.com/Releases/Mobile_CPU_releases_(2015).html
2. Get highest score from http://browser.geekbench.com/geekbench3/search?dir=desc&sort=score&q= and http://browser.geekbench.com/geekbench3/search?dir=desc&sort=multicore_score&q=.
3. combine and deal with data.

Then plot.

All code and some data is list in https://github.com/sharpzhao/Computer_Architecture

Question 2

2.1

According to the Amdahl's Law, $f(e) = 0.25$, $Speedup(e) = 20$, hence, the over all speedup is:

$$\begin{aligned} Speedup_{all} &= \frac{1}{(1 - f(e)) + \frac{f(e)}{Speedup(e)}} \\ &= \frac{1}{(1 - 0.25) + \frac{0.25}{20}} \\ &= \frac{80}{61} \end{aligned}$$

2.2

According to Amdahl's Law, the maximum possible theoretical speedup is:

$$MaxSpeedup = \frac{1}{1 - f(x)}$$

According the the question, $f(x) = 0.4$, Hence,

$$MaxSpeedup = \frac{1}{1 - 0.4} = \frac{5}{3}$$

2.3

According to the question, $Speedup_{gpu\_cpu} = \frac{80}{61}$ and Vector can improve 20% code which means $f(e) = 0.2$, Hence, According to Amdahl's Law:

$$Speedup_{max} = \frac{1}{1 - f(x)} = \frac{5}{4} = 1.25$$

But $Speedup_{gpu\_cpu} = \frac{80}{61} = 1.31$, which is greater than 1.25. Which means this configuration will never reach the configuration of GPU-CPU configuration.

Hence, Vector to match the overall speedup of the GPU+CPU configuration in the part one is impossible.

Question 3

According to the question, instruction run like below:

1	add a3,a5,32	F0 F1 D0 X0 W0
2	lw a4,0(a5)	F0 F1 D0 X0 X1 X2 W0
3	addw a1,a1,a4	F0 F1 D0 D0 D0 X0 W0
4	add a5,a5,4	F0 F1 F1 F1 D0 X0 W0
5	bne a5,a3,.L2	F0 F0 F0 F1 D0 X0 W0
6	lw a4,0(a5)	/ / / / / F0 F1 D0 X0 X1 X2 W0
7	addw a1,a1,a4	F0 F1 D0 D0 D0 X0 W0
8	add a5,a5,4	F0 F1 F1 F1 D0 X0 W0
9	bne a5,a3,.L2	F0 F0 F0 F1 D0 X0 W0
10	lui a0,%hi(.LC1)	/ / / / / F0 F1 D0 X0 W0

Because Load instruction need to takes 3 cycle. Line 2 need 3 cycles to excute load word.

Also, this data hazerd can be solute by data forwarding. Hence, line 3 need to wait in Instruction Decode for 2 cycles. line 4, 5 also need to wait 2 cycles in F1 and F0 individually.

As well as RISCV ISA don't have delay slot, therefor, in line 6, CPU must stall for 5 cycles to wait the answer of instruction BNE.

BNE will one taken instruction. So, we loop one time.

Finally, cycle of every instruction as below:

Instruction		F	D	X	W
add	a3,a5,32	1, 3	3, 4	4, 5	5, 6
lw	a4,0(a5)	2, 4	4, 5	5, 8	8, 9
addw	a1,a1,a4	3, 5	5, 8	8, 9	9, 10
add	a5,a5,4	4, 8	8, 9	9, 10	10, 11
bne	a5,a3,.L2	5, 9	9, 10	10, 11	11, 12
lw	a4,0(a5)	11, 13	13, 14	14, 17	17, 18
addw	a1,a1,a4	12, 14	14, 17	17, 18	18, 19
add	a5,a5,4	13, 17	17, 18	18, 19	19,20
bne	a5,a3,.L2	14, 18	18, 19	19, 20	20, 21
lui	a0,%hi(.LC1)	20, 22	22, 23	23, 24	24, 25