Open

fir.v
~/Desktop/fir

Save

```
module fir(clk,x,y);
 input clk;
 input signed [15:0] x;
 output signed [31:0] y ;
 parameter signed [15:0] b0 = 16'h1000;
 parameter signed [15:0] b1 = 16'h2000;
 parameter signed [15:0] b2 = 16'h3000;
 parameter signed [15:0] b3 = 16'h2000;
 parameter signed [15:0] b4 = 16'h1000;
 reg signed [15:0] xde [3:0];
 wire signed [31:0] yt;
 assign y_temp = (b0 * x) + (b1 * xde[0]) + (b2 * xde[1]) + (b3 * xde[2]) + (b4 * xde[3]);
 assign y = yt;
 always @(posedge clk) begin
 xde[3] <= xde[2];
 xde[2] <= xde[1];
 xde[1] <= xde[0];
 xde[0] <= x;
 end
endmodule
```

Open

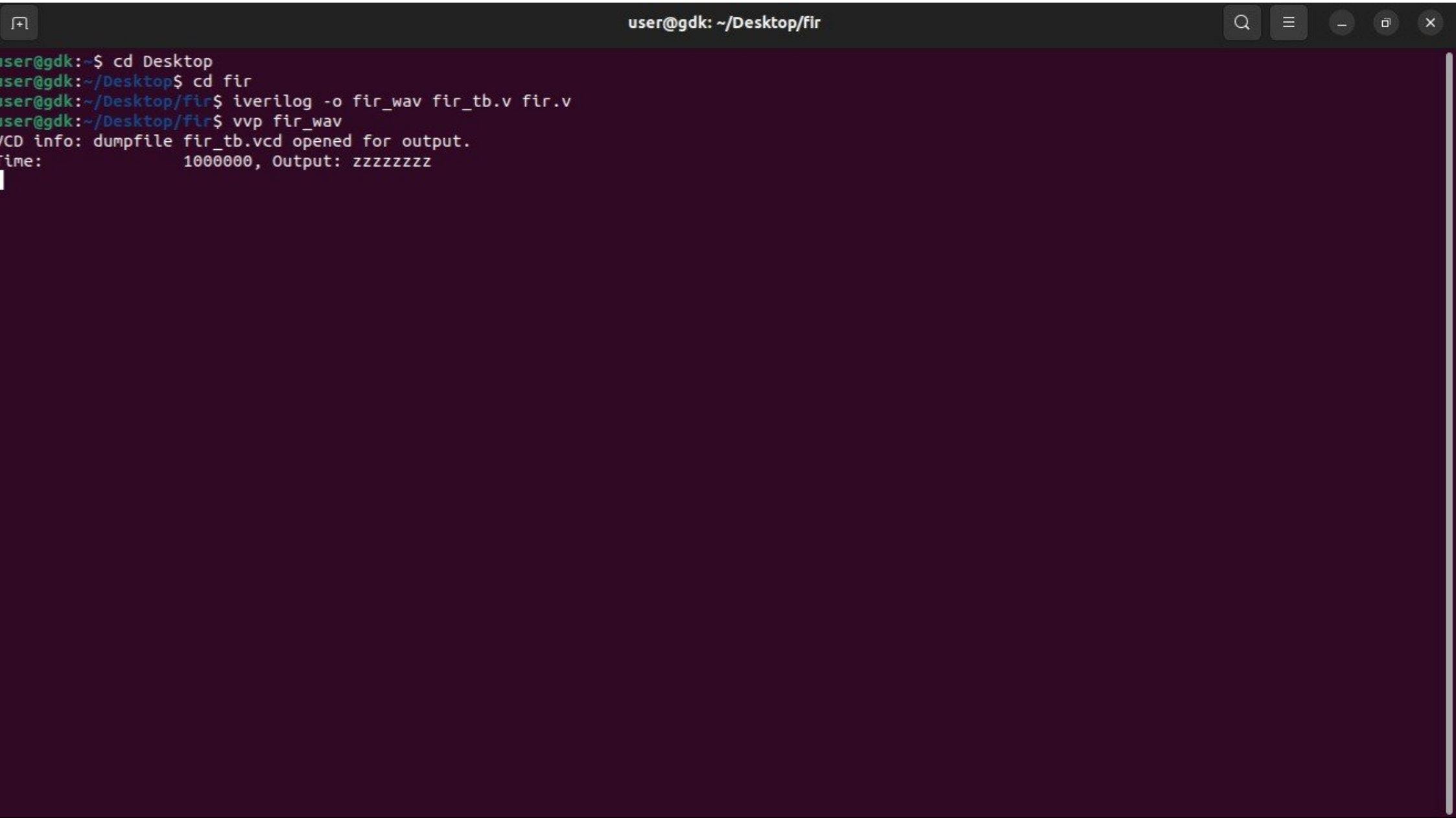
fir_tb.v
~/Desktop/fir

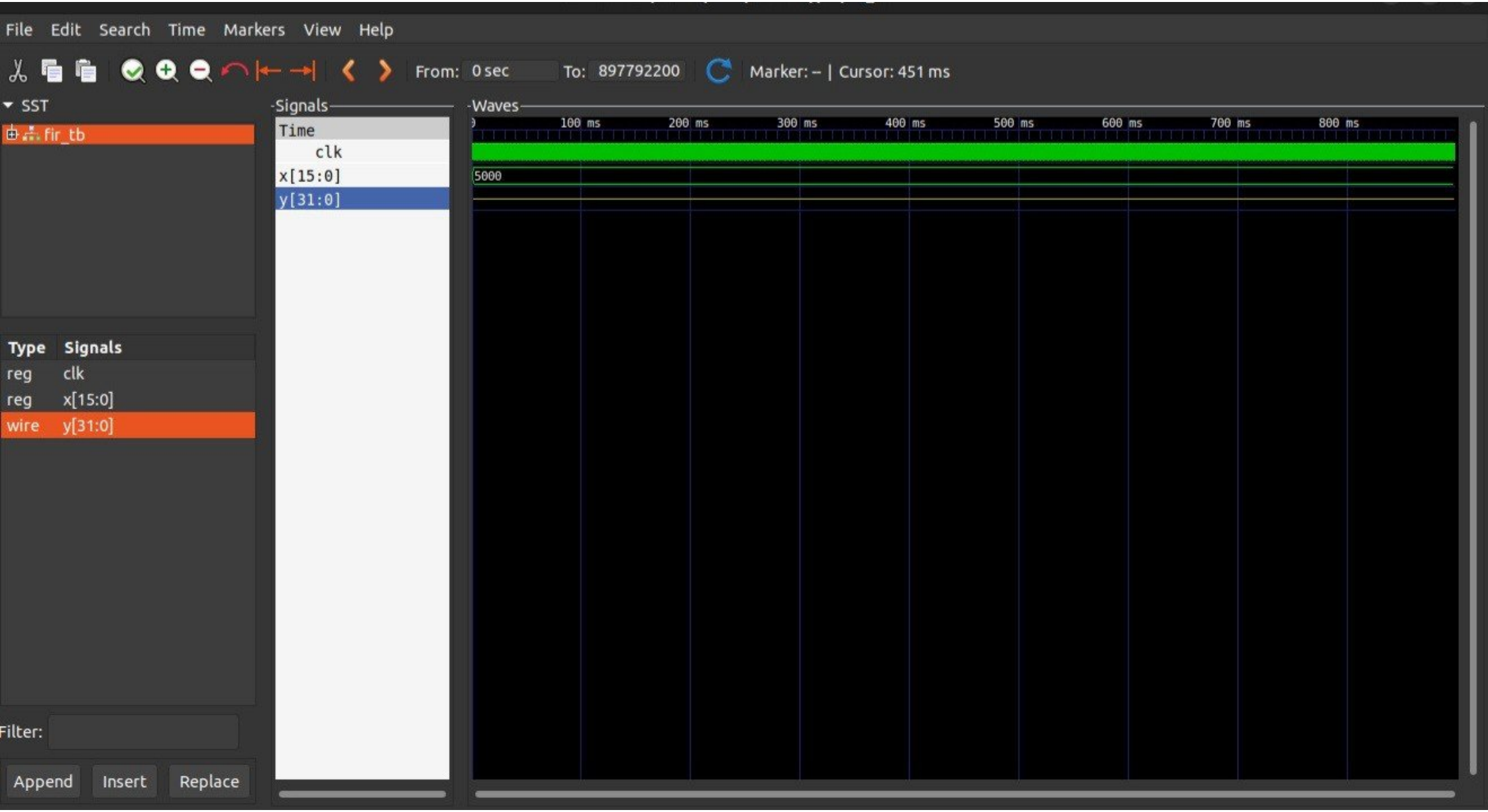
Save

fir.v

fir_tb.v

```
`timescale 1ns / 1ps
module fir_tb;
reg clk;
reg signed [15:0] x;
wire signed [31:0] y;
fir u0(
              .clk(clk),
              .x(x),
              .y(y));
       always #100 clk = ~clk;
       initial begin
       $dumpfile("fir_tb.vcd");
       $dumpvars(0,fir_tb);
       x = 0;
       clk=0;
       #200 x = 16'h1000;
       #200 x = 16'h2000;
       #200 x = 16'h3000;
       #200 x = 16'h4000;
       #200 x = 16'h5000;
       $monitor("Time: %t, Output: %h", $time, y);
       #100;
       end
     endmodule
```


user@gdk: ~/Desktop/fir
user@gdk:~$ cd Desktop
user@gdk:~/Desktop$ cd fir
user@gdk:~/Desktop/fir$ iverilog -o fir_wav fir_tb.v fir.v
user@gdk:~/Desktop/fir$ vvp fir_wav
VCD info: dumpfile fir_tb.vcd opened for output.
Time: 1000000, Output: zzzzzzzz


File Edit Search Time Markers View Help
From: 0 sec
To: 897792200
Marker: – | Cursor: 451 ms
SST
fir_tb
Type Signals
reg clk
reg x[15:0]
wire y[31:0]
Filter:
Append Insert Replace
Signals
Time
clk
x[15:0]
y[31:0]
Waves
100 ms 200 ms 300 ms 400 ms 500 ms 600 ms 700 ms 800 ms
5000