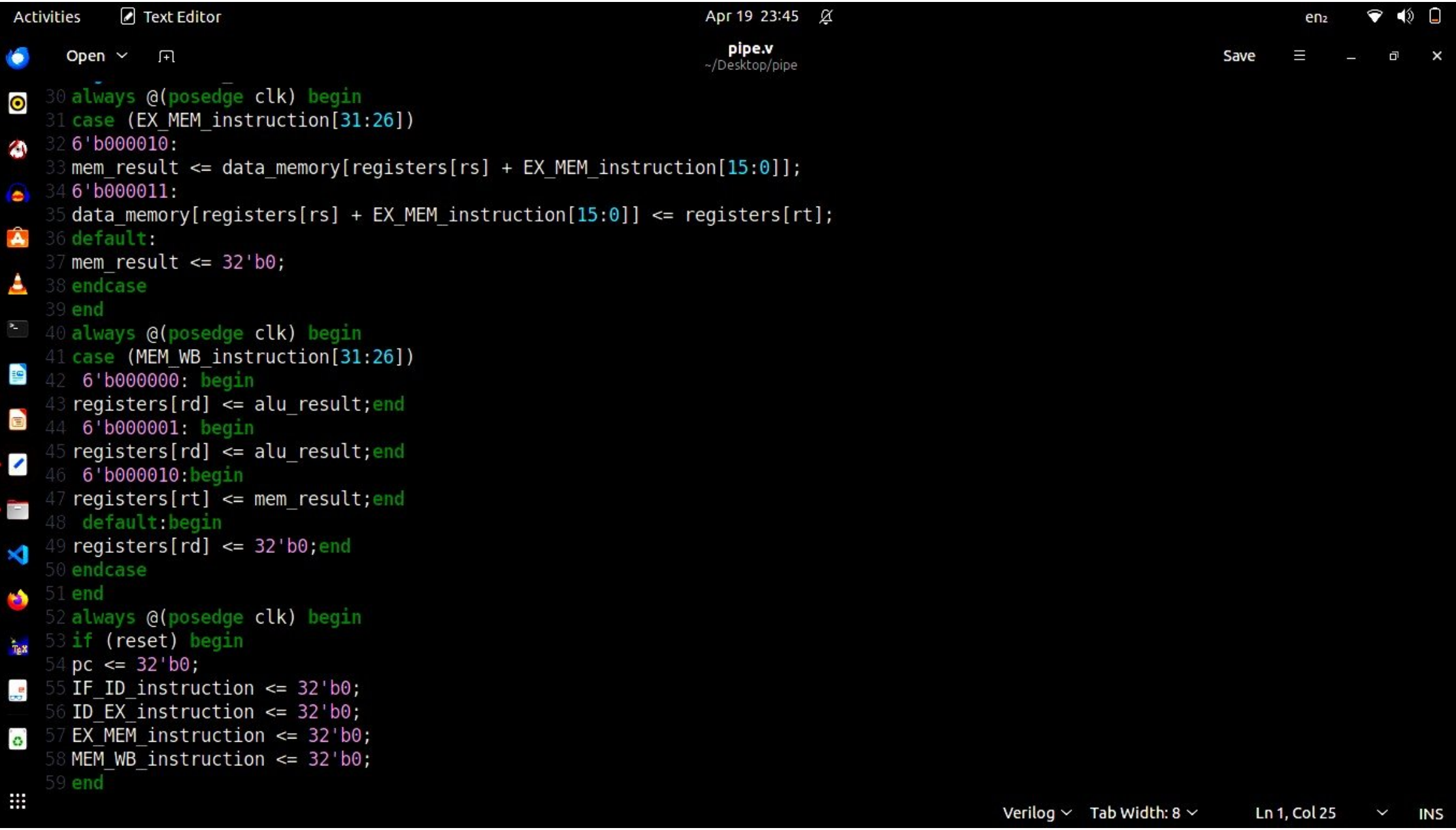
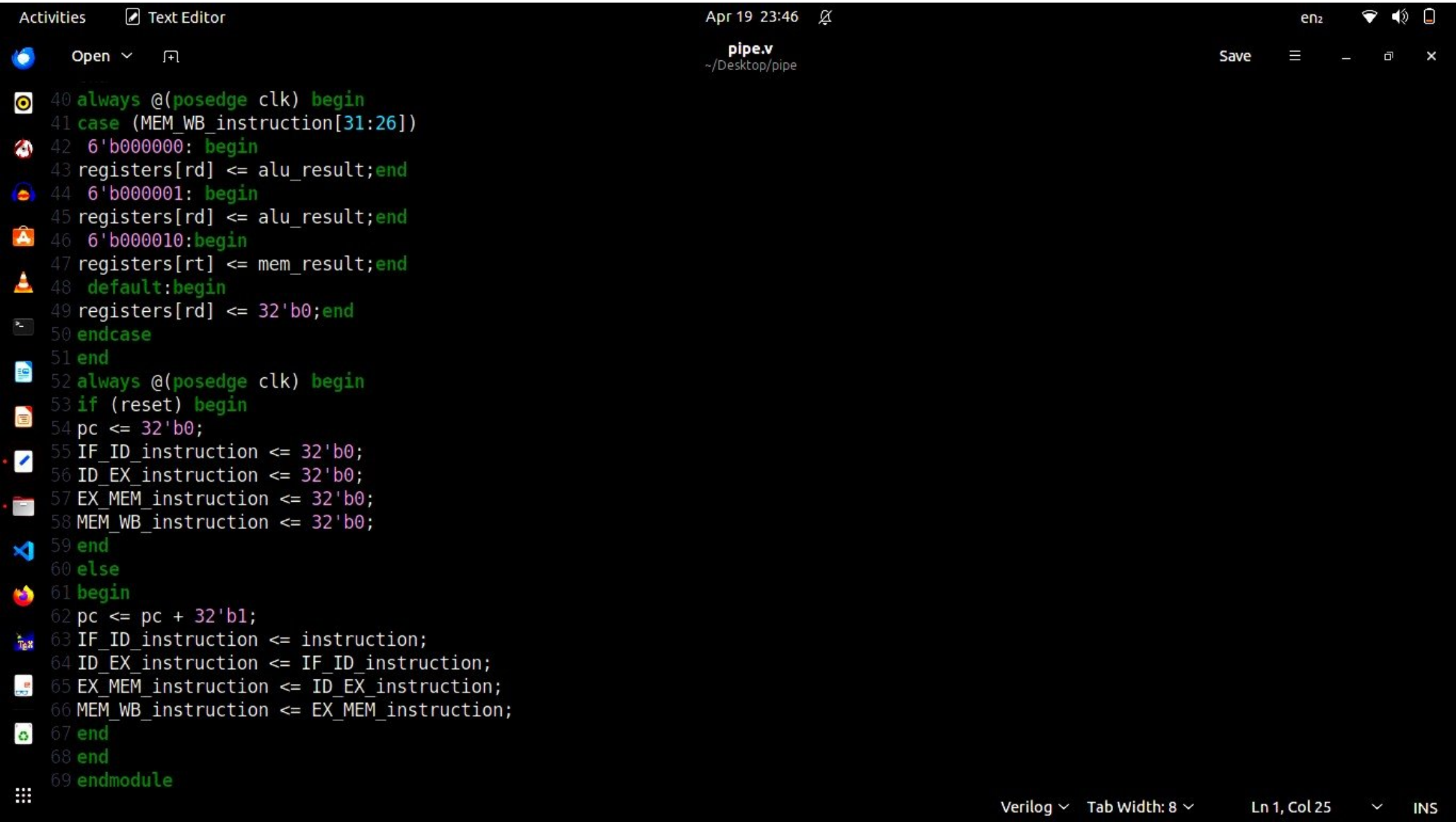
Activities Text Editor Apr 19 23:45 en2

Open pipe.v ~/Desktop/pipe Save

```
1 module pipe (clk,reset);
2 input clk;
3 input reset;
4 reg [31:0] instruction_memory[255:0];
5 reg [31:0] data_memory [255:0];
6 reg [31:0] registers [31:0];
7 reg [31:0] IF_ID_instruction;
8 reg [31:0] ID_EX_instruction;
9 reg [31:0] EX_MEM_instruction;
10 reg [31:0] MEM_WB_instruction;
11 reg [31:0] pc;
12 wire [31:0] instruction;
13 assign instruction = instruction_memory[pc];
14 wire [4:0] rs, rt, rd;
15 assign rs = IF_ID_instruction[25:21];
16 assign rt = IF_ID_instruction[20:16];
17 assign rd = IF_ID_instruction[15:11];
18 reg [31:0] alu_result;
19 always @(posedge clk) begin
20 case (ID_EX_instruction[31:26])
21 6'b000000:
22 alu_result <= registers[rs] + registers[rt];
23 6'b000001:
24 alu_result <= registers[rs] - registers[rt];
25 default:
26 alu_result <= 32'b0;
27 endcase
28 end
29 reg [31:0] mem_result;
30 always @(posedge clk) begin
```

Verilog Tab Width: 8 Ln 1, Col 25 INS


Activities
Text Editor
Apr 19 23:45
Open
pipe.v
~/Desktop/pipe
Save
always @(posedge clk) begin
case (EX_MEM_instruction[31:26])
6'b000010:
mem_result <= data_memory[registers[rs] + EX_MEM_instruction[15:0]];
6'b000011:
data_memory[registers[rs] + EX_MEM_instruction[15:0]] <= registers[rt];
default:
mem_result <= 32'b0;
endcase
end
always @(posedge clk) begin
case (MEM_WB_instruction[31:26])
6'b000000: begin
registers[rd] <= alu_result;end
6'b000001: begin
registers[rd] <= alu_result;end
6'b000010:begin
registers[rt] <= mem_result;end
default:begin
registers[rd] <= 32'b0;end
endcase
end
always @(posedge clk) begin
if (reset) begin
pc <= 32'b0;
IF_ID_instruction <= 32'b0;
ID_EX_instruction <= 32'b0;
EX_MEM_instruction <= 32'b0;
MEM_WB_instruction <= 32'b0;
end
Verilog
Tab Width: 8
Ln 1, Col 25
INS

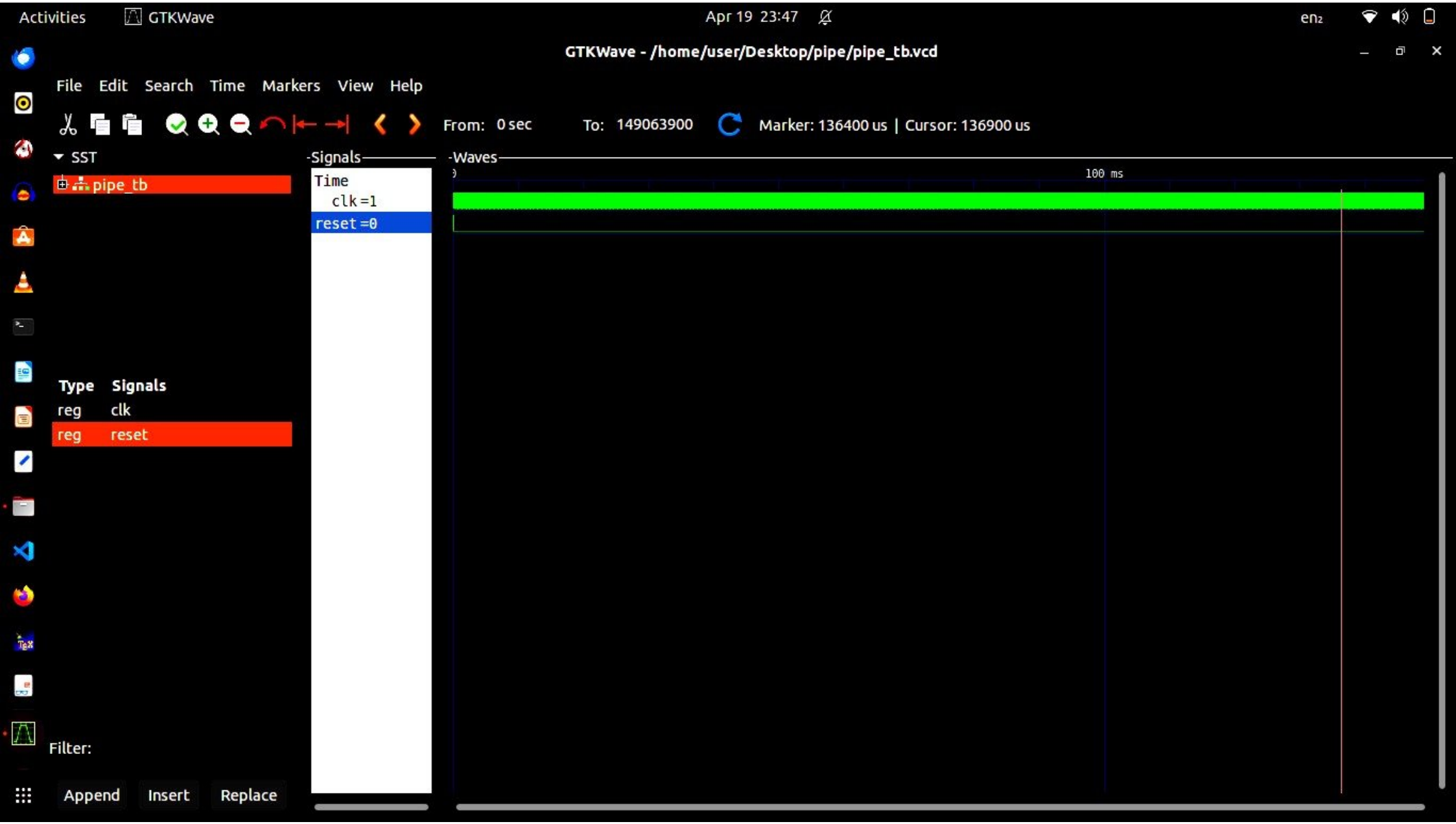

Activities
Text Editor
Apr 19 23:46
en2
Open
pipe.v
~/Desktop/pipe
Save
always @(posedge clk) begin
case (MEM_WB_instruction[31:26])
6'b000000: begin
registers[rd] <= alu_result;end
6'b000001: begin
registers[rd] <= alu_result;end
6'b000010:begin
registers[rt] <= mem_result;end
default:begin
registers[rd] <= 32'b0;end
endcase
end
always @(posedge clk) begin
if (reset) begin
pc <= 32'b0;
IF_ID_instruction <= 32'b0;
ID_EX_instruction <= 32'b0;
EX_MEM_instruction <= 32'b0;
MEM_WB_instruction <= 32'b0;
end
else
begin
pc <= pc + 32'b1;
IF_ID_instruction <= instruction;
ID_EX_instruction <= IF_ID_instruction;
EX_MEM_instruction <= ID_EX_instruction;
MEM_WB_instruction <= EX_MEM_instruction;
end
end
endmodule
Verilog
Tab Width: 8
Ln 1, Col 25
INS

Activities Text Editor Apr 19 23:46 en2

Open pipe_tb.v ~/Desktop/pipe Save

```
`timescale 1ns / 1ps
module pipe_tb;
    reg clk;
    reg reset;
    pipe uut(
            .clk(clk),
            .reset(reset));
        always #50 clk = ~clk;
    initial begin
    $dumpfile("pipe_tb.vcd");
    $dumpvars(0,pipe_tb);
    clk=1;
        reset = 1;
        #100;
        reset = 0;
        uut.instruction_memory[0] = 32'h20010001;
        uut.instruction_memory[1] = 32'h20020002;
        uut.instruction_memory[2] = 32'h00052820;
        uut.instruction_memory[3] = 32'h00053021;
        uut.data_memory[1] = 32'h00000005;
        uut.data_memory[2] = 32'h00000003;
        #100;
    end
endmodule
```

Verilog Tab Width: 8 Ln 12, Col 11 INS


Activities
GTKWave
Apr 19 23:47
GTKWave - /home/user/Desktop/pipe/pipe_tb.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 149063900
Marker: 136400 us | Cursor: 136900 us
SST
pipe_tb
Type Signals
reg clk
reg reset
Filter:
Append Insert Replace
Signals
Time
clk=1
reset=0
Waves
100 ms