Generating PWM Signals with Variable Duty Cycle using FPGA for LED Brightness Controller

For

Mini Project – 2B: FPGA Design Project (ECM501)

(REV- 2019 'C' Scheme) of Third Year (Semester-VI)

Bachelors in Engineering

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Mini Project-2B Approval

Project entitled by **Generating PWM Signals with Variable Duty Cycle using FPGA for LED Brightness Controller** by **Trisha Gaur, Advait Kulhada, Sharvani Sawant & Shubham Sangani** is approved for the degree of Bachelor of Engineering.

Examiners

1. _____
2. _____

Supervisors

1. _____
2. _____

Date:

Place:

Certificate

This is to certify that **Trisha Gaur, Advait Kulhada, Sharvani Sawant, and Shubham Sangani** have completed the project report on the topic **Generating PWM Signals With Variable Duty Cycle using FPGA for LED Brightness Controller** satisfactorily in partial fulfillment of the requirements for the award of Mini Project 2B (REV- 2019 'C' Scheme) of Third Year, (Semester-VI) in Electronics and Telecommunication under the guidance of **Dr. Monali Chaudhari** during the year **2021-2022** as prescribed by University of Mumbai.

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Examiner 1 **Examiner 2**

Declaration

We declare that this written submission represents our ideas in our words and where others' ideas or words have been included, we have adequately cited and referenced the original sources. We also declare that we have adhered to all principles of academic honesty and integrity and have not misinterpreted or fabricated or falsified any idea/data/fact/source in my submission. We understand that any violation of the above will be cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

_____

(Trisha Gaur)

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Date:

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Abstract

The pulse width modulation (PWM) principle is widely used in power electronics applications for controlling power converters (DC/DC, DC/AC) which can be seen in controlling the brightness of LEDs. The conventional method of generating the PWM pulses using analog circuitry has disadvantages of complex circuitry, limited function, and low flexibility in circuit modification. Due to limitations offered by analog circuit designing, the digital methods of generating the pulses are getting more popular.

The project aims to generate the Pulse width modulation (PWM) signals which are to be used in various power electronics applications like power converters and inverters. The pulses are generated using Verilog language which is suitable for usage in the Spartan-6 Field Programmable Gate Array (FPGA) board which is used as a high-performance controller in vector control of an induction motor. By adjusting the duty cycle, the brightness of the LED can be controlled. Simulation results are validated with a register transfer level (RTL) schematic.

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Abbreviations

DC	Direct Current	06
LED	Light Emitting Diode	09
PWM	Pulse Width Modulation	09
CPLD	Complex Programmable Logic Device	10
IC	Integrated Circuit	10
DCM	Discontinuous Conduction Mode	11
LSB	Least Significant Bit	11
DPWM	Digital Pulse Width Modulation	11
MCU	Microcontroller Unit	11
DDR	Double Data Rate	15
SDRAM	Synchronous Dynamic RAM	15
SPI	Serial Peripheral Interface	15
USB	Universal Serial Bus	15
ISE	Integrated Synthesis Environment	18
HDL	Hardware Description Language	18
JTAG	Joint Test Action Group	18
RGB	Red Green Blue	19

Chapter 1

Introduction

Special effects lighting is an important part of the entertainment industry, and the decreasing cost of electronics has increased the potential for lighting control in both private and commercial applications. In addition, the advances in Light Emitting Diode (LED) technology and the continuing reduction in cost have made the use of LED light sources more affordable. Our project combines these two ideas, creating a lighting device with multi-level intensity capabilities.

Pulse-width modulation (PWM) is a modulation technique used to encode a message into a pulsing signal. It is achieved by changing the width of the signal & keeping the period or frequency the same. Pulse width modulation (PWM) is widely used in applications of communication and control systems. Implementation of PWM on FPGA can process the data faster and controller architecture can be optimized for space or speed. PWM is a technique to provide logic ‘0’ and logic ‘1’ for a controlled period. It is a signal source that involves the modulation of its duty cycle to control the amount of power sent to the load. In PWM, the time period of the square wave is kept constant and the time for which the signal remains HIGH is varied.

Chapter 2

Review of Literature

2.1 Survey

2.1.1 Generation of PWM Using Verilog in FPGA

This system describes an approach to generating the PWM signals using Verilog on the FPGA board; which are to be used in various power electronics applications like power converters and inverters. Generation of PWM pulses is investigated and the program code is developed on Verilog which is implemented on the FPGA Board. RTL Schematic validates the output of the Pulse Generation. The issue with this system is that the PWM signals may give inaccurate results as the counters utilized are not turned on and off at more precise intervals. [1]

2.1.2 Pulse Width Modulation Implementation using FPGA and CPLD ICs

A high-frequency PWM generator architecture for power converter control, using FPGA and CPLD ICs, has been presented. The architecture is based on a synchronous binary counter and can be easily interfaced with a microcontroller. The post-layout timing simulation results prove that using the proposed method, PWM frequencies up to 3.985 MHz can be produced with a duty cycle resolution of 1.56%, which is adequate for most applications. The PWM frequency depends on the target FPGA or CPLD device speed grade and the duty cycle resolution required in the system that hinders the performance of the system. [2]

2.1.3 FPGA-Based Digital Pulse Width Modulator with Optimized Linearity

This system proposes an architecture with a DCM-based synchronous delay line suitable for the implementation of high-speed high-resolution DPWM with good linearity on low-cost FPGAs using only a few logic cells. The proposed manually optimized DPWM reduces the integral non-linearity error by 0.5 LSB. A DPWM implementation with a 9-bit resolution with a switching frequency of 1 MHz has been verified on a Xilinx Spartan-3 FPGA. However, when connecting the FPGA to a power stage or other circuit, an external driver must be used to ensure adequate driving strength and speed. [3]

2.2 Research Gap

- Due to limitations offered by analog circuit designing in the market, the digital method of generating the pulses using the FPGA board is used.
- Since FPGA allows users to have all features on a single chip and have the advantage of flexibility due to their reprogramming capability, it is considered over traditional MCUs.
- Special effects lighting is an important part of the entertainment industry, and the decreasing cost of electronics has increased the potential for lighting control in both private and commercial applications. The proposed prototype is very flexible and less sensitive to environmental noise.
- The given project can be integrated with other technical and commercial floating-point applications but considering the cost of the FPGA boards, it would be difficult to endorse it commercially from an economic perspective in the current times.

Chapter 3

Project Description

3.1 Problem Statement

The pulse width modulation (PWM) principle is widely used in power electronics applications for controlling power converters which can be seen in controlling the brightness of LEDs. The conventional method of generating the PWM pulses using analog circuitry has disadvantages of complex circuitry, limited function, and low flexibility in circuit modification. Due to limitations offered by analog circuit designing, the digital methods of generating the pulses are getting more popular.

3.2 Steps Involved

Today engineers use various switches, functions, and microcontrollers to make control systems but these all are being replaced by FPGA (Field Programmable Gate Array) since it allows users to have all features on a single chip. It is an array of programmable logic blocks that can be connected by using Hardware Description Language. The development of a field-programmable gate array (FPGA) provides an alternative solution for the implementation of various duty cycles which can be used to control the LED's brightness and mixing of colors by dimming it into various amounts. They have the advantage of flexibility due to their reprogramming capability, while their operating frequency can be as much as hundreds of MHz of duty cycle.

3.3 Block Diagram of proposed project:

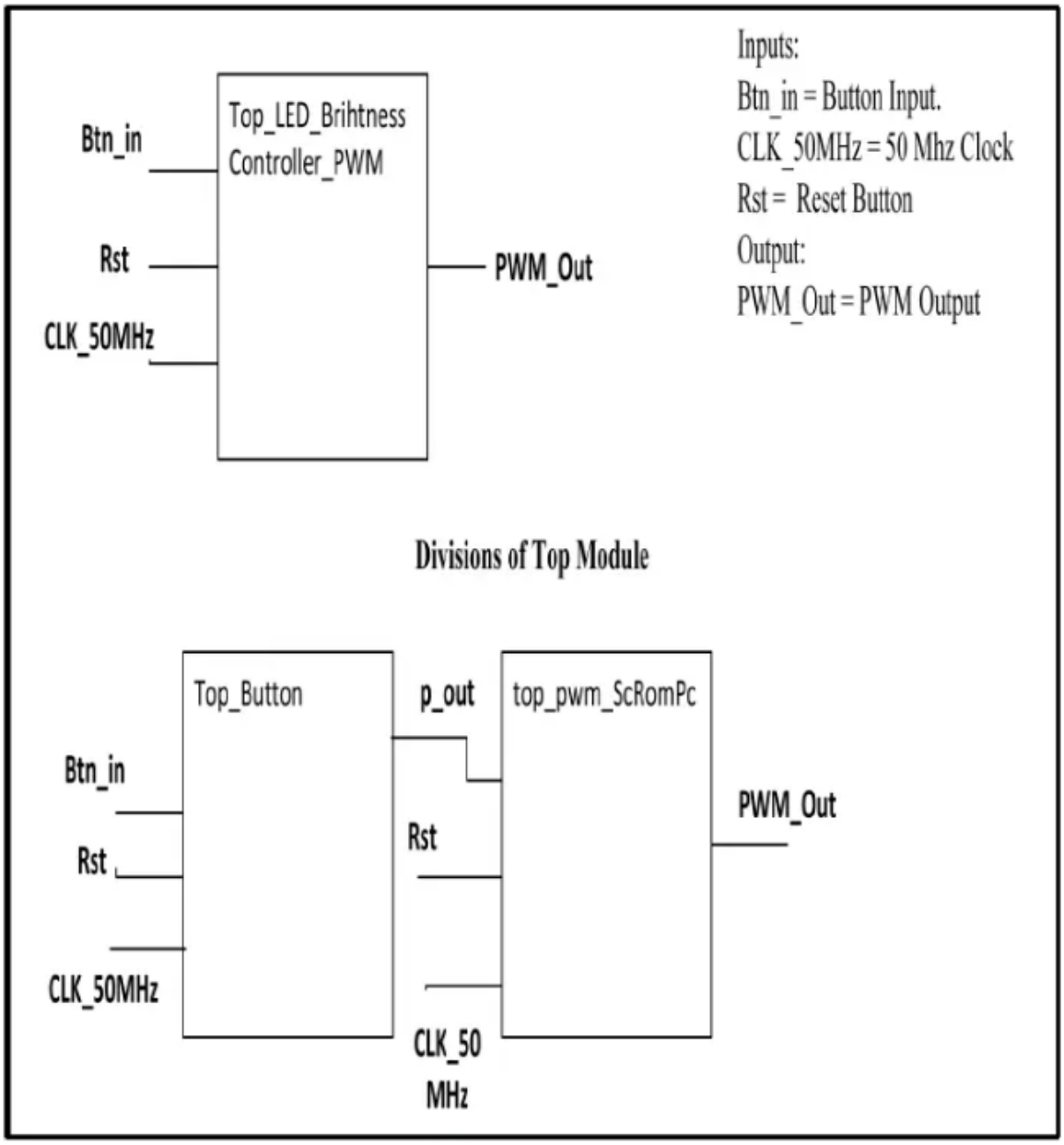


Fig 3.3. 1 Block Diagram of Proposed System

3.3.1 Block Diagram Description

Main Module-

The main module has three inputs **Clock, Reset & Button** & **one output PWM.**
The clock on the FPGA has a frequency of 50Mhz (The time period of 20 Nanoseconds) the frequency of our output must be 1KHz (The time period of 1 millisecond). The output turns on and off so quickly that eyes take this phenomenon as variance in intensity of LED light.
Main module connects the top modules **'Top_button'** & **'top_PWM_Generator'**.

Top Button Module-

The top button module connects the **Synchronizer**, **Top debounce**, and **Level-to-pulse converter**.

- The **Synchronizer** takes asynchronous input along with a clock and resets inputs.
- Making and breaking contact is called **Debouncing**.
- A **Level-to-pulse converter** produces a single-cycle pulse each time its input goes high.
  It's a synchronous rising-edge detector.

Top PWM Generator Module-

This module connects the **Selection Counter, ROM,** and **PWM generator.**

- The **Selection Counter** decodes each input of our system.
- **ROM** stores different values of the time for which the counters have to run. It sends a specific value of time when it receives a code from the 'Selection Counter'.
- The **PWM generator** has two counters, one counter counts for how much time output remains High i.e., 1 & the other counter counts for how much time output remains Low i.e., 0.

3.4 Component Description

3.4.1 Hardware

1. Mimas V2 Spartan 6 FPGA Development Board

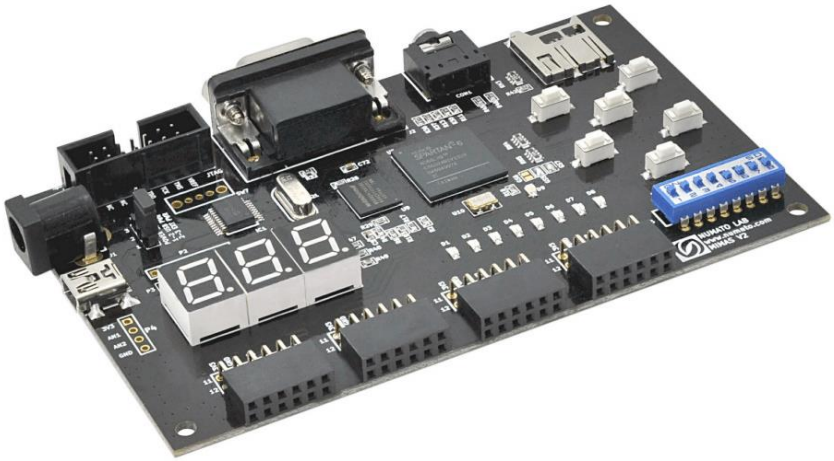


Fig. 3.4. 1 Mimas V2 Spartan 6 FPGA Development Board

MIMAS V2 is a feature-packed yet low-cost FPGA Development board featuring Xilinx Spartan-6 FPGA. It is specially designed for experimenting and learning system design with FPGAs. This development board features SPARTAN XC6SLX9 CSG324 FPGA with onboard 512Mb DDR SDRAM. The USB 2.0 interface provides a fast and easy configuration download to the onboard SPI flash. No need to buy an expensive programmer or special downloader cable to download the bitstream to the board.

Applications:

- Product Prototype Development
- Signal Processing
- Learning Digital Electronics
- An educational tool for schools and universities

2. Cathode Ray Oscilloscope (CRO)

Fig. 3.4. 2 Cathode Ray Oscilloscope (CRO)

A Cathode Ray Oscilloscope (CRO) is an instrument generally used in a laboratory to display, measure, and analyze various waveforms of electrical circuits. A cathode-ray oscilloscope is a very fast X-Y plotter that can display an input signal versus time or another signal.

Applications:

While numerous, a CRO can be used for the following purposes.

- To determine the amplitude of a waveform.
- Comparison between the phases and frequencies of electrical signals.
- Help measure capacitance and inductance values.
- In the medical field and medical trials, it can be used for monitoring various body parameters like heartbeat rates and nervous reactions.

3. LED

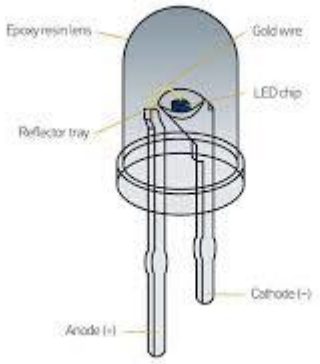


Fig. 3.4. 3 LED

A light-emitting diode (LED) is a semiconductor light source that emits light when current flows through it. Electrons in the semiconductor recombine with electron holes, releasing energy in the form of photons.

LEDs (Light Emitting Diodes) are the latest development in the lighting industry. Made popular for their efficiency, range of color, and long lifespan, LED lights are ideal for numerous applications, including night lighting, art lighting, and outdoor lighting.

4. DAC (Digital to Analog Signal Converter)

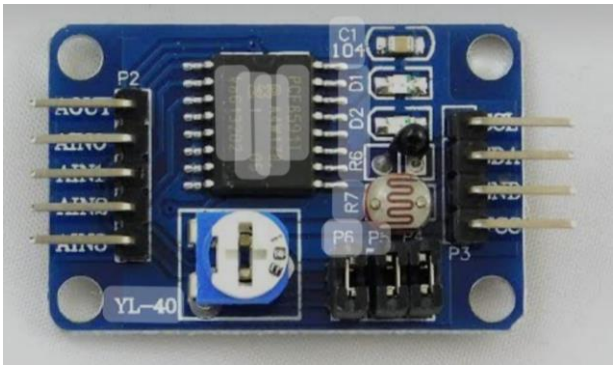


Fig. 3.4. 4 DAC

DAC is a system that converts a digital signal (consisting of a series of 0s and 1s) into an analog signal. The most popular DAC connection method is via USB from a computer.

A DAC converts a limited number of discrete digital codes to a corresponding number of discrete analog output values. The more digital bits represented by the DAC, the more accurate the analog output signal. You can think of a DAC as a digital potentiometer that produces an analog output that is a fraction of the full-scale analog voltage determined by the value of the digital code applied to the converter. DAC is determined by the number of samples it can process and the number of bits used in the conversion process. This operation produces an analog waveform that is discrete, not continuous. The discrete output can be integrated into the receiving device, which in this case is the CRO (Cathode Ray Oscilloscope).

Applications-

- DACs are used in Digital Signal Processing.
- They are also used in digital power supplies for Micro-controller.
- DACs are used in digital potentiometers.
- They are used in all digital data acquisition systems.

3.4.2 Software

- ### Xilinx ISE Webpack 14.7

  ISE WebPACK is used for the FPGA and CPLD design offering HDL synthesis and simulation, implementation, device fitting, and JTAG programming. ISE WebPACK delivers a complete, front-to-back design flow providing instant access to the ISE features and functionality at no cost. Xilinx has created a solution that allows convenient productivity by providing a design solution that is always up to date with error-free downloading and single file installation.

3.5 Working of the proposed project

The working principle of the generator is that it uses one counter and one comparator. The microcontroller unit provides 8-bit input into the PWM module. The counter used in the PWM module is 8-bit. It increments its value on the positive edge of the clock (positive edge-triggered). The comparator used in the PWM generator is also 8-bit. Input given to the PWM module is compared to the current value of the counter using the comparator. If the current value of the counter is greater than the value given to the module as input, PWM output is pulled low. However, if the current value of the counter is less than the value given as input to the module, the output of the PWM generator is pulled high. After completing the software simulation, the code is then uploaded to the FPGA board and the output is observed using a cathode-ray oscilloscope. With an RGB LED, you can control how much of each of the three colors you want in the mix of colors by dimming them with various amounts.

Chapter 4

Implementation

4.1 Hardware

1. Connect the board to the computer using a USB-B cable.
2. Connect the remaining components with the FPGA board.
3. Further process the code with Xilinx ISE Web pack. Using Bit-stream and User Constraint File obtained from the Xilinx software after successful execution of the code, the program code can be uploaded on the FPGA board.
4. On successful completion of initializing the code, we can test our PWM generator by inputting the binaries on the Spartan board.

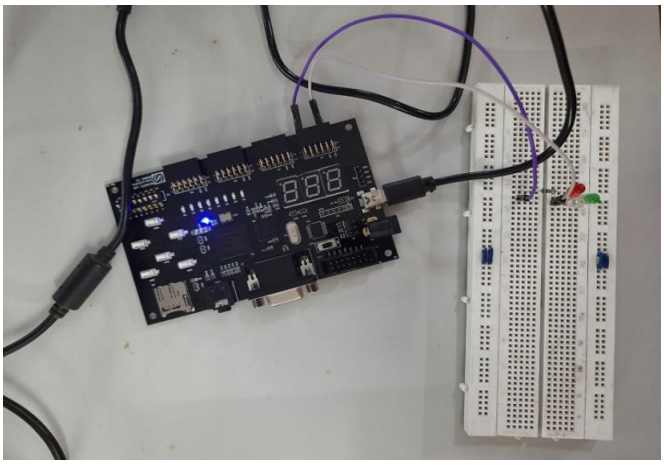


Fig. 4. 1 Hardware Implementation

4.2 Software

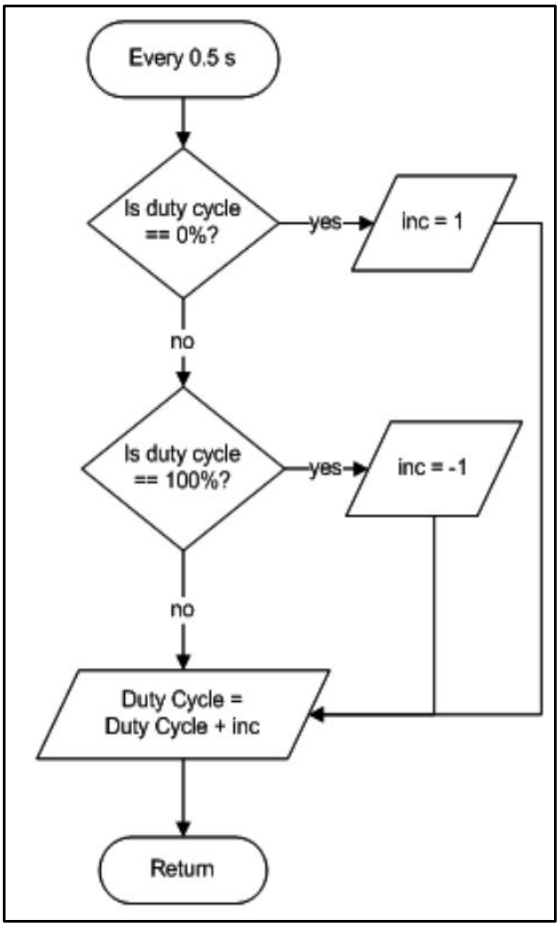


Fig. 4. 2 Software Flowchart

1. For generating the variable duty cycle of the PWM generator, an algorithm or a flow of steps can be followed.
2. In the software simulation, after every 0.5 seconds, the duty cycle can be verified if its value is equal to zero percentage.
3. If the duty cycle is zero percentage at that instant, the increment variable will be then set to 1.
4. Whereas if the duty cycle at that instant is not equal to zero percent, then another condition is checked.

5. Now if the percentage of the duty cycle is full i.e., 100%, then the increment variable is set to -1, which means that the value of the variable will now be decreased so that the percentage of the duty cycle changes.
6. But if the percentage of the duty cycle is not 100% at that instant, then an equation can be used such that the duty cycle will be equal to the duty cycle value in addition to the increment variable value. This equation shall be used even when the increment variable was set to 1 and -1 in the previous steps to change the value of the duty cycle for various combinations.

Chapter 5

Results

RTL Schematic and waveform for PWM generation

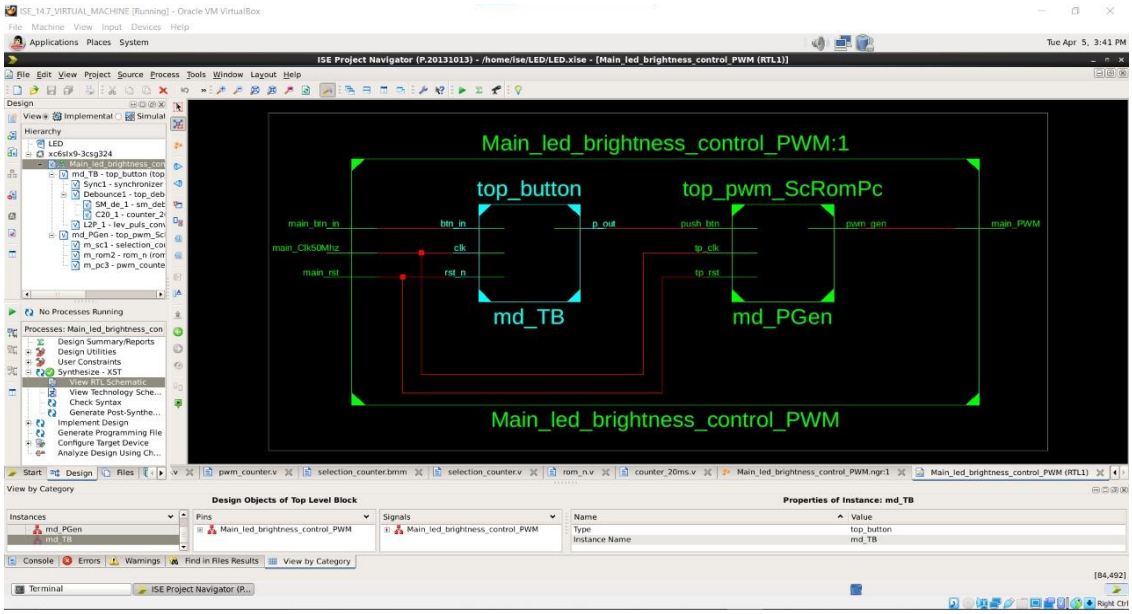


Fig. 5. 1 RTL Schematic for PWM Generation

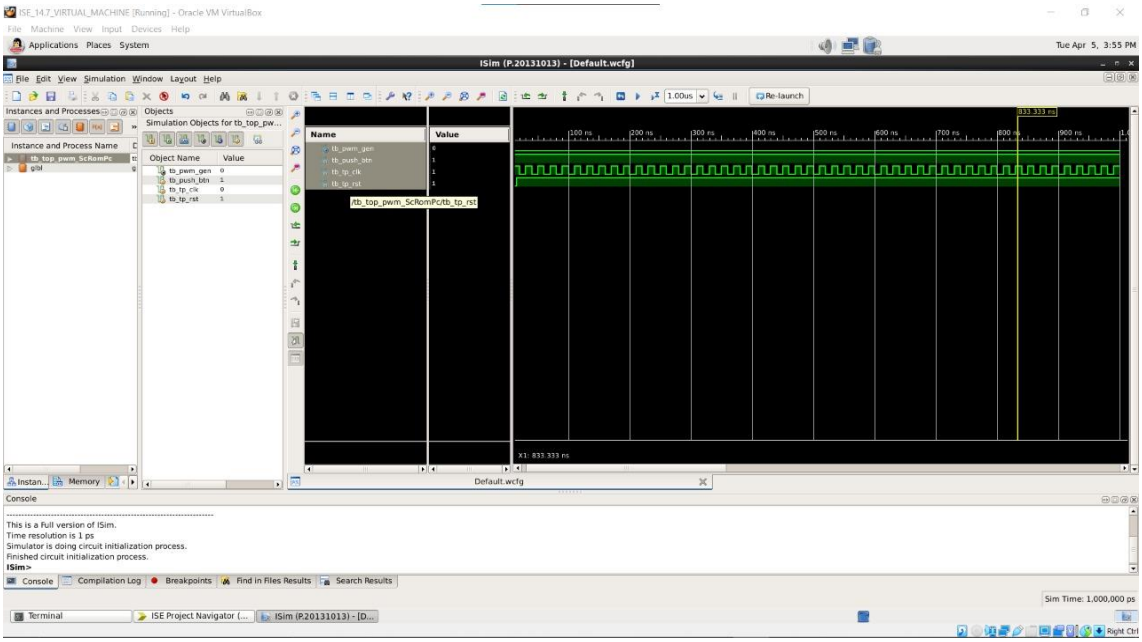


Fig. 5. 2 Waveform for PWM Generation

RTL Schematic and waveform for the LED Control

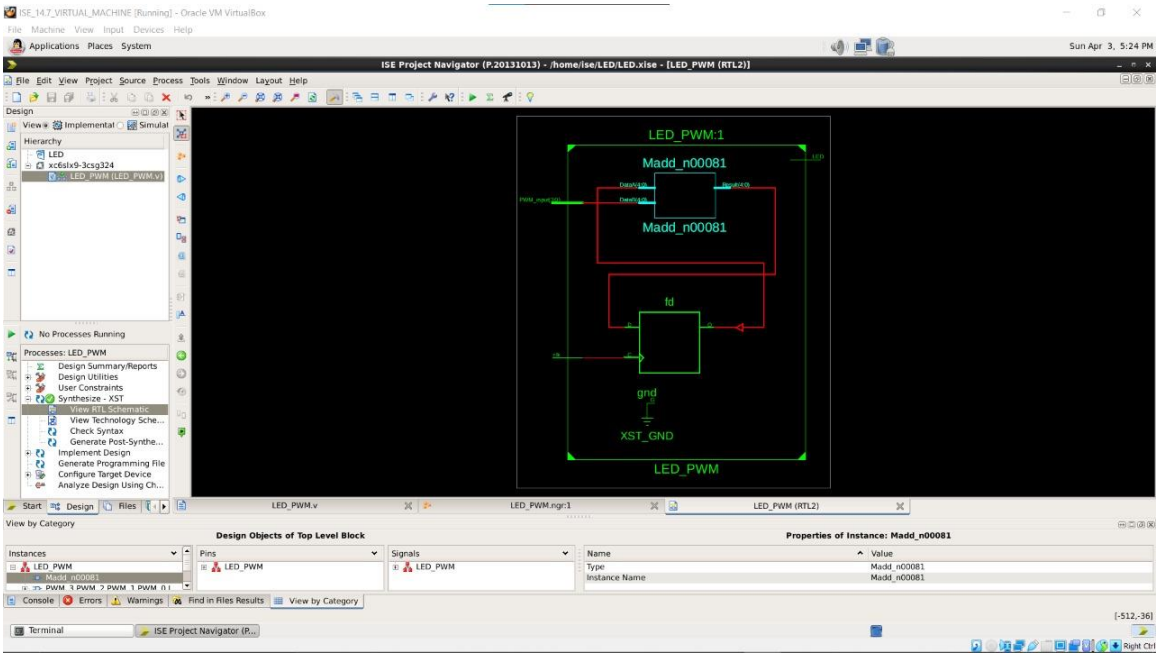


Fig. 5. 3 RTL Schematic for LED Control

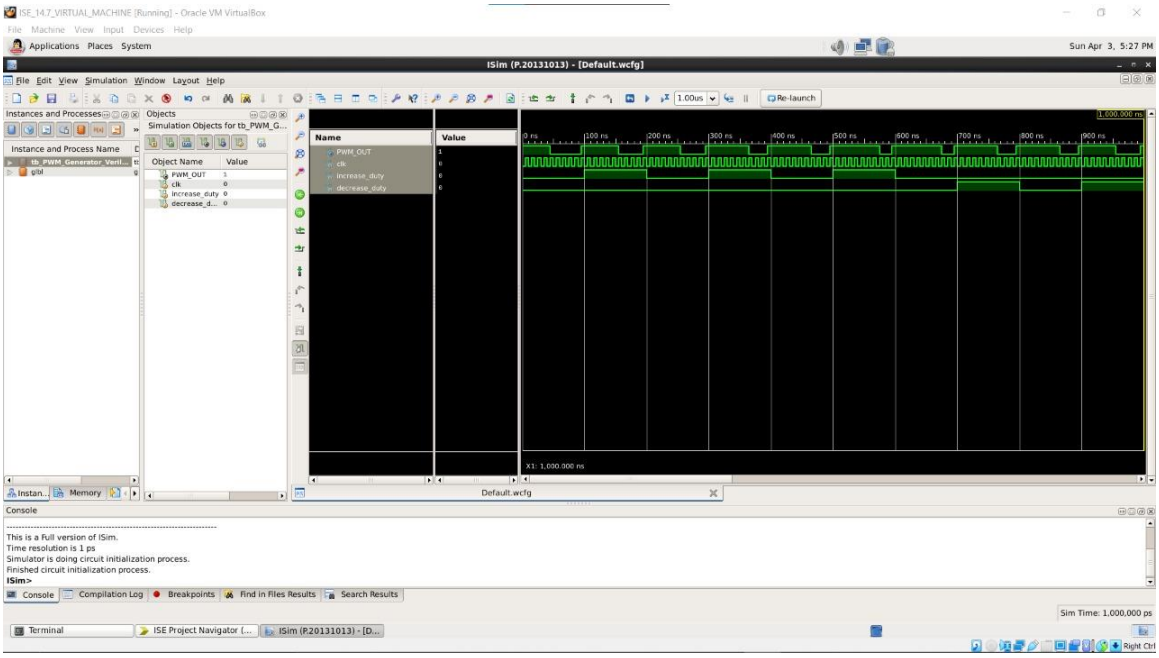


Fig. 5. 4 Waveform for LED Control

REFERENCES

[1] Rohan Shrivastava Yogesh K. Chauhan and Bhavnesh Kumar, "Generation Of PWM Using Verilog In FPGA", International Conference on Electrical, Electronics, and Optimization Techniques(ICEEOT), Uttar Pradesh, India,2016

[2] Jakirhusen I. Tamboli, Prof. Satyawan R. Jagtap, Amol R. Sutar, "Pulse Width Modulation Implementation using FPGA and CPLD ICs", International Journal of Scientific & Engineering Research (IJET), Maharashtra, India, Aug.2012

[3] Martin Scharrer, Mark Halton and Tony Scanlan, "FPGA-Based Digital Pulse Width Modulator With Optimized Linearity", Institute of Electrical and Electronics Engineers (IEEE), Limerick, Ireland, 2009

[4] Anju S. Nair, Savitha G. Kini, "FPGA-Based buck controller for LED white light tuning ", Institute of Electrical and Electronics Engineers (IEEE), 2014

5]"FPGA Based LED Brightness Controller Using PWM", Scribd,2017

[6]"FPGA Based LED Brightness Controller", Pdf Coffee, 2021

[7]"Generating PWM Signals with Variable Duty Cycle", Pantech Solutions, India, 2021

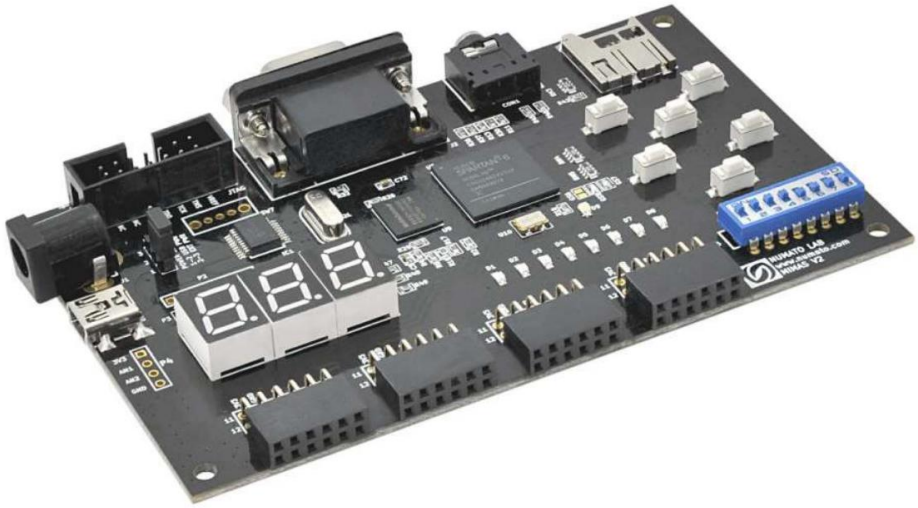
[8]"Generating PWM Signals with Variable Duty Cycle using FPGA", Elprocus, 2013

[9]"Mimas V2 Spartan 6 Development Board", Numato Labs

APPENDIX

- ## MIMAS V2 Spartan 6 FPGA Board

1. Introduction



(https://numato.com/help/wp-content/uploads/2016/03/mimasv2-introimg.png)

MIMAS V2 is a feature-packed yet low-cost FPGA Development board featuring Xilinx Spartan-6 FPGA. It is specially designed for experimenting and learning system design with FPGAs. This development board features SPARTAN XC6SLX9 CSG324 FPGA with onboard 512Mb DDR SDRAM. The USB 2.0 interface provides fast and easy configuration download to the on-board SPI flash. No need to buy an expensive programmer or special downloader cable to download the bitstream to the board.

Applications

- Product Prototype Development
- Signal Processing
- Learning Digital Electronics
- Educational tool for schools and universities

Board features

- FPGA: Spartan XC6SLX9 in CSG324 package
- DDR: 166MHz 512Mb LPDDR (MT46H32M16LF/W949D6CBHX6E)
- Flash memory: 16 Mb SPI flash memory (M25P16)
- USB 2.0 interface for On-board flash programming
- FPGA configuration via JTAG and USB
- 8 LEDs Six Push Buttons and 8 way DIP switch for user-defined purposes
- VGA Connector
- Stereo Jack
- Micro SD Card Adapter

- Three-Digit Seven Segment Display.
- 32 IOs for user-defined purposes
- Four 6×2 Expansion Connectors
- On-board voltage regulators for single power rail operation

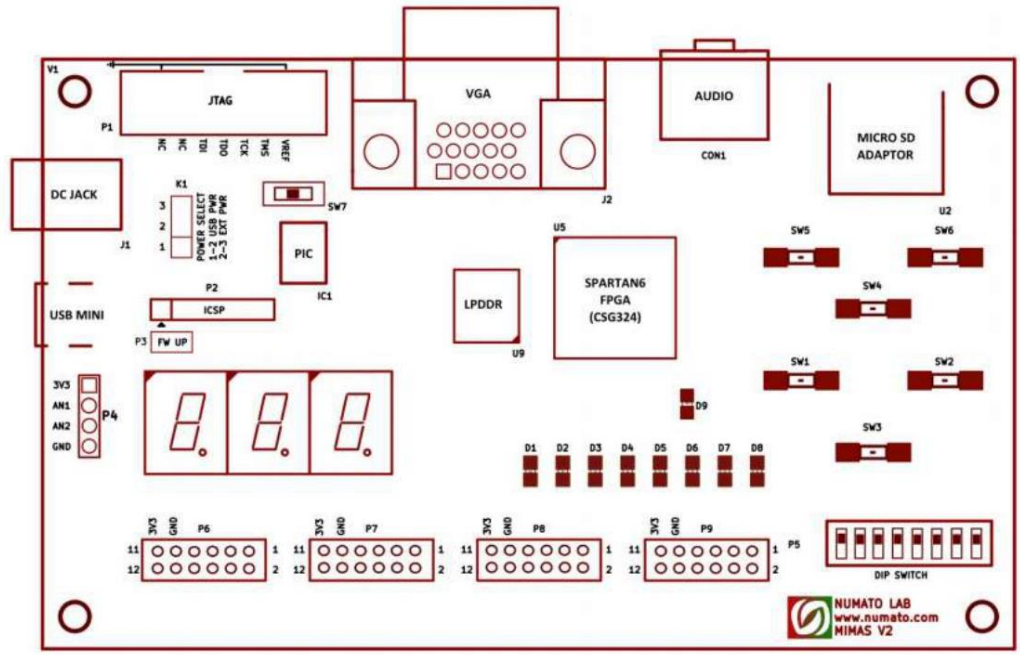
2. How to Use Mimas V2 Spartan 6 FPGA Development Board

2.1. Components/Tools Required

Along with the module, you may need the items in the list below for easy and fast installation.

1. USB A to Mini B cable.
2. DC Power supply (Optional).

2.2. Connection Diagram



(https://numato.com/help/wp-content/uploads/2016/03/mimasv2-condiagram.png)

This diagram should be used as a reference only. For detailed information, see MIMAS V2 schematics at the end of this documentation. The details of individual connectors are as below.

2.3. USB Interface

(https://numato.com/help/wp-content/uploads/2016/03/mimasv2-usbinterfaceimg.png)The onboard full-speed USB controller helps a computer to communicate with this module. Use a USB A to Mini B cable to connect with a PC. By default, the module is powered from USB so make sure not to overcrowd unpowered USB hubs.

2.4. DC Power Supply

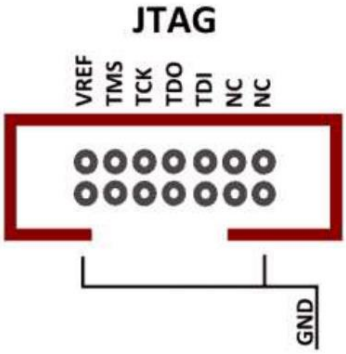
(https://numato.com/help/wp-content/uploads/2016/03/mimasv2-dcsupply.png)This module uses a +5V power supply to function properly. **By default, the board is configured to use the +5V supply from USB. So an external +5V power is not required unless the USB port is unable to supply enough current. In most cases, USB ports are capable of providing enough current for the module. The current requirement for this board largely depends on your application. Please consult the FPGA datasheet for more details on power requirements.** If for any reason, an external 5V power supply needs to be used for the module, the Power select jumper should be configured properly before connecting the power supply. Please refer to the marking on the board for more details.

2.5. Power Select

The Power Select header K1 is used to configure the power source for the board. The jumper in pin 1 and 2 is shorted to switch the power source to the onboard USB port and pin 2 and 3 to use the external DC power.

2.6. JTAG Connector

A JTAG connector provides access to FPGA's JTAG pins. A XILINX platform cable can be used for JTAG programming.



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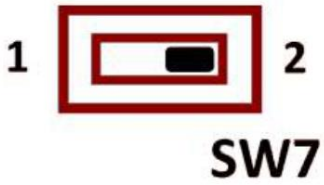
2.7. Configuration Mode Selection

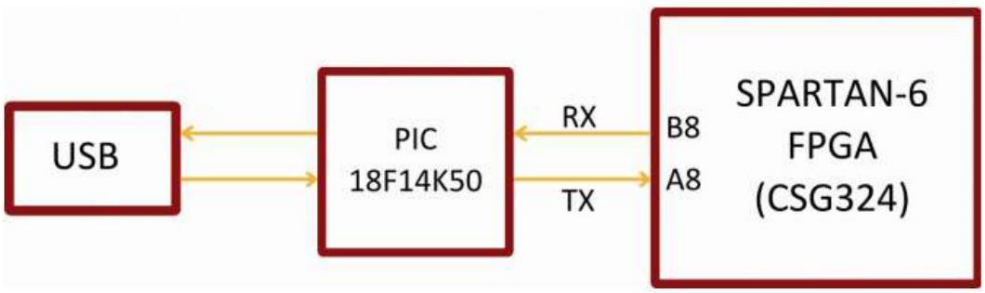
Slide switch SW7 is used to switch between the USB configuration mode and UART. Slide the switch to Position 1 to download bitstream through USB configuration tool and Position 2 to use the interface as a UART in order to communicate from your code in FPGA with the PC. By default, the board is shipped with a slide switch position in the USB configuration tool mode.



(https://numato.com/help/wp-content/uploads/2016/03/mimasv2-configmodesw7.png)

2.8. UART

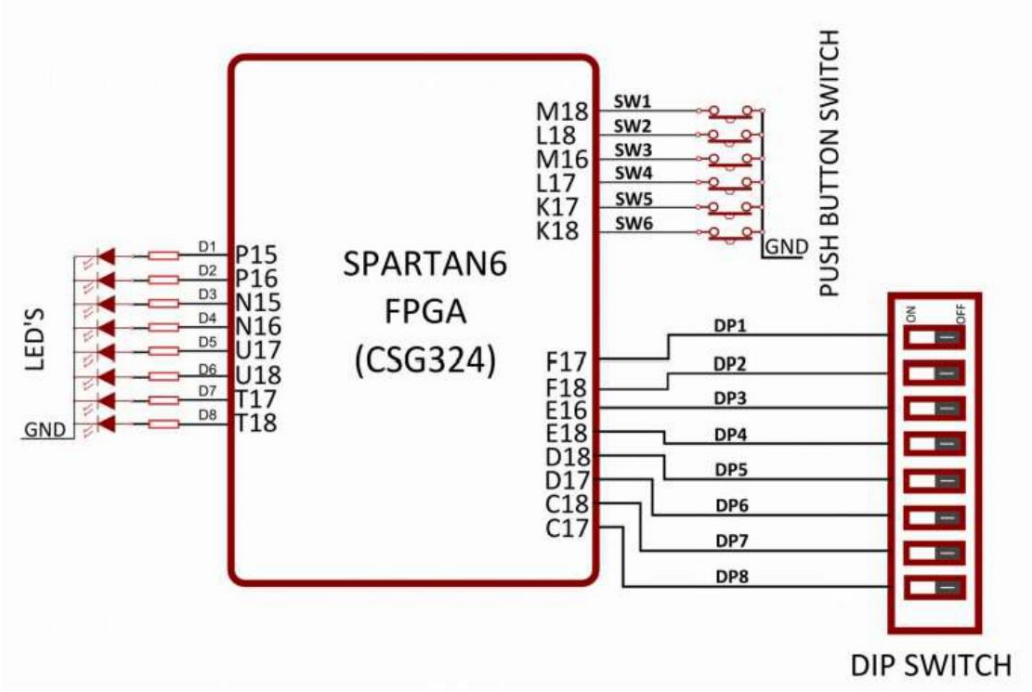
The MIMAS V2 includes USB-UART, which helps to establish the communication between the code in the FPGA and any application running on the PC. Data can be sent and received from the FPGA by using Serial Terminal at baud rate 19200.



(https://numato.com/help/wp-content/uploads/2016/03/mimasv2-uart.png)

2.9. LED, Push Button and Dip Switch

MIMAS V2 has six push-button switches, an eight-position DIP switch and eight LEDs for human interaction. All switches are directly connected to Spartan 6 FPGA and can be used in your design with minimal effort.



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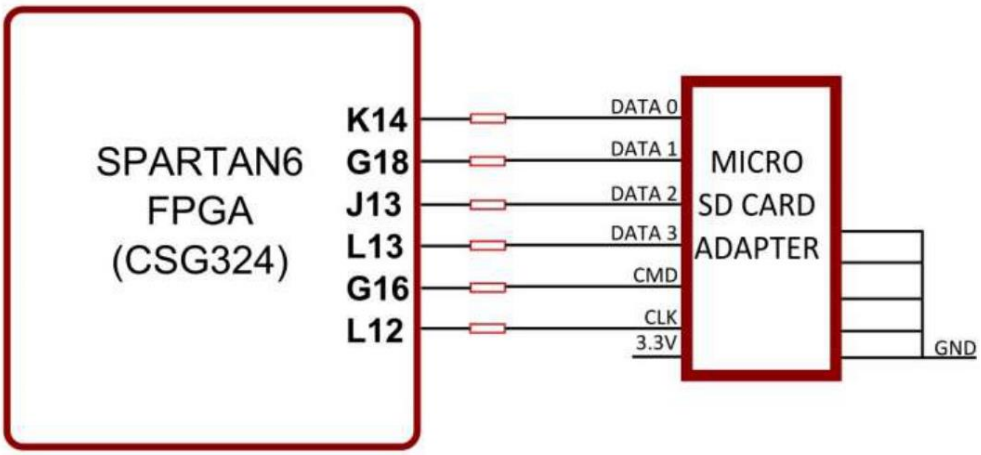
2.10. Micro SD

MIMAS V2 features a Micro SD adapter on-board. By installing a Micro SD card, you can add data logging, media storage and other file storage to your design.

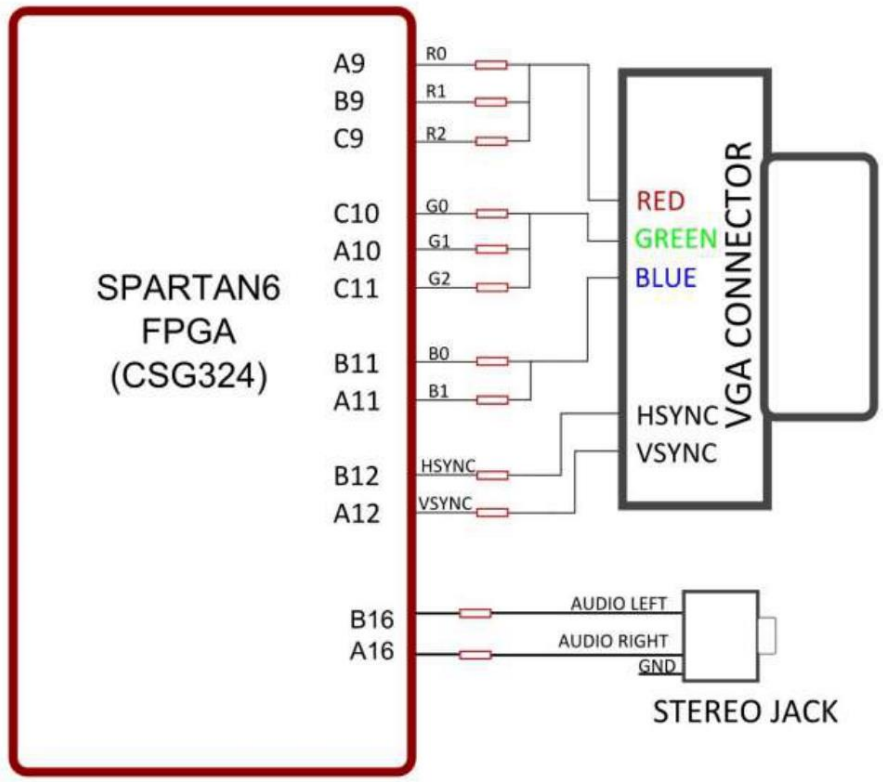


(https://numato.com/help/wp-content/uploads/2016/03/mimasv2-microsd.png)

2.11. VGA and Audio

The VGA interface provides this board the ability to generate VGA signals from FPGA and display information on any Display/monitor that supports standard VGA connector. This VGA interface uses resistor network-based DAC for easy code implementation. This 8 bit VGA interface can display up to 256 colors.

Two IOs on the FPGA is dedicated to generating two channels of audio. Different audio tones can be generated by using PWM and Frequency synthesis.



(https://numato.com/help/wp-content/uploads/2016/03/mimasv2-vga-audio.png)

2.12. 7Segment LED Display

This board features three 7-segment LED display multiplexed for low pin count operation. Each module can be separately turned on and off with the three switching transistors.

Note: All signals (*a, b, c, d, e, f, g, dot, enable 1, enable 2, enable 3*) used for controlling 7-Segment display are **active-low** signals**.** So, for example, for displaying "8" in display-2, users need to drive *Enable 2* to *0* as well as drive signals *a, b, c, d, e, f* to *0*. All other signals need to be driven to 1.

- **LIGHT EMITTING DIODE**

Standard LED

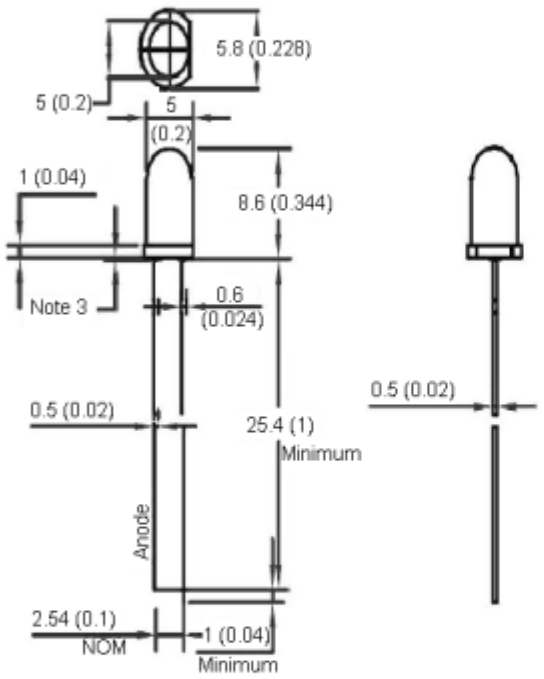
Red Emitting Colour

multicomp

Features:

- High intensity
- Standard T-1 3/4 diameter package
- General purpose leads
- Reliable and rugged

Package Dimensions:



Dimensions : Millimetres (Inches)

Specification Table

Chip Material	Lens Colour	Source Colour	Part Number
AlGaAs	Diffused	Red	MV5754A

Notes:

1. Tolerance is ±0.25 mm (0.01") unless otherwise noted
2. Protruded resin under flange is 1 mm (0.04") maximum
3. Lead spacing is measured where the leads emerge from the package

www.element14.com
www.farnell.com
www.newark.com

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Page <1>

18/10/11 V1.1

Standard LED

Red Emitting Colour

multicomp

Absolute Maximum Ratings at T_a = 25°C

Parameter	Maximum	Unit
Power Dissipation	80	mW
Peak Forward Current (1/10 Duty Cycle, 0.1 ms Pulse Width)	100	mA
Continuous Forward Current	20	
Derating Linear From 50°C	0.4	mA / °C
Reverse Voltage	5	V
Operating Temperature Range	-25°C to +80°C	
Storage Temperature Range	-40°C to +100°C	
Lead Soldering Temperature (4 mm (0.157) Inches from Body)	260°C for 5 s	

Electrical Optical Characteristics at T_a = 25°C

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Test Condition
Luminous Intensity	I_v		40		mcd	I_f = 20 mA (Note 1)
Viewing Angle	$2\theta_{1/2}$		25		Deg	(Note 2)
Peak Emission Wavelength	λp		640		nm	I_f = 20 mA
Dominant Wavelength	λd		635		nm	I_f = 20 mA (Note 3)
Spectral Line Half-Width	Δλ		25		nm	I_f = 20 mA
Forward Voltage	V_f		2	2.5	V	I_f = 20 mA
Reverse Current	I_R	-	-	100	µA	V_R = 5 V

Notes:

1. Luminous intensity is measured with a light sensor and filter combination that approximates the CIE eye-response curve
2. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity
3. The dominant wavelength (λd) is derived from the CIE chromaticity diagram and represents the single wavelength which defines the colour of the device

- **DIGITAL TO ANALOG CONVERTER**

TEXAS INSTRUMENTS

DAC5681

www.ti.com

SLLS864C – AUGUST 2007 – REVISED AUGUST 2012

16-BIT, 1.0 GSPS Digital-to-Analog Converter (DAC)

Check for Samples: DAC5681

FEATURES

- **16-Bit Digital-to-Analog Converter (DAC)**
- **1.0 GSPS Update Rate**
- **16-Bit Wideband Input LVDS Data Bus**
  - **8 Sample Input FIFO**
  - **On-Chip Delay Lock Loop**
- **High Performance**
  - **73 dBc ACLR WCDMA TM1 at 180 MHz**
- **On Chip 1.2 V Reference**
- **Differential Scalable Output: 2 to 20 mA**
- **Package: 64-Pin 9 × 9 mm QFN**

APPLICATIONS

- **Cellular Base Stations**
- **Broadband Wireless Access (BWA)**
- **WiMAX 802.16**
- **Fixed Wireless Backhaul**
- **Cable Modem Termination System (CMTS)**
- **Medical / Test Instrumentation**
- **Radar Systems**

DESCRIPTION

The DAC5681 is a 16-bit 1.0 GSPS digital-to-analog converter (DAC) with wideband LVDS data input and internal voltage reference. The DAC5681 offers superior linearity and noise performance.

The DAC5681 integrates a wideband LVDS port with on-chip termination, providing full 1.0 GSPS data transfer into the DAC and lower EMI than traditional CMOS data interfaces. An on-chip delay lock loop (DLL) simplifies LVDS interfacing by providing skew control for the LVDS input data clock.

The current-steering architecture of the DAC5681 consists of a segmented array of current sinking switches directing up to 20mA of full-scale current to complementary output nodes. An accurate on-chip voltage reference is temperature-compensated and delivers a stable 1.2-V reference voltage. Optionally, an external reference may be used.

The DAC5681 is characterized for operation over the industrial temperature range of –40°C to 85°C and is available in a 64-pin QFN package. The device is pin upgradeable to the other members of the family: the DAC5681Z and DAC5682Z. The single-channel DAC5681Z and dual-channel DAC5682Z both provide optional 2x/4x interpolation and a clock multiplying PLL.

ORDERING INFORMATION

T_A	ORDER CODE	PACKAGE DRAWING/TYPE (1) (2) (3)	TRANSPORT MEDIA	QUANTITY
–40°C to 85°C	DAC5681IRGCT	RGC / 64QFN Quad Flatpack No-Lead	Tape and Reel	250
	DAC5681IRGCR		Tape and Reel	2000

(1) Thermal Pad Size: 7,4 mm × 7,4 mm
(2) MSL Peak Temperature: Level-3-260C-168 HR
(3) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM