



Class:	SE	Semester:	III
Course Code:	CSC304	Course Name:	DLCA

Name of Student:	SHARVAT ANAND BHONDEKAR.
Roll No. :	06
Assignment No.:	03
Title of Assignment:	PROCESSOR ORGANISATION & ARCHITECTURE.
Date of Submission:	06/09/24
Date of Correction:	06/09/24.

Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Completeness	5	5
Demonstrated Knowledge	3	3
Legibility	2	2
Total	10	10

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Completeness	5	3-4	1-2
Demonstrated Knowledge Legibility	3	2	1
Legibility	2	1	0

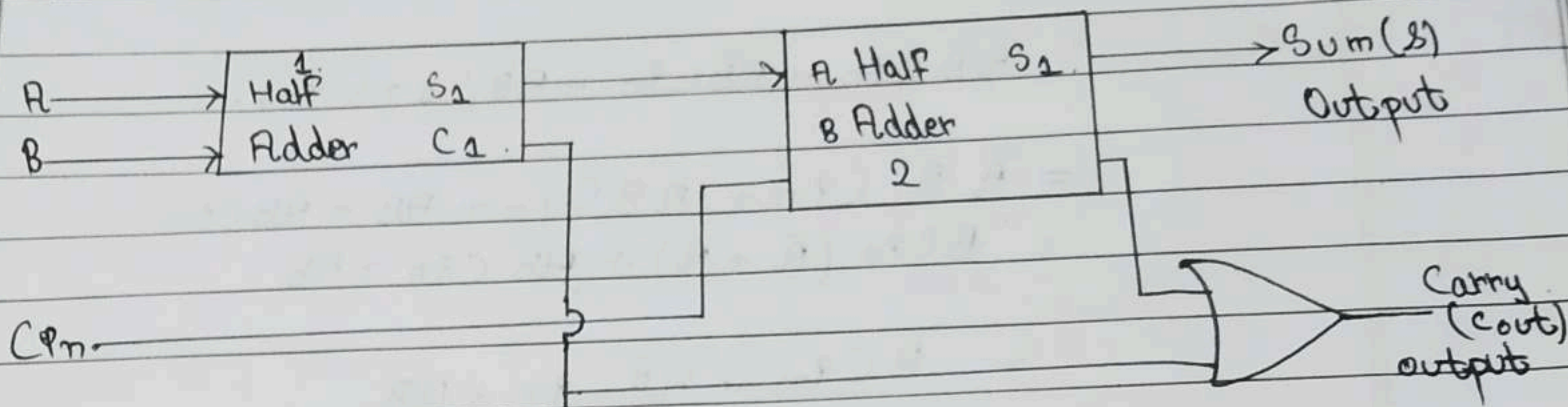
Checked by

Faculty : Miss. Kshitija Gharat.
: Gharat
: 6/9/24

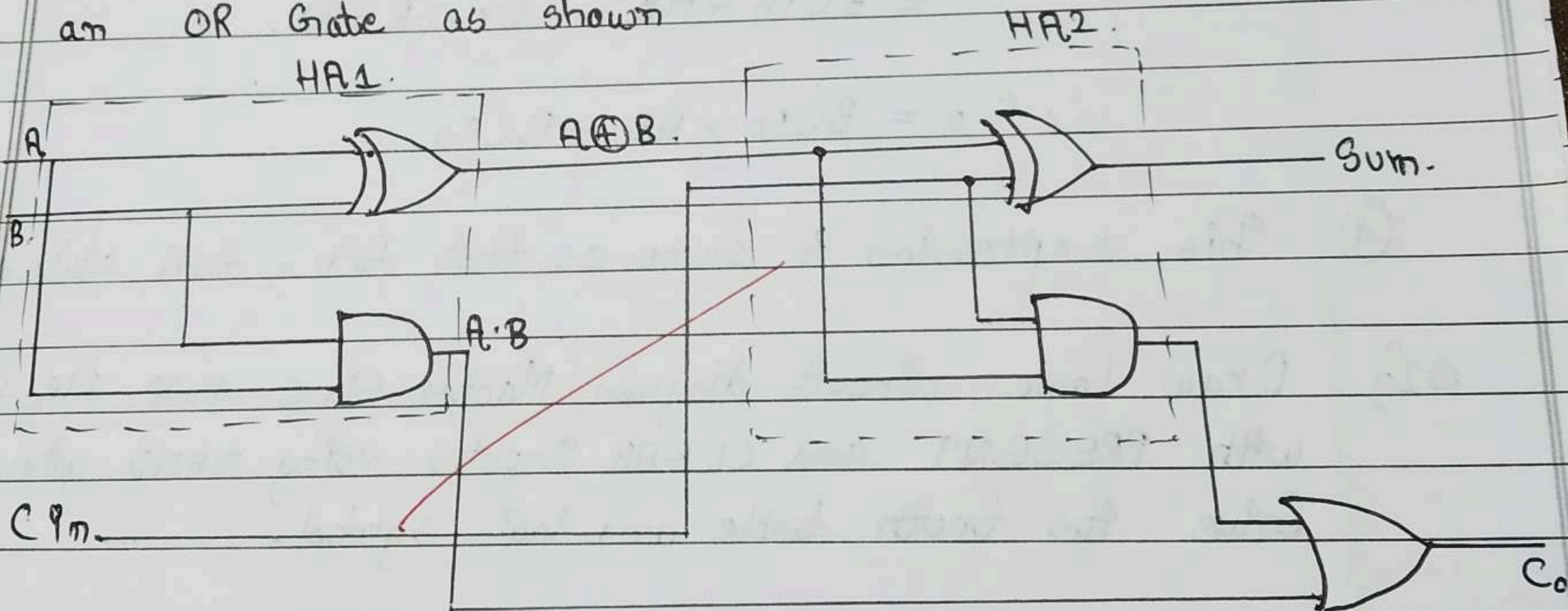
Assignment No. 3

Q1. Apply the concept of half adder and additional gates to design full adder.

→ A full adder circuit can be constructed using two half adder.



Q2. A full adder can be implemented using two half adders or an OR Gate as shown



$$\text{Here, } S = (A \oplus B) \oplus C_{in} = A \oplus B \oplus C_{in}.$$

Q3. This expression is same as that obtained from for the full adder. Thus the sum output has been successfully

Implemented by the circuit.

$$C_o = (A \oplus B) C_{in} + AB$$

$$C_o = (\overline{AB} + \overline{AB}) C_{in} + AB = \overline{A}B C_{in} + A\overline{B} C_{in} + AB$$

$$= \overline{A}B C_{in} + A\overline{B} C_{in} + AB(1 + C_{in})$$

$$= \overline{A}B C_{in} + A\overline{B} C_{in} + AB + AB C_{in}$$

$$= BC_{in}(\overline{A} + A) + A\overline{B} C_{in} + AB$$

$$= BC_{in} + A\overline{B} C_{in} + AB$$

$$= BC_{in} + A\overline{B} C_{in} + AB(1 + C_{in})$$

$$= BC_{in} + AB + AC_{in}(\overline{B} + B)$$

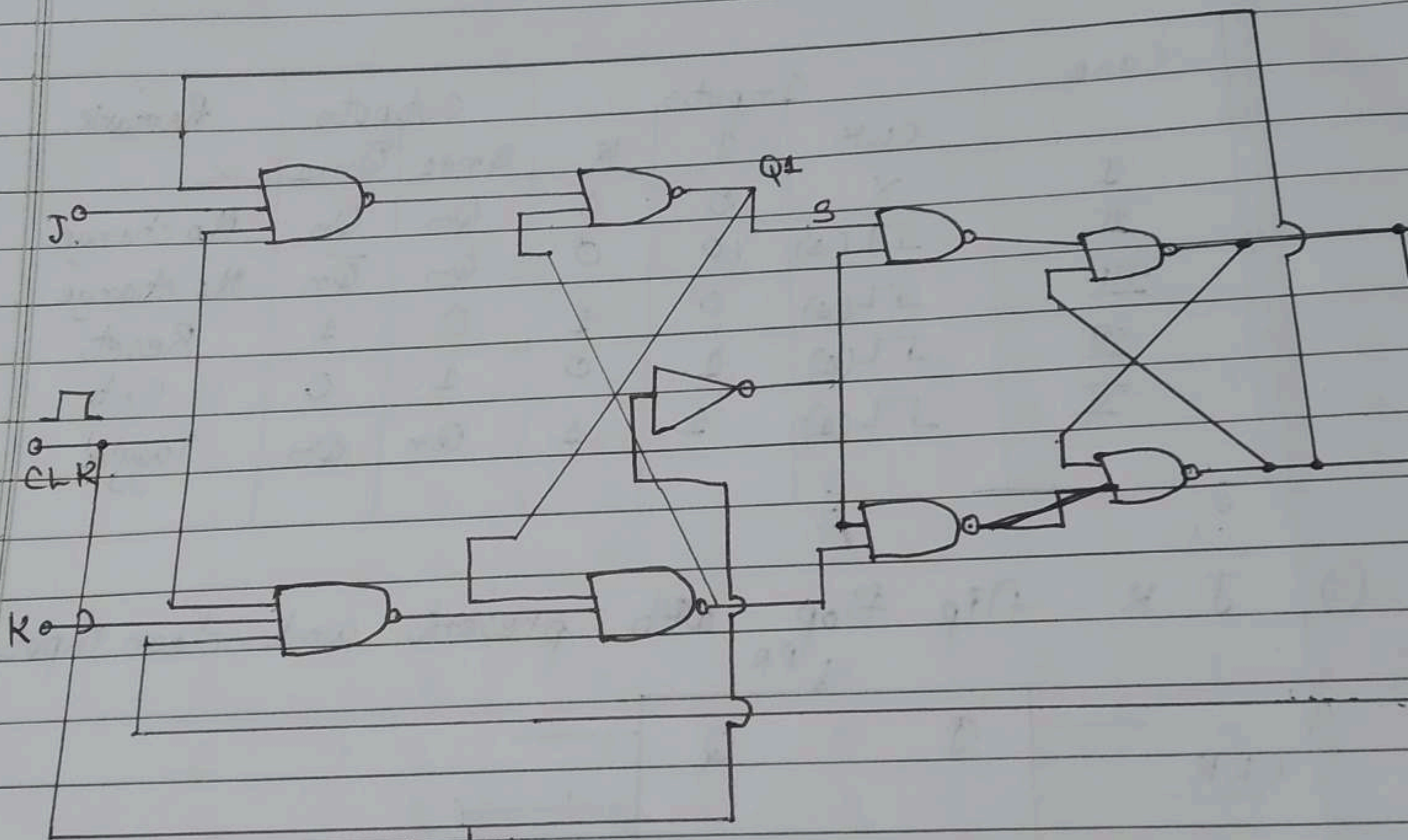
$$\therefore C_o = BC_{in} + AB + AC_{in}$$

④ This expression is same as that for a full adder.

Q2.) Draw logic circuit diagram Master-Slave J-K flip-flop with PRESENT and CLEAR inputs using NAND gates. Give its truth table and logic symbol.

→ ① Circuit Diagram:

The Circuit Diagram of Master Slave JK flip-flop with PRESENT & CLEAR inputs using NAND gates is shown as:

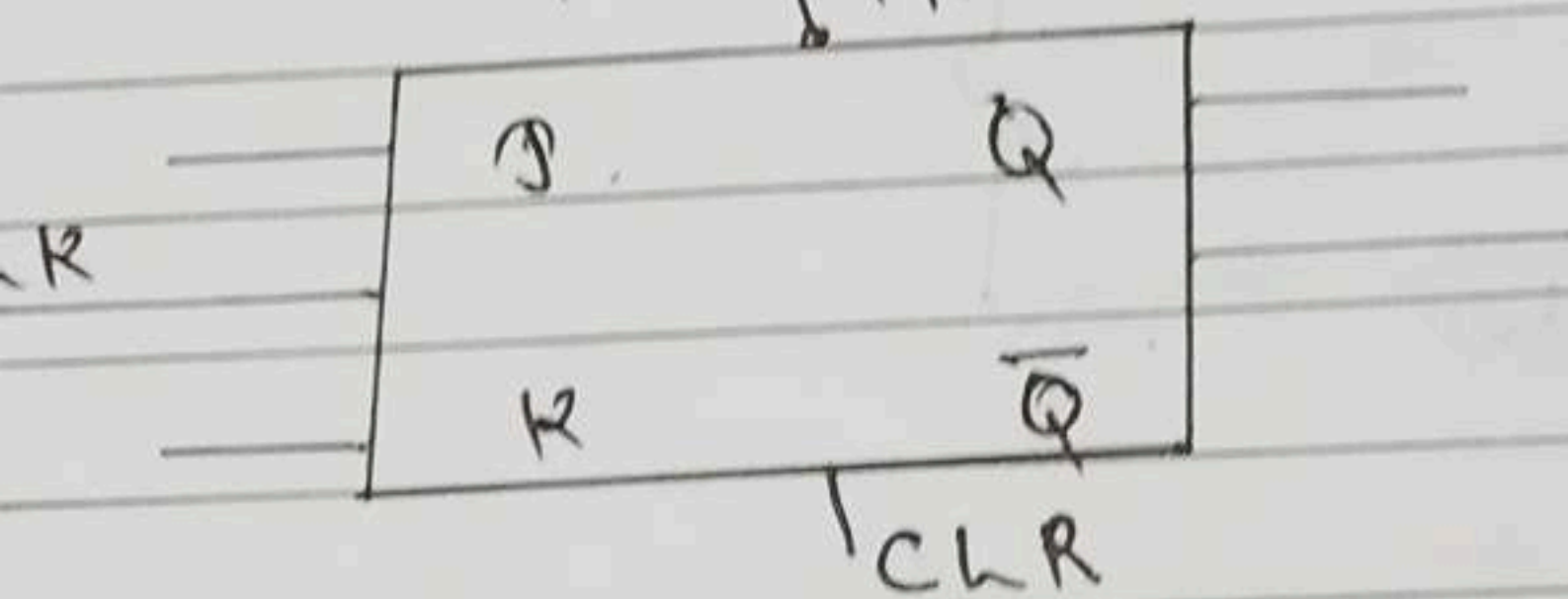


Master.

Truth table.

Case	Inputs			Outputs		Remark
	CLK	J	K	Q_{n+1}	\bar{Q}_{n+1}	
I	X	0	0	Q_n	\bar{Q}_n	No change
II	$\downarrow L(1)$	0	0	Q_n	\bar{Q}_n	No change
III	$\downarrow L(1)$	0	1	0	1	Reset
IV	$\downarrow L(1)$	1	0	1	0	Set
V	$\downarrow L(1)$	1	1	Q_n	\bar{Q}_n	Toggle

J K flip flop with present and clear inputs.



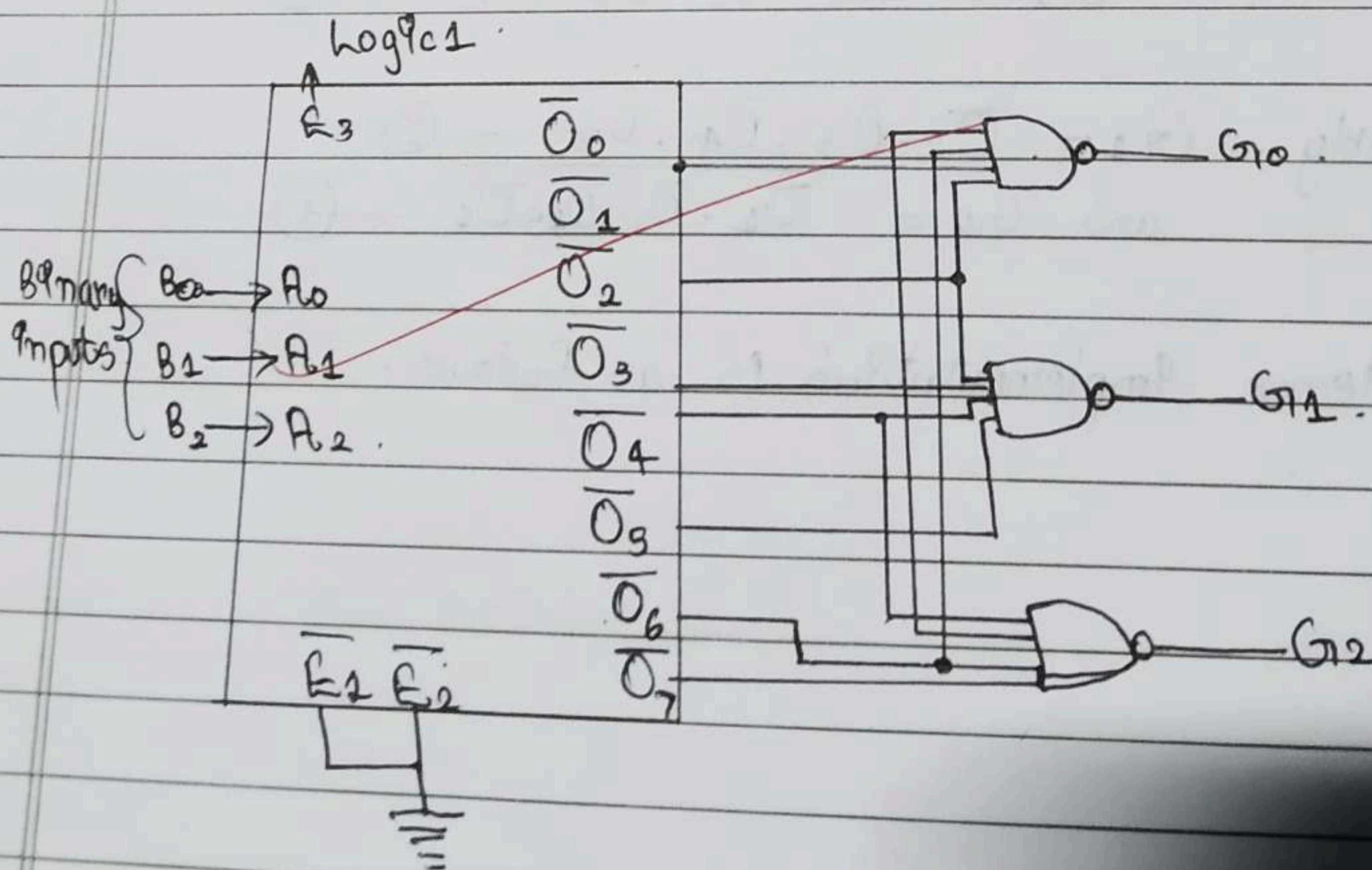
Truth table.

Input			Output	Operation performed.
J	PR	CLR		
1	1	1	Q_{n+1}	Normal JK FF.
0	1	1	1	FF is set.
1	0	0	0	FF is reset.

Q3. Implement a 3-bit binary to gray code converter using decoder IC 74138.

→ Step 1: Truth table relating the binary and gray code

Decimal	Binary Input			Gray outputs		
	B_2	B_1	B_0	G_2	G_1	G_0
0	0	0	0	0	0	0
1	0	0	1	0	0	1
2	0	1	0	0	1	1
3	0	1	1	0	1	0
4	1	0	0	1	1	0
5	1	0	1	1	1	1
6	1	1	0	1	0	1
7	1	1	1	1	0	0



Step 2: Expression for G_2 , G_1 and G_0 :

Normally the expressions for G_2 , G_1 , and G_0 would have been written as

$$G_2 = O_4 + O_5 + O_6 + O_7$$

$$G_1 = O_2 + O_3 + O_4 + O_5$$

$$G_0 = O_1 + O_2 + O_3 + O_6$$

But the outputs of IC 74138 are active low
Hence we will convert these equations.

$$G_2 = O_4 + O_5 + O_6 + O_7 = \overline{\overline{O_4 + O_5 + O_6 + O_7}}$$

$$\text{But } \overline{A+B} = \overline{A} \cdot \overline{B}$$

$$\therefore G_2 = \overline{O_4} \cdot \overline{O_5} \cdot \overline{O_6} \cdot \overline{O_7} \quad \text{--- (1)}$$

$$\text{Similarly, } G_1 = \overline{O_2} \cdot \overline{O_3} \cdot \overline{O_4} \cdot \overline{O_5} \quad \text{--- (2)}$$

$$\text{and } G_0 = \overline{O_1} \cdot \overline{O_2} \cdot \overline{O_3} \cdot \overline{O_6} \quad \text{--- (3)}$$

Hence implementation is as follows.