Team #25

Spi protocol implementation

Mentor TA: Nikhil

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INTRODUCTION

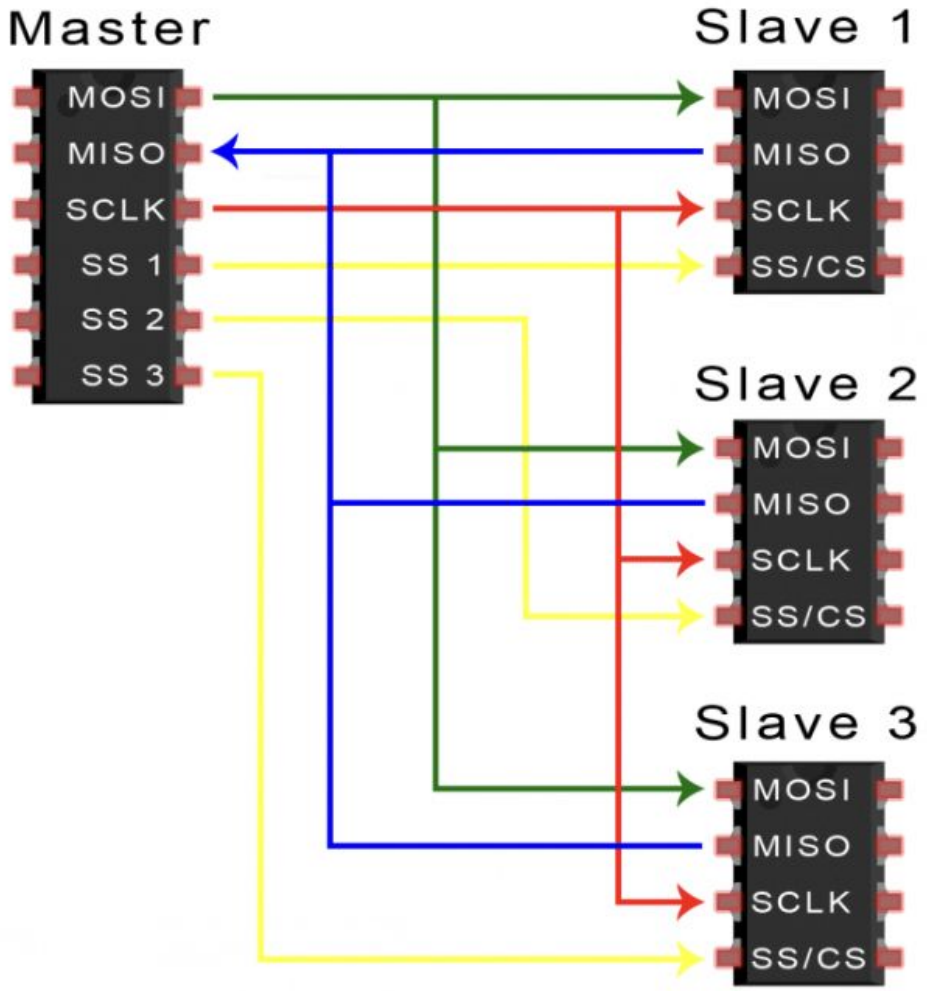
- SPI stands for Serial Peripheral Interface. It is a protocol that is synchronous serial communication. It is used to communicate between the peripheral devices i.e. input and output devices and microcontrollers. SPI can transfer the data and receive data from one device to another device at a time.
- Common applications:
  communicate with the sensors like temperature sensors, accelerometers, gyroscopes, actuators like motors and servos, memory devices like EEPROMs and flash memory, and displays like LCDs and OLEDs, etc.

Master-slave Relationship

- The master is the controlling device (usually a microcontroller), while the slave (usually a sensor, display, or memory chip) takes instruction from the master. The simplest configuration of SPI is a single master, single slave system, but one master can control more than one slave.
- **MOSI (Master Output/Slave Input)** – Line for the master to send data to the slave.
- **MISO (Master Input/Slave Output)** – Line for the slave to send data to the master.
- **SCLK (Clock)** – Line for the clock signal.
- **SS/CS (Slave Select/Chip Select)** – Line for the master to select which slave to send data to.

SPI mode	Clock polarity (CPOL)	Clock phase (CPHA)	Data is shifted out on	Data is sampled on
0	0	0	falling SCLK, and when $\overline{CS}$ activates	rising SCLK
1	0	1	rising SCLK	falling SCLK
2	1	0	rising SCLK, and when $\overline{CS}$ activates	falling SCLK
3	1	1	falling SCLK	rising SCLK

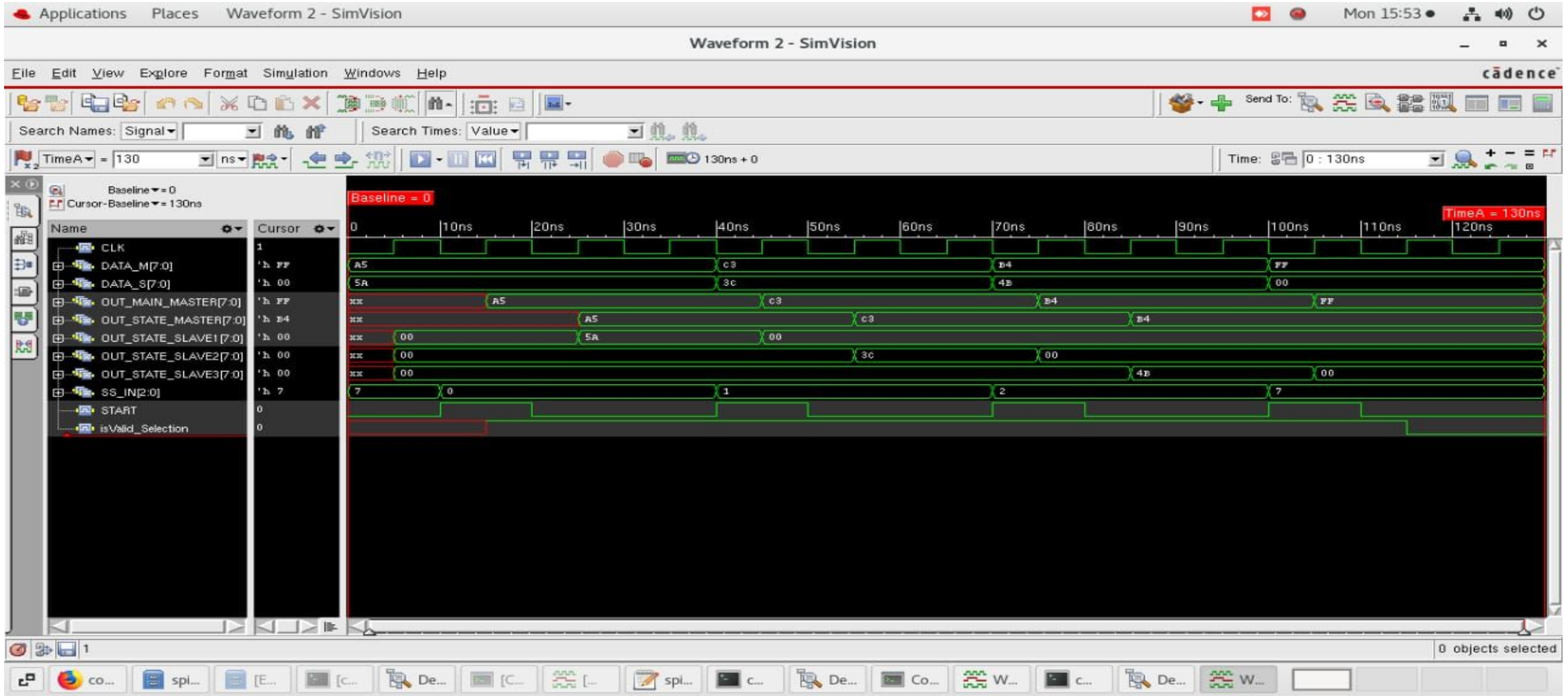
Block Diagrams



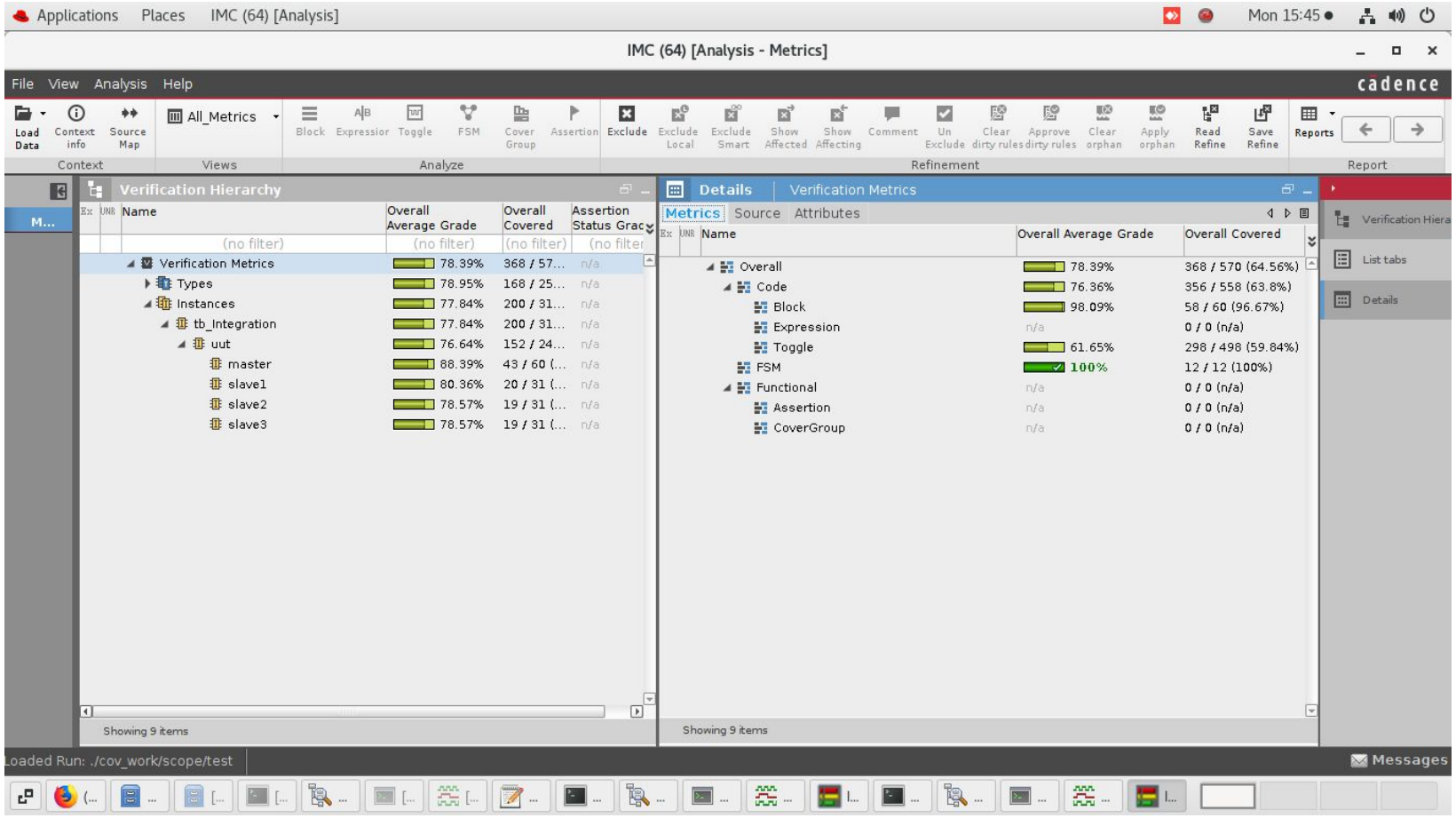
Individual Contribution

- Rohith: Master code implemented
- Yash More: Slave code implemented
- Sharvi Ranjan: Slave code implemented
- Dhanush: Master code implemented

Waveforms (and explanation of design)



Coverage


Applications
Places
IMC (64) [Analysis]
Mon 15:45
IMC (64) [Analysis - Metrics]
File
View
Analysis
Help
cadence
Load Data
Context info
Source Map
All_Metrics
Block
Expression
Toggle
FSM
Cover Group
Assertion
Exclude
Exclude Local
Exclude Smart
Show Affected
Show Affecting
Comment
Un Exclude
Clear dirty rules
Approve dirty rules
Clear orphan
Apply orphan
Read Refine
Save Refine
Reports
Context
Views
Analyze
Refinement
Report
Verification Hierarchy
Name
Overall Average Grade
Overall Covered
Assertion Status Grac
(no filter)
Verification Metrics 78.39% 368 / 57... n/a
Types 78.95% 168 / 25... n/a
Instances 77.84% 200 / 31... n/a
tb_Integration 77.84% 200 / 31... n/a
uut 76.64% 152 / 24... n/a
master 88.39% 43 / 60 (... n/a
slave1 80.36% 20 / 31 (... n/a
slave2 78.57% 19 / 31 (... n/a
slave3 78.57% 19 / 31 (... n/a
Showing 9 items
Details
Verification Metrics
Metrics
Source
Attributes
Name
Overall Average Grade
Overall Covered
Overall 78.39% 368 / 570 (64.56%)
Code 76.36% 356 / 558 (63.8%)
Block 98.09% 58 / 60 (96.67%)
Expression n/a 0 / 0 (n/a)
Toggle 61.65% 298 / 498 (59.84%)
FSM 100% 12 / 12 (100%)
Functional n/a 0 / 0 (n/a)
Assertion n/a 0 / 0 (n/a)
CoverGroup n/a 0 / 0 (n/a)
Showing 9 items
Verification Hiera
List tabs
Details
Loaded Run: ./cov_work/scope/test
Messages

Area Report

```
====================================================================
  Generated by:           Genus(TM) Synthesis Solution 20.11-s111_1
  Generated on:           Nov 07 2024  05:28:58 pm
  Module:                 Integration
  Technology library:     saed90nm_typ updated 30.Sep.2011
  Operating conditions:   _nominal_ (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
====================================================================

  Instance  Module  Cell Count  Cell Area  Net Area   Total Area   Wireload
--------------------------------------------------------------------------
Integration              135   2203.546     0.000     2203.546 <none> (D)
  (D) = wireload is default in technology library
```

Power Report

```
Instance: /Integration
Power Unit: W
PDB Frames: /stim#0/frame#0
  ---------------------------------------------------------------------------
    Category         Leakage      Internal    Switching        Total    Row%
  ---------------------------------------------------------------------------
       memory     0.00000e+00   0.00000e+00  0.00000e+00  0.00000e+00   0.00%
     register     8.75293e-06  -4.95837e-06  6.81132e-07  4.47569e-06  26.12%
        latch     0.00000e+00   0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        logic     1.96786e-06   2.22665e-06  2.23140e-06  6.42591e-06  37.50%
         bbox     0.00000e+00   0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        clock     0.00000e+00   0.00000e+00  6.23520e-06  6.23520e-06  36.38%
          pad     0.00000e+00   0.00000e+00  0.00000e+00  0.00000e+00   0.00%
           pm     0.00000e+00   0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ---------------------------------------------------------------------------
    Subtotal     1.07208e-05  -2.73173e-06  9.14774e-06  1.71368e-05 100.00%
  Percentage          62.56%       -15.94%       53.38%      100.00% 100.00%
  ---------------------------------------------------------------------------
```

Timing Report

Max Freq of your design:

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 20.11-s111_1
  Generated on:           Nov 07 2024  05:29:55 pm
  Module:                 Integration
  Operating conditions:   _nominal_ (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


Path 1: MET (19162 ps) Setup Check with Pin master_OUT_STATE_MASTER_reg[2]/CLK->SE
          Group: CLK
     Startpoint: (F) SS_IN[1]
          Clock: (R) CLK
       Endpoint: (F) master_OUT_STATE_MASTER_reg[2]/SE
          Clock: (R) CLK

                    Capture       Launch
        Clock Edge:+   20000            0
         Drv Adjust:+      0            0
        Src Latency:+      0            0
        Net Latency:+      0 (I)        0 (I)
            Arrival:=  20000            0
```

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 20.11-s111_1
  Generated on:           Nov 07 2024  05:29:55 pm
  Module:                 Integration
  Operating conditions:   _nominal_ (balanced_tree)
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     Startpoint: (F) SS_IN[1]
          Clock: (R) CLK
       Endpoint: (F) master_OUT_STATE_MASTER_reg[2]/SE
          Clock: (R) CLK

                    Capture       Launch
        Clock Edge:+   20000            0
         Drv Adjust:+      0            0
        Src Latency:+      0            0
        Net Latency:+      0 (I)        0 (I)
            Arrival:=  20000            0

              Setup:-    131
        Uncertainty:-    200
      Required Time:=  19669
       Launch Clock:-      0
        Input Delay:-    300
          Data Path:-    207
              Slack:=  19162

Exceptions/Constraints:
  input_delay             300             constraints.sdc_line_28_1_1

#-------------------------------------------------------------------------------------------------------------------
#           Timing Point            Flags    Arc    Edge   Cell      Fanout Load Trans Delay Arrival Instance
#                                                                      (fF)  (ps)  (ps)   (ps)  Location
#-------------------------------------------------------------------------------------------------------------------
  SS_IN[1]                          -       -       F     (arrival)      3  6.7     0     0     300    (-,-)
  g638__2398/QN                     -       IN3->QN R     NAND3X0        2  3.3    51    30     330    (-,-)
  g599__7482/Q                      -       IN3->Q  R     AND3X1         3  6.9    52    85     415    (-,-)
  g573__6417/QN                     -       IN1->QN F     NOR2X0         8 20.8   152    92     507    (-,-)
  master_OUT_STATE_MASTER_reg[2]/SE <<<     -       F     SDFFX1         8    -     -     0     507    (-,-)
#-------------------------------------------------------------------------------------------------------------------
```

Code B with both MISO and MOSI implementation

Our base code

References

- Base Code from:
  yahia3200/SPI-Protocol-Implementation-Using-Verilog

- Chatgpt link:

- Separate references(youtube ,google)
  https://github.com/daringpatil3134/SPI_Serial_Peripheral_Interface_Verilog_Modules

  https://www.youtube.com/watch?feature=shared&v=0LpfuZ1wz2w