

Specification

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1. Introduction

ILI9341 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes GRAM for graphic display data of 240RGBx320 dots, and power supply circuit.

ILI9341 supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

ILI9341 can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. ILI9341 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the ILI9341 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- Display resolution: [240xRGB](H) x 320(V)
- Output:
 - > 720 source outputs
 - > 320 gate outputs
 - Common electrode output (VCOM)
- a-TFT LCD driver with on-chip full display RAM: 172,800 bytes
- System Interface
 - ➤ 8-bits, 9-bits, 16-bits, 18-bits interface with 8080- I /8080- II series MCU
 - ➤ 6-bits, 16-bits, 18-bits RGB interface with graphic controller
 - > 3-line / 4-line serial interface
- Display mode:
 - > Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
 - > Reduce color mode (Idle mode ON): 8-color
- Power saving mode:
 - Sleep mode
- On chip functions:
 - VCOM generator and adjustment
 - Timing generator
 - Oscillator
 - DC/DC converter
 - Line/frame inversion
 - > 1 preset Gamma curve with separate RGB Gamma correction
- Content Adaptive Brightness Control
- MTP (3 times):
 - > 8-bits for ID1, ID2, ID3
 - > 7-bits for VCOM adjustment

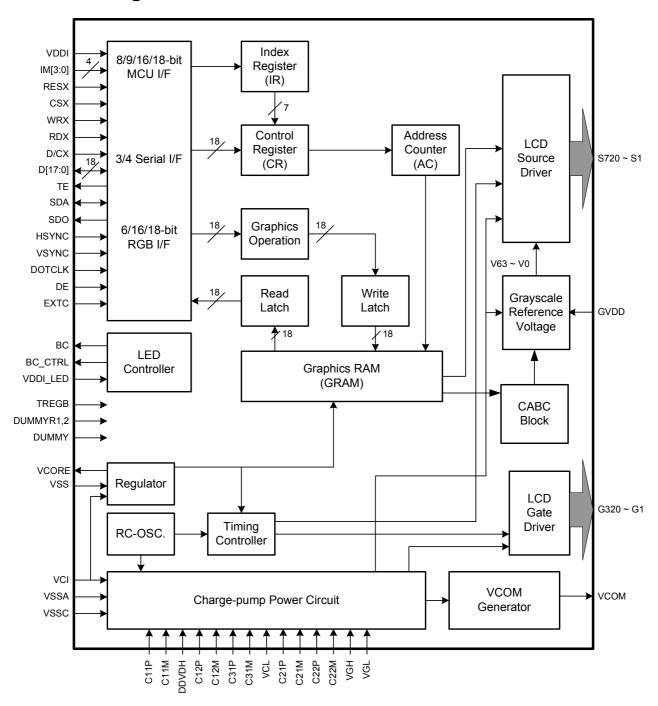




- Low -power consumption architecture
 - Low operating power supplies:
 - VDDI = 1.65V ~ 3.3V (logic)
 - VCI = 2.5V ~ 3.3V (analog)
- LCD Voltage drive:
 - Source/VCOM power supply voltage
 - DDVDH GND = 4.5V ~ 5.8V
 - VCL GND = -1.5V ~ -2.5V
 - > Gate driver output voltage
 - VGH GND = 10.0V ~ 16.0V
 - VGL GND = -5.0V ~ -10.0V
 - VGH VGL \leq 28V
 - > VCOM driver output voltage
 - VCOMH = 3.0V ~ (DDVDH 0.2)V
 - VCOML = (VCL+0.2)V ~ 0V
 - VCOMH VCOML ≤ 6.0 V
- ◆ Operate temperature range: -40°C to 85°C
- ◆ a-Si TFT LCD storage capacitor : Cst on Common structure only



3. Block Diagram







4. Pin Descriptions

	Power Supply Pins									
Pin Name	I/O	Type	Descriptions							
VDDI	I	Р	Low voltage power supply for interface logic circuits (1.65 ~ 3.3 V)							
VDDI_LED	LED I		Power supply for LED driver interface. (1.65 ~ 3.3 V) If LED driver is not used, fix this pin at VDDI.							
VCI	I	Analog Power	High voltage power supply for analog circuit blocks (2.5 ~ 3.3 V)							
Vcore	0	Digital Power	Regulated Low voltage level for interface circuits Connect a capacitor for stabilization. Don't apply any external power to this pad							
VSS3	I	I/O Ground	System ground level for I/O circuits.							
VSS	VSS I Digital Ground		System ground level for logic blocks							
VSSA I Analog Ground		Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise.							
VSSC I Analog Ground		Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise							

Interface Logic Signals Pin Name I/O Type Descriptions														
I/O	Туре		Descriptions											
						face mode	DR Pin in I	150						
		IM3	IM2	IM1	IM0	MCU-Interface Mode		GRAM						
		0	0	0	0	80 MCU 8-bit bus interface I	D[7:0]	D[7:0]						
		0	0	0	1	80 MCU 16-bit bus interface I	D[7:0]	D[15:0]						
		0	0	1	0	80 MCU 9-bit bus interface I	D[7:0]	D[8:0]						
		0	0	1	1	80 MCU 18-bit bus interface I	D[7:0]	D[17:0]						
I	(VDDI/VSS)	(VDDI/VSS)	(VDDI/VSS)	(VDDI/VSS)				0	1	0	1	3-wire 9-bit data serial interface I	SDA: In/Ol	JT
									0	1	1	0	4-wire 8-bit data serial interface I	SDA: In/Ol
					1	0	0	0	80 MCU 16-bit bus interface II	D[8:1]	D[17:10], D[8:1]			
					1	0	0	1	80 MCU 8-bit bus interface II	D[17:10]	D[17:10]			
		1	0	1	0	80 MCU 18-bit bus interface II	D[8:1]	D[17:0]						
			1	0	1	1	80 MCU 9-bit bus interface Ⅱ	D[17:10]	D[17:9]					
								1	1	0	1	3-wire 9-bit data serial interface II	SDI: In SDO: Ou	t
									1	1	1	0	4-wire 8-bit data serial interface II	SDI: In SDO: Ou
		MPU	Paral	lel int	erface	bus and serial inter	face select							
		If use	RGB	Inter	face r	nust select serial inte	erface.							
			I/O Type - Sele	I/O Type - Select the IM3 IM2	I/O Type - Select the MCU IM3 IM2 IM1	I/O Type - Select the MCU interest IM3 IM2 IM1 IM0	I/O Type	I/O Type						





	1						
DECV		MCU	This signal will reset the device and must be applied to properly				
RESX	I	(VDDI/VSS)	initialize the chip.				
EXTC	I	MCU (VDDI/VSS)	Signal is active low. Extended command set enable. Low: extended command set is discarded. High: extended command set is accepted. Please connect EXTC to VDDI to read/write extended registers (RB0h~RCFh, RE0h~RFFh)				
CSX	I	MCU (VDDI/VSS)	Chip select input pin ("Low" enable). This pin can be permanently fixed "Low" in MPU interface mode only. * note1,2				
			This pin is used to select "Data or Command" in the parallel interface				
			or 4-wire 8-bit serial data interface.				
		14011	When DCX = '1', data is selected.				
D/CX (SCL)	I	MCU (VDDI/VSS)	When DCX = '0', command is selected.				
		,	This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit				
			serial data interface.				
			If not used, this pin should be connected to VDDI or VSS.				
RDX	I	MCU (VDDI/VSS)	8080- I /8080- II system (RDX): Serves as a read signal and MCU read data at the rising edge. Fix to VDDI level when not in use.				
WRX (D/CX) I MCU (VDDI/VSS)			 - 8080- I /8080- II system (WRX): Serves as a write signal and writes data at the rising edge. - 4-line system (D/CX): Serves as command or parameter select. Fix to VDDI level when not in use. 				
D[17:0]	I/O	MCU (VDDI/VSS)	18-bit parallel bi-directional data bus for MCU system and RGB interface mode Fix to VSS level when not in use				
			When IM[3] : Low, Serial in/out signal.				
SDI/SDA	I/O	MCU	When IM[3]: High, Serial input signal.				
SDI/SDA	1/0	(VDDI/VSS)	The data is applied on the rising edge of the SCL signal.				
			If not used, fix this pin at VDDI or VSS.				
	_	MCU	Serial output signal.				
SDO	0	(VDDI/VSS)	The data is outputted on the falling edge of the SCL signal.				
			If not used, open this pin Tearing effect output pin to synchronize MPU to frame writing,				
		MCU	activated by S/W command. When this pin is not activated, this pin is				
TE	0	(VDDI/VSS)	low.				
			If not used, open this pin.				
DOTCLK	I	MCU (VDDI/VSS)	Dot clock signal for RGB interface operation. Fix to VDDI or VSS level when not in use.				
VSYNC	I	MCU (VDDI/VSS)	Frame synchronizing signal for RGB interface operation. Fix to VDDI or VSS level when not in use.				
HSYNC	I	MCU (VDDI/VSS)	Line synchronizing signal for RGB interface operation. Fix to VDDI or VSS level when not in use.				
DE	I	MCU (VDDI/VSS)	Data enable signal for RGB interface operation. Fix to VDDI or VSS level when not in use.				





Note.

1. If CSX is connected to VSS in Parallel interface mode, there will be no abnormal visible effect to the display module.

Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions.

Furthermore there will be no influence to the Power Consumption of the display module.

2. When CSX='1', there is no influence to the parallel and serial interface.



LCD Driver Input/Output Pins										
Pin Name	I/O	Туре	Descriptions							
S720~S1	0	Source	Source output signals Leave the pin to open when not in use.							
G320~G1	0	Gate	Gate output signals. Leave the pin to open when not in use.							
DDVDH	0	Power Stabilizing capacitor	Output voltage of 1st step up circuit (2 x VCI). Input voltage to 2nd step up circuit. Generated power output pad for source driver block. Connect this pad to the capacitor for stabilization.							
VGH	0	Power Stabilizing capacitor	Power supply for the gate driver. Adjust the VGH level with the BT[2:0] bits. Connect this pad with a stabilizing capacitor.							
VGL	0	Power Stabilizing capacitor	Power supply for the gate driver. Adjust the VGL level with the BT[2:0] bits. Connect this pad with a stabilizing capacitor.							
VCL	0	Power Stabilizing capacitor	Power supply for VCOML. VCL = 0~ - VCI Connect this pad with a stabilizing capacitor.							
C11P, C11M C12P, C12M	Р	Stabilizing capacitor	Connect the charge-pumping capacitor for generating DDVDH level.							
C21P, C21M C22P, C22M	Р	Stabilizing capacitor	Connect the charge-pumping capacitor for generating VGH, VGL level.							
GVDD	0		High reference voltage for grayscale voltage generator. Internal register can be used to adjust the voltage.							
VCOM	0		Power supply pad for the TFT- display counter electrode. Charge recycling method is used with VCI and VSSA voltage. Connect this pad to the TFT-display counter electrode.							
LEDPWM	0		Output pin for PWM (Pulse Width Modulation) signal of LED driving. If not used, open this pad.							
LEDON	0		Output pin for enabling LED driving. If not used, open this pad.							

Test Pins									
Pin Name	I/O	Type	Descriptions						
DUMMY	_	Open	Input pads used only for test purpose at IC-side.						
BOWNVI		Орсп	During normal operation, leave these pads open.						





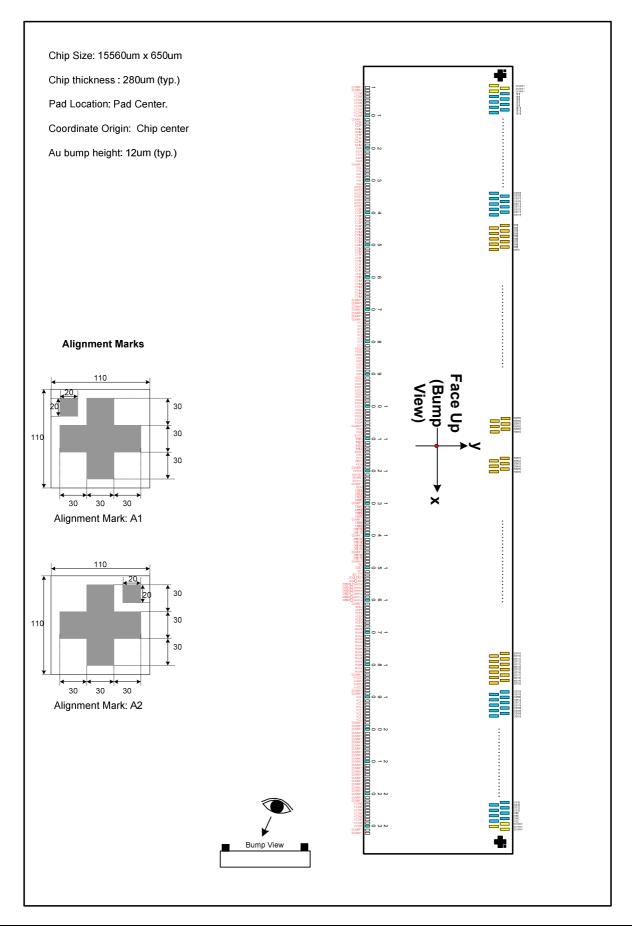
Liquid crystal power supply specifications Table

No.	Item		Description				
1	TFT Source Driver		720 pins (240 x RGB)				
2	TFT Gate Driver		320 pins				
3	TFT Display's Capacitor Structu	re	Cst structure only (Cs on Common)				
		S1 ~ S720	V0 ~ V63 grayscales				
4	Liquid Crystal Drive Output	G1 ~ G320	VGH - VGL				
1 TF 2 TF 3 TF 4 Liq 5 Inp		VCOM	VCOMH - VCOML: Amplitude = electronic volumes				
5	5 Input Voltage	VDDI	1.65V ~ 3.30V				
5	input voitage	VCI	2.50V ~ 3.30V				
		DDVDH	4.5V ~ 5.8V				
		VGH	10.0V ~ 16.0V				
6	Liquid Crystal Drive Voltages	VGL	-5.0V ~ -10.0V				
		VCL	-1.5V ~ -2.5V				
		VGH - VGL	Max. 28.0V				
		DDVDH	VCI x2,				
7	Internal Step-up Circuits	VGH	VCI x6, x7				
'	internal Step-up Circuits	VGL	VCI x-3, x-4,				
		VCL	VCI x-1				





5. Pad Arrangement and Coordination







No.	Pad name	Χ	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ
1	DUMMY	-7292.5	-248	51	C12M	-4292.5	-248	101	VSSA	-1292.5	-248	151	LEDPWM	2245	-248
2	DUMMY	-7232.5	-248	52	C12M	-4232.5	-248	102	VSSA	-1232.5	-248	152	LEDON	2330	-248
3	VCOM	-7172.5	-248	53	C11P	-4172.5	-248	103	VSSA	-1172.5	-248	153	VDDI LED	2402.5	-248
4	VCOM	-7112.5	-248	54	C11P	-4112.5	-248	104	VSSA	-1112.5	-248	154	VDDI LED	2462.5	-248
5	VCOM	-7052.5	-248	55	C11P	-4052.5	-248	105	VSSA	-1052.5	-248	155	DB[18] Dummy		-248
6	VCOM	-6992.5	-248	56	C11P	-3992.5	-248	106	DUMMY	-992.5	-248	156	DB[19] Dummy		-248
7	VCOM	-6932.5	-248	57	C11P	-3932.5	-248	107	VGS	-932.5	-248	157	DB[20] Dummy		-248
8	VCOM	-6872.5	-248	58	C11P	-3872.5	-248	108	VGS	-872.5	-248	158	DB[21]_Dummy	2790	-248
9	VCOM	-6812.5	-248	59	C11P	-3812.5	-248	109	EXTC	-812.5	-248	159	DB[22] Dummy		-248
10	VCOM	-6752.5	-248	60	C11M	-3752.5	-248	110	IM<3>	-752.5	-248	160	DB[23]_Dummy	2960	-248
11	DUMMY	-6692.5	-248	61	C11M	-3692.5	-248	111	IM<2>	-692.5	-248	161	DUMMY	3032.5	-248
12	C22P	-6632.5	-248	62	C11M	-3632.5	-248	112	IM<1>	-632.5	-248	162	VDDI	3092.5	-248
13	C22P	-6572.5	-248	63	C11M	-3572.5	-248	113	IM<0>	-572.5	-248	163	VDDI	3152.5	-248
14	C22M	-6512.5	-248	64	C11M	-3512.5	-248	114	RESX	-512.5	-248	164	VDDI	3212.5	-248
15	C22M	-6452.5	-248	65	C11M	-3452.5	-248	115	CSX	-452.5	-248	165	VDDI	3272.5	-248
16	C21P	-6392.5	-248	66	C11M	-3392.5	-248	116	DCX	-392.5	-248	166	VDDI	3332.5	-248
17	C21P	-6332.5	-248	67	(GND)	-3332.5	-248	117	WRX	-332.5	-248	167	VDDI	3392.5	-248
18	C21M	-6272.5	-248	68	(GND)	-3272.5	-248	118	RDX	-272.5	-248	168	VDDI	3452.5	-248
19	C21M	-6212.5	-248	69	(GND)	-3212.5	-248	119	DUMMY	-212.5	-248	169	Vcore	3512.5	-248
20	VGH	-6152.5	-248	70	(GND)	-3152.5	-248	120	VSYNC	-152.5	-248	170	Vcore	3572.5	-248
21	VGH	-6092.5	-248	71	(GND)	-3092.5	-248	121	HSYNC	-92.5	-248	171	Vcore	3632.5	-248
22	VGH	-6032.5	-248	72	(GND)	-3032.5	-248	122	ENABL	-32.5	-248	172	Vcore	3692.5	-248
23	VGH	-5972.5	-248	73	(GND)	-2972.5	-248	123	DOTCLK	27.5	-248	173	Vcore	3752.5	-248
24	VGH	-5912.5	-248	74	VCI	-2912.5	-248	124	DUMMY	87.5	-248	174	Vcore	3812.5	-248
25	DUMMY	-5852.5	-248	75	VCI	-2852.5	-248	125	SDA	160	-248	175	Vcore	3872.5	-248
26	VGL	-5792.5	-248	76	VCI	-2792.5	-248	126	DB[0]	245	-248	176	Vcore	3932.5	-248
27	VGL	-5732.5	-248	77	VCI	-2732.5	-248	127	DB[1]	330	-248	177	Vcore	3992.5	-248
28	VGL	-5672.5	-248	78	VCI	-2672.5	-248	128	DB[2]	415	-248	178	Vcore	4052.5	-248
29	VGL	-5612.5	-248	79	VCI	-2612.5	-248	129	DB[3]	500	-248	179	Vcore	4112.5	-248
30	VGL	-5552.5	-248	80	VCI	-2552.5	-248	130	DUMMY	572.5	-248	180	Vcore	4172.5	-248
31	VGL	-5492.5	-248	81	VCI	-2492.5	-248	131	DB[4]	645	-248	181	Vcore	4232.5	-248
32	DDVDH	-5432.5	-248	82	VSS3	-2432.5	-248	132	DB[5]	730	-248	182	Vcore	4292.5	-248
33	DDVDH	-5372.5	-248	83	VSS3	-2372.5	-248	133	DB[6]	815	-248	183	DUMMY	4352.5	-248
34	DDVDH	-5312.5	-248	84	VSS3	-2312.5	-248	134	DB[7]	900	-248	184	GVDD	4412.5	-248
35	DDVDH	-5252.5	-248	85	VSS	-2252.5	-248	135	DUMMY	972.5	-248	185	GVDD	4472.5	-248
36	DDVDH	-5192.5	-248	86	VSS	-2192.5	-248	136	DB[8]	1045	-248	186	GVDD	4532.5	-248
37	DDVDH	-5132.5	-248	87	VSS	-2132.5	-248	137	DB[9]	1130	-248	187	GVDD	4592.5	-248
38	DDVDH	-5072.5	-248	88	VSS	-2072.5	-248	138	DB[10]	1215	-248	188	DUMMY	4652.5	-248
39	C12P	-5012.5	-248	89	VSS	-2012.5	-248	139	DB[11]	1300	-248	189	DUMMY	4712.5	-248
40	C12P	-4952.5	-248	90	VSS	-1952.5	-248	140	DUMMY	1372.5	-248	190	VCL	4772.5	-248
41	C12P	-4892.5	-248	91	VSSC	-1892.5	-248	141	DB[12]	1445	-248	191	VCL	4832.5	-248
42	C12P	-4832.5	-248	92	VSSC	-1832.5	-248	142	DB[13]	1530	-248	192	VCL	4892.5	-248
43	C12P	-4772.5	-248	93	VSSC	-1772.5	-248	143	DB[14]	1615	-248	193	VCL	4952.5	-248
44	C12P	-4712.5	-248	94	VSSC	-1712.5	-248	144	DB[15]	1700	-248	194	VCL	5012.5	-248
45	C12P	-4652.5	-248	95	VSSC	-1652.5	-248	145	DUMMY	1772.5	-248	195	VCL	5072.5	-248
46	C12M	-4592.5	-248	96	VSSC	-1592.5	-248	146	DB[16]	1845	-248	196	VCL	5132.5	-248
47	C12M	-4532.5	-248	97	VSSC	-1532.5	-248	147	DB[17]	1930	-248	197	VCL	5192.5	-248
48	C12M	-4472.5	-248	98	VSSA	-1472.5	-248	148	DUMMY	2002.5	-248	198	DUMMY	5252.5	-248
49	C12M	-4412.5	-248	99	VSSA	-1412.5	-248	149	TE	2075	-248	199	DUMMY	5312.5	-248
50	C12M	-4352.5	-248	100	VSSA	-1352.5	-248	150	SDO	2160	-248	200	DUMMY	5372.5	-248





DUMMMY S492.5 248 251 G322 7147 224 301 G132 G447 224 351 G232 G344 7133 33 302 G134 G433 33 352 G234 5733 33 33 303	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ
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DUMMY 552.5 248 253 G36 719 224 305 G136 G419 224 355 G236 5719 224 325 DUMMY 552.5 248 256 G40 7091 224 305 G140 G391 224 355 G236 5991 224 326 G17 G180 5792.5 248 256 G40 7091 224 305 G140 G391 224 355 G242 5977 93 396 G142 G377 93 356 G242 5977 93 396 G140 G391 224 355 G242 5977 93 396 G140 G391 224 355 G242 5977 93 396 G140 G391 224 355 G242 5977 93 396 G140 G391 224 357 G244 583 224 329 G180 5972.5 248 258 G460 7049 33 308 G146 G349 33 358 G246 5849 33 329 G180 5972.5 248 260 G50 7021 93 310 G150 G321 93 360 G250 5821 93 321 G180 G190																1
DUMMMY S612.5 248 256 G40 7097 34 366 G410 5391 224 355 G240 5591 224 320																
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200																
208		(GND)		-248		G42		93		G142		93				93
299 GAND 5912.5 248 289 GA8 7035 224 310 G150 6321 33 360 G250 6321 32 32 360 G250 6321 33 310 G150 6321 33 360 G250 6321 33 32 32 34 34 34 34 34	207	(GND)	5792.5	-248	257	G44	7063	224	307	G144	6363	224	357	G244	5663	224
210	208	(GND)	5852.5	-248	258	G46	7049	93	308	G146	6349	93	358	G246	5649	93
211	209	(GND)	5912.5	-248	259	G48	7035	224	309	G148	6335	224	359	G248	5635	224
212	210	(GND)	5972.5	-248	260	G50	7021	93	310	G150	6321	93	360	G250	5621	93
213	211	(GND)	6032.5	-248	261	G52	7007	224	311	G152	6307	224	361	G252	5607	224
214	212	(GND)	6092.5	-248	262	G54	6993	93	312	G154	6293	93	362	G254	5593	93
215 DUMMY 6372.5 -248 266 G60 6951 224 315 G160 6251 224 365 G260 5551 224 216 DUMMY 6392.5 -248 266 G62 6937 93 316 G162 6237 93 366 G262 5537 93 321 321 321 321 321 321 321 321 321 321 321 321 322 321 322 322 323 366 G262 5537 93 321 321 321 321 321 321 321 321 321 321 322 32	213	(GND)	6152.5	-248	263	G56	6979	224	313	G156	6279	224	363	G256	5579	224
216 DUMMY 6332.5 248 266 G62 6937 93 316 G162 6237 93 366 G262 5537 93 327 328	214	DUMMY	6212.5	-248	264	G58	6965	93	314	G158	6265	93	364	G258	5565	93
217	215	DUMMY	6272.5	-248	265	G60	6951	224	315	G160	6251	224	365	G260	5551	224
218 DUMMY 6452.5 -248 268 G66 6909 93 318 G166 6209 93 368 G266 5509 93 329 DUMMY 6572.5 -248 270 G70 6881 6895 224 321 G170 6167 224 370 G270 5481 93 322 G170 6167 224 371 G272 5467 224 322 DUMMY 6632.5 -248 272 G74 6853 93 322 G174 6153 93 372 G274 5453 93 322 G170 6167 224 371 G272 5467 224 322 DUMMY 6632.5 -248 272 G74 6853 93 322 G174 6153 93 372 G274 5453 93 322 G170 6167 224 373 G276 5439 224 322 C174 6153 93 374 G272 5467 224 322 C174 6153 93 374 G272 5467 224 322 C174 6153 93 374 G278 5453 93 322 G178 6167 224 375 G280 5411 224 325 G180 6111 224 375 G280 5411 224 325 G180 6111 224 375 G280 5411 224 322 323 G176 6167 224 375 G280 5411 224 325 G180 6111 224 375 G280 5411 224 322 323 G176 6167 324 325 G180 6111 224 375 G280 5411 224 325 G180 6111 224 375 G280 5411 324 3	216	DUMMY	6332.5	-248	266	G62	6937	93	316	G162	6237	93	366	G262	5537	93
DUMMY 6512.5 248 269 G68 6895 224 319 G168 6195 224 369 G268 5495 224 220 DUMMY 6502.5 2-248 270 G70 6881 93 320 G170 6181 93 370 G270 5481 93 321 DUMMY 6692.5 2-248 272 G74 6865 93 322 G174 6153 93 370 G270 5467 224 222 222 223 VCOM 6752.5 2-248 273 G76 6889 224 323 G176 6139 224 373 G276 5453 93 322 225 VCOM 6812.5 2-248 275 G80 6811 224 225 VCOM 6892.5 2-248 275 G80 6811 224 225 VCOM 6892.5 2-248 276 G822 6797 93 326 G182 6097 93 374 G278 5425 593 322 325 G180 6111 224 375 G280 5411 224 226 VCOM 6992.5 2-248 276 G822 6797 93 326 G182 6097 93 376 G282 5397 93 322	217	DUMMY	6392.5	-248	267	G64	6923	224	317	G164	6223	224	367	G264	5523	224
DUMMY 6572.5 248 270 G70 6881 93 320 G170 6181 93 370 G270 5481 93 321 DUMMY 6632.5 248 271 G72 6867 224 321 G172 6167 224 371 G272 5467 224 323 C0M 6752.5 248 273 G76 6893 324 323 G176 6193 224 373 G276 5439 324 322 370 375 G280 5439 224 325 C0M 6872.5 248 274 G78 6853 83 324 G178 6153 93 374 G278 5453 93 322 375 G280 5411 224 325 G180 6111 224 375 G280 5411 224 327 C0M 6892.5 248 276 G882 6797 93 326 G180 6111 224 375 G280 5397 93 322 3	218	DUMMY	6452.5	-248	268	G66	6909	93	318	G166	6209	93	368	G266	5509	93
221 DUMMY 6632.5 248 271 G72 6867 224 321 G172 6167 224 371 G272 5467 224 222 DUMMY 6692.5 -248 272 G74 6853 93 322 G174 6153 93 372 G274 5453 93 223 VCOM 6812.5 -248 274 G768 6839 224 323 G176 6135 93 374 G276 5439 224 226 VCOM 6932.5 -248 276 G80 6811 224 325 G180 6111 224 375 G280 5411 224 228 VCOM 6932.5 -248 276 G88 6769 93 326 G182 6097 93 376 G282 5397 93 229 VCOM 7172.5 -248 279 G886 6769 93 328 G186 <td>219</td> <td>DUMMY</td> <td>6512.5</td> <td>-248</td> <td>269</td> <td>G68</td> <td>6895</td> <td>224</td> <td>319</td> <td>G168</td> <td>6195</td> <td>224</td> <td>369</td> <td>G268</td> <td>5495</td> <td>224</td>	219	DUMMY	6512.5	-248	269	G68	6895	224	319	G168	6195	224	369	G268	5495	224
222 DUMMY 6692.5 -248 272 G74 6853 93 322 G174 6153 93 372 G274 5453 93 223 VCOM 6752.5 -248 274 G78 6825 93 324 G178 6139 224 373 G276 5439 224 225 VCOM 6812.5 -248 274 G78 6825 93 324 G178 6125 93 374 G278 5429 924 225 VCOM 6892.5 -248 276 G82 6797 93 326 G182 6097 93 376 G282 5397 93 227 VCOM 7052.5 -248 278 G88 6769 93 328 G186 6069 93 376 G282 5397 93 229 VCOM 7052.5 -248 280 G96 6799 93 328 G186 6069	220	DUMMY	6572.5	-248	270	G70	6881	93	320	G170	6181	93	370	G270	5481	93
223 VCOM 6752.5 -248 273 G76 6839 224 323 G176 6139 224 373 G276 5439 224 224 VCOM 6812.5 -248 275 G80 6811 224 325 G80 6811 224 325 G80 6811 224 326 G180 6111 224 375 G280 531 324 G178 6125 93 376 G282 5397 93 227 VCOM 6992.5 -248 277 G84 6783 224 327 G184 6083 224 228 VCOM 7052.5 -248 279 G88 6755 224 329 G188 6069 93 378 G286 5369 93 229 VCOM 7112.5 -248 280 G90 6741 93 330 G190 6041 93 376 G288 5355 224	221	DUMMY	6632.5	-248	271	G72	6867	224	321	G172	6167	224	371	G272	5467	224
224 VCOM 6812.5 -248 274 G78 6825 93 324 G178 6125 93 374 G278 5425 93 225 VCOM 6872.5 -248 275 G80 6811 224 325 G180 6111 224 375 G280 5411 224 226 VCOM 6932.5 -248 277 G84 6783 224 327 G184 6087 93 376 G282 5397 93 228 VCOM 7052.5 -248 278 G86 6769 33 328 G186 6069 93 378 G286 5369 33 229 VCOM 717.5 -248 280 G90 6741 93 330 G190 6041 93 380 G290 5341 93 231 DUMMY 7393 224 282 G94 6713 93 332 G196	222	DUMMY	6692.5	-248	272	G74	6853	93	322	G174	6153	93	372	G274	5453	93
225 VCOM 6872.5 -248 275 G80 6811 224 325 G180 6111 224 375 G280 5411 224 226 VCOM 6932.5 -248 276 G82 6797 93 326 G182 6097 93 376 G282 5397 93 227 VCOM 6992.5 -248 278 G86 6769 33 328 G186 6069 93 378 G286 5397 93 229 VCOM 7172.5 -248 280 G80 6755 224 320 G186 6055 224 379 G288 5355 224 230 VCOM 7172.5 -248 280 G90 6741 93 330 G190 6041 93 380 G290 5341 93 231 DUMMY 7399 224 282 G94 6713 93 332 G194	223	VCOM	6752.5	-248	273	G76	6839	224	323	G176	6139	224	373	G276	5439	224
226 VCOM 6932.5 -248 276 G82 6797 93 326 G182 6097 93 376 G282 5397 93 227 VCOM 6992.5 -248 277 G84 6783 224 327 G184 6083 224 377 G284 5383 224 228 VCOM 7172.5 -248 279 G88 6755 224 329 G188 6055 224 379 G288 5355 224 230 VCOM 7172.5 -248 280 G90 6741 33 30 G190 6041 33 380 G290 5341 93 231 DUMMY 7292.5 -248 281 G92 6727 224 331 G192 6027 224 381 G292 5327 224 232 DUMMY 7399 224 283 G96 6699 224 333 G196	224	VCOM	6812.5	-248	274	G78	6825	93	324	G178	6125	93	374	G278	5425	93
227 VCOM 6992.5 -248 277 G84 6783 224 327 G184 6083 224 377 G284 5383 224 228 VCOM 7052.5 -248 278 G86 6769 93 328 G186 6069 93 378 G286 5369 93 229 VCOM 7172.5 -248 280 G90 6741 93 330 G190 6041 93 380 G290 5341 93 231 DUMMY 7232.5 -248 282 G94 6713 93 332 G190 6041 93 380 G290 5341 93 232 DUMMY 7399 224 283 G96 6669 224 333 G196 5999 224 383 G296 5299 224 234 DUMMY 7371 224 285 G100 6671 224 335 G200		VCOM		-248	275		6811	224	325	G180	6111	224	375	G280	5411	224
228 VCOM 7052.5 -248 278 G86 6769 93 328 G186 6069 93 378 G286 5369 93 229 VCOM 7112.5 -248 279 G88 6755 224 329 G188 6055 224 379 G288 5355 224 230 VCOM 7172.5 -248 280 G90 6741 93 330 G190 6041 93 380 G290 5341 93 231 DUMMY 7292.5 -248 281 G92 6727 224 331 G192 6027 224 381 G292 5327 224 232 DUMMY 7399 224 283 G96 6699 224 333 G196 5999 224 383 G296 5299 224 235 DUMMY 7371 224 285 G100 6671 224 335 G200																
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448 S668 4347 93 498 S618 3647 93 548 S568 2947 93 598 S518 2247 9				1										Î		224
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1449 IS667 - 14333 1224 H499 IS617 - 13633 1224 H549 IS567 - 12033 1224 H500 IS517 - 12233 12		S667	4333	224	499	S617	3633	224	549	S567	2933	224	599	S517	2233	224
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No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ
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604	S512	2163	93	654	S462	1463	93	704	S412	763	93	754	S362	63	93
605	S511	2149	224	655	S461	1449	224	705	S411	749	224	755	S361	49	224
606	S510	2135	93	656	S460	1435	93	706	S410	735	93	756	S360	-49	93
607	S509	2121	224	657	S459	1421	224	707	S409	721	224	757	S359	-63	224
608	S508	2107	93	658	S458	1407	93	708	S408	707	93	758	S358	-77	93
609	S507	2093	224	659	S457	1393	224	709	S407	693	224	759	S357	-91	224
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611	S505	2065	224	661	S455	1365	224	711	S405	665	224	761	S355	-119	224
612	S504	2051	93	662	S454	1351	93	712	S404	651	93	762	S354	-133	93
613	S503	2037	224	663	S453	1337	224	713	S403	637	224	763	S353	-147	224
614	S502	2023	93	664	S452	1323	93	714	S402	623	93	764	S352	-161	93
615	S501	2009	224	665	S451	1309	224	715	S401	609	224	765	S351	-175	224
616	S500	1995	93	666	S450	1295	93	716	S400	595	93	766	S350	-189	93
617	S499	1981	224	667	S449	1281	224	717	S399	581	224	767	S349	-203	224
618	S498	1967	93	668	S448	1267	93	718	S398	567	93	768	S348	-217	93
619	S497	1953	224	669	S447	1253	224	719	S397	553	224	769	S347	-231	224
620	S496	1939	93	670	S446	1239	93	720	S396	539	93	770	S346	-245	93
621	S495	1925	224	671	S445	1225	224	721	S395	525	224	771	S345	-259	224
622	S494	1911	93	672	S444	1211	93	722	S394	511	93	772	S344	-273	93
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624	S492	1883	93	674	S442	1183	93	724	S392	483	93	774	S342	-301	93
625	S491	1869	224	675	S441	1169	224	725	S391	469	224	775	S341	-315	224
626	S490	1855	93	676	S440	1155	93	726	S390	455	93	776	S340	-329	93
627	S489	1841	224	677	S439	1141	224	727	S389	441	224	777	S339	-343	224
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633	S483	1757	224	683	S433	1057	224	733	S383	357	224	783	S333	-427	224
634	S482	1743	93	684	S432	1043	93	734	S382	343	93	784	S332	-441	93
635	S481	1729	224	685	S431	1029	224	735	S381	329	224	785	S331	-455	224
636	S480	1715	93	686	S430	1015	93	736	S380	315	93	786	S330	-469	93
637	S479	1701	224	687	S429	1001	224	737	S379	301	224	787	S329	-483	224
638	S478	1687	93	688	S428	987	93	738	S378	287	93	788	S328	-497	93
639	S477	1673	224	689	S427	973	224	739	S377	273	224	789	S327	-511	224
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641	S475	1645	224	691	S425	945	224	741	S375	245	224	791	S325	-539	224
642	S474	1631	93	692	S424	931	93	742	S374	231	93	792	S324	-553	93
643	S473	1617	224	693	S423	917	224	743	S373	217	224	793	S323	-567	224
644	S472	1603	93	694	S422	903	93	744	S372	203	93	794	S322	-581	93
645	S471	1589	224	695	S421	889	224	745	S371	189	224	795	S321	-595	224
646	S470	1575	93	696	S420	875	93	746	S370	175	93	796	S320	-609	93
647	S469	1561	224	697	S419	861	224	747	S369	161	224	797	S319	-623	224
648	S468		93	698	S418	847	93	748	S368	147	93	798	S318	-637	93
649	S467	1533	224	699	S417	833	224	749	S367	133	224	799	S317	-651	224
650	S466	1519	93	700	S416	819	93	750	S366	119	93	800	S316	-665	93





Bot Sa15	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ
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803 \$313 707 224 853 \$263 -1407 224 903 \$213 -210 224 953 \$163 -2007 804 \$312 -721 93 854 \$562 -1442 93 905 \$211 213 224 955 \$261 -2235 48 162 -2821 806 \$300 -763 224 857 \$259 -1443 224 905 \$211 213 224 955 \$160 -28263 807 \$309 -763 224 859 \$2559 -1497 39 908 \$200 2216 2824 957 \$159 2268 809 \$307 -791 224 859 \$257 -1491 224 907 \$209 \$207 2191 224 915 \$158 289 956 \$156 309 916 \$200 \$201 \$260 \$261 \$241 \$241 \$241 \$24				93		S264		93	902	1	-2093	93		S164		93
805 \$311 .735 224 855 \$261 .1435 224 905 \$211 .2135 224 955 \$161 .2835 806 \$310 .749 93 856 \$269 .1463 224 907 \$209 .2163 224 957 \$299 .1263 224 907 \$309 \$307 .777 33 858 \$258 .1477 93 908 \$209 .2177 93 958 \$157 .2881 908 \$209 \$207 .2191 224 959 \$157 .2881 959 \$157 .2881 959 \$157 .2881 959 \$157 .2881 959 \$157 .2881 959 \$157 .2881 959 \$157 .2881 959 \$157 .2881 911 \$200 .2219 .224 961 \$155 .2919 .903 804 .2824 865 \$255 .15619 224 911 \$200 <td< td=""><td>803</td><td>S313</td><td>-707</td><td>224</td><td>853</td><td>S263</td><td>-1407</td><td>224</td><td>903</td><td>S213</td><td>-2107</td><td>224</td><td>953</td><td>S163</td><td>-2807</td><td>224</td></td<>	803	S313	-707	224	853	S263	-1407	224	903	S213	-2107	224	953	S163	-2807	224
806 \$310 -749 93 856 \$260 -1449 93 906 \$210 -2149 93 956 \$160 -2849 807 \$309 -63 224 857 \$259 +1473 90 \$200 -2163 224 97 \$159 \$2863 860 \$256 +1477 93 90 \$2500 -2177 93 \$95 \$155 -2877 93 90 \$2500 -2179 39 958 \$155 -2891 90 \$200 91 \$200 91 \$200 91 \$200 91 \$200 90 \$207 -2191 224 96 \$155 -2891 90 \$150 \$200 \$156 \$200 \$100	804	S312	-721	93	854	S262	-1421	93	904	S212	-2121	93	954	S162	-2821	93
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907 \$309 .763 .224 857 \$259 .1463 .224 907 \$209 .2163 .224 957 \$159 .2863 .2860 .9307 .791 224 859 \$257 .1491 .224 909 \$207 .2919 .224 958 \$550 .2919 .294 .908 .800 .205 .2919 .294 .908 .8508 .205 .2919 .294 .908 .8508 .205 .2919 .294 .908 .8508 .2919 .294 .908 .813 .203 .908 .861 .8525 .15169 .294 .911 .200 .2219 .224 .908 .8525 .15619 .294 .911 .200 .2223 .924 .961 .1515 .2919 .903 .966 .8252 .1561 .933 .916 .200 .2223 .939 .966 .85251 .1561 .931 .941 .802 .2249 .916 .8200	806	S310	-749	93	856	S260	-1449	93	906	S210	-2149	93	956	S160	-2849	93
808 \$308 -777 93 858 \$258 1477 93 908 \$2007 -791 224 859 \$257 1491 224 909 \$207 -2191 224 909 \$11 \$306 \$206 -805 93 860 \$256 \$1509 93 910 \$205 \$205 93 908 \$207 -2191 224 961 \$155 -2905 93 908 \$207 -2191 224 960 \$156 -2905 93 910 \$205 -2219 224 961 \$155 -2919 93 861 \$255 1561 93 911 \$205 -2219 224 962 \$154 -2933 93 962 \$154 -2933 93 962 \$154 -2931 941 \$202 -2261 93 962 \$154 -2933 93 962 \$154 -2933 93 962 \$154 -2929 961 \$152 <t< td=""><td>807</td><td>S309</td><td>-763</td><td>224</td><td>857</td><td>S259</td><td>-1463</td><td>224</td><td>907</td><td></td><td>-2163</td><td>224</td><td>957</td><td>S159</td><td>-2863</td><td>224</td></t<>	807	S309	-763	224	857	S259	-1463	224	907		-2163	224	957	S159	-2863	224
810 \$306 -805 93 860 \$256 -1505 93 910 \$206 2219 224 961 \$255 -1519 224 961 \$255 -1519 224 961 \$255 -2919 224 961 \$155 2219 224 961 \$155 2291 224 961 \$155 2219 224 963 \$155 2219 224 963 \$155 221 363 \$255 -1561 93 914 \$202 -2261 93 964 \$152 -2961 804 \$152 -1561 93 914 \$202 -2261 93 966 \$150 -2993 964 \$152 -2967 91 224 865 \$250 -1589 93 916 \$200 -2289 93 966 \$150 -2969 91 91 291 2245 224 917 \$149 -3003 294 916 \$200 \$2289 93 <td< td=""><td>808</td><td>S308</td><td>-777</td><td>93</td><td>858</td><td>S258</td><td>-1477</td><td>93</td><td>908</td><td>S208</td><td>-2177</td><td>93</td><td>958</td><td>S158</td><td>-2877</td><td>93</td></td<>	808	S308	-777	93	858	S258	-1477	93	908	S208	-2177	93	958	S158	-2877	93
811 \$305 819 \$24 861 \$255 1519 \$24 911 \$204 \$219 \$24 961 \$155 \$2919 812 \$304 833 93 947 \$24 863 \$253 1547 \$224 913 \$203 \$2247 \$244 963 \$153 \$2937 \$246 \$66 \$251 1575 \$224 \$158 \$203 \$247 \$224 \$66 \$255 \$158 \$201 \$2275 \$224 \$66 \$150 \$2989 \$93 \$66 \$150 \$2989 \$93 \$66 \$150 \$2989 \$93 \$66 \$150 \$2989 \$93 \$66 \$150 \$2989 \$93 \$66 \$150 \$2989 \$93 \$66 \$151 \$2975 \$149 \$93 \$163 \$200 \$2289 \$93 \$66 \$150 \$2989 \$93 \$160 \$93 \$160 \$149 \$93 \$870 \$244 \$163 \$925<	809	S307	-791	224	859	S257	-1491	224	909	S207	-2191	224	959	S157	-2891	224
811 \$305 819 \$24 861 \$255 -1519 \$24 911 \$205 -2219 \$24 961 \$155 -2919 812 \$304 -833 93 947 \$224 863 \$253 -1547 \$24 863 \$253 -1547 \$24 863 \$253 -1576 \$24 863 \$253 -1576 \$24 865 \$251 -1576 \$24 865 \$251 -1576 \$24 \$15 \$2001 -2275 \$224 966 \$150 -2989 816 \$300 -889 93 866 \$250 -1589 93 916 \$150 -2289 93 966 \$150 -2989 917 \$199 \$200 -2289 93 966 \$150 -2989 936 \$153 -2989 93 966 \$151 -2975 \$161 -2975 \$161 -2975 \$162 \$1798 \$24 \$1799 \$230 \$24 </td <td>810</td> <td>S306</td> <td>-805</td> <td>93</td> <td>860</td> <td>S256</td> <td>-1505</td> <td>93</td> <td>910</td> <td>S206</td> <td>-2205</td> <td>93</td> <td>960</td> <td>S156</td> <td>-2905</td> <td>93</td>	810	S306	-805	93	860	S256	-1505	93	910	S206	-2205	93	960	S156	-2905	93
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814 S302 -861 93 864 S252 -1561 93 914 S202 -2261 93 964 S152 -2961 816 S300 -889 93 866 S250 -1589 93 916 S200 -2289 93 966 S150 -2989 817 S299 -903 224 867 S249 -1603 224 917 S199 -2303 224 967 S149 -3003 818 S298 -917 93 868 S248 -1617 93 918 S197 -2331 224 967 S149 -3003 820 S296 -945 39 870 S246 -1645 93 970 S146 -3045 821 S295 -959 224 871 S245 -1669 224 921 S195 -2359 224 971 S145 -3069 822 S292 -1001 </td <td>812</td> <td>S304</td> <td>-833</td> <td>93</td> <td>862</td> <td>S254</td> <td>-1533</td> <td>93</td> <td>912</td> <td>S204</td> <td>-2233</td> <td>93</td> <td>962</td> <td>S154</td> <td>-2933</td> <td>93</td>	812	S304	-833	93	862	S254	-1533	93	912	S204	-2233	93	962	S154	-2933	93
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816 S300 -889 93 866 S250 -1589 93 916 S200 -2289 93 966 S150 -2989 817 S299 -903 224 867 S249 -1603 224 917 S199 -2303 224 967 5149 -3003 818 S298 -917 33 868 S248 -1617 93 918 S198 -2317 23 968 S148 -3017 820 S296 -945 93 870 S246 -1645 93 920 S196 -2345 93 970 S146 -3045 821 S293 -997 224 873 S243 -1667 224 921 S196 -2345 93 972 S144 -3073 822 S293 -987 224 873 S243 -1667 224 923 S193 -2367 224 971 S144 -3073	814	S302	-861	93	864	S252	-1561	93	914		-2261	93	964	S152	-2961	93
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817 S299 -903 224 867 S249 -1603 224 917 S199 -2303 224 967 S149 -3003 818 S298 -917 93 868 S248 -1617 93 918 S198 -2317 93 968 S147 -3031 819 S296 -945 93 870 S246 -1645 93 919 S197 -2345 93 970 S146 -3045 821 S295 -959 224 871 S245 -1659 224 921 S195 -2359 224 971 S145 -3005 93 972 S144 -3073 93 972 S144 -3073 93 972 S144 -3073 93 922 S199 -2373 93 972 S144 -3073 93 922 S199 -2373 93 972 S144 -3073 93 922 S199 -24				93			-1589	93	916		-2289	1 1	966	S150		93
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No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ
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1004	S112	-3521	93	1054	S62	-4221	93	1104	S12	-4921	93	1154	G243	-5663	93
1005	S111	-3535	224	1055	S61	-4235	224	1105	S11	-4935	224	1155	G241	-5677	224
1006	S110	-3549	93	1056	S60	-4249	93	1106	S10	-4949	93	1156	G239	-5691	93
1007	S109	-3563	224	1057	S59	-4263	224	1107	S9	-4963	224	1157	G237	-5705	224
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1022	S94	-3773	93	1072	S44	-4473	93	1122	G307	-5215	93	1172	G207	-5915	93
1023	S93	-3787	224	1073	S43	-4487	224	1123	G305	-5229	224	1173	G205	-5929	224
1024	S92	-3801	93	1074	S42	-4501	93	1124	G303	-5243	93	1174	G203	-5943	93
1025	S91	-3815	224	1075	S41	-4515	224	1125	G301	-5257	224	1175	G201	-5957	224
1026	S90	-3829	93	1076	S40	-4529	93	1126	G299	-5271	93	1176	G199	-5971	93
1027	S89	-3843	224	1077	S39	-4543	224	1127	G297	-5285	224	1177	G197	-5985	224
1028	S88	-3857	93	1078	S38	-4557	93	1128	G295	-5299	93	1178	G195	-5999	93
1029	S87	-3871	224	1079	S37	-4571	224	1129	G293	-5313	224	1179	G193	-6013	224
1030	S86	-3885	93	1080	S36	-4585	93	1130	G291	-5327	93	1180	G191	-6027	93
1031	S85	-3899	224	1081	S35	-4599	224	1131	G289	-5341	224	1181	G189	-6041	224
1032	S84	-3913	93	1082	S34	-4613	93	1132	G287	-5355	93	1182	G187	-6055	93
1033	S83	-3927	224	1083	S33	-4627	224	1133	G285	-5369	224	1183	G185	-6069	224
1034	S82	-3941	93	1084	S32	-4641	93	1134	G283	-5383	93	1184	G183	-6083	93
1035	S81	-3955	224	1085	S31	-4655	224	1135	G281	-5397	224	1185	G181	-6097	224
1036	S80	-3969	93	1086	S30	-4669	93	1136	G279	-5411	93	1186	G179	-6111	93
1037	S79	-3983	224	1087	S29	-4683	224	1137	G277	-5425	224	1187	G177	-6125	224
1038	S78	-3997	93	1088	S28	-4697	93	1138	G275	-5439	93	1188	G175	-6139	93
1039	S77	-4011	224	1089	S27	-4711	224	1139	G273	-5453	224	1189	G173	-6153	224
1040	S76		93	1090	S26	-4725	93	1140	G271	-5467	93	1190	G171	-6167	93
1041	S75	-4039	224	1091	S25	-4739	224	1141	G269	-5481	224	1191	G169	-6181	224
1042	S74	-4053	93	1092	S24	-4753	93	1142	G267	-5495	93	1192	G167	-6195	93
	S73	-4067	224	1093	S23	-4767	224	1143	G265	-5509	224	1193	G165	-6209	224
	S72	-4081	93	1094	S22	-4781	93	1144	G263	-5523	93	1194	G163	-6223	93
	S71	-4095	224	1095	S21	-4795	224	1145	G261	-5537	224	1195	G161	-6237	224
	S70	-4109	93	1096	S20	-4809	93	1146	G259	-5551	93	1196	G159	-6251	93
	S69		224	1097	S19	-4823	224	1147	G257	-5565	224	1197	G157	-6265	224
	S68	-4137	93	1098	S18	-4837	93	1148	G255	-5579	93	1198	G155	-6279	93
	S67		224	1099	S17	-4851	224	1149	G253	-5593	224	1199	G153	-6293	224
1050			93		S16	-4865	93	1150	G251	-5607	93	1200	G151	-6307	93



No.	Pad name	Χ	Υ	_
1201	G149	-6321	224	12
1202	G147	-6335	93	12
1203	G145	-6349	224	12
1204	G143	-6363	93	12
1205	G141	-6377	224	12
1206	G139	-6391	93	12
1207	G137	-6405	224	12
1208	G135	-6419	93	12
1209	G133	-6433	224	12
1210	G131	-6447	93	12
1211	G129	-6461	224	12
1212	G127	-6475	93	12
1213	G125	-6489	224	12
1214	G123	-6503	93	12
1215	G121	-6517	224	12
1216	G119	-6531	93	12
1217	G117	-6545	224	12
1218	G115	-6559	93	12
1219	G113	-6573	224	12
1220	G111	-6587	93	12
1221	G109	-6601	224	12
1222	G107	-6615	93	12
1223	G105	-6629	224	12
1224	G103	-6643	93	12
1225	G101	-6657	224	12
1226	G99	-6671	93	12
1227	G97	-6685	224	12
1228	G95	-6699	93	12
1229	G93	-6713	224	
1230	G91	-6727	93	
1231	G89	-6741	224	
1232	G87	-6755	93	
1233	G85	-6769	224	
1234	G83	-6783	93	
1235	G81	-6797	224	
1236	G79	-6811	93	
1237	G77	-6825	224	
1238	G75	-6839	93	
1239	G73	-6853	224	
1240	G71	-6867	93	
1241	G69	-6881	224	
1242	G67	-6895	93	
1243	G65	-6909	224	
1244	G63	-6923	93	
1245	G61	-6937	224	
1246	G59	-6951	93	
1247	G57	-6965	224	
1248	G55	-6979	93	
1249	G53	-6993	224	
4050	1054	1 7007	100	i

1250 G51

-7007 93

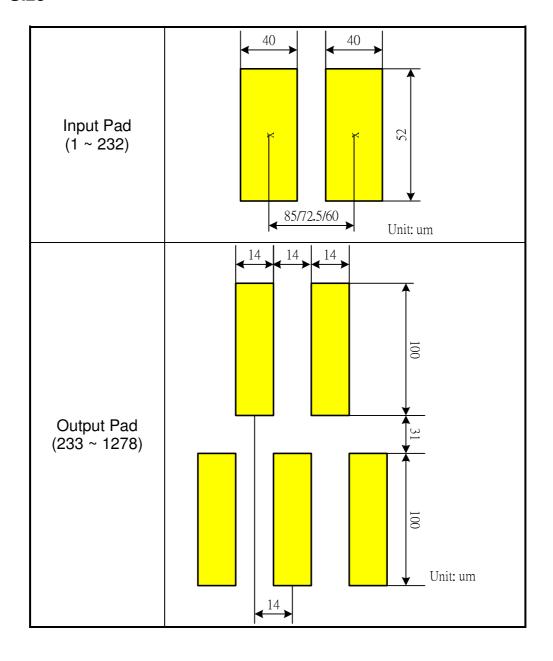
	No.	Pad name	Х	Υ
1	1251	G49	-7021	224
	1252	G47	-7035	93
1	1253	G45	-7049	224
	1254	G43	-7063	93
1	1255	G41	-7077	224
	1256	G39	-7091	93
1	1257	G37	-7105	224
	1258	G35	-7119	93
1	1259	G33	-7133	224
	1260	G31	-7147	93
1	1261	G29	-7161	224
	1262	G27	-7175	93
1	1263	G25	-7189	224
	1264	G23	-7203	93
1	1265	G21	-7217	224
	1266	G19	-7231	93
1	1267	G17	-7245	224
	1268	G15	-7259	93
1	1269	G13	-7273	224
	1270	G11	-7287	93
1	1271	G9	-7301	224
	1272	G7	-7315	93
1	1273	G5	-7329	224
	1274	G3	-7343	93
1	1275	G1	-7357	224
	1276	DUMMY	-7371	93
1	1277	DUMMY	-7385	224
	1278	DUMMY	-7399	93
1				

Alignment mark	X	Υ
Left COG Align	-7480	225
Right COG Align	7480	225





BUMP Size







6. Block Function Description

MCU System Interface

ILI9341 provides four kinds of MCU system interface with 8080- I /8080- II series parallel interface and 3-/4-line serial interface. The selection of the given interfaces are done by external IM [3:0] pins and shown as below:

IM3	IM2	IM1	IMO	MCU-Interface Mode		Pins in use	
IIVIO	IIVIZ	IIVII	IIVIO	MCO-interface Mode	Register/Content	GRAM	
0	0	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX	
0	0	0	1	8080 MCU 16-bit bus interface I	D[7:0]	D[15:0],WRX,RDX,CSX,D/CX	
0	0	1	0	8080 MCU 9-bit bus interface I	D[7:0]	D[8:0],WRX,RDX,CSX,D/CX	
0	0	1	1	8080 MCU 18-bit bus interface I	D[7:0]	D[17:0],WRX,RDX,CSX,D/CX	
0	1	0	1	3-wire 9-bit data serial interface I		SCL,SDA,CSX	
0	1	1	0	4-wire 8-bit data serial interface I		SCL,SDA,D/CX,CSX	
1	0	0	0	8080 MCU 16-bit bus interface II	D[8:1]	D[17:10],D[8:1],WRX,RDX,CSX,D/CX	
1	0	0	1	8080 MCU 8-bit bus interface II	D[17:10]	D[17:10],WRX,RDX,CSX,D/CX	
1	0	1	0	8080 MCU 18-bit bus interface II	D[8:1]	D[17:0],WRX,RDX,CSX,D/CX	
1	0	1	1	8080 MCU 9-bit bus interface II	D[17:10]	D[17:9],WRX,RDX,CSX,D/CX	
1	1	0	1	3-wire 9-bit data serial interface II		SCL,SDI,SDO, CSX	
1	1	1	0	4-wire 8-bit data serial interface II	II SCL,SDI,D/CX,SDO, CSX		

In 8080- I /8080- II series parallel interface, the registers are accessed by the D[17:0] data pins.

	8080- I	Series			8080- п	Series		Operation
CSX	D/CX	RDX	WRX	CSX	D/CX	RDX	WRX	
"L"	"L"	"H"		"L"	"L"	"H"		Write command
"L"	"H"		"H"	"L"	"H"		"H"	Read parameter
"L"	"H"	"H"		"L"	"H"	"H"		Write parameter

Parallel RGB Interface

ILI9341 also supports the RGB interface for displaying a moving picture. When the RGB interface is selected, display operation is synchronized with externally signals, VSYNC, HSYNC, and DOTCLK and input display data is written in synchronization with these signals according to the polarity of enable signal (DE).

Graphic RAM (GRAM)

GRAM is a graphic RAM to store display data. GRAM size is 172,800 bytes with 18 bits per pixel for a maximum 240(RGB) x320 dot graphic display.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the gamma correction register. ILI9341 can display maximum 262,144 colors.





Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels as GVDD, VGH, VGL and VCOM for driving TFT LCD panel.

Timing controller

The timing controller generates all the timing signals for display and GRAM access.

Oscillator

ILI9341 incorporates RC oscillator circuit and output a stable output frequency for operation.

Panel Driver Circuit

Liquid crystal display driver circuit consists of 720-output source driver (S1~S720), 320-output gate driver (G1~G320), and VCOM signal.





7. Function Description

7.1. MCU interfaces

ILI9341 provides the 8-/9-/16-/18-bit parallel system interface for 8080- I /8080- II series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [3:0] and the bit formal per pixel color order is selected by DBI [2:0] bits of 3Ah register.

7.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

IM3	IM2	18.44	IMO	MOLL Interface Made		Pins in use	
IIVI3	IIVIZ	IM1	IM0	MCU-Interface Mode	Register/Content	GRAM	
0	0	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX	
0	0	0	1	8080 MCU 16-bit bus interface I	D[7:0]	D[15:0] ,WRX,RDX,CSX,D/CX	
0	0	1	0	8080 MCU 9-bit bus interface I	D[7:0]	D[8:0] ,WRX,RDX,CSX,D/CX	
0	0	1	1	8080 MCU 18-bit bus interface I	D[7:0]	D[17:0] ,WRX,RDX,CSX,D/CX	
0	1	0	1	3-wire 9-bit data serial interface I		SCL,SDA,CSX	
0	1	1	0	4-wire 8-bit data serial interface I	SCL,SDA,D/CX,CSX		
1	0	0	0	8080 MCU 16-bit bus interface II	D[8:1]	D[17:10],D[8:1],WRX,RDX,CSX,D/CX	
1	0	0	1	8080 MCU 8-bit bus interface II	D[17:10]	D[17:10],WRX,RDX,CSX,D/CX	
1	0	1	0	8080 MCU 18-bit bus interface II	D[8:1]	D[17:0],WRX,RDX,CSX,D/CX	
1	0	1	1	8080 MCU 9-bit bus interface II	D[17:10]	D[17:9],WRX,RDX,CSX,D/CX	
1	1	0	1	3-wire 9-bit data serial interface II		SCL,SDI,SDO, CSX	
1	1	1	0	4-wire 8-bit data serial interface II	SCL,SDI,D/CX,SDO, CSX		





7.1.2. 8080- I Series Parallel Interface

ILI9341 can be accessed via 8-/9-/16-/18-bit MCU 8080- I series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9341 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

ILI9341 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

The 8080- I series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080- I Interface selection is done when IM3 pin is low state (VSS level). Interface bus width can be selected by IM [2:0] bits.

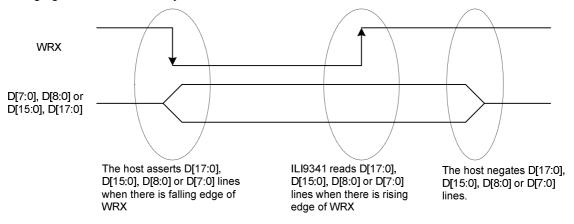
The selection of 8080- I series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	WRX	RDX	D/CX	Function
					"L"	ſ	"H"	"L"	Write command code.
			•	0000 MOLLO hit have betaufage. T	"L"	"H"	ſ	"H"	Read internal status.
0	0	0	0	8080 MCU 8-bit bus interface I	"L"	ſ	"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
					"L"		"H"	"L"	Write command code.
		0	4	0000 MOLL to bit bus interfered.	"L"	"H"	$ \leftarrow $	"H"	Read internal status.
0	0	0	1	8080 MCU 16-bit bus interface I	"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
					"L"	ſ	"H"	"L"	Write command code.
		_	•	0000 MOLLO littleve listerfees. T	"L"	"H"	Ţ	"H"	Read internal status.
0	0	1	0	8080 MCU 9-bit bus interface I	"L"	ſ	"H"	"H"	Write parameter or display data.
					"L"	"H"	$ \leftarrow $	"H"	Reads parameter or display data.
					"L"		"H"	"L"	Write command code.
		4	4	2000 MOLL 10 hit hug interfers. I	"L"	"H"		"H"	Read internal status.
0	0	1	1	8080 MCU 18-bit bus interface I	"L"	ſ	"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.

7.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080- I MCU interface.



Note: WRX is an unsynchronized signal (It can be stopped)



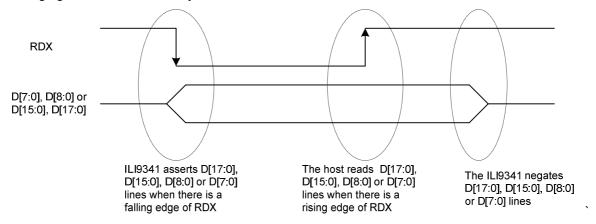




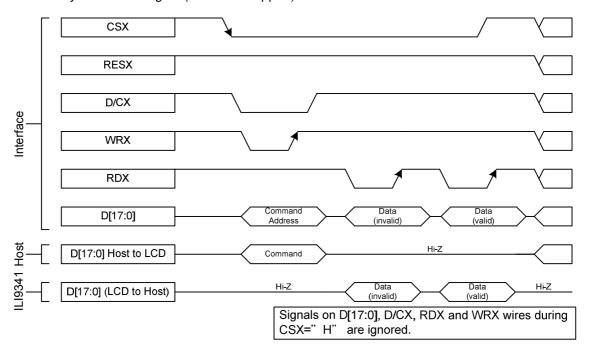
7.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080- I MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.





7.1.5. 8080- II Series Parallel Interface

ILI9341 can be accessed via 8-/9-/16-/18-bit MCU 8080- series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9341 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

ILI9341 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

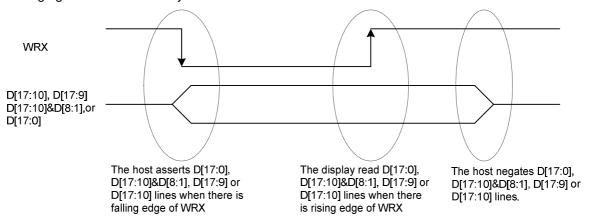
The 8080- II series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080- II Interface selection is done when IM3 pin is high state (VDDI level). Interface bus width can be selected by IM [2:0] bits.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	WRX	RDX	D/CX	Function
1	0	0	0	8080 MCU 16-bit bus interface II	"L"	ſ	"H"	"L"	Write command code.
					"L"	"H"	<u> </u>	"H"	Read internal status.
					"L"	\int	"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
	0	0	1	8080 MCU 8-bit bus interface II	"L"	<u></u>	"H"	"L"	Write command code.
1					"L"	"H"		"H"	Read internal status.
					"L"	$ \leftarrow $	"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
	0	1	0	8080 MCU 18-bit bus interface II	"L"		"H"	"L"	Write command code.
1					"L"	"H"	\vdash	"H"	Read internal status.
					"L"	$ \leftarrow $	"H"	"H"	Write parameter or display data.
					"L"	"H"	$ \leftarrow $	"H"	Reads parameter or display data.
1	0	1	1	8080 MCU 9-bit bus interface II	"L"		"H"	"L"	Write command code.
					"L"	"H"		"H"	Read internal status.
					"L"	ſ	"H"	"H"	Write parameter or display data.
					"L"	"H"	ſ	"H"	Reads parameter or display data.

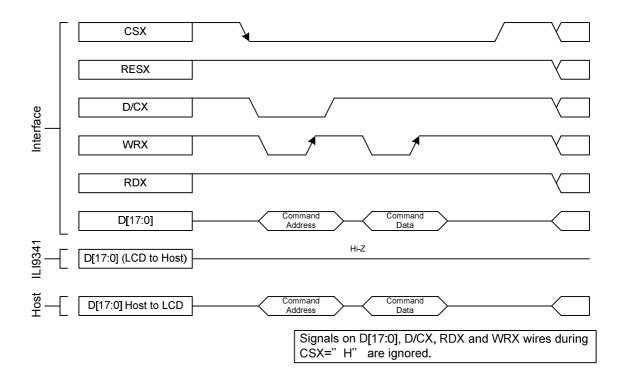


7.1.6. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.



Note: WRX is an unsynchronized signal (It can be stopped)



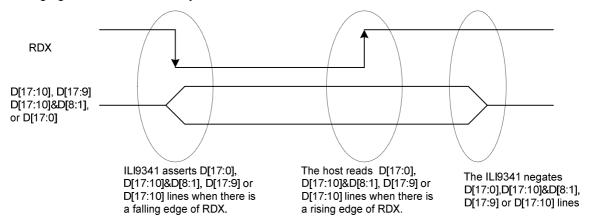




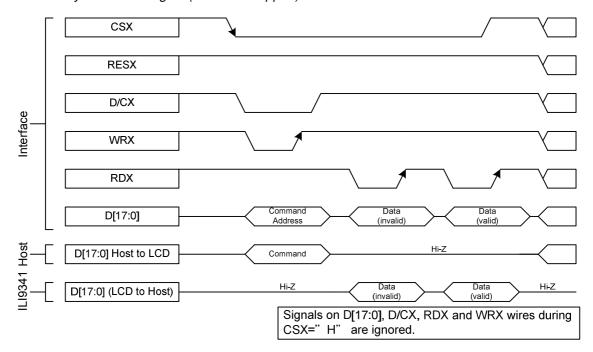
7.1.7. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080- II MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.





7.1.8. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

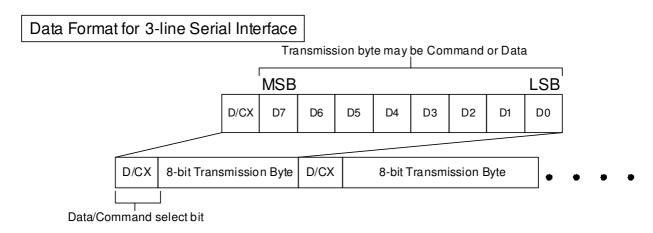
IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
0	1	0	1	3-line serial interface	"L"	-		Read/Write command, parameter or display data.
0	1	1	0	4-line serial interface	"L"	'H/L"	ſ	Read/Write command, parameter or display data.
1	1	0	1	3-line serial interface	"L"	-	ſ	Read/Write command, parameter or display data.
1	1	1	0	4-line serial interface	"L"	'H/L"	ſ	Read/Write command, parameter or display data.

ILI9341 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and ILI9341. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO) for data transmission. The data bus (D [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

7.1.9. Write Cycle Sequence

The write mode of the interface means that host writes commands or data to ILI9341. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is "low", the transmission byte is interpreted as a command byte. If the D/CX bit is "high", the transmission byte is stored as the display data RAM (Memory write command), or command register as parameter.

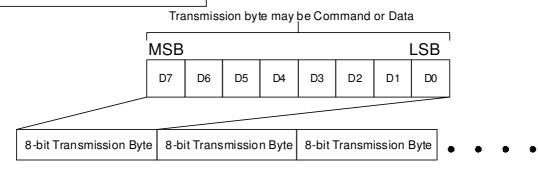
Any instruction can be sent in any order to ILI9341 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.







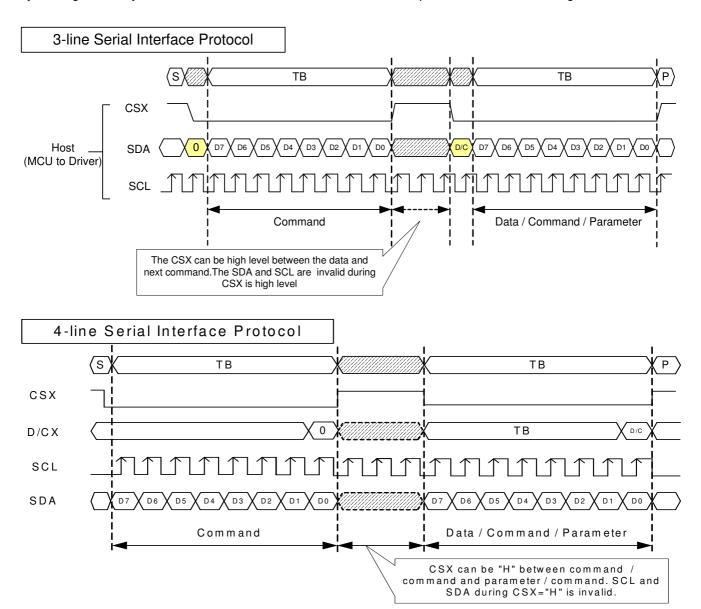
Data Format for 4-line Serial Interface







Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by ILI9341 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.



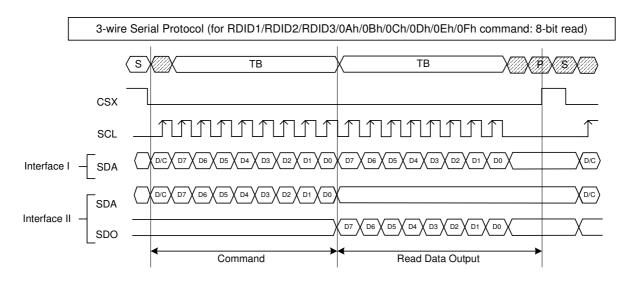


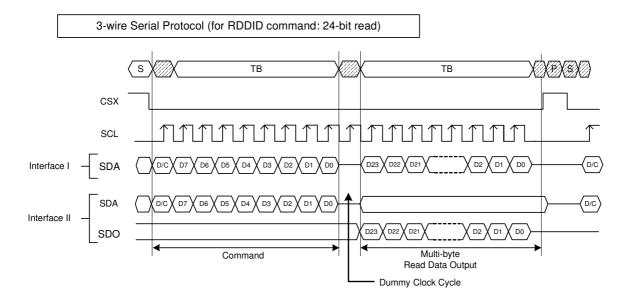


7.1.10. Read Cycle Sequence

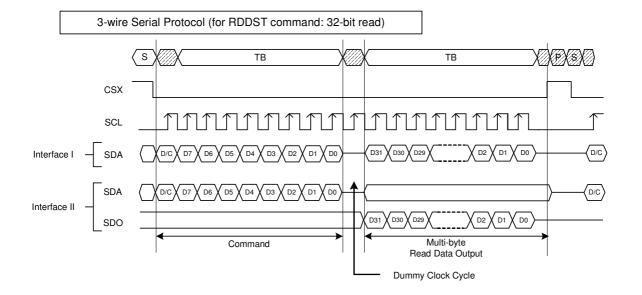
The read mode of interface means that the host reads register's parameter or display data from ILI9341. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. ILI9341 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

3-wire Serial Interface Protocol



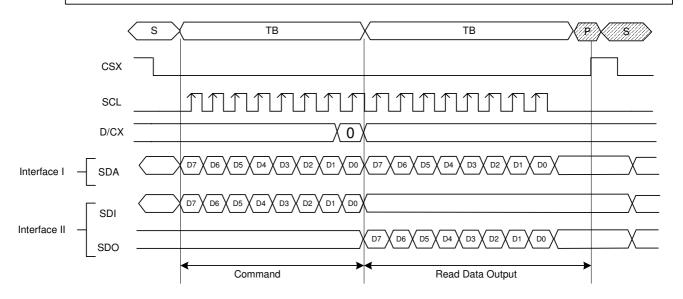




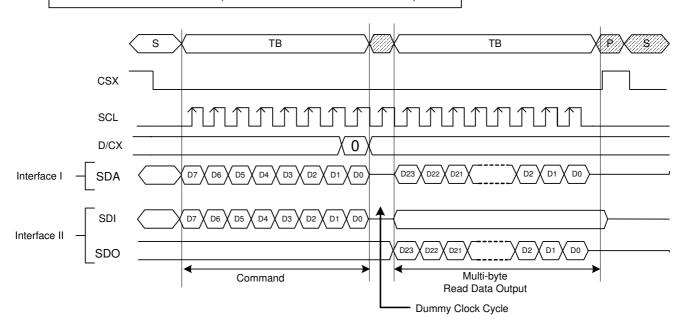


4-wire Serial Interface Protocol

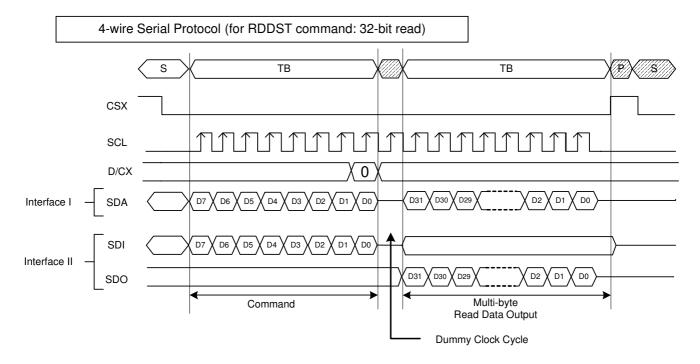
4-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



4-wire Serial Protocol (for RDDID command: 24-bit read)



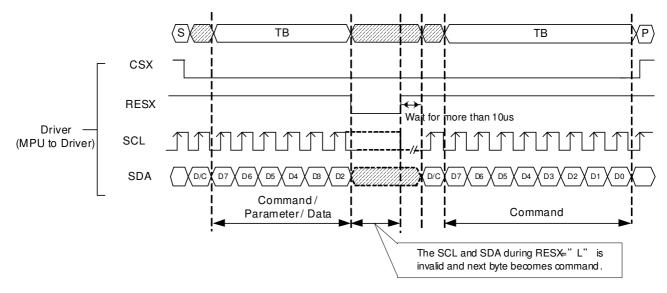




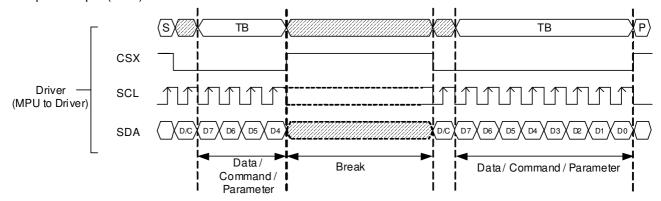


7.1.11. Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.

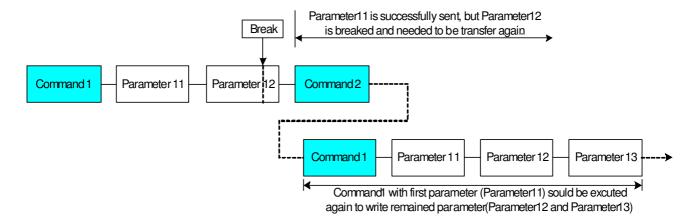


If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.

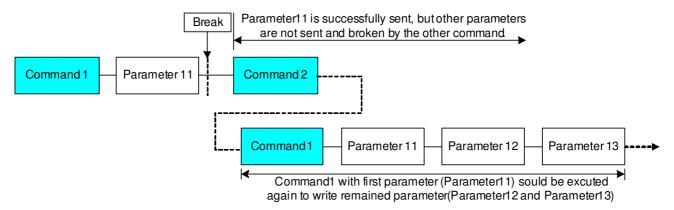


If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.





If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.





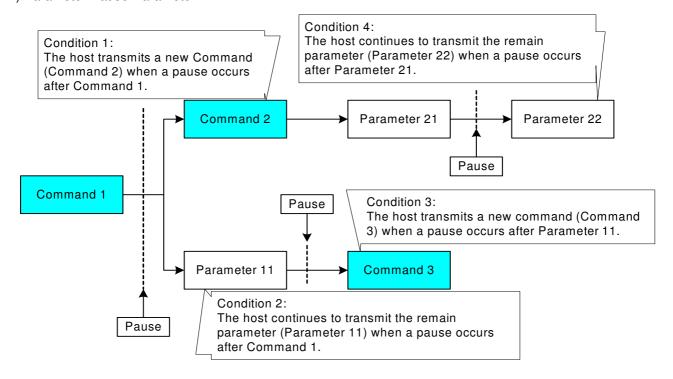


7.1.12. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then ILI9341 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.

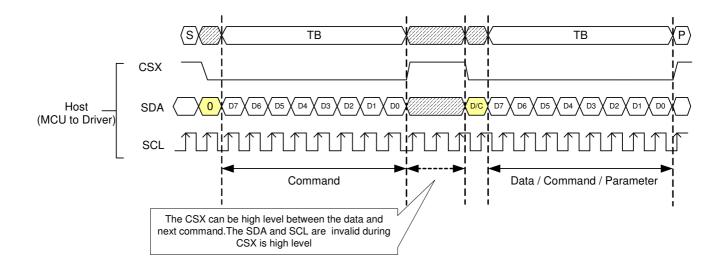
This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

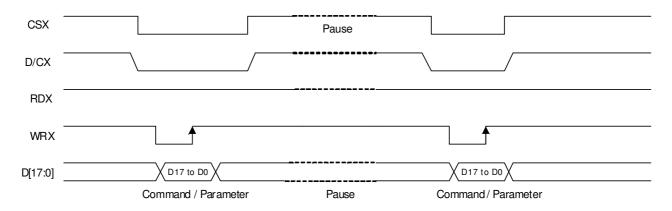




7.1.13. Serial Interface Pause (3_wire)



7.1.14. Parallel Interface Pause





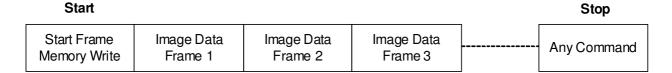


7.1.15. Data Transfer Mode

ILI9341 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

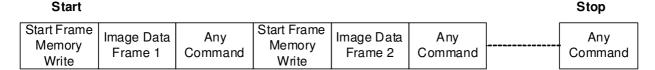
7.1.16. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



7.1.17. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.





7.2. RGB Interface

7.2.1. RGB Interface Selection

ILI9341 has two kinds of RGB interface and these interfaces can be selected by RCM [1:0] bits. When RCM [1:0] bits are set to "10", the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM [1:0] bits are set to "11", the SYNC mode is selected which utilizes which utilizes VSYNC, HSYNC, DOTCLK, D [17:0] pins. Using RGB interface must selection serial interface.

ILI9341 supports several pixel formats that can be selected by DPI [2:0] bits of "Pixel Format Set (3Ah)" and RIM bit of RF6h command. The selection of a given interfaces is done by setting RCM [1:0] and DPI [2:0] as show in the following table.

RCM	I[1:0]	RIM	D	PI[2:	:0]	RGB Interface Mode	RGB Mode	Used Pins
1	0	0	1	1	0	18-bit RGB interface (262K colors)		VSYNC, HSYNC, DE, DOTCLK,D[17:0]
1	0	0	1	0	1	16-bit RGB interface (65K colors)	DE Mode	VSYNC, HSYNC, DE, DOTCLK, D[17:13] & D[11:1]
1	0	1	1	1	0	6-bit RGB interface (262K colors)	Valid data is determined by the DE signal	VSYNC, HSYNC, DE, DOTCLK, D[5:0]
1	0	1	1	0	1	6-bit RGB interface (65K colors)		VSYNC, HSYNC, DE, DOTCLK, D[5:0]
1	1	0	1	1	0	18-bit RGB interface (262K colors)		VSYNC, HSYNC, DOTCLK, D[17:0]
1	1	0	1	0	1	16-bit RGB interface (65K colors)	SYNC Mode In SYNC mode, DE signal is ignored;	VSYNC, HSYNC, DOTCLK, D[17:13] & D[11:1]
1	1	1	1	1	0	6-bit RGB interface (262K colors)	blanking porch is determined by B5h command.	VSYNC, HSYNC, DOTCLK, D[5:0]
1	1	1	1	0	1	6-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, D[5:0]

The LSB data of red/blue color depends on the EPF[1:0] setting.

Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, DE and D [17:0] states when there is a rising edge of the DOTCLK. Vertical synchronization (VSYNC) is used to tell when

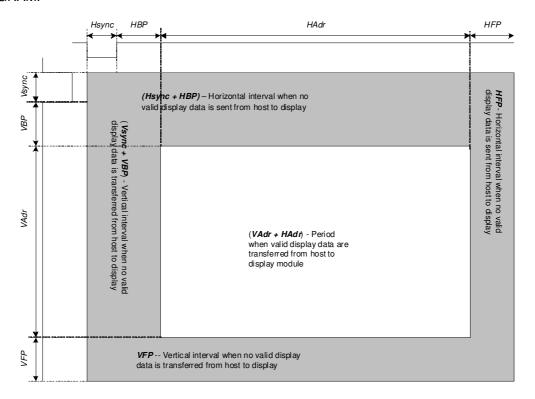




there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= '0' (low) and there is a rising edge of DOTCLK). D [17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data in inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.



Parameters	Symbols	Condition	Min.	Тур.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP		3	4	-	Line

Typical values are setting example when used with panel resolution 240 x 320 (QVGA), clock frequency 6.35MHz and frame





frequency about 70Hz.

Notes:

- 1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
- 2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
- 3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

Also make sure that

(Number of PCLK per 1 line) ≥ (Number of RTN clock) x Division ratio (DIV) x PCDIV

Setting Example for Display Control Clock in RGB Interface Operation

Register Display operation using DPI is in synchronization with internal clock PCLKD which is generated by dividing DOTCLK.

PCDIV [5:0]: Number of DOTCLK during internal clock PCLKD's high / low period. In units of 1 clock.

PCDIV specifying DOTCLK's division ratio, are determined so that difference between PCLKD's frequency and internal oscillation clock 615KHz is the smallest. Set PCDIV follow the restriction (Number of PCLK in 1H) ≥ (Number of RTN clock) x Division ratio (DIV) x PCDIV.

Setting Example: To set frame frequency to 70Hz:

Internal Clock

```
Internal Oscillation Clock: 615KHz
DIV[1:0] = 2'b0 (x 1/1)
RTN[4:0] = 5'h1b (27 clocks)
FP = 7'h2 (2 lines), BP = 7'h2 (2 lines), NL = 6'h27 (320 lines)
Frame Rate \rightarrow 70.30Hz
```

DOTCLK

```
HSYNC = 10 CLK

HBP = 20 CLK

HFP=10 CLK

70Hz x (2 + 320 + 2) lines x (10 + 20 + 240 + 10) clocks = 6.35MHz

DOTCLK frequency = 6.35MHz

6.35 MHz / 615KHz = 10.32 \Box Set PCDIV so that PCLK is divided by 10.

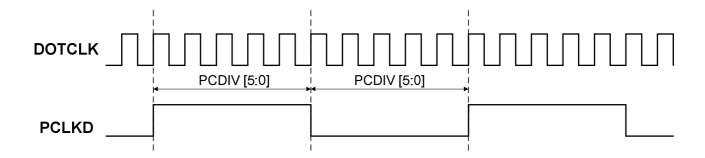
external fosc = 6.35 MHz / 10 = 635KHz

PCDIV = [6.35MHz / 10 = 635KHz

PCDIV = [6.35MHz / 10 = 635KHz

PCDIV = [6.35MHz / 10 = 635KHz
```

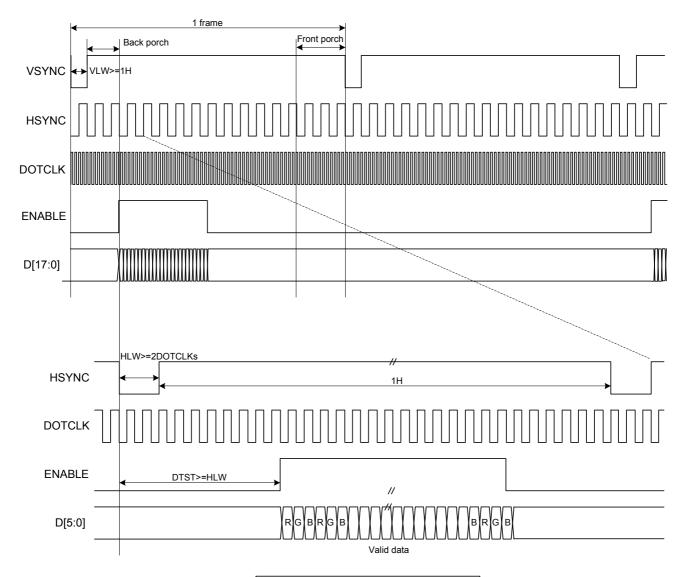






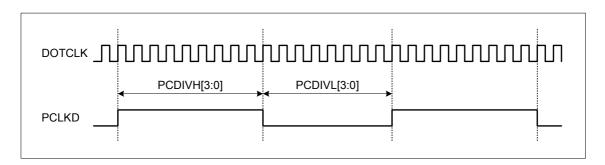
7.2.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as below.



VLW: VSYNC Low Width HLW: HSYNC Low Width

DTST: Data Transfer Startup Time



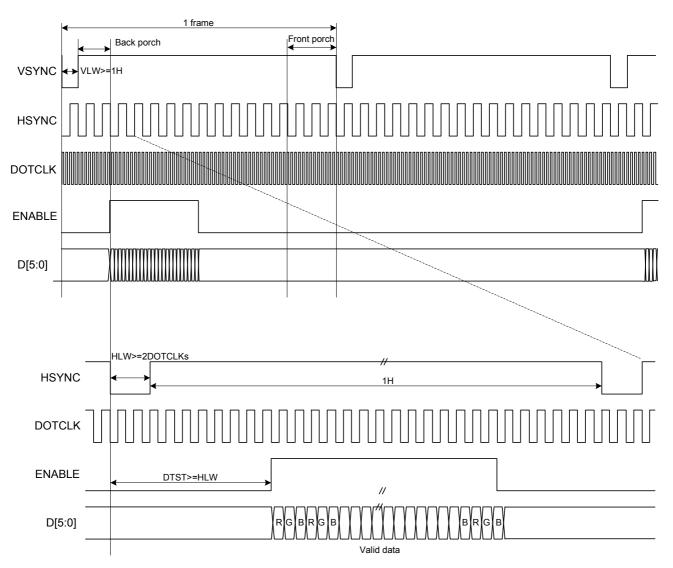
Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.



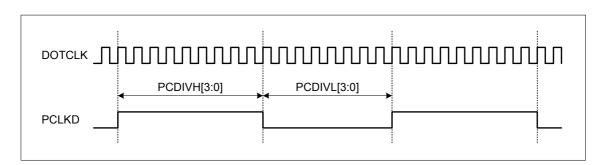


The timing chart of 6-bit RGB interface mode is shown as below:



VLW: VSYNC Low Width HLW: HSYNC Low Width

DTST: Data Transfer Startup Time



Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.



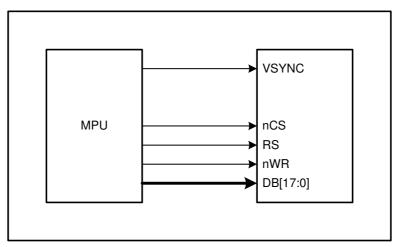


Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.

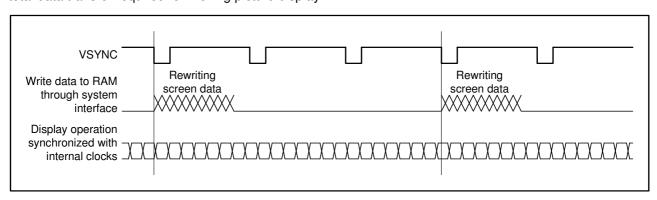


7.3. VSYNC Interface

ILI9341 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the 8080- I /8080- I system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = "10" and RM = "0".

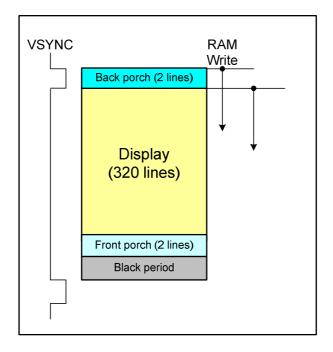


In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.









The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (VFP) + BackPorch (VBP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.

$$\textit{Minimum RAM write speed [Hz]} > \frac{240 \times \textit{DisplayLines(NL)}}{[\textit{BackPorch(VBP)} + \textit{DisplayLines(NL)} - \textit{margins]} \times \textit{Clocks per line} \times (1/\textit{fosc})}$$

Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

[Example]

Display size: 240 RGB × 320 lines Lines: 320 lines (NL = 100111)

Back porch: 2 lines (VBP = 0000010) Front porch: 2 lines (VFP = 0000010)

Frame frequency: 70 Hz Frequency fluctuation: 10%

Internal oscillator clock (fosc.) [Hz] = $70 \times [320+2+2] \times 27$ clocks $\times (1.1/0.9) = 748$ KHz





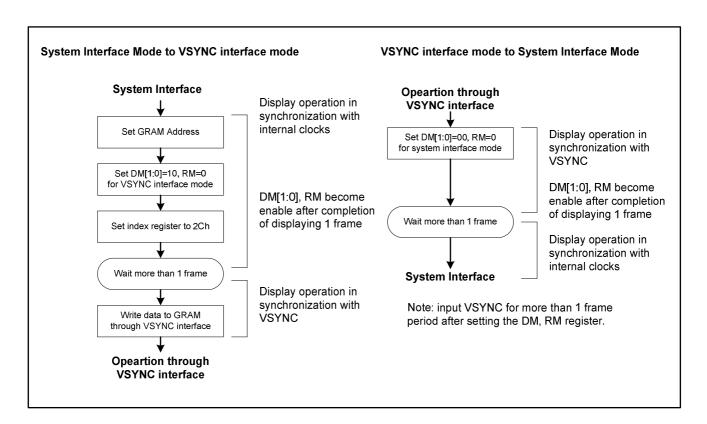
When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with ±10% margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

Minimum speed for RAM writing [Hz] > 240 x 320 x 748K / [(2 + 320 - 2)lines x 27clocks] = 6.65 MHz

The above theoretical value is calculated based on the premise that the ILI9341 starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 6.65MHz or more will guarantee the completion of GRAM write operation before the ILI9341 starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

Notes in using the VSYNC interface

- 1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
- 2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
- 3. When switching from the internal clock operation mode (DM[1:0] = "00") to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
- 4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.







7.4. Color Depth Conversion Look Up Table

When ILI9341 operates in parallel 16-bit interface, the color depth conversion is done by look-up table and extend input data format to 18-bit. See the detailed for look-up table of color depth conversion.

R input (5-bit) 16-bit/pixel -mode 65,536 colors	R output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	R ₀₀₅ R ₀₀₄ R ₀₀₃ R ₀₀₂ R ₀₀₁ R ₀₀₀	1
00001	R ₀₁₅ R ₀₁₄ R ₀₁₃ R ₀₁₂ R ₀₁₁ R ₀₁₀	2
00010	R ₀₂₅ R ₀₂₄ R ₀₂₃ R ₀₂₂ R ₀₂₁ R ₀₂₀	3
00011	R ₀₃₅ R ₀₃₄ R ₀₃₃ R ₀₃₂ R ₀₃₁ R ₀₃₀	4
00100	R ₀₄₅ R ₀₄₄ R ₀₄₃ R ₀₄₂ R ₀₄₁ R ₀₄₀	5
00101	R ₀₅₅ R ₀₅₄ R ₀₅₃ R ₀₅₂ R ₀₅₁ R ₀₅₀	6
00110	R ₀₆₅ R ₀₆₄ R ₀₆₃ R ₀₆₂ R ₀₆₁ R ₀₆₀	7
00111	R ₀₇₅ R ₀₇₄ R ₀₇₃ R ₀₇₂ R ₀₇₁ R ₀₇₀	8
01000	R ₀₈₅ R ₀₈₄ R ₀₈₃ R ₀₈₂ R ₀₈₁ R ₀₈₀	9
01001	R ₀₉₅ R ₀₉₄ R ₀₉₃ R ₀₉₂ R ₀₉₁ R ₀₉₀	10
01010	R ₁₀₅ R ₁₀₄ R ₁₀₃ R ₁₀₂ R ₁₀₁ R ₁₀₀	11
01011	R ₁₁₅ R ₁₁₄ R ₁₁₃ R ₁₁₂ R ₁₁₁ R ₁₁₀	12
01100	R ₁₂₅ R ₁₂₄ R ₁₂₃ R ₁₂₂ R ₁₂₁ R ₁₂₀	13
01101	R ₁₃₅ R ₁₃₄ R ₁₃₃ R ₁₃₂ R ₁₃₁ R ₁₃₀	14
01110	R ₁₄₅ R ₁₄₄ R ₁₄₃ R ₁₄₂ R ₁₄₁ R ₁₄₀	15
01111	R ₁₅₅ R ₁₅₄ R ₁₅₃ R ₁₅₂ R ₁₅₁ R ₁₅₀	16
10000	$R_{165}R_{164}R_{163}R_{162}R_{161}R_{160}$	17
10001	R ₁₇₅ R ₁₇₄ R ₁₇₃ R ₁₇₂ R ₁₇₁ R ₁₇₀	18
10010	R ₁₈₅ R ₁₈₄ R ₁₈₃ R ₁₈₂ R ₁₈₁ R ₁₈₀	19
10011	$R_{195} R_{194} R_{193} R_{192} R_{191} R_{190}$	20
10100	$R_{205} R_{204} R_{203} R_{202} R_{201} R_{200}$	21
10101	$R_{215}R_{214}R_{213}R_{212}R_{211}R_{210}$	22
10110	$R_{225} \: R_{224} \: R_{223} \: R_{222} \: R_{221} \: R_{220}$	23
10111	R ₂₃₅ R ₂₃₄ R ₂₃₃ R ₂₃₂ R ₂₃₁ R ₂₃₀	24
11000	R ₂₄₅ R ₂₄₄ R ₂₄₃ R ₂₄₂ R ₂₄₁ R ₂₄₀	25
11001	R ₂₅₅ R ₂₅₄ R ₂₅₃ R ₂₅₂ R ₂₅₁ R ₂₅₀	26
11010	R ₂₆₅ R ₂₆₄ R ₂₆₃ R ₂₆₂ R ₂₆₁ R ₂₆₀	27
11011	R ₂₇₅ R ₂₇₄ R ₂₇₃ R ₂₇₂ R ₂₇₁ R ₂₇₀	28
11100	R ₂₈₅ R ₂₈₄ R ₂₈₃ R ₂₈₂ R ₂₈₁ R ₂₈₀	29
11101	R ₂₉₅ R ₂₉₄ R ₂₉₃ R ₂₉₂ R ₂₉₁ R ₂₉₀	30
11110	R ₃₀₅ R ₃₀₄ R ₃₀₃ R ₃₀₂ R ₃₀₁ R ₃₀₀	31
11111	$R_{315}R_{314}R_{313}R_{312}R_{311}R_{310}$	32



G input (6-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
000000	G ₀₀₅ G ₀₀₄ G ₀₀₃ G ₀₀₂ G ₀₀₁ G ₀₀₀	33
000001	G ₀₁₅ G ₀₁₄ G ₀₁₃ G ₀₁₂ G ₀₁₁ G ₀₁₀	34
000010	$G_{025} G_{024} G_{023} G_{022} G_{021} G_{020}$	35
000011	G ₀₃₅ G ₀₃₄ G ₀₃₃ G ₀₃₂ G ₀₃₁ G ₀₃₀	36
000100	G ₀₄₅ G ₀₄₄ G ₀₄₃ G ₀₄₂ G ₀₄₁ G ₀₄₀	37
000101	G ₀₅₅ G ₀₅₄ G ₀₅₃ G ₀₅₂ G ₀₅₁ G ₀₅₀	38
000110	G ₀₆₅ G ₀₆₄ G ₀₆₃ G ₀₆₂ G ₀₆₁ G ₀₆₀	39
000111	G ₀₇₅ G ₀₇₄ G ₀₇₃ G ₀₇₂ G ₀₇₁ G ₀₇₀	40
001000	G ₀₈₅ G ₀₈₄ G ₀₈₃ G ₀₈₂ G ₀₈₁ G ₀₈₀	41
001001	G ₀₉₅ G ₀₉₄ G ₀₉₃ G ₀₉₂ G ₀₉₁ G ₀₉₀	42
001010	G ₁₀₅ G ₁₀₄ G ₁₀₃ G ₁₀₂ G ₁₀₁ G ₁₀₀	43
001011	G ₁₁₅ G ₁₁₄ G ₁₁₃ G ₁₁₂ G ₁₁₁ G ₁₁₀	44
001100	G ₁₂₅ G ₁₂₄ G ₁₂₃ G ₁₂₂ G ₁₂₁ G ₁₂₀	45
001101	$G_{135}G_{134}G_{133}G_{132}G_{131}G_{130}$	46
001110	G ₁₄₅ G ₁₄₄ G ₁₄₃ G ₁₄₂ G ₁₄₁ G ₁₄₀	47
001111	$G_{155}G_{154}G_{153}G_{152}G_{151}G_{150}$	48
010000	G ₁₆₅ G ₁₆₄ G ₁₆₃ G ₁₆₂ G ₁₆₁ G ₁₆₀	49
010001	G ₁₇₅ G ₁₇₄ G ₁₇₃ G ₁₇₂ G ₁₇₁ G ₁₇₀	50
010010	G ₁₈₅ G ₁₈₄ G ₁₈₃ G ₁₈₂ G ₁₈₁ G ₁₈₀	51
010011	G ₁₉₅ G ₁₉₄ G ₁₉₃ G ₁₉₂ G ₁₉₁ G ₁₉₀	52
010100	G ₂₀₅ G ₂₀₄ G ₂₀₃ G ₂₀₂ G ₂₀₁ G ₂₀₀	53
010101	$G_{215}G_{214}G_{213}G_{212}G_{211}G_{210}$	54
010110	G ₂₂₅ G ₂₂₄ G ₂₂₃ G ₂₂₂ G ₂₂₁ G ₂₂₀	55
010111	G ₂₃₅ G ₂₃₄ G ₂₃₃ G ₂₃₂ G ₂₃₁ G ₂₃₀	56
011000	$G_{245}G_{244}G_{243}G_{242}G_{241}G_{240}$	57
011001	$G_{255}G_{254}G_{253}G_{252}G_{251}G_{250}$	58
011010	$G_{265}G_{264}G_{263}G_{262}G_{261}G_{260}$	59
011011	$G_{275} G_{274} G_{273} G_{272} G_{271} G_{270}$	60
011100	$G_{285}G_{284}G_{283}G_{282}G_{281}G_{280}$	61
011101	$G_{295}G_{294}G_{293}G_{292}G_{291}G_{290}$	62
011110	$G_{305}G_{304}G_{303}G_{302}G_{301}G_{300}$	63
011111	$G_{315}G_{314}G_{313}G_{312}G_{311}G_{310}$	64
100000	$G_{325}G_{324}G_{323}G_{322}G_{321}G_{320}$	65
100001	$G_{335}G_{334}G_{333}G_{332}G_{331}G_{330}$	66





G input (6-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
100010	G ₃₄₅ G ₃₄₄ G ₃₄₃ G ₃₄₂ G ₃₄₁ G ₃₄₀	67
100011	G ₃₅₅ G ₃₅₄ G ₃₅₃ G ₃₅₂ G ₃₅₁ G ₃₅₀	68
100100	G ₃₆₅ G ₃₆₄ G ₃₆₃ G ₃₆₂ G ₃₆₁ G ₃₆₀	69
100101	G ₃₇₅ G ₃₇₄ G ₃₇₃ G ₃₇₂ G ₃₇₁ G ₃₇₀	70
100110	G ₃₈₅ G ₃₈₄ G ₃₈₃ G ₃₈₂ G ₃₈₁ G ₃₈₀	71
100111	G ₃₉₅ G ₃₉₄ G ₃₉₃ G ₃₉₂ G ₃₉₁ G ₃₉₀	72
101000	G ₄₀₅ G ₄₀₄ G ₄₀₃ G ₄₀₂ G ₄₀₁ G ₄₀₀	73
101001	G ₄₁₅ G ₄₁₄ G ₄₁₃ G ₄₁₂ G ₄₁₁ G ₄₁₀	74
101010	G ₄₂₅ G ₄₂₄ G ₄₂₃ G ₄₂₂ G ₄₂₁ G ₄₂₀	75
101011	G ₄₃₅ G ₄₃₄ G ₄₃₃ G ₄₃₂ G ₄₃₁ G ₄₃₀	76
101100	G ₄₄₅ G ₄₄₄ G ₄₄₃ G ₄₄₂ G ₄₄₁ G ₄₄₀	77
101101	G ₄₅₅ G ₄₅₄ G ₄₅₃ G ₄₅₂ G ₄₅₁ G ₄₅₀	78
101110	G ₄₆₅ G ₄₆₄ G ₄₆₃ G ₄₆₂ G ₄₆₁ G ₄₆₀	79
101111	G ₄₇₅ G ₄₇₄ G ₄₇₃ G ₄₇₂ G ₄₇₁ G ₄₇₀	80
110000	G ₄₈₅ G ₄₈₄ G ₄₈₃ G ₄₈₂ G ₄₈₁ G ₄₈₀	81
110001	G ₄₉₅ G ₄₉₄ G ₄₉₃ G ₄₉₂ G ₄₉₁ G ₄₉₀	82
110010	G ₅₀₅ G ₅₀₄ G ₅₀₃ G ₅₀₂ G ₅₀₁ G ₅₀₀	83
110011	G ₅₁₅ G ₅₁₄ G ₅₁₃ G ₅₁₂ G ₅₁₁ G ₅₁₀	84
110100	G ₅₂₅ G ₅₂₄ G ₅₂₃ G ₅₂₂ G ₅₂₁ G ₅₂₀	85
110101	G ₅₃₅ G ₅₃₄ G ₅₃₃ G ₅₃₂ G ₅₃₁ G ₅₃₀	86
110110	G ₅₄₅ G ₅₄₄ G ₅₄₃ G ₅₄₂ G ₅₄₁ G ₅₄₀	87
110111	G ₅₅₅ G ₅₅₄ G ₅₅₃ G ₅₅₂ G ₅₅₁ G ₅₅₀	88
111000	G ₅₆₅ G ₅₆₄ G ₅₆₃ G ₅₆₂ G ₅₆₁ G ₅₆₀	89
111001	G ₅₇₅ G ₅₇₄ G ₅₇₃ G ₅₇₂ G ₅₇₁ G ₅₇₀	90
111010	G ₅₈₅ G ₅₈₄ G ₅₈₃ G ₅₈₂ G ₅₈₁ G ₅₈₀	91
111011	$G_{595} G_{594} G_{593} G_{592} G_{591} G_{590}$	92
111100	G ₆₀₅ G ₆₀₄ G ₆₀₃ G ₆₀₂ G ₆₀₁ G ₆₀₀	93
111101	G ₆₁₅ G ₆₁₄ G ₆₁₃ G ₆₁₂ G ₆₁₁ G ₆₁₀	94
111110	G ₆₂₅ G ₆₂₄ G ₆₂₃ G ₆₂₂ G ₆₂₁ G ₆₂₀	95
111111	G ₆₃₅ G ₆₃₄ G ₆₃₃ G ₆₃₂ G ₆₃₁ G ₆₃₀	96



B input (5-bit) 16-bit/pixel -mode 65,536 colors	B output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	B ₀₀₅ B ₀₀₄ B ₀₀₃ B ₀₀₂ B ₀₀₁ B ₀₀₀	97
00001	B ₀₁₅ B ₀₁₄ B ₀₁₃ B ₀₁₂ B ₀₁₁ B ₀₁₀	98
00010	B ₀₂₅ B ₀₂₄ B ₀₂₃ B ₀₂₂ B ₀₂₁ B ₀₂₀	99
00011	B ₀₃₅ B ₀₃₄ B ₀₃₃ B ₀₃₂ B ₀₃₁ B ₀₃₀	100
00100	B ₀₄₅ B ₀₄₄ B ₀₄₃ B ₀₄₂ B ₀₄₁ B ₀₄₀	101
00101	B ₀₅₅ B ₀₅₄ B ₀₅₃ B ₀₅₂ B ₀₅₁ B ₀₅₀	102
00110	B ₀₆₅ B ₀₆₄ B ₀₆₃ B ₀₆₂ B ₀₆₁ B ₀₆₀	103
00111	B ₀₇₅ B ₀₇₄ B ₀₇₃ B ₀₇₂ B ₀₇₁ B ₀₇₀	104
01000	B ₀₈₅ B ₀₈₄ B ₀₈₃ B ₀₈₂ B ₀₈₁ B ₀₈₀	105
01001	B ₀₉₅ B ₀₉₄ B ₀₉₃ B ₀₉₂ B ₀₉₁ B ₀₉₀	106
01010	B ₁₀₅ B ₁₀₄ B ₁₀₃ B ₁₀₂ B ₁₀₁ B ₁₀₀	107
01011	B ₁₁₅ B ₁₁₄ B ₁₁₃ B ₁₁₂ B ₁₁₁ B ₁₁₀	108
01100	B ₁₂₅ B ₁₂₄ B ₁₂₃ B ₁₂₂ B ₁₂₁ B ₁₂₀	109
01101	B ₁₃₅ B ₁₃₄ B ₁₃₃ B ₁₃₂ B ₁₃₁ B ₁₃₀	110
01110	B ₁₄₅ B ₁₄₄ B ₁₄₃ B ₁₄₂ B ₁₄₁ B ₁₄₀	111
01111	B ₁₅₅ B ₁₅₄ B ₁₅₃ B ₁₅₂ B ₁₅₁ B ₁₅₀	112
10000	B ₁₆₅ B ₁₆₄ B ₁₆₃ B ₁₆₂ B ₁₆₁ B ₁₆₀	113
10001	B ₁₇₅ B ₁₇₄ B ₁₇₃ B ₁₇₂ B ₁₇₁ B ₁₇₀	114
10010	B ₁₈₅ B ₁₈₄ B ₁₈₃ B ₁₈₂ B ₁₈₁ B ₁₈₀	115
10011	B ₁₉₅ B ₁₉₄ B ₁₉₃ B ₁₉₂ B ₁₉₁ B ₁₉₀	116
10100	B ₂₀₅ B ₂₀₄ B ₂₀₃ B ₂₀₂ B ₂₀₁ B ₂₀₀	117
10101	B ₂₁₅ B ₂₁₄ B ₂₁₃ B ₂₁₂ B ₂₁₁ B ₂₁₀	118
10110	B ₂₂₅ B ₂₂₄ B ₂₂₃ B ₂₂₂ B ₂₂₁ B ₂₂₀	119
10111	B ₂₃₅ B ₂₃₄ B ₂₃₃ B ₂₃₂ B ₂₃₁ B ₂₃₀	120
11000	B ₂₄₅ B ₂₄₄ B ₂₄₃ B ₂₄₂ B ₂₄₁ B ₂₄₀	121
11001	B ₂₅₅ B ₂₅₄ B ₂₅₃ B ₂₅₂ B ₂₅₁ B ₂₅₀	122
11010	B ₂₆₅ B ₂₆₄ B ₂₆₃ B ₂₆₂ B ₂₆₁ B ₂₆₀	123
11011	B ₂₇₅ B ₂₇₄ B ₂₇₃ B ₂₇₂ B ₂₇₁ B ₂₇₀	124
11100	B ₂₈₅ B ₂₈₄ B ₂₈₃ B ₂₈₂ B ₂₈₁ B ₂₈₀	125
11101	B ₂₉₅ B ₂₉₄ B ₂₉₃ B ₂₉₂ B ₂₉₁ B ₂₉₀	126
11110	B ₃₀₅ B ₃₀₄ B ₃₀₃ B ₃₀₂ B ₃₀₁ B ₃₀₀	127
11111	B ₃₁₅ B ₃₁₄ B ₃₁₃ B ₃₁₂ B ₃₁₁ B ₃₁₀	128





7.5. Display Data RAM (DDRAM)

ILI9341 has an integrated 240x320x18-bit graphic type static RAM. This 172,800-byte memory allows storing a 240xRGBx320 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.



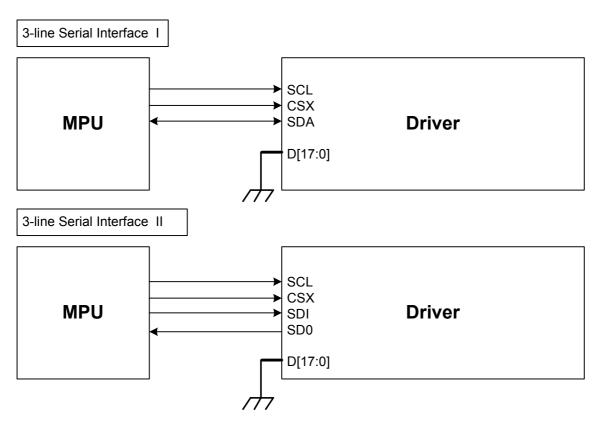


7.6. Display Data Format

ILI9341 supplies 18-/16-/9-/8-bit parallel MCU interface with 8080- I /8080- II series, 3-/4-line serial interface and 6-/16-18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM[1:0].

7.6.1. 3-line Serial Interface

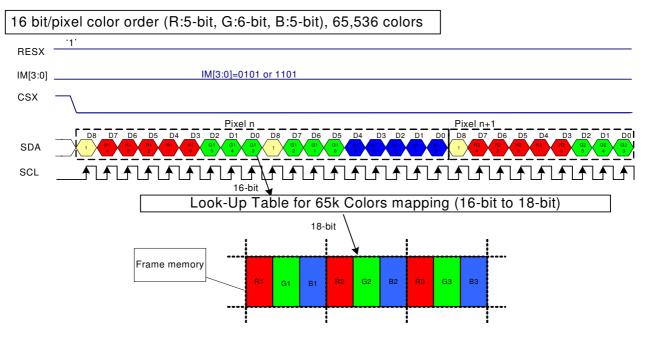
The 3-line/9-bit serial bus interface of ILI9341 can be used by setting external pin as IM [3:0] to "0101" for serial interface I or IM [3:0] to "1101" for serial interface II. The shown figure is the example of 3-line SPI interface.



In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

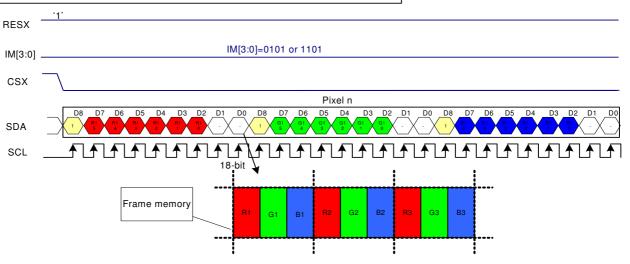
- -65k colors, RGB 5, 6, 5 -bits input
- -262k colors, RGB 6, 6, 6 -bits input.





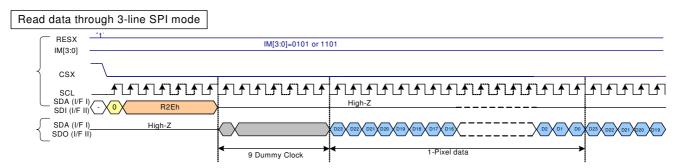
- Note 1: The pixel data with 16-bit color depth information.
- Note 2: The most significant bits are: Rx4, Gx5 and Bx4.
- Note 3: The least significant bits are: Rx0, Gx0 and Bx0.
- Note 4: '-'= Don't care -Can be set "0" or "1".

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



- Note 1: The pixel data with 18-bit color depth information.
- Note 2: The most significant bits are: Rx5, Gx5 and Bx5.
- Note 3: The least significant bits are : Rx0, Gx0 and Bx0.
- Note 4: '-'= Don't care Can be set "0" or "1".





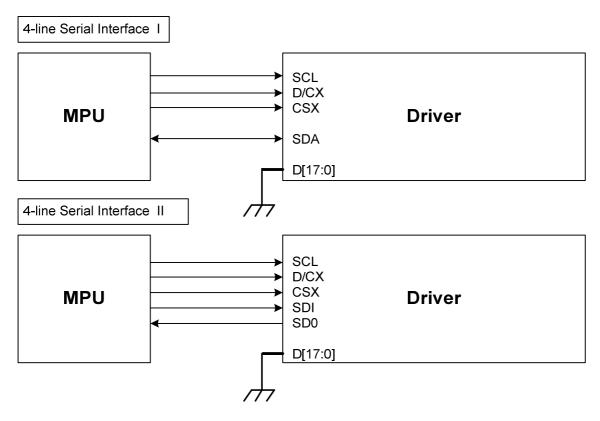
Note 1: '-'= Don't care -Can be set "0" or "1".





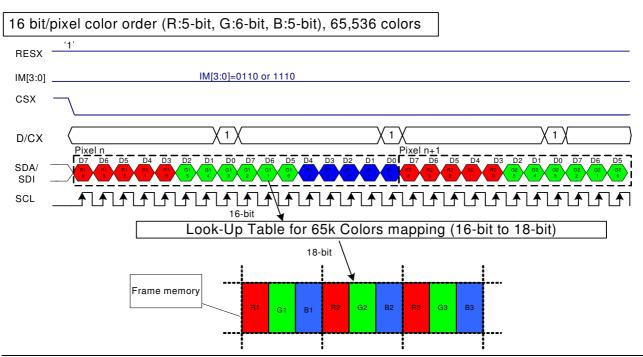
7.6.2. 4-line Serial Interface

The 4-line/8-bit serial bus interface of ILI9341 can be used by setting external pin as IM [3:0] to "0110" for serial interface I or IM [3:0] to "1110" for serial interface II. The shown figure is the example of 4-line SPI interface.



In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

- -65k colors, RGB 5, 6, 5 -bits input.
- -262k colors, RGB 6, 6, 6 -bits input.



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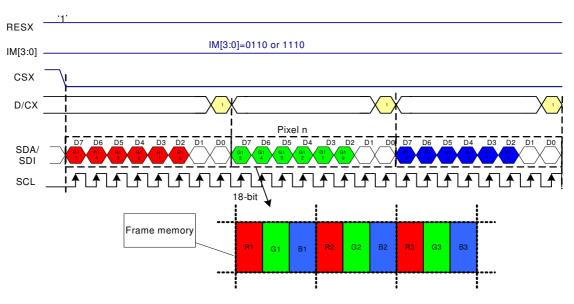
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care -Can be set "0" or "1".

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



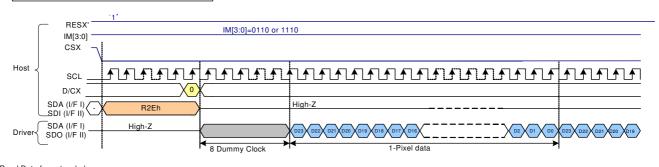
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care -Can be set "0" or "1".

Read data through 4-line SPI mode





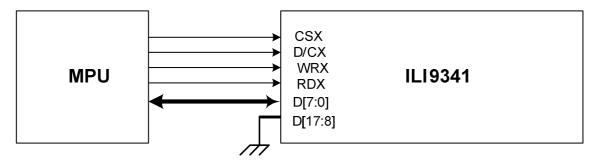
Note 1: '-'= Don't care - Can be set "0" or "1".





7.6.3. 8-bit Parallel MCU Interface

The 8080- I system 8-bit parallel bus interface of ILI9341 can be used by setting external pin as IM [3:0] to "0000". The following shown figure is the example of interface with 8080- I MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	 477	478	479	480
D/CX	0	1	1	1	1	 1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	 238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	 238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	 238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	 238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	 238R0		239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	 238G5		239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	 238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	 238G3		239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

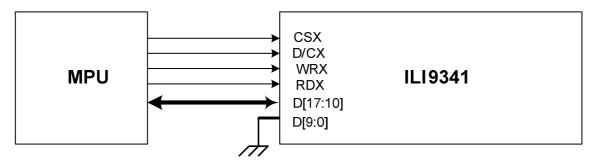
One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	 718	719	720
D/CX	0	1	1	1	 1	1	1
D7	C7	0R5	0G5	0B5	 239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	 239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	 239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	 239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	 239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	 239R0	239G0	239B0
D1	C1						
D0	C0						





The 8080- Π system 8-bit parallel bus interface of ILI9341 can be used by settings as IM [3:0] ="1001". The following shown figure is the example of interface with 8080- Π MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	 477	478	479	480
D/CX	0	1	1	1	1	 1	1	1	1
D17	C7	0R4	0G2	1R4	1G2	 238R4	238G2	239R4	239G2
D16	C6	0R3	0G1	1R3	1G1	 238R3	238G1	239R3	239G1
D15	C5	0R2	0G0	1R2	1G0	 238R2	238G0	239R2	239G0
D14	C4	0R1	0B4	1R1	1B4	 238R1	238B4	239R1	239B4
D13	C3	0R0		1R0	1B3	 238R0		239R0	239B3
D12	C2	0G5		1G5	1B2	 238G5		239G5	239B2
D11	C1	0G4	0B1	1G4	1B1	 238G4	238B1	239G4	239B1
D10	C0	0G3	0B0	1G3	1B0	 238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to "110".

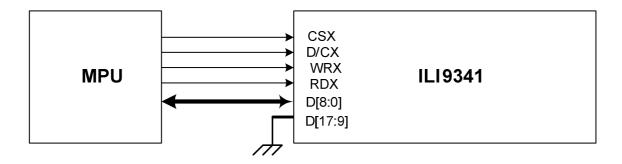
Count	0	1	2	3	 718	719	720
D/CX	0	1	1	1	 1	1	1
D17	C7	0R5	0G5	0B5	 239R5	239G5	239B5
D16	C6	0R4	0G4	0B4	 239R4	239G4	239B4
D15	C5	0R3	0G3	0B3	 239R3	239G3	239B3
D14	C4	0R2	0G2	0B2	 239R2	239G2	239B2
D13	C3	0R1	0G1	0B1	 239R1	239G1	239B1
D12	C2	0R0	0G0	0B0	 239R0	239G0	239B0
D11	C1						
D10	C0						





7.6.4. 9-bit Parallel MCU Interface

The 8080- I system 9-bit parallel bus interface of ILI9341 can be selected by setting hardware pin IM [3:0] to "0010". The following shown figure is the example of interface with 8080- I MCU system interface.



65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	 477	478	479	480
D/CX	0	1	1	1	1	 1	1	1	1
D8									
D7	C7	0R4	0G2	1R4	1G2	 238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	 238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	 238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	 238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	 238R0		239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	 238G5		239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	 238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	 238G3		239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

Count	0	1	2	3	4	 478	478	479	480
D/CX	0	1	1	1	1	 1	1	1	1
D8		0R5	0G2	1R5	1G2	238R5	238G2	239R5	239G2
D7	C7	0R4	0G1	1R4	1G1	 238R4	238G1	239R4	239G1
D6	C6	0R3	0G0	1R3	1G0	 238R3	238G0	239R3	239G0
D5	C5	0R2		1R2	1B5	 238R2		239R2	
D4	C4	0R1	0B4	1R1	1B4	 238R1	238B4	239R1	239B4
D3	C3	0R0		1R0	1B3	 238R0		239R0	
D2	C2	0G5		1G5	1B2	 238G5		239G5	
D1	C1	0G4	0B1	1G4	1B1	 238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	 238G3	238B0	239G3	239B0

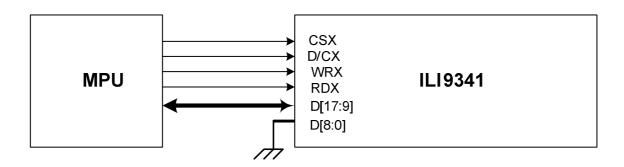




MDT[1:0]="01"

Count	0	1	2	3	 718	719	720
D/CX	0	1	1	1	 1	1	1
D8							
D7	C7	0R5	0G5		 239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	 239R4	239G4	239B4
D5	C5	0R3	0G3		 239R3	239G3	239B3
D4	C4	0R2	0G2		 239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	 239R1	239G1	239B1
D2	C2	0R0	0G0		 239R0	239G0	239B0
D1	C1						
D0	C0						

The 8080- Π system 9-bit parallel bus interface of ILI9341 can be selected by setting hardware pin IM [3:0] to "1011". The following shown figure is the example of interface with 8080- Π MCU system interface.



65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "101".

•		,			•			•	
Count	0	1	2	3	4	 477	478	479	480
D/CX	0	1	1	1	1	 1	1	1	1
D17	C7								
D16	C6	0R4	0G2	1R4	1G2	 238R4	238G2	239R4	239G2
D15	C5	0R3	0G1	1R3	1G1	 238R3	238G1	239R3	239G1
D14	C4	0R2	0G0	1R2	1G0	 238R2	238G0	239R2	239G0
D13	C3	0R1	0B4	1R1	1B4	 238R1	238B4	239R1	239B4
D12	C2	0R0	0B3	1R0	1B3	 238R0		239R0	
D11	C1	0G5	0B2	1G5	1B2	 238G5		239G5	
D10	C0	0G4	0B1	1G4	1B1	 238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	 238G3		239G3	





262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

Count	0	1	2	3	4	 478	478	479	480
D/CX	0	1	1	1	1	 1	1	1	1
D17	C7	0R5	0G2	1R5	1G2	238R5	238G2	239R5	239G2
D16	C6	0R4	0G1	1R4	1G1	 238R4	238G1	239R4	239G1
D15	C5	0R3	0G0	1R3	1G0	 238R3	238G0	239R3	239G0
D14	C4	0R2	0B5	1R2	1B5	 238R2		239R2	239B5
D13	C3	0R1	0B4	1R1	1B4	 238R1	238B4	239R1	239B4
D12	C2	0R0	0B3	1R0	1B3	 238R0		239R0	
D11	C1	0G5	0B2	1G5	1B2	 238G5		239G5	
D10	C0	0G4	0B1	1G4	1B1	 238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	 238G3		239G3	

MDT[1:0]="01"

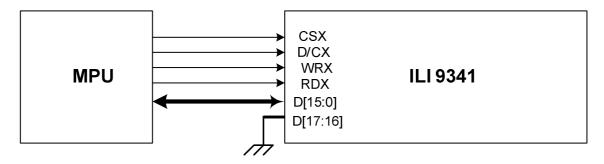
	=						
Count	0	1	2	3	 718	719	720
D/CX	0	1	1	1	 1	1	1
D17	C7						
D16	C6	0R5	0G5		 239R5	239G5	239B5
D15	C5	0R4	0G4	0B4	 239R4	239G4	239B4
D14	C4	0R3	0G3		 239R3	239G3	239B3
D13	C3	0R2	0G2		 239R2	239G2	239B2
D12	C2	0R1	0G1	0B1	 239R1	239G1	239B1
D11	C1	0R0	0G0		 239R0	239G0	
D10	C0						
D9							





7.6.5. 16-bit Parallel MCU Interface

The 8080- I system 16-bit parallel bus interface of ILl9341 can be selected by setting hardware pin IM[3:0] to "0001". The following shown figure is the example of interface with 8080- I MCU system interface.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

	•	, ,		•		0	
Count	0	1	2	3	 238	239	240
D/CX	0	1	1	1	 1	1	1
D15		0R4	1R4	2R4	 237R4	238R4	239R4
D14		0R3	1R3	2R3	 237R3	238R3	239R3
D13		0R2	1R2	2R2	 237R2	238R2	239R2
D12		0R1	1R1	2R1	 237R1	238R1	239R1
D11		0R0	1R0	2R0	 237R0	238R0	239R0
D10		0G5	1G5	2G5	 237G5	238G5	239G5
D9		0G4	1G4	2G4	 237G4	238G4	239G4
D8		0G3	1G3	2G3	 237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	 237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	 237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	 237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	237B4	238B4	239B4
D3	C3	0B3	1B3				239B3
D2	C2	0B2	1B2				239B2
D1	C1	0B1	1B1	2B1	237B1	238B1	239B1
D0	C0	0B0	1B0				239B0





262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

Count	0	1	2	3	 358	359	360
D/CX	0	1	1	1	 1	1	1
D15		0R5		1G5	 238R5		239G5
D14		0R4	0B4	1G4	 238R4	238B4	239G4
D13		0R3		1G3	 238R3		239G3
D12		0R2		1G2	 238R2		239G2
D11		0R1	0B1	1G1	 238R1	238B1	239G1
D10		0R0		1G0	 238R0		239G0
D9							
D8							
D7	C7	0G5	1R5	1B5	 238G5	239R5	239B5
D6	C6	0G4	1R4	1B4	 238G4	239R4	239B4
D5	C5	0G3	1R3	1B3	 238G3	239R3	239B3
D4	C4	0G2	1R2	1B2	 238G2	239R2	239B2
D3	C3	0G1	1R1	1B1	 238G1	239R1	239B1
D2	C2	0G0	1R0	1B0	 238G0	239R0	239B0
D1	C1						
D0	C0						

MDT[1:0]="01"

[] -	-								
Count	0	1	2	3		 357	358	479	480
D/CX	0	1	1	1			1	1	1
D15		0R5		1R5	1B5	 238R5		239R5	239B5
D14		0R4	0B4	1R4	1B4	 238R4	238B4	239R4	239B4
D13		0R3		1R3	1B3	 238R3		239R3	239B3
D12		0R2		1R2	1B2	 238R2		239R2	239B2
D11		0R1	0B1	1R1	1B1	 238R1	238B1	239R1	239B1
D10		0R0		1R0	1B0	 238R0		239R0	239B0
D9									
D8									
D7	C7	0G5		1G5		 238G5		239G5	
D6	C6	0G4		1G4		 238G4		239G4	
D5	C5	0G3		1G3		 238G3		239G3	
D4	C4	0G2		1G2		 238G2		239G2	
D3	C3	0G1		1G1		 238G1		239G1	
D2	C2	0G0		1G0		 238G0		239G0	
D1	C1		·						
D0	C0								





MDT[1:0]="10"

Count	0	1	2	3		 357	358	479	480
D/CX	0	1	1	1			1	1	1
D15		0R5	0B1	1R5	1B1	 238R5	238B1	239R5	239B1
D14		0R4		1R4	1B0	 238R4		239R4	239B0
D13		0R3		1R3		 238R3		239R3	
D12		0R2		1R2		 238R2		239R2	
D11		0R1		1R1		 238R1		239R1	
D10		0R0		1R0		 238R0		239R0	
D9		0G5		1G5		 238G5		239G5	
D8		0G4		1G4		 238G4		239G4	
D7	C7	0G3		1G3		 238G3		239G3	
D6	C6	0G2		1G2		 238G2		239G2	
D5	C5	0G1		1G1		 238G1		239G1	
D4	C4	0G0		1G0		 238G0		239G0	
D3	C3			1B5				239B5	
D2	C2	0B4		1B4		 238B4		239B4	
D1	C1			1B3				239B3	
D0	C0			1B2				239B2	

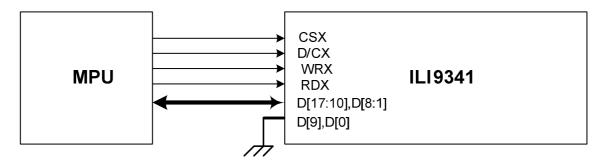
MDT[1:0]="11"

Count	0	1	2	3		 357	358	479	480
D/CX	0	1	1	1			1	1	1
D15			0R3		1R3		238R3		239R3
D14			0R2		1R2		238R2		239R2
D13			0R1		1R1		238R1		239R1
D12			0R0		1R0		238R0		239R0
D11			0G5		1G5		238G5		239G5
D10			0G4		1G4		238G4		239G4
D9			0G3		1G3		238G3		239G3
D8			0G2		1G2		238G2		239G2
D7	C7		0G1		1G1		238G1		239G1
D6	C6		0G0		1G0		238G0		239G0
D5	C5				1B5				239B5
D4	C4		0B4		1B4		238B4		239B4
D3	C3				1B3				239B3
D2	C2				1B2				
D1	C1	0R5	0B1	1R5	1B1	 238R5	238B1	239R5	239B1
D0	C0	0R4	0B0	1R4	1B0	 238R4	238B0	239R4	239B0





The 8080- Π system 16-bit parallel bus interface of ILI9341 can be selected by settings IM [3:0] ="1000". The following shown figure is the example of interface with 8080- Π MCU system interface.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	 238	239	240
D/CX	0	1	1	1	 1	1	1
D17		0R4	1R4	2R4	 237R4	238R4	239R4
D16		0R3	1R3	2R3	 237R3	238R3	239R3
D15		0R2	1R2	2R2	 237R2	238R2	239R2
D14		0R1	1R1	2R1	 237R1	238R1	239R1
D13		0R0	1R0	2R0	 237R0	238R0	239R0
D12		0G5	1G5	2G5	 237G5	238G5	239G5
D11		0G4	1G4	2G4	 237G4	238G4	239G4
D10		0G3	1G3	2G3	 237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	 237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	 237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	 237G0	238G0	239G0
D5	C4	0B4	1B4	2B4	237B4	238B4	239B4
D4	C3		1B3				239B3
D3	C2		1B2				239B2
D2	C1	0B1	1B1	2B1	237B1	238B1	239B1
D1	C0	0B0	1B0	2B0	 237B0	238B0	239B0





262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

Count	0	1	2	3	 358	359	360
D/CX	0	1	1	1	 1	1	1
D17		0R5		1G5	 238R5		239G5
D16		0R4	0B4	1G4	 238R4	238B4	239G4
D15		0R3		1G3	 238R3		239G3
D14		0R2		1G2	 238R2		239G2
D13		0R1	0B1	1G1	 238R1	238B1	239G1
D12		0R0		1G0	 238R0		239G0
D11							
D10							
D8	C7	0G5	1R5	1B5	 238G5	239R5	239B5
D7	C6	0G4	1R4	1B4	 238G4	239R4	239B4
D6	C5	0G3	1R3	1B3	 238G3	239R3	239B3
D5	C4	0G2	1R2	1B2	 238G2	239R2	239B2
D4	C3	0G1	1R1	1B1	 238G1	239R1	239B1
D3	C2	0G0	1R0	1B0	 238G0	239R0	239B0
D2	C1						
D1	C0						

MDT[1:0]="01"

Count	0	1	2	3		 357	358	479	480
D/CX	0	1	1	1			1	1	1
D17		0R5		1R5	1B5	 238R5		239R5	239B5
D16		0R4	0B4	1R4	1B4	 238R4	238B4	239R4	239B4
D15		0R3		1R3	1B3	 238R3		239R3	239B3
D14		0R2		1R2	1B2	 238R2		239R2	239B2
D13		0R1	0B1	1R1	1B1	 238R1	238B1	239R1	239B1
D12		0R0		1R0	1B0	 238R0		239R0	239B0
D11									
D10									
D8	C7	0G5		1G5		 238G5		239G5	
D7	C6	0G4		1G4		 238G4		239G4	
D6	C5	0G3		1G3		 238G3		239G3	
D5	C4	0G2		1G2		 238G2		239G2	
D4	C3	0G1		1G1		 238G1		239G1	
D3	C2	0G0		1G0		 238G0		239G0	
D2	C1		·						
D1	C0								





MDT[1:0]="10"

Count	0	1	2	3		 357	358	479	480
D/CX	0	1	1	1			1	1	1
D17		0R5	0B1	1R5	1B1	 238R5	238B1	239R5	239B1
D16		0R4		1R4	1B0	 238R4		239R4	239B0
D15		0R3		1R3		 238R3		239R3	
D14		0R2		1R2		 238R2		239R2	
D13		0R1		1R1		 238R1		239R1	
D12		0R0		1R0		 238R0		239R0	
D11		0G5		1G5		 238G5		239G5	
D10		0G4		1G4		 238G4		239G4	
D8	C7	0G3		1G3		 238G3		239G3	
D7	C6	0G2		1G2		 238G2		239G2	
D6	C5	0G1		1G1		 238G1		239G1	
D5	C4	0G0		1G0		 238G0		239G0	
D4	C3			1B5				239B5	
D3	C2	0B4		1B4		 238B4		239B4	
D2	C1			1B3				239B3	
D1	C0	0B2		1B2		 238B2		239B2	

MDT[1:0]="11"

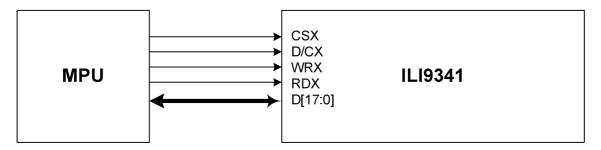
Count	0	1	2	3		 357	358	479	480
D/CX	0	1	1	1			1	1	1
D17			0R3		1R3		238R3		239R3
D16			0R2		1R2		238R2		239R2
D15			0R1		1R1		238R1		239R1
D14			0R0		1R0		238R0		239R0
D13			0G5		1G5		238G5		239G5
D12			0G4		1G4		238G4		239G4
D11			0G3		1G3		238G3		239G3
D10			0G2		1G2		238G2		239G2
D8	C7		0G1		1G1		238G1		239G1
D7	C6		0G0		1G0		238G0		239G0
D6	C5				1B5				239B5
D5	C4		0B4		1B4		238B4		239B4
D4	C3				1B3				239B3
D3	C2				1B2				239B2
D2	C1	0R5	0B1	1R5	1B1	 238R5	238B1	239R5	239B1
D1	C0	0R4	0B0	1R4	1B0	 238R4	238B0	239R4	239B0





7.6.6. 18-bit Parallel MCU Interface

The 8080- I system 18-bit parallel bus interface of ILl9341 can be selected by setting hardware pin IM[3:0] to "0011". The following shown figure is the example of interface with 8080- I MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

. ,		· · ·	,		 		
Count	0	1	2	3	 238	239	240
D/CX	0	1	1	1	 1	1	1
D17							
D16							
D15		0R4	1R4	2R4	 237R4	238R4	239R4
D14		0R3	1R3	2R3	 237R3	238R3	239R3
D13		0R2	1R2	2R2	 237R2	238R2	239R2
D12		0R1	1R1	2R1	 237R1	238R1	239R1
D11		0R0	1R0	2R0	 237R0	238R0	239R0
D10		0G5	1G5	2G5	 237G5	238G5	239G5
D9		0G4	1G4	2G4	 237G4	238G4	239G4
D8		0G3	1G3	2G3	 237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	 237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	 237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	 237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	237B4	238B4	239B4
D3	C3		1B3				
D2	C2		1B2				
D1	C1	0B1	1B1	2B1	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	 237B0	238B0	239B0





262K color: 18-bit/pixel (RGB 6-6-6 bits input)

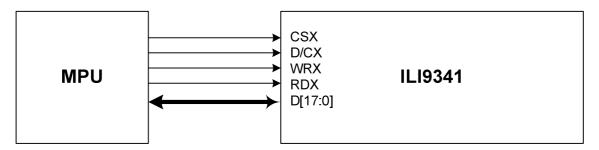
One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	 238	239	240
D/CX	0	1	1	1	 1	1	1
D17		0R5	1R5	2R5	 237R5	238R5	239R5
D16		0R4	1R4	2R4	 237R4	238R4	239R4
D15		0R3	1R3	2R3	 237R3	238R3	239R3
D14		0R2	1R2	2R2	 237R2	238R2	239R2
D13		0R1	1R1	2R1	 237R1	238R1	239R1
D12		0R0	1R0	2R0	 237R0	238R0	239R0
D11		0G5	1G5	2G5	 237G5	238G5	239G5
D10		0G4	1G4	2G4	 237G4	238G4	239G4
D9		0G3	1G3	2G3	 237G3	238G3	239G3
D8		0G2	1G2	2G2	 237G2	238G2	239G2
D7	C7	0G1	1G1	2G1	 237G1	238G1	239G1
D6	C6	0G0	1G0	2G0	 237G0	238G0	239G0
D5	C5		1B5				239B5
D4	C4	0B4	1B4	2B4	237B4	238B4	239B4
D3	C3		1B3				239B3
D2	C2		1B2				239B2
D1	C1	0B1	1B1	2B1	237B1	238B1	239B1
D0	C0		1B0				239B0





The 8080- Π system 18-bit parallel bus interface mode can be selected by settings IM [3:0] ="1010". The following shown figure is the example of interface with 8080- Π MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	 238	239	240
D/CX	0	1	1	1	 1	1	1
D17							
D16							
D15		0R4	1R4	2R4	 237R4	238R4	239R4
D14		0R3	1R3	2R3	 237R3	238R3	239R3
D13		0R2	1R2	2R2	 237R2	238R2	239R2
D12		0R1	1R1	2R1	 237R1	238R1	239R1
D11		0R0	1R0	2R0	 237R0	238R0	239R0
D10		0G5	1G5	2G5	 237G5	238G5	239G5
D9		0G4	1G4	2G4	 237G4	238G4	239G4
D8	C7	0G3	1G3	2G3	 237G3	238G3	239G3
D7	C6	0G2	1G2	2G2	 237G2	238G2	239G2
D6	C5	0G1	1G1	2G1	 237G1	238G1	239G1
D5	C4	0G0	1G0	2G0	 237G0	238G0	239G0
D4	C3	0B4	1B4	2B4	237B4	238B4	239B4
D3	C2		1B3				239B3
D2	C1		1B2				239B2
D1	C0	0B1	1B1	2B1	237B1	238B1	239B1
D0		0B0	1B0	2B0	 237B0	238B0	239B0





262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	 238	239	240
D/CX	0	1	1	1	 1	1	1
D17		0R5	1R5	2R5	 237R5	238R5	239R5
D16		0R4	1R4	2R4	 237R4	238R4	239R4
D15		0R3	1R3	2R3	 237R3	238R3	239R3
D14		0R2	1R2	2R2	 237R2	238R2	239R2
D13		0R1	1R1	2R1	 237R1	238R1	239R1
D12		0R0	1R0	2R0	 237R0	238R0	239R0
D11		0G5	1G5	2G5	 237G5	238G5	239G5
D10		0G4	1G4	2G4	 237G4	238G4	239G4
D9		0G3	1G3	2G3	 237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	 237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	 237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	 237G0	238G0	239G0
D5	C4		1B5				239B5
D4	C3	0B4	1B4	2B4	237B4	238B4	239B4
D3	C2		1B3				239B3
D2	C1		1B2				239B2
D1	C0	0B1	1B1	2B1	237B1	238B1	239B1
D0			1B0				239B0

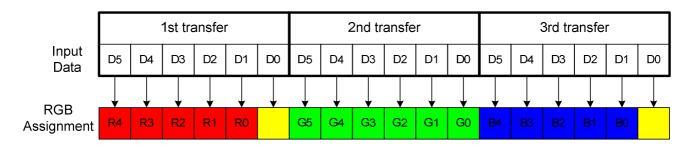




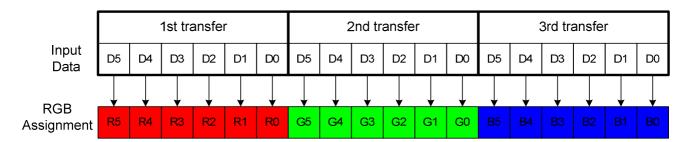
7.6.7. 6-bit Parallel RGB Interface

The 6-bit RGB interface is selected by setting the DPI [2:0] bit to "110". When RCM [1:0] are set to "10" and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (D [5:0]) according to the data enable signal (DE) when RCM [1:0] are set to "10". The RGB interface SYNC mode is selected by setting the RCM [1:0] to "11", the valid display data is inputted in pixel unit via D [5:0] according to the VFP/VBP and HFP/HBP settings. Unused pins must be connected to GND to ensure normally operation. Registers can be set by the SPI system interface.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)



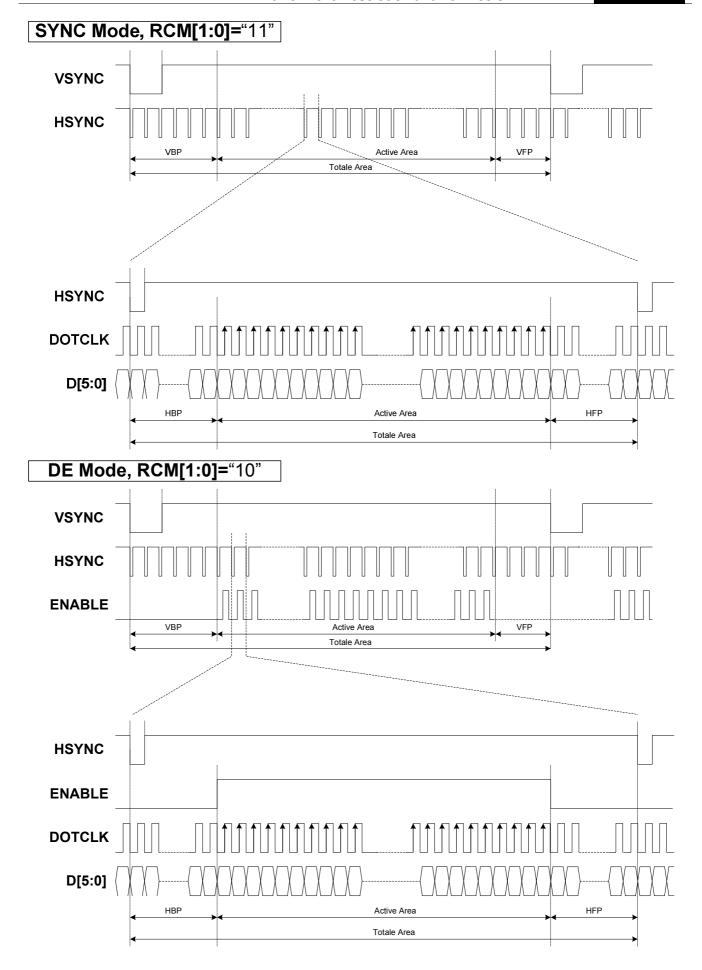
262K color: 18-bit/pixel (RGB 6-6-6 bits input)



ILI9341 has data transfer counters to count the first, second, third data transfer in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.





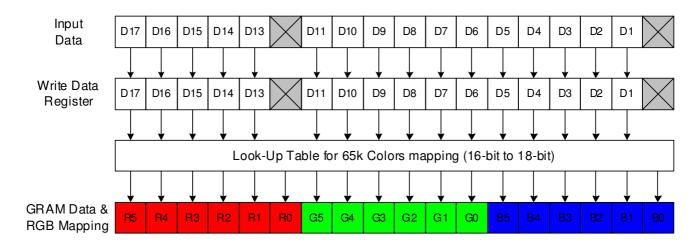






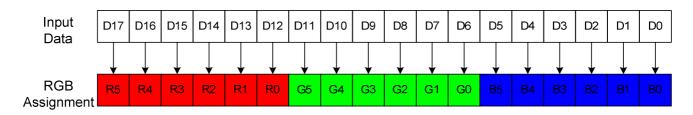
7.6.8. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits to "101". When RCM [1:0] are set to "10" and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data is transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D [17:13] & D [11:1]) according to the data enable signal (DE). The RGB interface SYNC mode is selected by setting the RCM [1:0] to "11", the valid display data is inputted in pixel unit via D [17:13] and D [11:1] according to the VFP/VBP and HFP/HBP settings. The unused D12 and D0 pins must be connected to GND for ensure normally operation. Registers can be set by the SPI system interface.



7.6.9. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits to "110". When RCM [1:0] are set to "10" and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (D [17:0]) according to the data enable signal (DE) when RCM [1:0] are set to "10". The RGB interface SYNC mode is selected by setting the RCM [1:0] to "11", the valid display data is inputted in pixel unit via D [17:0] according to the VFP/VBP and HFP/HBP settings. Registers can be set by the SPI system interface.







8. Command

8.1. Command List

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex
No Operation	0	1	↑	XX	0	0	0	0	0	0	0	0	00h
Software Reset	0	1	↑	XX	0	0	0	0	0	0	0	1	01h
	0	1	1	XX	0	0	0	0	0	1	0	0	04h
Dood Display Identification	1	1	1	XX	Х	X	Х	Χ	Χ	Х	Х	Χ	XX
Read Display Identification Information	1	1	1	XX				ID1 [7:0]				XX
IIIOIIIIatioii	1	1	1	XX				ID2 [7:0]				XX
	1	1	1	XX				ID3 [7:0]				XX
	0	1	1	XX	0	0	0	0	1	0	0	1	09h
	1	↑	1	XX	Х	X	Х	Χ	Χ	Х	X	Χ	XX
Road Diaplay Status	1	1	1	XX			D	[31:25]				Χ	00
Read Display Status	1	1	1	XX	Х		D [22:20]		D [19	9:16]		61
	1	1	1	XX	Х	X	Х	Χ	Х		D [10:8]		00
	1	↑	1	XX		D [7:5]		Χ	Χ	Х	X	Χ	00
	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah
Read Display Power Mode	1	1	1	XX	Х	Х	Х	Χ	Χ	Х	Х	Χ	XX
	1	1	1	XX			D [7	:2]			0	0	08
	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh
Read Display MADCTL	1	1	1	XX	Х	X	Х	Χ	Χ	Х	Х	Χ	XX
	1	1	1	XX			D [7	:2]			0	0	00
	0	1	1	XX	0	0	0	0	1	1	0	0	0Ch
Read Display Pixel Format	1	1	1	XX	Х	X	Х	Χ	Χ	Х	Х	Χ	XX
	1	↑	1	XX	RIM		DPI [2:0]		Χ	I	DBI [2:0]		06
	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh
Read Display Image Format	1	1	1	XX	Х	X	Х	Χ	Χ	Х	Х	Χ	XX
	1	1	1	XX	Х	Х	Х	Χ	Χ		D [2:0]		00
	0	1	1	XX	0	0	0	0	1	1	1	0	0Eh
Read Display Signal Mode	1	1	1	XX	Х	X	Х	Χ	Χ	Х	Х	Χ	XX
	1	1	1	XX			D [7	:2]			0	0	00
Read Display Self-Diagnostic	0	1	1	XX	0	0	0	0	1	1	1	1	0Fh
Result	1	1	1	XX	Х	Х	Х	Χ	Χ	Х	Х	Χ	XX
rtesuit	1	1	1	XX	D [7	ː6]	Х	Χ	Χ	Х	Х	Χ	00
Enter Sleep Mode	0	1	1	XX	0	0	0	1	0	0	0	0	10h
Sleep OUT	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Partial Mode ON	0	1	1	XX	0	0	0	1	0	0	1	0	12h
Normal Display Mode ON	0	1	1	XX	0	0	0	1	0	0	1	1	13h
Display Inversion OFF	0	1	1	XX	0	0	1	0	0	0	0	0	20h
Display Inversion ON	0	1	1	XX	0	0	1	0	0	0	0	1	21h
Gamma Set	0	1	1	XX	0	0	1	0	0	1	1	0	26h
Gamma Set	1	1	↑	XX				GC [7:0]				01
Display OFF	0	1	1	XX	0	0	1	0	1	0	0	0	28h
Display ON	0	1	1	XX	0	0	1	0	1	0	0	1	29h
	0	1	1	XX	0	0	1	0	1	0	1	0	2Ah
	1	1	1	XX				SC [1	5:8]				XX
Column Address Set	1	1	1	XX			_	SC [7	7:0]	_	_		XX
	1	1	1	XX				EC [1	5:8]				XX
	1	1	1	XX				EC [7:0]				XX
	0	1	1	XX	0	0	1	0	1	0	1	1	2Bh
	1	1	<u></u>	XX				SP [1	5:8]				XX
Page Address Set	1	1	1	XX				SP [7	7:0]				XX
	1	1	↑	XX				EP [1					XX
	1	1	↑	XX		_		EP [7					XX





			I				1		1		1	1	
Memory Write	0	1	1	XX	0	0	1	0	1	1	0	0	2Cł
-	1	1	1	207				0 [17:0]		· .	1 _	1 .	XX
	0	1	1	XX	0	0	1	0	1	1	0	1	2DI
	1	1	1	XX						00 [5:0]			XX
	1	1	1	XX						nn [5:0]			XX
	1	1	1	XX		1				31 [5:0]			XX
Color SET	1	1	1	XX		1				00 [5:0]			XX
	1	1	1	XX		1				nn [5:0]			XX
	1	1	1	XX						64 [5:0]			XX
	1	1	1	XX						00 [5:0]			XX
	1	1	1	XX						nn [5:0]			XX
	1	1	1	XX		l	1		В	31 [5:0]	1	1	XX
	0	1	1	XX	0	0	1	0	1	1	1	0	2Eł
Memory Read	1	1	1	XX	X	Χ	Χ	Χ	Х	Χ	X	X	XX
	1	1	1		1	1	[0 [17:0]		1	1	1	XX
	0	1	1	XX	0	0	1	1	0	0	0	0	30h
	1	1	1	XX					R [15:8]				00
Partial Area	1	1	1	XX	SR [7:0]								00
	1	1	1	XX				E	R [15:8]				01
	1	1	1	XX		1	1	E	R [7:0]	1	1	1	3F
	0	1	1	XX	0	0	1	1	0	0	1	1	33h
	1	1	1	XX				TF	A [15:8]				00
	1	1	1	XX				T	FA [7:0]				00
Vertical Scrolling Definition	1	1	1	XX				VS	A [15:8]				01
	1	1	1	XX				V	SA [7:0]				40
	1	1	1	XX				BF	A [15:8]				00
	1	1	1	XX				В	FA [7:0]				00
Tearing Effect Line OFF	0	1	1	XX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line ON	0	1	1	XX	0	0	1	1	0	1	0	1	35h
rearing Ellect Elle ON	1	1	1	XX	Χ	Χ	Χ	Х	Х	Χ	X	М	00
Memory Access Control	0	1	1	XX	0	0	1	1	0	1	1	0	36h
Memory Access Control	1	1	1	XX	MY	MX	MV	ML	BGR	МН	Х	Х	00
	0	1	1	XX	0	0	1	1	0	1	1	1	37h
Vertical Scrolling Start Address	1	1	1	XX				VS	SP [15:8]				00
	1	1	1	XX				V:	SP [7:0]				00
Idle Mode OFF	0	1	1	XX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	1	XX	0	0	1	1	1	0	0	1	39h
Dival Format Cat	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ał
Pixel Format Set	1	1	↑	XX	Χ		DPI [2:0)]	Х		DBI [2:0)]	66
Mysta Maman, Cantinua	0	1	1	XX	0	0	1	1	1	1	0	0	3Cł
Write Memory Continue	1	1	↑				[0 [17:0]					XX
	0	1	1	XX	0	0	1	1	1	1	1	0	3Eł
Read Memory Continue	1	↑	1	XX	Χ	Χ	Χ	Х	Х	Χ	Х	Х	XX
	1	↑	1				[0 [17:0]					XX
	0	1	1	XX	0	1	0	0	0	1	0	0	44h
Set Tear Scanline	1	1	↑	XX	Х	Х	Х	Χ	Х	Х	Х	STS [8]	00
	1	1	1	XX					TS [7:0]				00
	0	1	1	XX	0	1	0	0	0	1	0	1	45h
	1	1	1	XX	Х	Х	Х	Х	Х	Х	Х	Х	XX
Get Scanline	1	1	1	XX	Х	Х	Х	Х	Х	Х		S [9:8]	00
	1	1	1	XX					TS [7:0]				00
	0	1	· 1	XX	0	1	0	1	0	0	0	1	51h
Write Display Brightness		+		t	 			D				· · · · · · · · · · · · · · · · · · ·	





	0	1	1	XX	0	1	0	1	0	0	1	0	52h
Read Display Brightness	1	1	1	XX	Х	Х	Х	Х	Х	Х	Х	Х	XX
	1	1	1	XX			•	DBV	[7:0]				00
Mile OTDI Diseles	0	1	1	XX	0	1	0	1	0	0	1	1	53h
Write CTRL Display	1	1	1	XX	Х	Х	BCTRL	Х	DD	BL	Х	Х	00
	0	1	1	XX	0	1	0	1	0	1	0	0	54h
Read CTRL Display	1	1	1	XX	Х	Х	Х	Х	Х	Х	Х	Х	XX
	1	1	1	XX	Х	Х	BCTRL	Х	DD	BL	Х	Х	00
Write Content Adaptive	0	1	1	XX	0	1	0	1	0	1	0	1	55h
Brightness Control	1	1	1	XX	Х	Х	Х	Х	Х	Х	C [1:0]	00
Deed Content Adouting	0	1	↑	XX	0	1	0	1	0	1	1	0	56h
Read Content Adaptive Brightness Control	1	1	1	XX	Χ	Χ	Х	Х	Х	Х	Х	Х	XX
Brightiness Control	1	1	1	XX	Х	Х	Х	Х	Х	Х	0 [1:0]	00
Write CABC Minimum	0	1	1	XX	0	1	0	1	1	1	1	0	5Eh
Brightness	1	1	↑	XX				CME	8 [7:0]				00
Read CABC Minimum	0	1	1	XX	0	1	0	1	0	1	1	1	5Fh
Brightness	1	1	1	XX	Χ	Χ	Χ	X	Х	Х	Х	Χ	XX
Brighthood	1	↑	1	XX				CME	8 [7:0]				00
	0	1	1	XX	1	1	0	1	1	0	1	0	DAh
Read ID1	1	1	1	XX	Χ	Χ	Χ	X	Х	Х	Х	Χ	XX
	1	1	1	XX			Modu	ıle's Maı	nufacture	e [7:0]			XX
	0	1	1	XX	1	1	0	1	1	0	1	1	DBh
Read ID2	1	1	1	XX	Х	X	Х	X	Х	Х	Χ	Χ	XX
	1	1	1	XX			LCD Mo	dule / Di	river Ver	sion [7:0]		XX
	0	1	1	XX	1	1	0	1	1	1	0	0	DCh
Read ID3	1	1	1	XX	Х	Χ	X	Χ	Χ	Х	Х	Χ	XX
	1	1	1	XX			LCD I	Module /	Driver I	D [7:0]			XX

Extended Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RGB Interface	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
Signal Control	1	1	↑	XX	ByPass_MODE	RCM	[1:0]	Χ	VSPL	HSPL	DPL	EPL	40
France Control	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h
Frame Control	1	1	↑	XX	Χ	Χ	Χ	Χ	Х	Х	DIVA	(1:0]	00
(In Normal Mode)	1	1	↑	XX	Χ	Χ	Χ		B	TNA [4:0)]		1B
Frame Control	0	1	1	XX	1	0	1	1	0	0	1	0	B2h
(In Idle Mode)	1	1	↑	XX	Χ	Χ	Χ	Χ	Х	Х	DIVE	8 [1:0]	00
(III lale Mode)	1	1	1	XX	X	Χ	Χ		B	TNB [4:0	0]		1B
Frame Control	0	1	↑	XX	1	0	1	1	0	0	1	1	B3h
(In Partial Mode)	1	1	1	XX	X	Χ	Χ	Χ	Х	Х	DIVC	[1:0]	00
(III Fartiai Mode)	1	1	1	XX	X	Χ	Χ		R	TNC [4:0	0]		1B
Display Inversion Control	0	1	1	XX	1	0	1	1	0	1	0	0	B4h
Display inversion Control	1	1	↑	XX	Χ	Χ	Χ	Χ	Х	NLA	NLB	NLC	02
	0	1	1	XX	1	0	1	1	0	1	0	1	B5h
Blanking Porch Control	1	1	↑	XX	0				VFP [6:	0]			02
	1	1	1	XX	0				VBP [6:	0]			02
	1	1	1	XX	0	0	0			HFP [4:0]		0A
	1	1	↑	XX	0	0	0			HBP [4:0]		14





	0	1	1	XX	1	0	1	1	0	1	1	0	B6h
	1	1	↑	XX	Х	Х	Х	Х	PTG	i [1:0]	PT	[1:0]	0A
Display Function Control	1	1	1	XX	REV	GS	SS	SM			SC [3:0]	•	82
	1	1	1	XX	Х	Х				NL [5:0]			27
	1	1	1	XX	Х	Х			P	CDIV [5:	0]		XX
Entry Mada Cat	0	1	1	XX	1	0	1	1	0	1	1	1	B7h
Entry Mode Set	1	1	1	XX	Х	Х	Χ	Х	0	GON	DTE	GAS	07
	0	1	1	XX	1	0	1	1	1	0	0	0	B8h
Backlight Control 1	1	1	1	XX	X	Х	Χ	Х	Χ	Х	X	Х	XX
	1	1	1	XX	X	Х	Χ	Χ		T <u></u>	I_UI [3:0]		04
	0	1	1	XX	1	0	1	1	1	0	0	1	B9h
Backlight Control 2	1	1	1	XX	Х	Х	Χ	Х	Χ	Х	X	Х	XX
	1	1	1	XX		TH_MV	[3:0]			TH	_ST [3:0]	_	B8
	0	1	1	XX	1	0	1	1	1	0	1	0	BAh
Backlight Control 3	1	1	1	XX	Х	Х	Х	Х	Х	Х	Х	Х	XX
	1	1	1	XX	Х	Х	Х	Х		DTI	H_UI [3:0]		04
	0	1	1	XX	1	0	1	1	1	0	1	1	BBh
Backlight Control 4	1	1	1	XX	Х	X	Х	X	Х	Χ	Х	Х	XX
	1	1	1	XX		DTH_M\					H_ST [3:0]		C9
	0	1	1	XX	1	0	1	1	1	1	0	0	BCh
Backlight Control 5	1	1	1	XX	Х	Χ	Χ	Х	Х	Х	Х	Х	XX
	1	1		XX		DIM2 [Х		DIM1 [2:		44
Backlight Control 7	0	1		XX	1	0	1	1	1	1	1	0	BEh
•	1	1	1	XX		1			_DIV [7		I .		0F
Backlight Control 8	0	1		XX	1	0	1	1	1	1	1	1	BFh
•	1	1	1	XX	X	X	X	X	X	LEDONR		LEDPWMOPL	
Power Control 1	0	1	1	XX	1	1	0	0	0	0	0	0	C0h
	1	1		XX	X	X	_			/RH [5:0]			26
Power Control 2	0	1	1	XX	1	1	0	0	0	0	0	1	C1h
	1	1	1	XX	X	X	X	X	X		BT [2:		00
VCOM Control 1	0	1	1	XX	1	1	0	0	0	1	0	1	C5h
VCOW CONTROL I	1	1		XX	X				VMH				31 3C
	0	1	<u> </u>	XX	1	1	0	0	VML 0	1	1	1	C7h
VCOM Control 2	1	1		XX	nVM	1	U	U	VMF		l l		C0
						4	0	4			0	0	
NV Memory Write	1	1	<u> </u>	XX	1 X	1 X	0 X	1 X	0 X	0	<u>0</u> GM_ADR	0 0	D0h 00
NV Wemory Wille	1	1	<u> </u>	XX	^	_ ^	_ ^		DATA [GIVI_ADA	[2.0]	XX
	0	1	<u> </u>	XX	1	1	0	1 1	0	0	0	1	D1h
	1	1	<u> </u>	XX	'	'			/ [23:16			!	55
NV Memory Protection Key	1	1	<u> </u>	XX	1				Y [15:8]				AA
	1	1	<u> </u>	XX	1				Y [7:0]	<u> </u>			66
	0	1	<u> </u>	XX	1	1	0	1	0	0	1	0	D2h
	1	<u> </u>	1	XX	X	X	X	X	X	X	X	X	XX
NV Memory Status Read	1	<u> </u>	1	XX	X		_CNT		X		D1_CNT	1	XX
	1		1	XX	BUSY		_CNT		X		D3_CNT		XX





	_		,	1									
	0	1	1	XX	1	1	0	1	0	0	1	1	D3h
	1	1	1	XX	Х	Χ	Х	Χ	Х	Χ	Χ	Х	XX
Read ID4	1	1	1	XX	0	0	0	0	0	0	0	0	00
	1	1	1	XX	1	0	0	1	0	0	1	1	93
	1	1	1	XX	0	1	0	0	0	0	0	1	41
	0	1	1	XX	1	1	1	0	0	0	0	0	E0h
	1	1	1	XX	Х	Χ	Χ	Χ		VP	0 [3:0]		08
	1	1	1	XX	Х	Х			VP1 [5	:0]			0E
	1	1	1	XX	Х	Х			VP2 [5	:0]			12
	1	1	1	XX	Х	X	X	Χ		VP	4 [3:0]		05
	1	1	1	XX	Х	Χ	Χ		V	P6 [4	:0]		03
	1	1	1	XX	Х	X	Χ	Χ		VP1	13 [3:0]		09
Positive Gamma	1	1	1	XX	Х			VI	P20 [6:0]				47
Correction	1	1	1	XX		VP36	[3:0]			VP2	27 [3:0]		86
	1	1	1	XX	X			VI	P43 [6:0]				2B
	1	1	↑	XX	Х	Χ	X	Χ		VP	50 [3:0]		0B
	1	1	1	XX	Х	Χ	Χ		VF	P57 [4	1:0]		04
	1	1	1	XX	Х	Χ	Χ	Χ		VPS	59 [3:0]		00
	1	1	1	XX	X	Χ			VP61 [5	5:0]			00
	1	1	1	XX	X	X			VP62 [5	5:0]			00
	1	1	↑	XX	Х	Χ	Χ	Χ		VP6	3 [3:0]	_	00
	0	1	1	XX	1	1	1	0	0	0	0	1	E1h
	1	1	1	XX	X	Χ	Χ	Χ		VN	0 [3:0]		08
	1	1	↑	XX	Χ	Χ			VN1 [5	:0]			1A
	1	1	↑	XX	Χ	Χ			VN2 [5	:0]			20
	1	1	1	XX	Χ	Χ	Χ	Χ		VN	4 [3:0]		07
	1	1	↑	XX	Χ	Χ	Χ		V	N6 [4	:0]		0E
	1	1	1	XX	X	X	Χ	Χ		VN1	13 [3:0]		05
Negative Gamma	1	1	1	XX	X			1V	N20 [6:0]				3A
Correction	1	1	↑	XX		VN36	[3:0]			VN2	27 [3:0]		8A
	1	1	1	XX	X			1V	N43 [6:0]				40
	1	1	↑	XX	Х	Χ	X	Χ		VNS	50 [3:0]		04
	1	1	↑	XX	Χ	Χ	Χ		1V	N57 [4	1:0]		18
	1	1	↑	XX	Х	Х	Х	Χ		VNS	59 [3:0]		0F
	1	1	↑	XX	Χ	Χ			VN61 [5:0]			3F
	1	1	↑	XX	Х	Χ			VN62 [5:0]			3F
	1	1	↑	XX	Х	Х	Х	Χ		VN6	33 [3:0]		0F
Digital Gamma Control 1	0	1	↑	XX	1	1	1	0	0	0	1	0	E2h
1 st Parameter	1	1	<u></u>	XX		RCA0	[3:0]			BCA	A0 [3:0]		XX
:	1	1	1	XX		RCAx	[3:0]			BCA	Ax [3:0]		XX
16 th Parameter	1	1	↑	XX		RCA15					15 [3:0]		XX
Digital Gamma Control 2	0	1	↑	XX	1	1	1	0	0	0	1	1	E3h
1 st Parameter	1	1	↑	XX		RFA0	[3:0]			BF/	0:6]		XX
:	1	1	<u></u>	XX		RFAx	[3:0]				Ax [3:0]		XX
64 th Parameter	1	1		XX		RFA63	[3:0]				63 [3:0]		XX
	0	1		XX	1	1	1	1	0	1	1	0	F6h
late (O : 1	1	1	1	XX	MY_EOR	MX_EOR	MV_EOR	Х	BGR_EOR	Χ	Х	WEMODE	01
Interface Control	1	1	1	XX	X	X	EPF [X	Χ		T [1:0]	00
	1	1	1	XX	Х	Х	ENDIAN	X	DM [1:		RM	RIM	00
	<u> </u>												

Note 1: Undefined commands are treated as NOP (00h) command.

Note 2: B0 to D9 and DE to FF are for factory use of display supplier. USER can decide if these commands are available or they are treated as NOP (00h) commands before shipping to USER. Default value is NOP





(00h).

Note 3: Commands 10h, 12h, 13h, 26h, 28h, 29h, 30h, 36h (Bit B4 only), 38h and 39h are updated during V-SYNC when ILI9341 is in Sleep OUT mode to avoid abnormal visual effects. During Sleep IN mode, these commands are updated immediately. Read status (09h), Read display power mode (0Ah), Read display MADCTL (0Bh), Read display pixel format (0Ch), Read display image mode (0Dh), Read display signal mode (0Eh) and Read display self diagnostic result (0Fh) of these commands are updated immediately both in Sleep IN mode and Sleep OUT mode.







8.2. Description of Level 1 Command

8.2.1. NOP (00h)

00h					NOP (No	Opera	ation)								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	↑	XX	0	0	0	0	0	0	0	0	00h		
Parameter					No Pa	aramete	er.								
				nmand; it does not ha	,			•					erminate		
Description	Frame Me	emory Writ	e or Read a	as described in RAM	WR (Men	nory W	rite) and	RAMRI	O (Memo	ory Read	d) Comm	ands.			
	X = Don't	care.													
Restriction	None	one													
		Status Availability													
		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes													
Register				Normal Mode On	·		- '		Yes	-					
Availability				Partial Mode On,					Yes						
Availability				Partial Mode On,					Yes						
					Sleep In	5 5, 5	лоор ос		Yes						
					'										
					Status		Default '	مبراد/							
					On Seque		N/A								
Default					V Reset		N/A								
					V Reset		N/A								
Flow Chart	None														





8.2.2. Software Reset (01h)

01h					SV	/RESET	•								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	↑	XX	0	0	0	0	0	0	0	1	01h		
Parameter					No F	aramete	er.								
Description				mand is written, it c					s the co	mmands	s and pa	ırameter	s to the		
Description	Note: The		emory conte	ents are unaffected b	y this co	ommand									
Restriction	supplier fa	actory defa	ult values to	ec before sending ne o the registers during ore sending Sleep o	this 5m	sec. If S	oftware	Reset is	applied	l during	Sleep O	ut mode	, it will b		
					Status			Ava	ailability	1					
				Normal Mode On,		de Off, S	Sleep O		Yes						
Register				Normal Mode On,					Yes						
Availability				Partial Mode On,	Idle Mo	de Off, S	Sleep Ou	ut	Yes						
,				Partial Mode On,	Idle Mo	de On, S	Sleep Ou	ıt	Yes						
					Sleep In				Yes						
Default		Status Default Value Power On Sequence N/A SW Reset N/A HW Reset N/A													
Flow Chart			Disj	SWRESET(01h) Set Commands to S/W Default Values Sleep In Mode	een			Cool Part D	mmand rameter risplay action Mode						





8.2.3. Read display identification information (04h)

04h				RDDIDIF (Re	ad Disp	lay Ider	ntificatio	n Inforr	nation)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	↑	XX	0	0	0	0	0	1	0	0	04h		
1 st Parameter	1	1	1	XX	Χ	Χ	Х	Χ	Χ	Χ	Χ	Χ	Х		
2 nd Parameter	1	1	1	XX				ID1	[7:0]				XX		
3 rd Parameter	1	1	1	XX				ID2	[7:0]				XX		
4 th Parameter	1	1	1	XX				ID3	[7:0]				XX		
Description	The 1 st The 2 nd The 3 rd	paramete paramete paramete	r is dumm er (ID1 [7:0 r (ID2 [7:0	its display identificati y data.)]): LCD module's ma]): LCD module/drive]): LCD module/drive	anufactur er versior	er ID.									
Restriction															
Register Availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes													
Default					Status On Seq SW Rese	et	See de		1						
Flow Chart	SW Reset See description HW Reset See description RDDIDIF(04h) Host Driver Display 1st Parameter: Dummy Read 2nd Parameter: Send LCD module's manufacturer information 3rd Parameter: Send panel type and LCM/driver version information 4th Parameter: Send module/driver information Sequential transfer Sequential transfer														



Description

a-Si TFT LCD Single Chip Driver 240RGBx320 Resolution and 262K color



8.2.4. Read Display Status (09h)

09h				RDI	OST (Re	ad Disp	lay Stat	us)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
1 st Parameter	1	↑	1	XX	Χ	Х	Х	Х	Х	Х	Х	Х	Χ
2 nd Parameter	1	↑	1	XX				D [31:25]			0	00
3 rd Parameter	1	↑	1	XX	0	I	D [22:20]		D [1	9:16]		61
4 th Parameter	1	↑	1	XX	0 0 0			0	0		D [10:8]		00
5 th Parameter	1	↑	1	XX		D [7:5]		0	0	0	0	0	00

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Status
D04	Deceley well and other	0	Booster OFF
D31	Booster voltage status	1	Booster ON
Doo	Danie addieses and an	0	Top to Bottom (When MADCTL B7='0')
D30	Row address order	1	Bottom to Top (When MADCTL B7='1')
Doo	Only many or deliver a constant	0	Left to Right (When MADCTL B6='0').
D29	Column address order	1	Right to Left (When MADCTL B6='1').
Doo	Davids I was a such a suc	0	Normal Mode (When MADCTL B5='0').
D28	Row/column exchange	1	Reverse Mode (When MADCTL B5='1').
D07	Mautical vaturals	0	LCD Refresh Top to Bottom (When MADCTL B4='0')
D27	Vertical refresh	1	LCD Refresh Bottom to Top (When MADCTL B4='1').
Doc	DCD/DCD and an	0	RGB (When MADCTL B3='0')
D26	RGB/BGR order	1	BGR (When MADCTL B3='1')
Doc	Hard-antal refusals and a	0	LCD Refresh Left to Right (When MADCTL B2='0')
D25	Horizontal refresh order	1	LCD Refresh Right to Left (When MADCTL B2='1')
D24	Not used	0	
D23	Not used	0	
D22		101	4.C. hit/nival
D01	Interface color pixel format	101	16-bit/pixel
D21	definition	110	10 hit/nivol
D20		110	18-bit/pixel
D19	Idle mode ON/OFF	0	Idle Mode OFF
סוט	Idle IIIode ON/OFF	1	Idle Mode ON
D18	Partial mode ON/OFF	0	Partial Mode OFF
D10	Faitial Hidde ON/OFF	1	Partial Mode ON.
D17	Sleep IN/OUT	0	Sleep IN Mode
DIT	Зіеер іі (/ООТ	1	Sleep OUT Mode.
D16	Display permal made ON/OFF	0	Display Normal Mode OFF.
D10	Display normal mode ON/OFF	1	Display Normal Mode ON.
D15	Vertical scrolling status	0	Scroll OFF
D14	Not used	0	
D13	Inversion status	0	Not defined
D12	All pixel ON	0	Not defined
D11	All pixel OFF	0	Not defined
D10	Display ON/OFF	0	Display is OFF
טוט	Display Olivol I	1	Display is ON
D9	Tearing effect line ON/OFF	0	Tearing Effect Line OFF
פט	rearing enectime ON/OFF	1	Tearing Effect ON
		000	GC0
		001	
D[8:6]	Gamma curve selection	010	
		011	
		other	Not defined

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				0		Mode 1, V-BI	anking only
		D5	Tearing effect line mode	1	Mode		king and V-Blanking.
		D4	Not used	0			
		D3	Not used	0			
		D2	Not used	0			-
		D1	Not used	0			-
		D0	Not used	0			-
	X = Don	't care					
Restriction							
				Status		Availability	
			Normal Mode On		Off. Sleep Out	Yes	
Register			Normal Mode On			Yes	
Availability			Partial Mode On,			Yes	
			Partial Mode On,	Idle Mode C	n, Sleep Out	Yes	
				Sleep In		Yes	
			Sta	atus	Default Va	lue	
Default			Power Or	Sequence	32'h006100	00h	
				Reset	32'h006100		
			HW	Reset	32'h006100	00h	
							Li
							Legend
			RDDST(09	9h)			Command
					Host		Parameter
					Driver		
Flow Chart	_	1	st Parameter: Dummy Read		Dilvei		Display
		2	and Parameter: Send D[31:25] display and Parameter: Send D[19:16] display			/	Action
		4	th Parameter: Send D[10:8] display s	tatus			Mode
		5	th Parameter: Send D[7:5] display st	atus		/	
							Sequential transfer





8.2.5. Read Display Power Mode (0Ah)

0Ah		<u> </u>			· ·	M (Read	Display	/ Power	Mode)				
6 7	DICY	DDV	WRX	l	D17-8		1 -			1	Do	D1	D0	LIEV
Command	D/CX 0	RDX 1	WHA ↑		XX	D7 0	D6 0	D5 0	D4 0	D3 1	D2 0	D1 1	D0 0	HEX 0Ah
1 st Parameter	1	<u>'</u>	1		XX	X	X	X	X	X	X	X	X	X
2 nd Parameter	1	<u> </u>	1		XX	D7	D6	D5	D4	D3	D2	D1	D0	08
	This co	mmand inc		current	status of the								_	
			Г	Bit	Value		escriptio			Commer	nt			
						Booster	•		t.					
				D7		Booster C								
			Ī	DC	0		e Mode (
				D6	1	Idle	e Mode (On.						
				D5	0	Part	ial Mode	Off.						
			-		1		ial Mode							
Description				D4	0		ep In Mo							
			-		0	Slee Display I	ep Out M		,					
			-											
		D2 0 Display is Off 1 Display is On												
				D1	Set to '0	,								
		D1 Not Defined Set to '0 D0 Not Defined Set to '0												
	X = Dor	n't care	_											
Restriction														
ricstriction														
						Ctatur			Ι,					
				No	rmal Mode C	Status		Sloop (vailability Yes				
Register					rmal Mode C					Yes	+			
Availability					artial Mode O					Yes				
rivaliability					artial Mode O					Yes				
						Sleep I	ln			Yes				
					-	Status		Defaul						
Default						r On Seq SW Rese		8'h		_				
						HW Rese		8'h		-				
						111 11000	,,	011	3011					
				· <u> </u>			7				٦		egend	
					RDDPM((0Ah)								一 !
				L	· · · · · · · · · · · · · · · · · · ·	·- /					-		ommand	<u></u>
							H	ost 			_ !	P	arameter	_/ ¦
Flow Chart							Dı	river			!		Display	
r iow chart			1 at D		mv Da								Action	> !
			1st Paramete 2nd Paramet		my Read d D[7:2] display	power mo	de status			/	/		Mode	<u> </u>
	<u> </u>									/	į		wiode	
											į	Seque	ential trans	sfer
											i i_			
	<u> </u>													





8.2.6. Read Display MADCTL (0Bh)

8.2.6. Rea		Piay IV	ADOII		ADOT! "	Deci Di		ADOT!	,						
0Bh					ADCTL (I	Т			1						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	XX	0	0	0	0	1	0	1	1	0Bh		
1 st Parameter	1	1	1	XX	X	X	X	X	X	X	X	X	Х		
2 nd Parameter	1	<u> </u>	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	00		
	This co	mmand inc	licates the	current status of the	display	as desci	ribed in	the table	e below:						
			Bit V	alue	I	Descripti	ion			Comi	ment				
			D7 -	0 Top to	Bottom	(When I	MADCTI	L B7='0')).		-				
			J ,		n to Top).						
			D6 -		to Right (-				
					t to Left (-				
			D5 -		al Mode										
Description					se Mode										
Description			D4	0 LCD Refresh1 LCD Refresh											
					RGB (Wh				D4= 1).						
			D3		GR (Who										
			D2												
			D1	RAM	Set t	o '0'									
			D0	Set t	o '0'										
	X = Dor	D0 Switching between Segment outputs and RAM Set to X = Don't care													
Restriction															
riestriction															
					01-1				9 - 1. 996						
				Normal Mada C	Status		Clean		vailability						
Register				Normal Mode C					Yes Yes	-					
Avoilobility				Partial Mode C					Yes						
Availability				Partial Mode C					Yes						
				T dittal Mode C	Sleep l		Cicop C) ut	Yes						
					<u> </u>			ı							
									-						
					Status		Defaul	t Value							
Default				Powe	r On Seq	uence	8'h	00h							
					SW Rese			hange							
					HW Rese	et	8'h	00h							
						7				Г	 -		;		
											L	_egend	_ !		
				RDDMADC	TL(0Bh)							Command	_		
						_ 	lost			 		Parameter	-		
							 river			- ¦			=		
Flow Chart	_			▼						$\neg \vdots$		Display	\rightarrow !		
	/			er: Dummy Read						/ !	<_	Action	$>$ \mid		
			2nd Parame	ter: Send D[7:2] display	power mo	de status			/	/ !		Mode	$\supset \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$		
									/						
										 	Sequ	ential trans	sfer		
										<u> </u>			=		





8.2.7. Read Display Pixel Format (0Ch)

		piay		<u> </u>	<u> </u>	PDDCO	LMOD /	Dood Di	onlo	v Dis	ral E	'o uma	a#\				
0Ch		ı				RDDCO	1	1	1						I	l	I
	D/CX	RDX	W	/RX		D17-8	D7	D6	D:		D4	_	D3	D2	D1	D0	HEX
Command	0	1		1		XX	0	0	0		0	-	1	1	0	0	0Ch
1 st Parameter	1	1		1		XX	X	Х	X		Х		X	Х	X	Х	X
2 nd Parameter	1	1		1 .		XX	RIM		<u>DPI </u>				0		DBI [2:0]		06
	This co	mmano r	indica			urrent status of th	ne dispia	y as des	cribe								
			RIM		PI [2:			ormat		DI	BI [2		MCL		ce Forma	at	
		-	0	0	0		eserved		4	0	0	0		Reser		_	
		-	0	0	0		eserved		_	0	0	1		Reser			
		ŀ	0	0	1		eserved		-	0	1	0		Reser			
		ŀ	0	1	0		eserved eserved		-	1	0	0		Reser			
Description		-	0	1	0		oits / pixe	اد	1	1	0	1		16 bits /			
·		-	0	1	1		oits / pixe			1	1	0		18 bits /			
		Ī	0	1	1		eserved			1	1	1		Reser			
			-	4	^	16 k	oits / pixe	el								<u></u>	
			1	1	0	1 (6-bit 3 tim											
			1	1	1	()	oits / pixe										
		L				(6-bit 3 tim	es data	transfer)									
	X = Doi	X = Don't care															
Restriction																	
		<u> </u>															
							Stat	us				A۱	/ailabilit	.y			
						Normal Mode	On, Idle	Mode O	ff, SI	еер	Out		Yes				
Register						Normal Mode	On, Idle	Mode O	n, SI	еер	Out		Yes				
Availability						Partial Mode (On, Idle	Mode Of	ff, Sle	ер (Out		Yes				
						Partial Mode (n, Sle	еер (Out	-	Yes				
							Slee	o In					Yes				
						Ctatus			D	efau	lt Va	lue					
						Status		RIM		DP	I [2:0)]	DB	I [2:0]			
Default				-	Pov	er On Sequence		1'b0		3't	000		3'l	b110			
				=		SW Reset	+	Chang		No (Chang			
				<u>_</u>		HW Reset		1'b0		3't	0000		3'l	b110			
								7						·		egenc	
														į	L	-cyciic	<u> </u>
						RDDCOLN	MOD(0Ch)							į		Command	
									Hos	t				į	F	Parameter	-7
							 ,		– – - Drive	– – – er				i		Display	= $ $
Flow Chart	_					· · · · · · · · · · · · · · · · · · ·	<u> </u>							─7			\prec \sqcup
			1st	Para	mete	: Dummy Read r: Send D[7:2] displa	u nival far	mat atatu	_					/ i	\leq	Action	<u> </u>
	/		2n	u rari	amete	i. פווט טן ו.צן aispia	y pixel 101	ıııaı Statüs	5				/	/ į		Mode	
													/	į			-
														į	Sequ	ential tran	ster
														<u>i.</u>			





8.2.8. Read Display Image Format (0Dh)

0Dh					RDD	IM (Read	d Displa	y Image	Mode)					
	D/CX	RDX	WRX	D1	7-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	>	Χ	0	0	0	0	1	1	0	1	0Dh
1 st Parameter	1	1	1	>	X	Х	Χ	Χ	Χ	Х	Χ	Χ	Χ	Χ
2 nd Parameter	1	1	1	>	ΧX	0	0	0	0	0		D [2:0]		00
Description	This cor		dicates the	e current s	D [2 00 00 01 01 Oth	2:0] 00 11 0	Gamr	Descripent of the control of the con	tion e 1 (G2.2					
Restriction														
Register Availability				Norn Part	nal Mode (nal Mode (ial Mode C ial Mode C	On, Idle I On, Idle I	Mode Of Mode Or Mode Off Mode Or	n, Sleep , Sleep (Out Out Out	vailability Yes Yes Yes Yes Yes Yes Yes	/			
Default					Power On SW I	atus Sequen Reset Reset	ice	3'b 3'b	lt Value 0000 0000 0000					
Flow Chart				eter: Dummy eter: Send [RDDIM]	Host Driver		/		P	Command Carameter Display Action Mode	





8.2.9. Read Display Signal Mode (0Eh)

0Eh				·	RDDSM (Read Disp	lay Sign	al Mode	<u>:</u>)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	0	0	1	1	1	0	0Eh
1 st Parameter	1	1	1	XX	Х	Х	Х	Χ	Х	Χ	Х	Х	Х
2 nd Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	00
Description				Bit Va D7 C C C C C C C C C	us of the dis ue Tearir Tearir Tearir Tearir Horizo Vertic Vertic Pixel o Data e Data e Reser	g effect ling ling effect ling effect ling effect ling effect ling ling effect	pescribed in Descript e OFF e ON e mode 1 e mode 2 (RGB int (RGB int GB interf GB interf GB interf GLK, RG CLK, RG , RGB int	the tablicant th	DFF DN F ace) OFF	:	,		
Restriction	X = Bont out												
Register Availability	Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes												
Default					Power Or SW	atus Sequence Reset Reset	e 8'	ult Value h00h h00h h00h	9				
Flow Chart				meter: Dummy R meter: Send D[7		al mode stat	Host Driver					Command Parameter Display Action Mode	





8.2.10. Read Display Self-Diagnostic Result (0Fh)

0Fh				RDDSD	R (Read D		-	gnostic	Result)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh
1 st Parameter	1	↑	1	XX	Х	Χ	Χ	Х	Х	Χ	Х	Х	Х
2 nd Parameter	1	1	1	XX	D7	D6	0	0	0	0	0	0	00
	Bit		Descript						ction				
	D7		ter Loading		Invert the					•	operly.		
	D6	Fur	nctionality E		Invert the	e D6 bit	if the dis	splay is f		lity			
Description	D5		Not Use						'0'				
Description	D4		Not Use						'0'				
	D3		Not Use						ʻ0'				
	D2		Not Use						ʻ0'				
	<u>D1</u>		Not Use						'0'				
	D0		Not Use	eu					U				
Restriction													
					Sta	tus			Availabil	itv			
				Normal Mod			Off. Slee		Yes	ity .			
Register				Normal Mod					Yes				
Availability				Partial Mod					Yes				
,				Partial Mod	e On, Idle	Mode C	n, Sleep	Out	Yes				
					Slee	p In			Yes				
					Statu	IS	Defa	ault Valu	е				
Default				Po	ower On S	equence	9 8	3'h00h					
20.00.1					SW Re	eset	8	3'h00h					
					HW Re	eset	8	3'h00h					
						<u> </u>						Legeno	₁
				RDD	SDR(0Fh)								\neg \Box
							Host			į		Command	<u> </u>
										İ		Parameter	=
Flow Chart							Driver			İ		Display	_)
		1:	st Parameter:	Dummy Read						/ ¦		Action	$> \mid \mid$
		21	nd Parameter	: Send D[7:6] dis	splay self-dia	gnostic st	atus					Mode	$\supset \Box$
											Seq	uential trar	nsfer





8.2.11. Enter Sleep Mode (10h)

Command 0 1 1 XX 0 0 0 1 1 0 0 0 0 1 100 Parameter This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DCD converter is stopped, Internal oscillator is stopped, and panel scanning is stopped. Description MCU interface and memory are still working and the memory keeps its contents. X = Don't care This command has no effect when module is already in sleep in mode. Sleep in Mode can only be left by the Sleep O Command (111h). It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep in Mode) before Sleep in command can be sent. Register Availability Register Availability Default Default Default Default This command be sent. Status Availability Normal Mode On, Idle Mode Off, Sleep Out Tyes Partial Mode On, Idle Mode Off, Sleep Out Tyes Partial Mode On, Idle Mode Off, Sleep Out Tyes Partial Mode On, Idle Mode Off, Sleep Out Tyes Partial Mode On, Idle Mode Off, Sleep Out Tyes Partial Mode On, Idle Mode Off, Sleep Out Tyes Partial Mode On, Idle Mode Off, Sleep Out Tyes Partial Mode On, Idle Mode Off, Sleep Out Tyes Power On Sequence Sleep In Mode HW Reset Sleep In Mode It takes 120msec to get into Sleep In mode after SLPIN command issued. Legend Command Flow Chart Flow	10h			oue (10	/	SPLIN	(Enter S	Sleep Mo	ode)					
Default Parameter	1011	D/CY	BDX	WRY	D17-8	ı	ì	1	1	D3	D2	D1	DO	HEY
Parameter This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/D converter is stopped, Internal oscillator is stopped, and panel scanning is stopped. MCU interface and memory are still working and the memory keeps its contents. X = Don't care This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep O Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supp voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleet In Mode) before Sleep in command can be sent. Registor Availability Registor Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Sleep in Mode Status Default Valve Power On Sequence Sleep IN Mode Sty Reset Sleep IN Mode It takes 120msec to get into Sleep In mode after SLPIN command issued. Legend Command Parameter Display whole blank screen (Automatic No effect to DISP ONOFF commands) Step DC/DC Stop Internal Cocillator Step In Mode	Command			↑ ↑										
Converter is stopped, Internal oscillator is stopped, and panel scanning is stopped. MCU interface and memory are still working and the memory keeps its contents. X = Don't care This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep O Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supprotate of the supprotation of the supprotation of the supprotation in Mode) before Sleep In command can be sent. Register Register Availability Register Availability Default Default Default It takes 120msec to get into Sleep In mode after SLPIN command issued. Legend Status Default Value Power On Sequence Sleep In Mode SW Reset Sleep In Mode SW Reset Sleep In Mode It takes 120msec to get into Sleep In mode after SLPIN command issued. Legend Command Parameter Display whole blank screen (Automatic No effect to DISP ONOFF commands) Sleep In Mode		-		l l			No Para							
Description MCU interface and memory are still working and the memory keeps its contents. X = Don't care This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep O Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supp voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleet in Mode) before Sleep In command can be sent. Status		This comn	nand cause	es the LCD	module to e	nter the	minimur	n power	consur	nption me	ode. In t	this mod	le e.g. th	e DC/DC
MCU interface and memory are still working and the memory keeps its contents. X = Don't care This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep O Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supprotein voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleet In Mode) before Sleep In command can be sent. Status		converter i	s stopped,	Internal osci	llator is stopp	ed, and	panel sc	anning is	stoppe	d.				
This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep O Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supproblems of	Description													
This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep O Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supp voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Slee In Mode) before Sleep In command can be sent. Status		MCU interf	face and m	emory are st	ill working an	d the me	emory ke	eps its co	ontents.					
Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supprovoltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleet In Mode) before Sleep In command can be sent. Status		X = Don't o	care											
Voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Slee In Mode) before Sleep In command can be sent. Status		This comm	nand has n	o effect whe	en module is	already	in sleep	in mode	e. Sleep	In Mode	can onl	y be left	by the S	Sleep Out
In Mode) before Sleep In command can be sent. Status	Restriction	Command	(11h). It w	vill be neces	sary to wait	5msec b	efore se	nding ne	ext to co	ommand,	this is to	allow t	ime for th	ne supply
Register Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence Sleep IN Mode SW Reset Sleep IN Mode HW Reset Sleep IN Mode HW Reset Sleep IN Mode It takes 120msec to get into Sleep In mode after SLPIN command issued. Legend Command Parameter Display whole blank screen (Automatic No effect to DISP ON/OFF commands) Stop Internal Cociliator Sequential transfer		voltages a	nd clock cir	cuits to stab	lize. It will be	necessa	ary to wa	t 120ms	ec after	sending S	Sleep Ou	ıt comma	and (wher	in Sleep
Normal Mode On, Idle Mode Off, Sleep Out		In Mode) b	efore Sleep	o In commar	id can be sen	ıt.								
Normal Mode On, Idle Mode On, Sleep Out						Sta	atus			Availabili	ty			
Availability Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Sleep In Yes Sleep In Yes Sleep In Mode Status Default Value Power On Sequence Sleep IN Mode SW Reset Sleep IN Mode HW Reset Sleep IN Mode HW Reset Sleep IN Mode It takes 120msec to get into Sleep In mode after SLPIN command issued. Legend Command Parameter Display whole blank screen (Automatic No effect to DISP ON/OFF commands) Stop Internal Oscillator Step In Mode Step In Mode Stop Internal Oscillator Step In Mode	Dogiator				Normal Mode	e On, Idle	e Mode C	Off, Sleep	Out	Yes				
Default Def	Register													
Sleep In Yes Status Default Value Power On Sequence Sleep IN Mode SW Reset Sleep IN Mode HW Reset Sleep IN Mode HW Reset Sleep IN Mode SPLIN (10h) Stop DC/DC Converter Display Adion Adion Mode Stop Internal Cscillator Sequential transfer Seque	Availability													
Default Status Default Value Power On Sequence Sleep IN Mode SW Reset Sleep IN Mode HW Reset Sleep IN Mode HW Reset Sleep IN Mode SPLIN (10h) Stop DC/DC Command Parameter Display Action Mode Stop Internal Command Sequential transfer Sequential					Partial Mode			n, Sleep	Out					
Power On Sequence Sleep IN Mode SW Reset Sleep IN Mode HW Reset Sleep IN Mode HW Reset Sleep IN Mode It takes 120msec to get into Sleep In mode after SLPIN command issued. Legend Command Parameter Display Action Stop DC/DC Converter Display Action Mode Stop Internal Oscillator Sequential transfer						2166	ер ш			res				
SW Reset Sleep IN Mode HW Reset Sleep IN Mode It takes 120msec to get into Sleep In mode after SLPIN command issued. Legend Command Parameter Display whole blank screen (Automatic No effect to DISP ON/OFF commands) Stop Internal Oscillator Sequential transfer Sleep In Mode Stop Internal Oscillator						Statu	IS	Defa	ult Valu	е				
SW Reset Sleep IN Mode HW Reset Sleep IN Mode It takes 120msec to get into Sleep In mode after SLPIN command issued. Legend Command Splin (10h) Stop DC/DC Converter Display Action Mode Stop Internal Oscillator Drain charge from LCD Sleep In Mode Sleep In Mode	Default				Pow	ver On S	equence	Sleep	IN Mod	de				
Flow Chart It takes 120msec to get into Sleep In mode after SLPIN command issued. Legend Command Parameter Display Action Stop DC/DC Converter Display Action Stop Internal Oscillator Sequential transfer	Delault					SW Re	eset	Sleep	IN Mod	de				
Flow Chart SPLIN (10h) Stop DC/DC Command						HW Re	eset	Sleep	IN Mod	de				
SPLIN (10h) Stop DC/DC Converter Display Action Mode Stop Internal Oscillator Stop Internal Oscillator Sequential transfer		It takes 12	0msec to g	et into Sleep	In mode afte	er SLPIN	commar	nd issued	i.					
Flow Chart Display whole blank screen (Automatic No effect to DISP ON/OFF commands) Drain charge from LCD Stop DC/DC Converter Display Action Stop Internal Oscillator Sequential transfer											Γ.	_L	egend	
Flow Chart Display whole blank screen (Automatic No effect to DISP ON/OFF commands) Stop DC/DC Converter Display Action Mode Stop Internal Oscillator Sequential transfer							▼							一 !
Flow Chart Display whole blank screen (Automatic No effect to DISP ON/OFF commands) Drain charge from LCD Stop Internal Oscillator Sleep In Mode Sleep In Mode											į	С	ommand	
Flow Chart Display Action Mode Stop Internal Oscillator Drain charge from LCD Sleep In Mode Sleep In Mode			SPLIN (10	h)							į	P	arameter	7
Flow Chart Display whole blank screen (Automatic No effect to DISP ON/OFF commands) Stop Internal Oscillator Sequential transfer Sequential transfer							onverter				l I		Dioploy	≓ į
Flow Chart Display whole blank screen (Automatic No effect to DISP ON/OFF commands) Stop Internal Oscillator Sequential transfer Sequential transfer			\downarrow			\		_/			ļ		Display	_/
Flow Chart (Automatic No effect to DISP ON/OFF commands) Stop Internal Oscillator Sequential transfer Drain charge from LCD Sleep In Mode											į		Action	> ¦
ON/OFF commands) Stop Internal Oscillator Sequential transfer Sequential transfer Sleep In Mode	Flow Chart				\			\neg			ļ		Mode	\neg :
Drain charge from LCD Sleep In Mode	1 low onart)	Sto	n Interna	. \			 			~/ į
Drain charge from LCD Sleep In Mode						("	Oscillator	. >			ĺ	Segue	ential trans	fer
from LCD \ (Sleep In Mode)		,									į	-		<u> </u>
from LCD \ (Sleep In Mode)								_			'			نـــــ
from LCD \ (Sleep In Mode)		/					▼	_						
						Slee	ep In Mod	le)						
panel				/				_/						
		\		/										

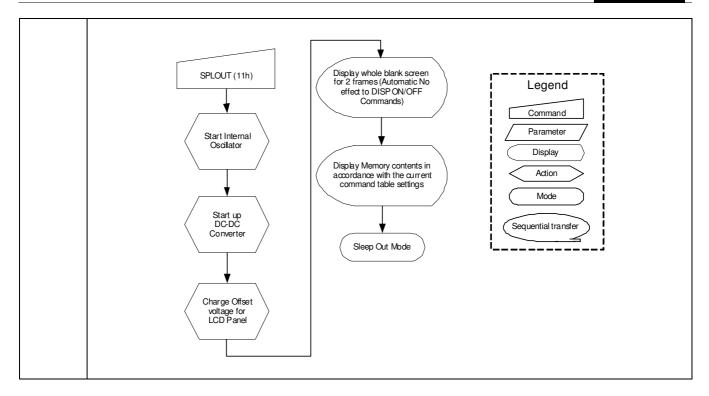




8.2.12. Sleep Out (11h)

11h					SLF	POUT (S	eep Out	:)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Parameter						No Para	meter						
Description		de e.g. the I	off sleep mo	de. erter is enabl	ed, Inter	nal oscill	ator is st	arted, a	nd panel :	scanning	j is starte	ed.	
Restriction	Command and clock 5msec and when this functions of	(10h). It wi circuits stal d there can load is done during this 5	Il be necessibilize. The donot be any as and when the and the	en module is ary to wait 5m lisplay module abnormal visuthe display m be necessare sent.	nsec before loads a	ore sendiall displation the called	ng next o y supplie display ir Gleep Ou	commarer's factor mage if t -mode	d, this is ory defau factory de . The dis	to allow to	time for t to the re d registe	he supply egisters of r values bing self-o	voltages luring this are same
Register Availability				Normal Mode Normal Mode Partial Mode Partial Mode	e On, Idle e On, Idle e On, Idle e On, Idle	Mode C	on, Sleep	Out Out Out	Availabili Yes Yes Yes Yes Yes	ty			
Default				Pov	Statu ver On S SW Re HW Re	equence set	Sleep	ult Valu IN Mod IN Mod IN Mod	le le				
Flow Chart	It takes 12	0msec to b	ecome Slee	p Out mode a	after SLP	OUT cor	nmand is	ssued.					









8.2.13. Partial Mode ON (12h)

12h					PTLOI	N (Partia	l Mode	On)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	XX	0	0	0	1	0	0	1	0	12h	
Parameter						No Para	meter							
Description		de, the Nor		node The part					the Part	ial Area	commar	id (30H).	To leave	
Restriction	This comm	This command has no effect when Partial mode is active.												
			[Sta	tus			Availabili	ty				
Dogiator				Normal Mode					Yes					
Register				Normal Mode					Yes					
Availability				Partial Mode					Yes					
				Partial Mode	On, Idle	Mode C	n, Sleep	Out	Yes					
•					Slee	p In			Yes					
Default				Power Or	tatus n Sequer Reset Reset	No	Defa ormal Dis ormal Dis	splay Mo	de ON de ON					
Flow Chart	See Partia	l Area (30h)											





8.2.14. Normal Display Mode ON (13h)

13h				NORON	(Norm	al Displa	ay Mode	e On)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
Parameter					No F	Paramete	er						
Description	Normal di	splay mode	e on means	ay to normal mode. Partial mode off. mode On command	l (12h)								
Restriction	This com	This command has no effect when Normal Display mode is active.											
Register Availability				Normal Mode On, Normal Mode On, Partial Mode On, Partial Mode On,	Idle Mo	de On, S de Off, S de On, S	Sleep Ou Sleep Ou	ut ut it	Yes Yes Yes Yes Yes Yes				
Default				Status Power On Sec SW Rese	et	Norma Norma	Default ' al Displa al Displa al Displa	y Mode y Mode	ON				
Flow Chart	See Partia	al Area (30	h)										





8.2.15. Display Inversion OFF (20h)

0.2.15.		y	110101	JII OFF (20									
20h					DIN	OFF (Dis	play Inve	rsion OF	F)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	0	0	0	0	0	20h
Parameter							Paramete	r					
	This co	ommand	is used t	o recover from o	display inv	ersion mo	de.						
	This co	ommand	makes n	o change of the	content c	of frame m	emory.						
	This co	mmand	doesn't d	change any othe	er status.								
				Mem	nory				Display I	Panel			
					+++	+		-		++++	_		
Description											_		
						$+$ \vdash	_/\	-			_		
							$\neg \checkmark$				_		
						+		-			_		
						1				1 1 1 1			
	X = Do	n't care											
Restriction	This co	ommand	has no e	ffect when mod	ule alread	y is invers	ion OFF r	mode.					
						Status			Availab	ility			
Register						n, Idle Mo			Yes				
						on, Idle Mo			Yes				
Availability						n, Idle Mo n, Idle Mo			Yes Yes				
				- Cartie		Sleep Ir		oop out	Yes				
				-		atus		efault Va ay Inversi					
Default						Sequence Reset		ay Inversi					
						Reset		ay Inversi					
							ľ						
				Display In	vorsion O	n Modo	\		Legen	d	i		
				Display III	version O	II WIOGE	ノi						
							ł		Comman	<u>a</u>	į		
					<u> </u>				Paramete	er /	i		
							į		Display		l I		
Flow Chart				IN/	/OFF(20h	1)				=	į		
							1		Action	_>	į		
					▼		į		Mode				
				Display In	version ∩	ff Mode	\				}		
							/ ¦	Sequ	ıential tra	nsfer			
							į			_	1		
							1_						





8.2.16. Display Inversion ON (21h)

21h				<u> </u>	_	VON (Dis	splay Inve	rsion Of	۷)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	0	0	0	0	1	21h
Parameter						No	Paramete	r					
Description	This co	ommano Display	d makes n d doesn't d v inversion	o enter into disposo change of the change any other mode, the Disposo	content o	f frame m	emory. Ev				rame men	nory to the	e display.
B		n't care											
Restriction	i nis co	mmanc	nas no e	effect when mode	ule alread	y is invers	sion UN m	oae.					
Register Availability				Norma Partia	al Mode C al Mode O	n, Idle Mo	ode Off, S ode On, S ode Off, SI ode On, SI	leep Out eep Out		i			
					Status		D	efault Va	alue				
Default				Powe	r On Sequ	uence		ay Invers					
Dorault					SW Reset			ay Invers					
				I	HW Reset		Displa	ay Invers	ion OFF				
Flow Chart				Display Inv	/ON(21h)			Sec	Comman Paramet Display Action Mode	er /			





8.2.17. Gamma Set (26h)

0.2.17.	Gaiiiiii	a Set (2	.011)										
26h					GAM	SET (Ga	mma S	et)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	0	0	1	1	0	26h
Parameter	1	1	1	XX					C [7:0]				01
	This comn	nand is use	d to select t	he desired G	amma cı	irve for th	ie currei	nt displ	ay. A max	imum of	4 fixed (gamma cı	urves can
	be selecte	d. The curv	e is selected	d by setting th	ne approp	oriate bit i	n the pa	ıramete	er as desci	ribed in tl	he Table	:	
				GC [7:	0]	Cur	ve Selec	cted					
				01h		Gamma	curve 1	(G2.2)				
Description				02h									
				04h 08h									
	Note: All o	ther values	are undefin										
			are andenn	ou.									
	X = Don't												
Restriction	Values of	GC [7:0] no	t shown in ta	able above ar	e invalid	and will r	not chan	ige the	current se	lected G	iamma c	urve until	valid
	value is re	ceived.											
			_										
			_			itus			Availabili	ty			
Register				Normal Mode					Yes				
Availability			_	Normal Mode Partial Mode					Yes Yes				
Availability				Partial Mode					Yes				
					Slee	ep In			Yes				
					Stat	10	Dofo	ult Valu	10				
5 ()				Po		Sequence		'h01h	<u> </u>				
Default					SW R			'h01h					
					HW R	eset	8	'h01h					
						7	ļ	 	Lege	end			
				GAMSET	(26h)		Ì	ĺ	9		1 7		
				GAIVIOL I	(201)		i	i r	Comm	and			
							1		Param	eter	- 7 !		
				▼			_				/ I		
Flow Chart			/ .	st Parameter	CC17·0	ı .			Displa	ay			
Flow Grian				St i ai airietei	. ao[<i>i</i> .o _.	/	ľ	¦ <	Actio	n	>		
		Δ	<u>'</u>			/	l l	 	N4		\ i		
				\downarrow			į		Mod	ie			
				▼			1		Sequential	transfer	\		
				New Gamma Loade					equential	u ansier	/ i		
							į	'					





8.2.18. Display OFF (28h)

0.2.10.	p	, <u>.</u>	11 (20	,		DIODO	F /D: :	OFF)					
28h		ı			T	DISPOF	T			T	T		T
0	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1 ↑	XX	0	0	1	0	1	0	0	0	28h
Parameter	This s		1:1	e antanimta DIC	PDL AV OF		Paramet			Гиана в M		مام مامام ما	بامرها امرا
		ommano nserted.	i is used t	o enter into DIS	SPLAY OF	·F mode. I	n this mo	ide, the out	tput from	Frame M	emory is o	disabled a	nd blank
			l makes n	o change of co	ntents of f	rame men	norv.						
				t change any ot			,						
				nal visible effect									
ı				Mei	mory				Display I	Panel			
Description						+	_	#			_ _ _		
											— —- —		
						+		#			<u> </u>		
	X = Do	n't care											
Restriction	This co	ommano	l has no e	effect when mod	lule is alre	ady in dis	play off n	node.					
						Status			Availab	oility			
				Norm	al Mode (On, Idle M	ode Off, S	Sleep Out	Yes	3			
Register								Sleep Out	Yes				
Availability						On, Idle Mo			Yes				
				Parti	al Mode C	On, Idle Mo		Sleep Out	Yes				
						Sleep I	n		Yes	<u> </u>			
						Status		Default Va	lue				
Default					Powe	er On Seq	uence	Display Ol	FF				
						SW Rese		Display Of					
						HW Rese	t	Display Ol	FF				
								<u> </u>	 Lege		- 7		
				Displa	ay On Mod	de		<u> </u>					
						/	/	¦	Comma		İ		
					▼			<u> </u>	Parame	=	İ		
Flow Chart				DISF	POFF (28h	1)			Display	=			
					<u> </u>				Action Mode		i i		
l				Displa	y Off Mod	de		Sea	uential tr				
						/	/				_		





8.2.19. Display ON (29h)

0.2.13.		· , ·	14 (23)	-,									
29h			1		T	DISPO	N (Display	(ON)		T			
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	0	1	0	0	1	29h
Parameter							Paramete						
	This co	ommano	l makes n	o recover from to change of corchange any other	ntents of f	rame men		from the	Frame Me	emory is e	nabled.		
				Memory					Disp	olay Par	nel		
			+	++++	+++	_		4	+	H	\coprod	_	
Description						- - - -						- - - - - -	
	X = Do	on't care						•	' '				
Restriction	This co	ommano	l has no e	ffect when mod	lule is alre	ady in dis	play on m	ode.					
Register Availability				Norm Partia	al Mode C al Mode C al Mode C al Mode C	On, Idle Mo	ode Off, S ode On, S ode Off, S ode On, S	leep Out	Availab Yes Yes Yes Yes	i			
Default						Status er On Sequ SW Rese HW Rese	uence I	Default Va Display O Display O Display O	FF FF				
Flow Chart				DI	SPON(29)	h)			Commander Parameter Display Action Mode				

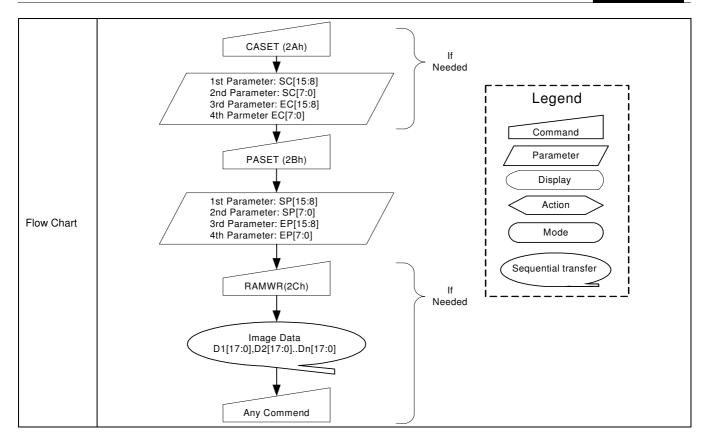




8.2.20. Column Address Set (2Ah)

		,	<u> 550</u>	S Set (ZAII)		SET (Oal	lum - A	ddras	. C	\					
2Ah						SET (Col	T			1					
	D/CX	RDX	WRX	D17-8	D7	D6	D5)4	D3	D2	D1	D0	HEX	
Command	0	1	<u> </u>	XX	0	0	1		0	1	0	1	0	2Ah	
1 st Parameter	1	1		XX	SC15	SC14	SC13		C12	SC11	SC10	SC9	SC8	Note1	
2 nd Parameter	1	1	<u> </u>	XX	SC7	SC6	SC5		C4	SC3	SC2	SC1	SC0		
3 rd Parameter	1	1	<u> </u>	XX	EC15	EC14	EC13		212	EC11	EC10	EC9	EC8	Note1	
4 th Parameter	1	1	<u> </u>	XX	EC7	EC6	EC5		C4	EC3	EC2	EC1	EC0		
Description	other o	driver sta	atus. Th	to define area of e values of SC line in the Frame	[15:0] a	nd EC [1:		e referr	ed w				_		
Restriction	SC [15	X = Don't care SC [15:0] always must be equal to or less than EC [15:0]. Note 1: When SC [15:0] or EC [15:0] is greater than 00EFh (When MADCTL's B5 = 0) or 013Fh													
	(When	MADCT	L's B5 =	= 1), data of out of	of range v	vill be ign	ored								
						Status				Availab	oility				
5				Norma	Mode C	n, Idle M	ode Off	, Sleep	Out	Yes	<u>. </u>				
Register				Norma	Mode C	n, Idle M	ode On	, Sleep	Out	Yes	<u>. </u>				
Availability				Partial	Mode O	n, Idle Mo	de Off,	Sleep	Out	Yes	;				
				Partial	Mode O	n, Idle Mo	de On,	Sleep	Out	Yes	;				
	Sleep In Yes														
				Status				Defa	ult \/o	due					
			Po	wer On Sequenc	e SCI	15:0]=000	00h	Deial		C [15:0]=0	00FFh				
Default			FO	SW Reset		15:0]=000	OOh II		CTL's	B5 = 0: E B5 = 1: E	C [15:0]=				
				HW Reset	901	15:0]=000		INIADO		C [15:0]=0		-013511			
			<u> </u>	TIVV NESEL	30	10.0]=000	1011		E	J [10.0]=€	VLI II				
	<u> </u>														





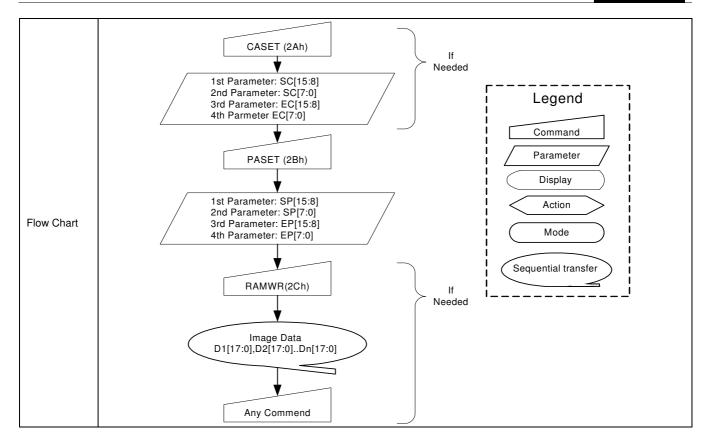




8.2.21. Page Address Set (2Bh)

	aye I	-uui c	,33 3	et (2Bn)									
2Bh					Р	ASET (Pa	age Add	ress Set)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	0	1	0	1	1	2Bh
1 st Parameter	1	1	1	XX	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Note1
2 nd Parameter	1	1	1	XX	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	140101
3 rd Parameter	1	1	1	XX	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Note1
4 th Parameter	1	1	1	XX	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	
Description	other of	driver st	atus. Th	to define area of e values of SP [ne in the Frame M SP[1!	[15:0] all lemory.	nd EP [1						_	
Restriction	Note 1	: When	SP [15:0	be equal to or less] or EP [15:0] is g			n (When	MADCTL's	s B5 = 0)	or 00EFh	(When M	ADCTL's	B5 = 1),
						Status			Availab				
Register								Sleep Out					
· ·								Sleep Out					
Availability								Sleep Out	Yes				
				Partial	ivioue O	n, idie ivid Sleep Ir		Sleep Out	Yes				
						Sieep II	1		1 1 65	•			
				_									
				Status	00.	45.01.000		Default Va					
Default			Po	wer On Sequence SW Reset		15:0]=000 15:0]=000	ooh If I	P [15:0]=01 MADCTL's MADCTL's	B5 = 0: E				
				HW Reset	SPI	15:0]=000		P [15:0]=01		[10.0]-	- UOL1 11		









8.2.22. Memory Write (2Ch)

		y **:	ne (2	J11)									
2Ch						RAMW	R (Memory	Write)			T	1	
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	0	1	1	0	0	2Ch
1 st Parameter	1	1	1					[17:0]					XX
: N th Parameter	1	1	<u></u>					[17:0]					XX
in Parameter			d :=		data fuana NAC	NI 4 - 4		ı [17:0]				- 4141-	XX
					data from MC						_		
	status.	When	this com	mand is ac	cepted, the c	olumn ı	register and	the page	e register	are rese	t to the S	tart Colur	mn/Start
Description	Page p	ositions	s. The St	art Column/	Start Page po	sitions	are differen	t in accord	dance wit	h MADCT	ΓL setting.) Then D	[17:0] is
	ctored	in frame	n momor	, and the co	lumn register	and the	o pago rogio	tor incren	nontod S	ondina ar	ov other or	ommand (oon eton
					iuiiiii registei	and the	e page regis	ster increm	nemeu. S	ending at	ly officer co	Jililianu (Jan Stop
	frame '	Write. X	= Don't	care.									
Restriction	In all c	olor mo	des, ther	e is no restr	ction on leng	th of pa	arameters.						
						Stati	us		Availab	oility			
				No	rmal Mode C	n, Idle	Mode Off, S	Sleep Out	Yes				
Register					rmal Mode C				Yes	5			
Availability				Pa	artial Mode O	n, Idle I	Mode Off, S	leep Out	Yes	3			
				Pa	artial Mode O	n, Idle I	Mode On, S	leep Out	Yes	<u> </u>			
						Sleep	o In		Yes	5			
					Status			Default Va	alue				
D ();				Pov	er On Seque	nce (Contents of			domly			
Default					SW Reset		Contents o						
					HW Reset		Contents o	f memory	is not cle	ared			
				CASE	T (2Ah)			_ If					
			/ 1	st Paramete	·· CC(1.E-01			Needed	I				
		,	/ 2	nd Paramete	er: SC[7:0]				Γ		end	;	
				rd Paramete th Parmeter					į	Leg	Jenu —	, į	
			•		<u></u>					Com	mand	<u> </u>	
					<u> </u>				'	Dara	matar	7 !	
				PASE	T (2Bh)					Para	meter		
					\forall				į	Disp	play) ¦	
				st Paramete			7			Ac	tion	, į	
Flow Chart		/		nd Paramete					<u> </u>	\geq	=	į	
				th Paramete						Mo	ode) ¦	
					<u> </u>		_		-			_	
				244	YD(201)				į	Sequentia	al transfer)	
				RAMI	VR(2Ch)			_ If Needed	, i			'	
					lack			1100000					
				Imag	e Data								
				D1[17:0],D2[—	17:0]Dn[17:0		'						
					\frown	3							
					<u> </u>								
				Any C	ommend		J						
I	Ī												





8.2.23. Color Set (2Dh)

2Dh		•				RGBSE	T (Color :	Set)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	0	1	1	0	1	2Dh
1 st Parameter	1	1	1	XX	0	0		•	R00	[5:0]			XX
n th Parameter	1	1	1	XX	0	0			Rnn	[5:0]			XX
32 nd Parameter	1	1	1	XX	0	0			R31	[5:0]			XX
33 rd Parameter	1	1	1	XX	0	0			G00	[5:0]			XX
n th Parameter	1	1	1	XX	0	0			Gnn	[5:0]			XX
96 th Parameter	1	1	1	XX	0	0			G64	[5:0]			XX
97 th Parameter	1	1	1	XX	0	0			B00	[5:0]			XX
n th Parameter	1	1	1	XX	0	0			Bnn	[5:0]			XX
128 th Parameter	1	1	1	XX	0	0			B31	[5:0]			XX
Description	128 by	tes mus ommand	t be writt has no e	to define the LU en to the LUT re effect on other o mory is written t	egardless command	of the co	lor mode.	Only the	values in				s effect
Restriction													
						Status			Availab	lity			
				Norma	Mode O	n, Idle Mo	de Off SI	een Out	Yes	iity			
Register						n, Idle Mo		•	Yes				
Availability						n, Idle Mo			Yes				
Availability						n, Idle Mo			Yes				
						Sleep In		Jop Gut	Yes				
Default				Pov	Status ver On Se SW Res HW Res	equence	Ra Contents	efault Val ndom val s of LUT ndom val	ues orotected				
Flow Chart				RGBSE* 1st Paramete: 32nd Parame 33rd Parame : 96th Parame 97th Parame : 128th Parame	er: R00[5: ter: R31[5 ter: G00[5 ter: G63[5 ter: B00[5	5:0] 5:0] 5:0] 5:0]			Comm Param Displ Actic	eter / ay / on / de	7		

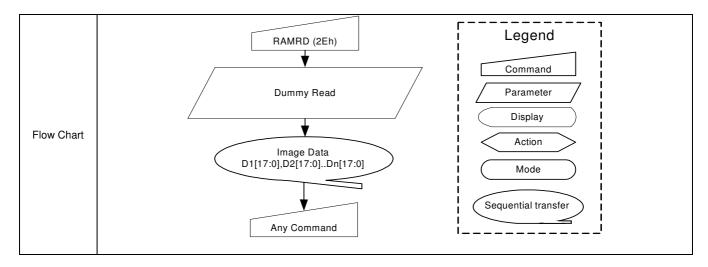




8.2.24. Memory Read (2Eh)

8.2.24. I	Memo	ry Ke	aa (2	En)											
2Eh						RAMRD	(Memory	Read)							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	XX	0	0	1	0	1	1	1	0	2Eh		
1 st Parameter	1	1	1	XX	X	Χ	X	X	X	X	X	X	Х		
2 nd Parameter	1	1	1				D.	1 [17:0]					XX		
:th	1	1	1				D	k [17:0]					XX		
(N+1) th Parameter	1	1	1				Dr	า [17:0]					XX		
	This co	ommano	transfe	rs image data	from ILI9	341's fra	me memo	ry to the	host prod	cessor sta	irting at t	he pixel l	ocation		
	specifie	ed by pr	eceding	set_column_ac	ldress and	set_pag	e_address	comman	ds.						
	If Mem	ory Acc	ess conti	rol B5 = 0:											
		ame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the plumn register equals the End Column (EC) value. The column register is then reset to SC and the page register is cremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host													
		the column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from ame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.													
		_	-					-							
	increm														
Description	proces	sor send	ds anoth	er command.											
	If Mem	Memory Access Control B5 = 1: the column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from													
	The co	ne column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from													
	frame	memory	at (SC,	SP). The page	register is	s then in	cremented	and pixel	s read fro	m the fra	me memo	ry until th	ie page		
	registe	r equals	the End	d Page (EP) va	alue. The p	oage reg	ister is the	n reset to	SP and	the colum	ın register	r is increr	nented.		
	Pixels	are reac	d from th	e frame memo	ry until the	column	register ed	quals the I	End Colur	mn (EC) v	alue or th	e host pro	ocessor		
	sends	another	commar	nd.											
Restriction	There	s no res	striction o	on length of par	ameters.										
						Status			Availab	ility					
Dogister				Norm	al Mode O	n, Idle M	ode Off, SI	eep Out	Yes						
Register						•		•							
Availability															
				Partia	al Mode Oi			eep Out							
						Sleep I	n		Yes						
					Status			Default Va	lue						
Default				Power		ence C				omly					
Deiauit				S	W Reset	С	ontents of	memory is	s set rand	omly					
				Н	IW Reset	С	ontents of	memory is	s set rand	omly					
	If Memory Access Control B5 = 1: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command. There is no restriction on length of parameters. Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes														









8.2.25. Partial Area (30h)

Discription Discription	8.2.25. F	artia	Area	a (30n	1)											
Command	30h						PLTAR	(Partial	Area)							
1º Parameter		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
2*Parameter 1 1 1 1 XX SR7 SR6 SR5 SR4 SR8 SR2 SR1 SR0 00 3*Parameter 1 1 1 1 XX ER15 ER14 ER13 ER12 ER11 ER10 ER9 ER8 01 4*Parameter 1 1 1 1 XX ER5 ER14 ER13 ER12 ER11 ER10 ER9 ER8 07 This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row-Start Row when MADCTL B4=0: Bend Row-Start Row when MADCTL B4=1: End Row ER[15:0] Partial Area If End Row-Start Row when MADCTL B4=0: Frame Removes the Start Row when MADCTL B4=0: Bend Row-Start Row when MADCTL B4=0: Bend Row-Start Row when MADCTL B4=1: End Row-Start Row when MADCTL B4=1: End Row-Start Row when MADCTL B4=0: Bend Row-Start Row when MADCTL B4=1: Bend Row-Start Row when MADCTL B4=1: Bend Row-Start Row when MADCTL B4=1: Bend Row-Start Row when MADCTL B4=1: Bend Row-Start Row when MADCTL B4=1: Bend Row-Start Row when MADCTL B4=1: Bend Row-Start Row when MADCTL B4=1: Bend Row-Start Row when MADCTL B4=1: Bend Row-Start Row when MADCTL B4=1: Bend Row-Start Row when MADCTL B4=1: Bend Row-Start Row when MADCTL B4=1: Bend Row-Start Row when MADCTL B4=1: Bend Row-Start Row when MADCTL B		0	1	1	XX	0	0	1	1	0	0	0	0	30h		
3"Parameter 1 1 1 1 XX ER15 ER14 ER10 ER18 ER19 ER19 ER19 O1 4"Parameter 1 1 1 7 XX ER1 ER1 ER10 ER18 ER19 ER19 ER10 O1 4"Parameter 1 1 1 7 XX ER1 ER1 ER10 ER18 ER10 ER19 ER10 O1 4"Parameter 1 1 1 7 XX ER1 ER10 ER18 ER10 ER10 O1 4"Parameter 1 1 1 7 XX ER15 ER14 ER10 ER10 ER10 O1 4"Parameter 1 1 1 7 XX ER15 ER14 ER10 ER10 ER10 O1 4"Parameter 1 1 1 7 XX ER15 ER14 ER10 ER10 ER10 O1 4"Parameter 1 1 1 7 XX ER15 ER10 ER10 ER10 O1 4"Parameter 1 1 1 7 XX ER15 ER10 ER10 ER10 O1 4"Parameter 1 1 1 7 XX ER15 ER10 ER10 ER10 ER10 O1 4"Parameter 1 1 1 7 XX ER15 ER10 ER10 ER10 ER10 O1 4"Parameter 1 1 1 7 XX ER15 ER10 ER10 ER10 ER10 ER10 O1 4"Parameter 1 1 1 7 XX ER15 ER10 ER10 ER10 ER10 ER10 ER10 ER10 O1 4"Parameter 1 1 1 7 XX ER15 ER10 ER10 ER10 ER10 ER10 ER10 O1 4"Parameter 1 1 1 7 XX ER15 ER10 ER10 ER10 ER10 ER10 ER10 ER10 ER10		1	1	1	XX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00		
This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row-Start Row when MADCTL 84=0:- Start Row SR[15:0] Description Description Description If End Row-Start Row when MADCTL 84=1:- End Row SR[15:0] End Row SR[15:0] Fartial Area If End Row-Start Row when MADCTL 84=0:- End Row SR[15:0] Fartial Area If End Row-Start Row when MADCTL 84=0:- End Row SR[15:0] Fartial Area If End Row-Start Row when MADCTL B4=0:-		1	1	1		SR7		SR5	SR4	SR3	SR2	SR1				
This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row-Start Row when MADCTL B4=0:- Start Row SR(15:0) Partial Area If End Row-Start Row when MADCTL B4=1:- End Row ER(15:0) Fartial Area If End Row-Start Row when MADCTL B4=0:- If End Row SR(15:0) Fartial Area If End Row = Start Row then the Partial Area will be one row deep. X = Don't care.				1												
defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row-Start Row when MADCTL B4=0: Start Row SR[15:0] End Row ER[15:0] Partial Area If End Row-Start Row when MADCTL B4=1: End Row ER[15:0] Fartial Area If End Row-Start Row when MADCTL B4=0: End Row SR[15:0] Fartial Area If End Row-Start Row when MADCTL B4=0: If End Row Start Row when MADCTL B4=0: If End Row SR[15:0] Partial Area If End Row Start Row when the Partial Area will be one row deep. X = Don't care.	4" Parameter			1												
Frame Memory Line Pointer. If End Rows-Start Row when MADCTL B4=0: Start Row End Row Start Row Start Row Start Row Start Row End R		This co	ommano	I defines	the partial mod	de's displ	ay area.	There are	2 paran	neters as	sociated	with this	command	, the first		
If End Row-Start Row when MADCTL B4=1: End Row ER[15:0] End Row ER[15:0] Partial Area If End Row-Start Row when MADCTL B4=1: End Row ER[15:0] If End Row-Start Row when MADCTL B4=1: End Row ER[15:0] Partial Area If End Row-Start Row when MADCTL B4=0: End Row ER[15:0] Partial Area If End Row = Start Row then the Partial Area will be one row deep. X = Don't care.		defines	the Sta	art Row	(SR) and the se	cond the	End Row	(ER), as	illustrate	d in the fi	gures be	low. SR a	ınd ER re	fer to the		
Start Row SR[15:0] Partial Area If End Row-Start Row when MADCTL B4=1: End Row ER[15:0] Fartial Area If End Row-Start Row when MADCTL B4=0: End Row SR[15:0] Fartial Area If End Row-Start Row when MADCTL B4=0: If End Row-Start Row when MADCTL B4=0: If End Row-Start Row when MADCTL B4=0: If End Row-Start Row when MADCTL B4=0: If End Row-Start Row when the Partial Area will be one row deep. X = Don't care.		Frame	Memory	/ Line Po	ointer.											
SR[15:0] Partial Area End Row ER[15:0] Partial Area End Row ER[15:0] Partial Area If End Row-Start Row when MADCTL B4=1: End Row ER[15:0] Partial Area If End Row-Start Row when MADCTL B4=0: Partial Area If End Row ER[15:0] Partial Area If End Row ER[15:0] Partial Area If End Row ER[15:0] Partial Area If End Row = Start Row then the Partial Area will be one row deep. X = Don't care.		If End	Row>St	art Row	when MADCTL	B4=0:-										
SR[15:0] Partial Area End Row ER[15:0] Partial Area End Row ER[15:0] Partial Area If End Row-Start Row when MADCTL B4=1: End Row ER[15:0] Partial Area If End Row-Start Row when MADCTL B4=0: Partial Area If End Row ER[15:0] Partial Area If End Row ER[15:0] Partial Area If End Row ER[15:0] Partial Area If End Row = Start Row then the Partial Area will be one row deep. X = Don't care.											F					
End Row ER[15:0] Bend Row ER[15:0] End Row ER[15:0] Fartial Area Partial Area Partial Area If End Row-Start Row when MADCTL B4=0: Find Row SR[15:0] Fartial Area Partial Area Partial Area Partial Area Find Row SR[15:0] Partial Area Find Row SR[15:0] Find Row SR[15:0] Partial Area Find Row SR[15:0] Partial Area Find Row SR[15:0] Partial Area Find Row SR[15:0] Partial Area											<u> </u>					
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If End Row Start Row when MADCTL B4=1:- End Row ER[15:0] Start Row SR[15:0] If End Row <start area="" b4="0:-" be="" care.<="" deep.="" end="" er[15:0]="" if="" madctl="" one="" partial="" row="" td="" the="" then="" when="" will="" x="Don't"><td></td><td></td><td></td><td></td><td>End Row -</td><td></td><td></td><td></td><td></td><td></td><td>_</td><td></td><td></td><td></td></start>					End Row -						_					
Description End Row ER[15:0] Partial Area If End Row-Start Row when MADCTL B4=0:- Partial Area End Row SR[15:0] Partial Area Partial Area If End Row = Start Row then the Partial Area will be one row deep. X = Don't care.					ER[15:0]						# /					
Description End Row ER[15:0] Partial Area If End Row-Start Row when MADCTL B4=0:- Partial Area End Row SR[15:0] Partial Area Partial Area If End Row = Start Row then the Partial Area will be one row deep. X = Don't care.					-											
Description End Row ER[15:0] Partial Area If End Row-Start Row when MADCTL B4=0:- Partial Area End Row SR[15:0] Partial Area Partial Area If End Row = Start Row then the Partial Area will be one row deep. X = Don't care.					_											
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If End Row <start area="" b4="0:-" be="" care.<="" deep.="" end="" er[15:0]="" if="" madctl="" one="" partial="" row="" sr[15:0]="" start="" td="" the="" then="" when="" will="" x="Don't"><td>-</td><td></td><td></td><td></td><td>_</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></start>	-				_											
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Start Row SR[15:0] Partial Area If End Row = Start Row then the Partial Area will be one row deep. X = Don't care.		If End	Row <st< td=""><td>art Row</td><td>when MADCTL</td><td>B4=0:-</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></st<>	art Row	when MADCTL	B4=0:-										
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Start Row SR[15:0] Partial Area If End Row = Start Row then the Partial Area will be one row deep. X = Don't care.					_						$\overline{}$					
Start Row SR[15:0] Partial Area If End Row = Start Row then the Partial Area will be one row deep. X = Don't care.					_						\Box	Partial				
Start Row SR[15:0] Partial Area If End Row = Start Row then the Partial Area will be one row deep. X = Don't care.											\vdash					
SR[15:0] Partial Area If End Row = Start Row then the Partial Area will be one row deep. X = Don't care.					ER[15:0] →						Γ					
SR[15:0] Partial Area If End Row = Start Row then the Partial Area will be one row deep. X = Don't care.					_											
If End Row = Start Row then the Partial Area will be one row deep. X = Don't care.											-					
If End Row = Start Row then the Partial Area will be one row deep. X = Don't care.					SR[15:0] →						\Box	Partial				
X = Don't care.					_						\perp					
X = Don't care.					_						\perp $^{\prime}$					
		If End	Row = S	Start Row	then the Partia	l Area will	be one r	ow deep.			_					
Restriction SR [150] and ER [150] cannot be 0000h nor exceed 013Fh.		X = Do	n't care.													
	Restriction	SR [15	0] and	d ER [15	0] cannot be (0000h nor	exceed (013Fh.								





	Status Availability
	Normal Mode On, Idle Mode Off, Sleep Out Yes
Register	Normal Mode On, Idle Mode On, Sleep Out Yes
Availability	Partial Mode On, Idle Mode Off, Sleep Out Yes
Availability	Partial Mode On, Idle Mode On, Sleep Out Yes
	Sleep In Yes
	3.635
	Status Default Value
Default	SR [15:0] ER [15:0]
Delault	Power On Sequence 16'h0000h 16'h013Fh SW Reset 16'h 0000h 16'h 013Fh
	SW Reset 16'h 0000h 16'h 013Fh HW Reset 16'h 0000h 16'h 013Fh
	HW Reset 1611 000011 1611 013F11
	1. To Enter Partial Mode
	PLTAR(30h)
	Legend
	i
	1st Parameter: SR[15:8] Command
	2nd Parameter. SR[7:0] Parameter
	3rd Parameter: ER[15:8] Display
	4th Parameter: ER[7:0] Action
	Action
	Mode
	PTLON(12h)
	Sequential transfer
	Sequential transfer
	Partial Mode
	2. To Leave Partial Mode
Flow Chart	(Partial Mode
Tiow Chart	
	Logond
	DISPOFF(28h)
	Command
	NOPON(13h) Parameter
	NORON(13h) Display
	Display
	Partial Mode OFF Action
	Mode
	RAMRW(2Ch)
	Sequential transfer
	Image Data
	D1[17:0],D2[17:0]
	<u> </u>
	DISPON(29h)





8.2.26. Vertical Scrolling Definition (33h)

33h					VSCRDE	F (Vertic	al Scrolli	ng Defini	tion)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h		
1 st Parameter	1	1	1	XX	TFA [15:8]										
2 nd Parameter	1	1	1	XX	TFA [7:0]										
3 rd Parameter	1	↑	1	XX				VSA	[15:8]				01		
4 th Parameter	1	1	1	XX				VSA	[7:0]				40		
5 th Parameter	1	1	1	XX	BFA [15:8]										
6 th Parameter	1	1	1	XX				BFA	[7:0]				00		

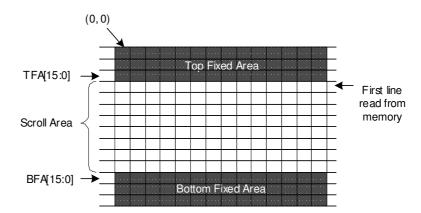
This command defines the Vertical Scrolling Area of the display.

When MADCTL B4=0

The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.



Description

When MADCTL B4=1

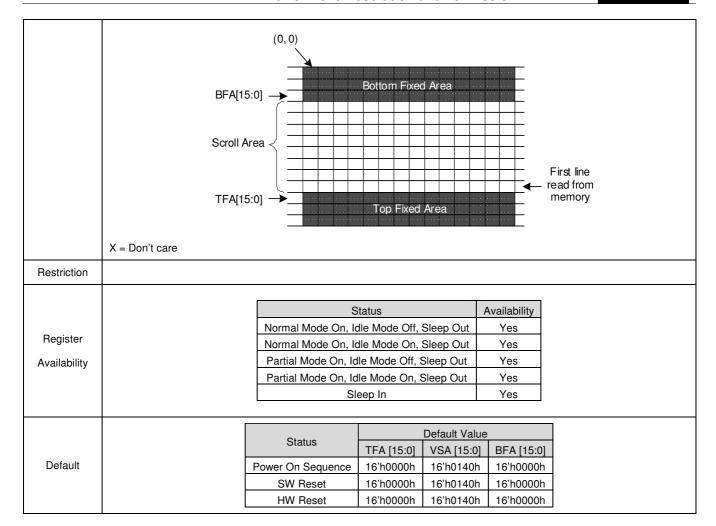
The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

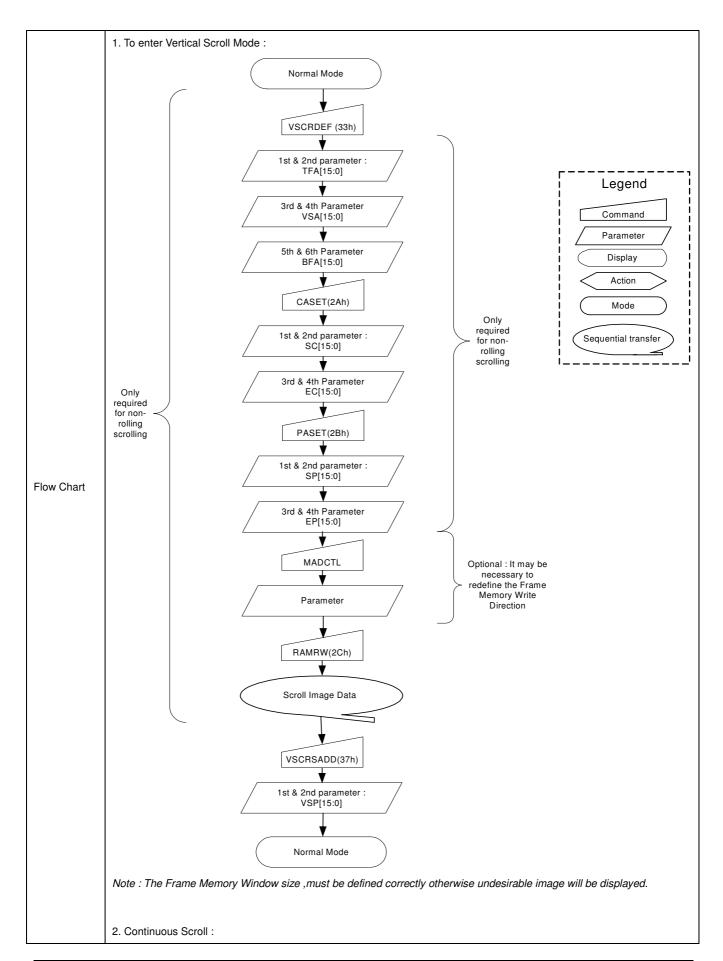
The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).





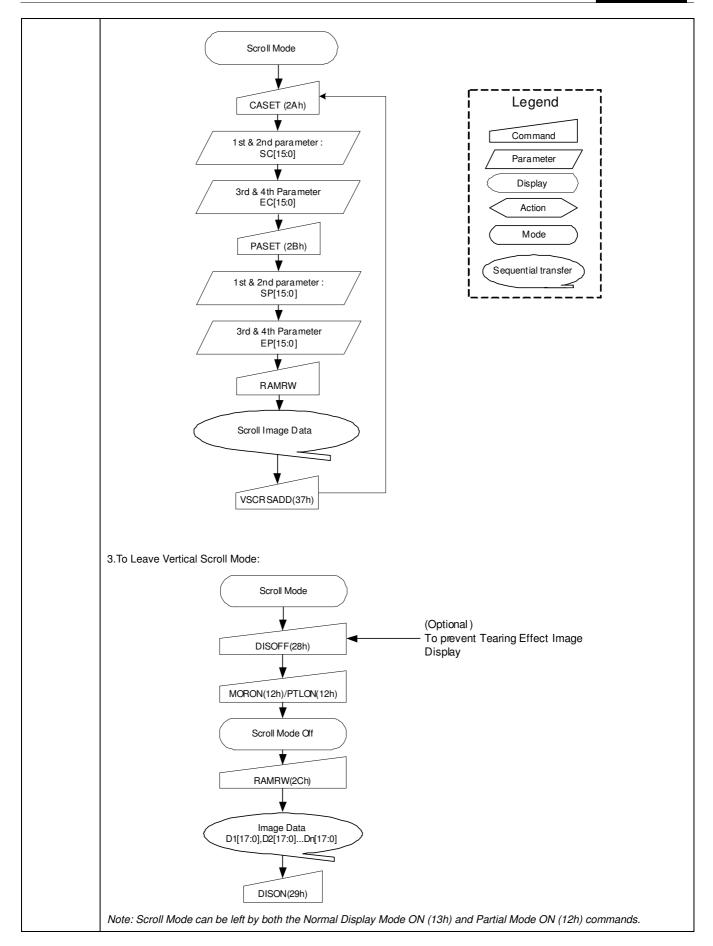
















8.2.27. Tearing Effect Line OFF (34h)

34h						TEOF	F (Tearin	g Effect	Line OFF	.)					
	D/CX	RDX	WRX	D17	7-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	X	X	0	0	1	1	0	1	0	0	34h	
Parameter							No P	arameter							
Description		mmand n't care.		to turn OF	F (Activ	e Low) the	e Tearing	Effect out	tput signa	Il from the	TE signa	al line.			
Restriction	This co	mmand	has no e	effect whe	n Tearin	g Effect o	output is a	lready OF	F.						
Register Availability					Normal Partial	Mode On	Status n, Idle Moo n, Idle Moo n, Idle Moo n, Idle Moo Sleep In	de On, Sle le Off, Sle	eep Out	Availabil Yes Yes Yes Yes	ity				
Default		Status Default Value Power On Sequence OFF SW Reset OFF HW Reset OFF													
Flow Chart					TEOF	Output O F(34h) V Output OF			C Pa	egend ommand arameter Display Action Mode					



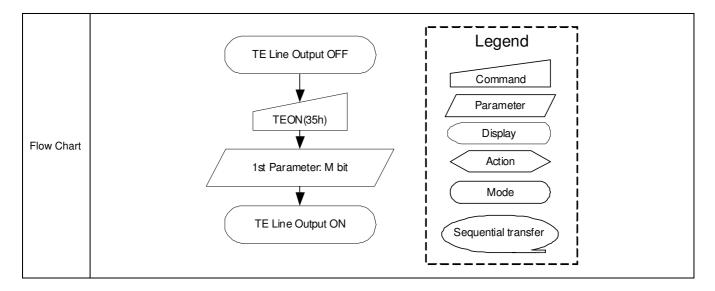


8.2.28. Tearing Effect Line ON (35h)

35h					TEO	N (Tearin	g Effect	Line ON))				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	1	0	1	0	1	35h
Parameter	1	1	↑	XX	0	0	0	0	0	0	0	М	00
		ng MAD Line.		to turn ON the T	_	•	_		_		•		-
Description	Verti When I The Te	ical Tir M=1: earing Ef	ne Sca fect Outp	out Line consists c	of both V-E	tv Blanking a	dl and H-Bla	anking info	tvdh	e active l	OW		
		n't care.	-	.ooo		o o, . o.	g =	or output	, p	0 400 1	-0		
Restriction	This co	mmand	has no e	effect when Tearin	g Effect o	utput is a	Iready O	N					
Register Availability	This command has no effect when Tearing Effect output is already ON Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes												
Default					Power	Status On Seque W Reset W Reset		Oefault Val OFF OFF OFF	lue				











8.2.29. Memory Access Control (36h)

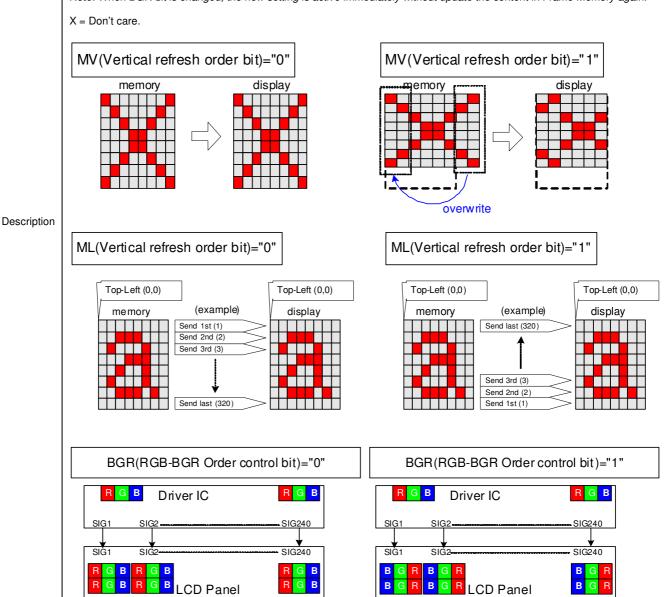
36h				MA	DCTL (N	lemory A	Access	Control)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
Parameter	1	1	↑	XX	MY	MX	MV	ML	BGR	МН	0	0	00

This command defines read/write scanning direction of frame memory.

This command makes no change on the other driver status.

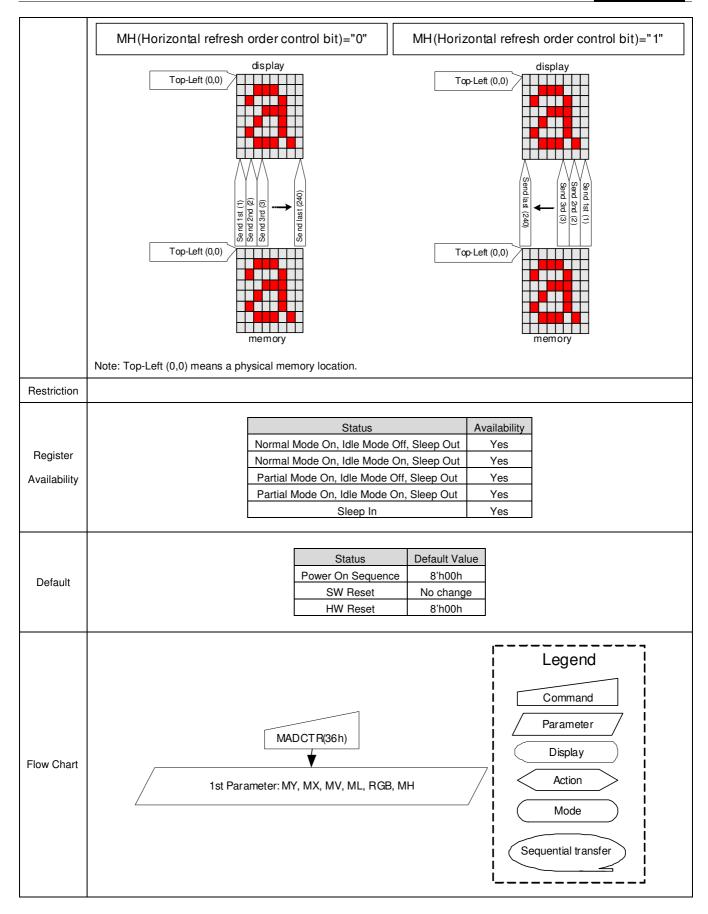
Bit	Name	Description
MY	Row Address Order	
MX	Column Address Order	These 3 bits control MCU to memory write/read direction.
MV	Row / Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control.
BGR	RGB-BGR Order	Color selector switch control
ban	NGB-BGN Older	(0=RGB color filter panel, 1=BGR color filter panel)
MH	Horizontal Refresh ORDER	LCD horizontal refreshing direction control.

Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.













8.2.30. Vertical Scrolling Start Address (37h)

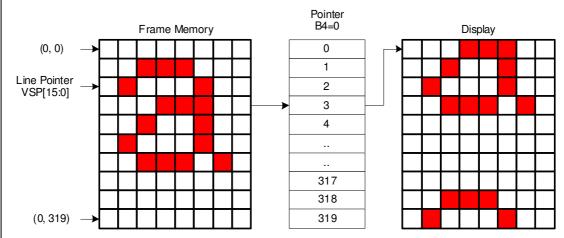
37h				VS	CRSADI	O (Vertica	I Scrollin	g Start A	ddress)						
	D/CX	RDX WRX D17-8 D7 D6 D5 D4 D3 D2 D1 D0 H													
Command	0	1	↑	XX	0	0	1	1	0	1	1	1	37h		
1 st Parameter	1	1	1	XX				VSP	[15:8]				00		
2 nd Parameter	1	1	1	XX	VSP [7:0]										

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-

When MADCTL B4=0

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.

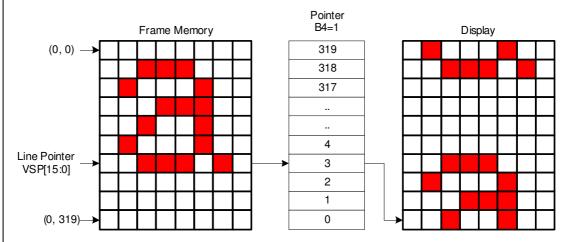


Description

When MADCTL B4=1

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.



Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan

to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

(2) This command is ignored when the ILI9341 enters Partial mode.

X = Don't care





Restriction						
			Status		Availability	
		Norm	al Mode On, Idle Mode (Off, Sleep Out	Yes	
Register		Norm	al Mode On, Idle Mode (On, Sleep Out	Yes	
Availability		Partia	al Mode On, Idle Mode C	Off, Sleep Out	No	
•		Partia	al Mode On, Idle Mode C	On, Sleep Out	No	
			Sleep In		Yes	
			Otatus	Default Val	ue	
			Status	VSP [15:0)]	
Default			Power On Sequence	16'h0000l	h	
			SW Reset	16'h0000l	h	
			HW Reset	16'h0000	h	
Flow Chart	See Vertical Scrolling Definition	(33h)	description.			





8.2.31. Idle Mode OFF (38h)

38h					IDM	OFF (Idle	Mode O	FF)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	XX	0	0	1	1	1	0	0	0	38h	
Parameter						No Para	meter							
	This cor	mmand is ι	used to red	over from Idl	e mode o	n.								
Description	In the id	le off mode	e, LCD cai	n display max	imum 262	2,144 colo	rs.							
	X = Don													
Restriction	This cor	nmand has	s no effect	when modul	e is alread	dy in idle o	ff mode.							
						Status			Availabili	ty				
Register						dle Mode			Yes					
						dle Mode dle Mode (Yes Yes					
Availability														
		Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes												
		Sleep In Yes												
						atus		ult Valu						
Default				-		Sequence Reset		node OF node OF						
						Reset		node OF						
							10.01.		· _					
						_	ı				7			
							l I	Le	egend		į			
			(Idle mod	de on)	į,				ļ			
				_					mmand	<u> </u>	į			
							! /	/ Pa	rameter					
				Ţ			i -		isplay	\equiv	1			
Flow Chart									портау	}	į			
				IDMOFF	(38h)		į.	</td <td>Action</td> <td>\geq</td> <td>!</td> <td></td> <td></td>	Action	\geq	!			
							Ι,		Mode		į			
						_	-		IVIOUE					
								0	4:-14		1			
			(Idle mod	de off		- (Sequer	ntial trans	ier	į			
							i				1			
İ	I					_								



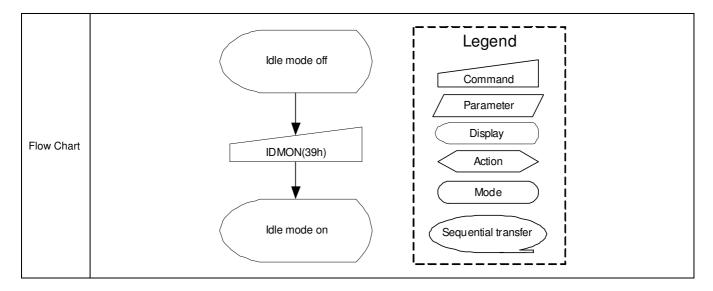


8.2.32. Idle Mode ON (39h)

39h	IDMON (Idle Mode ON)													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	XX	0	0	1	1	1	0	0	1	39h	
Parameter	_						Parame	ter	I	1		1		
	This co	mmand	is used t	o enter into Idl	e mode on									
										aira ar MC	'D -f l	- D. O	J D : 41-	
	in the i	ale on m	iode, col	or expression is	s reaucea.	i ne prim	ary and	ne secona	ary colors	s using ivis	B of each	n R, G and	3 B IN tN	
	Frame	Memory	, 8 color	depth data is c	displayed.									
				Memory						Panel Di	enlav			
			1.1						11'					
						_								
						_								
						_								
		_				_	1	_						
								> _						
						_		/ _						
Description						_								
						_								
						_								
		Memory Contents vs. Display Color												
					R ₅ R ₄ R ₃ F	$R_2 R_1 R_0$	G ₅ G ₄ (G_3 G_2 G_1 G_0	B ₅ B ₄	B ₃ B ₂ B ₁ B	ю			
				Black	0XXX			XXXX		XXXXX				
				Blue Red	0XXX 1XXX			XXXX		XXXXX				
				Magenta	1XXX	XX	0×	XXXX	1.	XXXXX				
				Green	0XXX			XXXX		XXXXX				
				Cyan Yellow	0XXX 1XXX			XXXX		XXXXX				
				White	1XXX	XX	1X	XXXX		XXXXX				
	X = Do	n't care.												
				<u> </u>										
Restriction	This co	mmand	has no e	effect when mo	dule is alre	ady in idl	e off mod	de.						
						_			I					
				.	134 1 6	Status		01 0 1	Availa					
Register								Sleep Out						
_								Sleep Out	Ye					
Availability					ial Mode C				Ye					
				Pari	ial Mode C	Sleep I		Sieep Out	Ye:					
						элеер і	III		16	5				
						Status		Default Va	llue					
Default					Power	r On Sequ	uence	Idle mode (OFF					
Dordan	SW Rese						t	Idle mode (OFF					
					H	HW Reset	t	Idle mode (OFF					











8.2.33. COLMOD: Pixel Format Set (3Ah)

0.2.33.	PIXSET (Pixel Format Set)																
3Ah							PIX	SET (Pi	cel Fo	orma	at Set)						
	D/CX	RDX	WRX		D17	7-8	D7	D6	D:	5	D4		D3	D2	D1	D0	HEX
Command	0	1	1		XΣ	<	0	0	1		1		1	0	1	0	3Ah
Parameter	1	1	1		XX	<	0		DPI	[2:0]		0		DBI [2:0)]	66
	This cor	mmand s	ets the pi	xel f	orma	t for the	RGB ima	ige data	used	by t	he inte	erface	. DPI [2	:0] is the	pixel form	nat select	of RGB
	interface	e and DE	3I [2:0] is t	he p	oixel f	ormat c	of MCU int	terface. I	f a pa	articu	ılar int	erface	e, either	RGB int	erface or	MCU inte	rface, is
				-			e paramete		-								
	Hot used	u men m	_													iow.	
			0	PI [:		RGB	Interface Reserved				[2:0]	MC		ace Forn erved	nat		
			0	0			Reserved				0 1			erved			
Description			0	1	0		Reserved				1 0			erved			
Description			0	1	1		Reserved				1 1			erved			
			1	0	0		Reserved	d		1	0 0		Rese	erved			
			1	0	1	1	6 bits / pi	xel		1	0 1		16 bits	/ pixel			
			1	1	0	1	8 bits / pi				1 0			/ pixel			
			1	1	1		Reserved		Ľ	1	1 1		Rese	erved			
	If using	RGB Inte	erface mu	st s	election	on seria	al interface) .									
	X = Dor	ı't care															
Restriction																	
							9	Status					Availab	ility			
Register							lode On, I						Yes				
							<u>lode On, I</u>						Yes				
Availability							ode On, Id ode On, Id						Yes Yes				
						artiai ivi		leep In	, OII,	Oloc	p Out		Yes				
												•		<u> </u>			
											Defa	ıult Va	alue				
					S	tatus			DPI	[2:0]	20.0			3I [2:0]			
Default			Pov	ver (On Se	equence	Э		3'b1	110			3	b110			
					SW	Reset		1	No Ch	nang	е		No	Change			
					HW	Reset			3'b1	110			3	b110			
															₁		
					_						į		Leger	nd	į		
						COL	MOD (3Ah)			į			$\overline{}$	į		
											-	<u></u>	Comma	nd	į		
							\downarrow					<u>/ </u>	Parame	ter	į		
				/	DD	חונסיטו ט	GB pixel fo		,	7	-		Display	,	į		
Flow Chart			/	/			ICU pixel f					\geq	Action				
			_						_/			\geq			ļ		
							\				1		Mode				
					٢		Command				/	Segu	uential tr	ansfer			
					L	АПУ	Command	<u>'</u>			(Jequ	Jonual II		'		
											!				'		





8.2.34. Write Memory Continue (3Ch)

3Ch					Write_	Memory	_Contin	iue					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
1 St Dovementar	4	4		D1	D1	D1	D1	D1	D1	D1	D1	D1	000
1 st Parameter	Į	Į	Ţ	[178]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	3FF
X th Parameter	4	4		Dx	Dx	Dx	Dx	Dx	Dx	Dx	Dx	Dx	000
X Parameter	Į	Į	T	[178]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	3FF
Nth Davanatas	4	4		Dn	Dn	Dn	Dn	Dn	Dn	Dn	Dn	Dn	000
N th Parameter	1	1	Î	[178]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	3FF

This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.

If set_address_mode B5 = 0:

Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

If set_address_mode B5 = 1:

Description

Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC - SC + 1) * (EP - SP + 1) the extra pixels are ignored.

Sending any other command can stop frame Write.

Frame Memory Access and Interface setting (B3h), WEMODE=0

When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.

Frame Memory Access and Interface setting (B3h), WEMODE=1

When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

Restriction

A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.





					 1
		Status		Availability	
		Normal Mode On, Idle M		Yes	
Register	<u> </u>	Normal Mode On, Idle M	ode On, Sleep Out	Yes	
Availability	<u> </u>	Partial Mode On, Idle Mo	ode Off, Sleep Out	Yes	
	<u> </u>	Partial Mode On, Idle Mo	ode On, Sleep Out	Yes	
	S	Sleep In		No	
		Status	Default Val	ue	
Defeat		Power On Sequence	Random va	lue	
Default		SW Reset	No chang	е	
		HW Reset	No chang	е	
Flow Chart	Image Data D1[17:0],D2[17,Dn[17:0] Next Comma	7:0]		Pa	egend ommand rameter Display Action Mode Sequential transfer

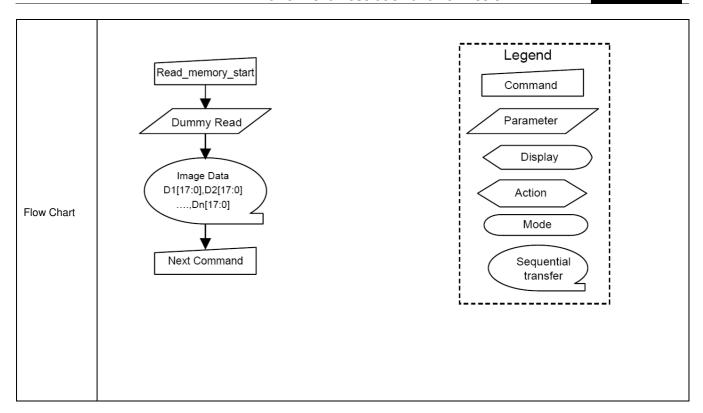




Read Memory Continue (3Fh)

	Read_Me												
3Eh					Read_l	Memory	_Contin	ue					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	1	1	1	1	0	3Eh
1 st Parameter	1	1	1	XX	Χ	Χ	Χ	Х	Χ	Χ	Х		Х
2 nd Parameter	1	1	1	D1	D1	D1	D1	D1	D1	D1			000
				[178]	[7]	[6]	[5]	[4]	[3]	[2]			3FF
x st Parameter	1	↑	1	Dx [178]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	1 0 X X D1 D1 [1] [0] Dx Dx [1] [0] Dn Dn [1] [0] ssor continuing from and.	000 3FF	
				Dn	ر را Dn	رە <u>ا</u> Dn	[ગ	Dn	Dn	<u>[∠]</u> Dn			000
N st Parameter	1	1	1	[178]	[7]	[6]	[5]	[4]	[3]	[2]			3FF
	This comma	and transfe	rs image d							t proces			
Description	If set_addre Pixels are r read_memore column regions incrementer column regions If set_addre Pixels are r read_memore register equ Pixels are r equals the life	ess_mode ead continuous continuous continuous ead continuous ead continuous ead continuous ead from the EP value, continuous EP value, continu	B5 = 0: uing from the column of the End Color read from the EC valuing from the EC th	n the frame malue, or the host	on after to the the the the the the the the the the	the read crement e column ntil the person sen the read emented ister is the register of the register is the register is the register is the register is the register is the register is the register is the register is the register in register is the register in register i	range of ed and positive age regions another and pixenen reserved.	f the pre pixels are r is then pister equ per comm f the pre pels are re pet to SP a	vious read from reset to vious read from and the control of the co	ad_mem om the fr SC and End Page ad_mem the fran	rame me the page e (EP) va	r is the the page ented.	
		and makes	no change	to the other o	driver sta	itus.							
Restriction	A read_me	mory_start	should foll		umn_ado	dress, se			s or set_	address	s_mode t	to define	the rea
Restriction	A read_me	mory_start	should foll	ow a set_colu	umn_ado	dress, se		d.			s_mode 1	to define	the rea
Restriction	A read_me	mory_start	should foll	ow a set_colu	umn_add pry_cont Stat	dress, se inue is u	ndefined	d.	s or set_ Availabili Yes		s_mode 1	to define	the rea
	A read_me	mory_start	should foll	ow a set_colu	umn_ado ory_cont Stat On, Idle	dress, se inue is u	ndefined	Out	Availabili		s_mode t	to define	the rea
-	A read_me	mory_start	should foll	ow a set_coluth read_memo	umn_ado ory_cont Stat On, Idle On, Idle	dress, se inue is u tus Mode C Mode C	ndefined ff, Sleep	Out Out	Availabili Yes		s_mode t	to define	the rea
Restriction Register Availability	A read_me	mory_start	should foll ata read wit	ow a set_colu th read_memo Normal Mode Normal Mode	umn_add ory_cont Stat On, Idle On, Idle On, Idle	dress, so inue is u tus Mode C Mode C Mode O	ndefined off, Sleep on, Sleep off, Sleep	Out Out	Availabili Yes Yes		s_mode t	to define	the rea
Register	A read_me	mory_start	should foll	ow a set_columb read_memo	umn_add ory_cont Stat On, Idle On, Idle On, Idle	dress, so inue is u tus Mode C Mode C Mode O	ndefined off, Sleep on, Sleep off, Sleep	Out Out	Availabili Yes Yes Yes		s_mode t	to define	the rea
Register	A read_me	mory_start	should foll	ow a set_column read_memo Normal Mode Normal Mode Partial Mode (Partial Mode)	umn_add ory_cont Stat On, Idle On, Idle On, Idle	dress, so inue is u tus Mode C Mode C Mode O	ndefined off, Sleep on, Sleep off, Sleep	Out Out	Availabili Yes Yes Yes Yes		s_mode t	to define	the rea
Register	A read_me	mory_start	should foll	ow a set_column read_memo Normal Mode Normal Mode Partial Mode (Partial Mode (Sleep In	umn_add ory_cont Stat On, Idle On, Idle On, Idle	dress, so inue is u tus Mode C Mode C Mode O	ndefined ff, Sleep n, Sleep ff, Sleep n, Sleep	O Out Out Out	Availabilii Yes Yes Yes Yes Yes Yes		s_mode t	to define	the rea
Register	A read_me	mory_start	should foll	ow a set_column read_memonomal Mode Normal Mode Partial Mode (Partial Mode (Sleep In	State On, Idle On, Idle On, Idle On, Idle On, Idle	dress, so inue is u tus Mode C Mode C Mode O	ff, Sleep n, Sleep ff, Sleep n, Sleep n, Sleep	O Out Out Out Out	Availabilir Yes Yes Yes Yes Yes		s_mode t	to define	the rea
Register	A read_me	mory_start	should foll	ow a set_column read_memo Normal Mode Normal Mode Partial Mode (Partial Mode (Sleep In	State On, Idle On, Idle On, Idle On, Idle On, Idle	dress, so inue is u tus Mode C Mode C Mode O	ndefined fff, Sleep nn, Sleep ff, Sleep nn, Sleep Defal Rand	O Out Out Out	Availabilir Yes Yes Yes Yes Yes		s_mode t	to define	the rea









8.2.36. Set_Tear_Scanline (44h)

0.2.30. S	et_rear_			-,	Set	Tear S	Scanline						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	1	0	0	0	1	0	0	44h
1 st Parameter	1	1	1	XX	0	0	0	0	0	0	0	STS [8]	00
2 nd Parameter	1	1	1	XX	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	00
Description	The TE sign describes the Vertical T	nal is not a ne Tearing ime Scal	e	ay Tearing Etchanging set_	_address	_mode b	tvo	ne Tearii				e parame	
				STS=0 is equall be active					ı Sleep m	node.			
Restriction	-												
Register Availability			1	Normal Mode Normal Mode Partial Mode Partial Mode Sleep In	On, Idle On, Idle	Mode C Mode C Mode O	n, Sleep	Out Out Out	Availabili Yes Yes Yes Yes Yes Yes	ity			
Default				Power On S SW Reset HW Reset		e	STS [8	ult Value 3:0]=000 3:0]=000 3:0]=000	0h 0h				
Flow Chart	TE Output On or Off Set_tear_scanline Parameter Send 1st parameter STS[8] Display Action Mode TE Output On the Nth line Sequential transfer												





8.2.37. Get_Scanline (45h)

	ici_Scai		J.1.,										
45h						Get_Sca	nline						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	1	0	0	0	1	0	1	45h
1 st Parameter	1	1	1	XX	Х	Х	Χ	Х	Х	Х	Χ	Χ	Χ
2 nd Parameter	1	1	1	XX	0	0	0	0	0	0	GTS [9]	GTS [8]	00
3 rd Parameter	1	1	1	XX	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	00
Description	display devi	ice is defin	ed as VSYI	an line, GTS NC + VBP + \ eturned by ge	VACT + '	VFP. The	e first sca	-					
Restriction	None												
Register Availability			١		On, Idle	Mode C	n, Sleep	Out Out	Availabili Yes Yes Yes	ity			
,		Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes											
				Stat			GT	ult Value					
Default				Power On S	Sequenc	е		9:0]=000					
Flow Chart	SW Reset GTS [9:0]=0000h HW Reset GTS [9:0]=0000h Get_scanline Command Parameter Display Action Send 1st parameter GTS[9:8] Mode Sequential transfer												





8.2.38. Write Display Brightness (51h)

51h		WRDISBV (Write Display Brightness)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	XX	0	1	0	1	0	0	0	1	51h	
Parameter	1	1	1	XX	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[2]	DBV[1]	DBV[0]	00	
Description	It should	be chec	ked what	is the rela	brightness ationship b ecification. value mean	etween thi	s written v	alue and o					ionship	
Restriction	None													
						Stat	us		Availab	oility				
				N	ormal Mod			Sleep Out						
Register					ormal Mod									
Availability		Partial Mode On, Idle Mode Off, Sleep Out Yes												
	Partial Mode On, Idle Mode On, Sleep Out Yes													
				S	leep In				Yes	3				
Default					State Power On S SW R HW F	Sequence leset		Default V DBV [7 8'h00l 8'h00l	:0] า า					
Flow Chart					DBV[70 New Displ Brightnes	lay		-	Leger Comm Parame Displ Action Mod Seque trans	and ter ay on le ntial				





8.2.39. Read Display Brightness (52h)

52h	RDDISBV (Read Display Brightness Value)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	1	0	1	0	0	1	0	52h
1 st Parameter	1	1	1	XX	Х	Х	Х	Х	Χ	Х	Х	Х	Х
2 nd Parameter	1	1	1	XX	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[2]	DBV[1]	DBV[0]	00
Description	It shou relatior	ld be ch	necked w	that the re	splay modu	between t	his returne ation.	ed value ar brightness	·				ness.
Restriction	(= more	e than 2	RDX cy	rcle) on D	e nd parame BI Mode. SI (The 1s			lines if the	e MCU wa	nts to reac	I more than	n one para	meter
						- C:	-1			- I- 1114.			
B				-	\.\		atus	" 01 0		ability			
								ff, Sleep O		es			
Register Availability								n, Sleep O f, Sleep Oı		es es			
Availability								n, Sleep Ot		es			
					Sleep In	<u>ao on, ian</u>	3 111000 01	i, 0.00p 0		es			
Default					Power Or	ratus n Sequenc Reset Reset	ee	Default DBV [8'h0 8'h0	7:0] 0h 0h				
Flow Chart					Send	1 RDDISB 1 st Parame Dand Parame	Dis	<u>Host</u> play	Parra D A See	egend mmand ameter isplay action Mode quential ansfer			



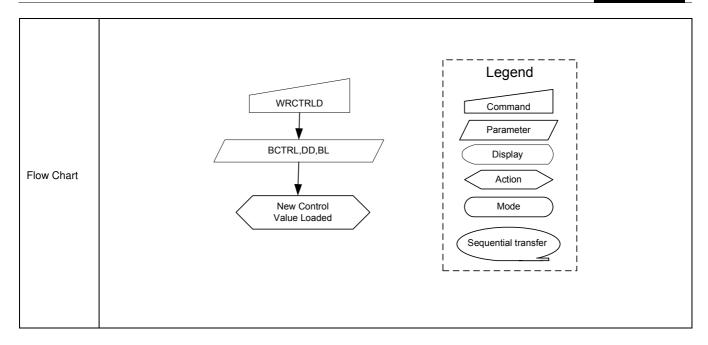


8.2.40. Write CTRL Display (53h)

53h				WR	CTRLD	(Write	Control D	isplay)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	XX	0	1	0	1	0	0	1	1	53h	
Parameter	1	1	1	XX	0	0	BCTRL	0	DD	BL	0	0	00	
	This command is used to control display brightness.													
	BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.													
	0 = Off (Brightness registers are 00h, DBV[70])													
	0 = 01	f (Brightne	ss registers	are oon, DB	V[70])									
	1 = On (Brightness registers are active, according to the other parameters.)													
	DD: Display	/ Dimming,	only for ma	anual brightne	ess setti	ng								
	DD = 0	0: Display	Dimming is	off										
	DD = 1	1: Display l	Dimming is	on										
		Biopiay	Dimming to	011										
Description	51 5 11		0 10"											
	BL: Backlig	nt Control	On/Off											
	0 = Of	f (Complet	ely turn off l	oacklight circu	uit. Con	trol lines	s must be lo	ow.)						
	1 = Or	1												
	Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 →													
			aaptoa to ti.		. 09.0.0.								IBI:U 🔿	
	4 - 4 > 0						17			angea a		9	IRL: U J	
	1 or 1→ 0.									ungou u	(55-1,	9	IRL: U J	
	1 or 1→ 0.						, ,			agou a	, ,		IKL: U J	
		it change f	rom "On" to	"Off", backlig	ht is tur									
	When BL bi	it change f	rom "On" to	"Off", backlig	ht is tur									
		it change f	rom "On" to	"Off", backlig	ht is tur									
	When BL bi	it change f	rom "On" to	"Off", backlig	ht is tur									
Restriction	When BL bi	it change f	rom "On" to	"Off", backlig	ht is tur									
Restriction	When BL bi	it change f	rom "On" to	"Off", backlig		ned off		dual din	nming, e	ven if di				
Restriction	When BL bi	it change f			Sta	ned off	without gra	dual din	nming, e	ven if di				
Restriction Register	When BL bi	it change f		"Off", backlig	Sta On, Idle	ned off	without gra	dual din	nming, e	ven if di				
	When BL bi	it change f	1	Normal Mode	Sta On, Idle On, Idle	ned off	without gra	dual din	nming, e vailabilii Yes	ven if di				
Register	When BL bi	it change f	1	Normal Mode Normal Mode	Sta On, Idle On, Idle	ned off	without gra Off, Sleep On, Sleep Off, Sleep ()	A Out Out Out	nming, e vailabilit Yes Yes	ven if di				
Register	When BL bi	it change f	1	Normal Mode Normal Mode Partial Mode	Sta On, Idle On, Idle	ned off	without gra Off, Sleep On, Sleep Off, Sleep ()	A Out Out Out	wailabilii Yes Yes Yes	ven if di				
Register	When BL bi	it change f	1	Normal Mode Normal Mode Partial Mode Partial Mode	Sta On, Idle On, Idle	ned off	without gra Off, Sleep On, Sleep Off, Sleep ()	A Out Out Out	vailabilii Yes Yes Yes Yes	ven if di				
Register	When BL bi	it change f	N	Normal Mode Normal Mode Partial Mode Partial Mode Sleep In	Sta On, Idle On, Idle	ned off	Off, Sleep On, S	A Out Out Out	vailabilii Yes Yes Yes Yes	ven if di				
Register	When BL bi	it change f	N	Normal Mode Normal Mode Partial Mode Partial Mode	Sta On, Idle On, Idle On, Idle	ned off	Off, Sleep On, S	Out Out Out	vailabilit Yes Yes Yes Yes Yes	ven if di				
Register Availability	When BL bi	it change f	1	Normal Mode Normal Mode Partial Mode Partial Mode Sleep In	Sta On, Idle On, Idle On, Idle	ned off	Off, Sleep On, S	dual din Out Out Out Out Out Out It Value	vailabilit Yes Yes Yes Yes Yes	ven if di				
Register	When BL bi	it change f	Power	Normal Mode Normal Mode Partial Mode Partial Mode Sleep In Status	Sta On, Idle On, Idle On, Idle	ned off atus Mode Mode Mode Mode Mode Mode Mode Mode	Off, Sleep On, Sleep Off, Sleep On, Sleep On, Sleep Defau Defau	dual din A Out Out Out Out Out Out Out Out Out Out	vailabilii Yes Yes Yes Yes Yes	ven if di				









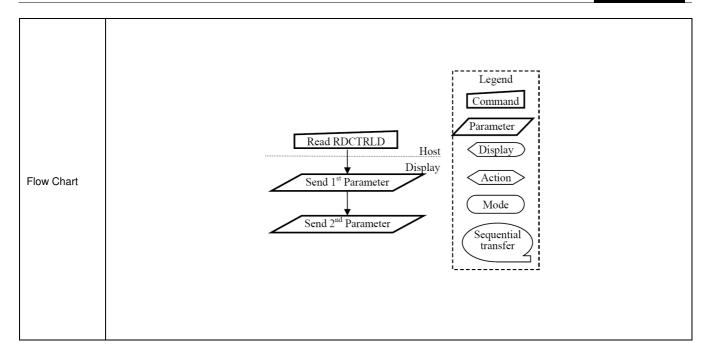


8.2.41. Read CTRL Display (54h)

54h					RDCTR	LD (Rea	d Control Dis	splay)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	<u> </u>	XX	0	1	0	1	0	1	0	0	54h
1 st Parameter	1	↑	1	XX	Χ	Х	Х	Χ	Х	Χ	Х	Χ	XX
2 nd Parameter	1	↑	1	XX	0	0	BCTRL	0	DD	BL	0	0	00
	BCTRL : E	Brightness Off (Brightne	Control Blo	n brightness ock On/Off, rs are 00h) rs are active			e DBV[70] p	arameto	ers.)				
Description	'0' = D		g ming is off ming is on										
				f backlight c	ircuit. C	ontrol lir	es must be lo	w.)					
Restriction	(= more th	nan 2 RDX	cycle) on I	DBI.			data lines if the	ne MCU	wants to	read m	nore tha	n one pa	arameter
Register Availability	Only 2nd parameter is sent on DSI (The 1st parameter is not sent). Status Availability Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes												
Default				Status er On Seque SW Reset HW Reset	nce	BCTR 1'b0 1'b0 1'b0	Default L D 1'1 1'1 1'1	D 00 00	B 1'1 1'1 1'1	00			











8.2.42. Write Content Adaptive Brightness Control (55h)

55h				WRCABC (\	Write C	ontent A	Adaptiv	e Bright	ness C	control)			
	D/CX	RDX	WRX	VRX D17-8 D7 D6 D5 D4					D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	1	0	1	0	1	0	1	55h
Parameter	1	1	1	XX	0	0	0	0	0	0	C [1]	C [0]	00
				parameters				•				•	ble
Description				CI	1:0]	Г	Default \	ا میراد/					
					000		Off						
					000	l lea		ce Imag	Δ				
					010	0301	Still Pic						
					011	N	Noving I						
					,			ago					
Restriction	None												
					9	Status			Ava	ilability			
			•	Normal Mod			e Off, S	leep Ou		Yes	1		
Register				Normal Mod	de On, I	dle Mod	e On, S	leep Ou	t '	Yes			
Availability				Partial Mod	le On, Id	dle Mode	e Off, SI	eep Out	,	Yes			
				Partial Mod	le On, Id	dle Mode	e On, SI	eep Out	,	Yes			
				Sleep In					,	Yes]		
Default				Power On	atus Sequel Reset Reset	nce		efault V C [1:0]=(C [1:0]=(C [1:0]=(00h 00h				
Flow Chart			,	WRC 1st parame New At Image	daptive		7			Leger Comm Parame Displ Action Mod Seque trans	and ster lay on le ntial		





8.2.43. Read Content Adaptive Brightness Control (56h)

56h			•	RDCABC (F					ess Cor	ntrol)			
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	1	0	1	0	1	1	0	56h
1 st Parameter	1	1	1	XX	Х	Х	Х	Х	Х	Х	Х	Х	XX
2 nd Parameter	1	<u>†</u>	1	XX	0	0	0	0	0	0	C [1]	C [0]	00
				the settings f	_			-	_			-	v .
Description				C	[1:0]	Г	Default \	/alue					
•					b00		Off						
					b01	User		ce Image	!				
					b10		Still Pic						
				2'	b11	N	loving I	mage					
Restriction	(= more th	nan 2 RDX	cycle) on	2nd paramet DBI. DSI (The 1st				es if the N	ICU wai	nts to re	ad more t	han one p	arameter
			L		St	atus			Availa	bility			
				Normal Mod					Ye	s			
Register			-	Normal Mod					Ye				
Availability				Partial Mode					Ye				
			-	Partial Mode	On, Idle	e Mode	On, Sle	ep Out	Ye				
			L	Sleep In					Ye	!S			
Default				Sta Power On SW F HW F	Sequen	се	C	efault Va (2 [1:0]=00 (2 [1:0]=00 (2 [1:0]=00)h)h				
Flow Chart				Read R Send 1 st I	Parame	eter	H Disp	ost lay	Par	egendomman ameter Display Action Mode	nd r		





8.2.44. Write CABC Minimum Brightness (5Eh)

5Eh					Backlight Control 1										
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	XX	0	1	0	1	1	1	1	0	5Eh		
Parameter	1	1	1	XX	CMB [7]	CMB [6]	CMB [5]	CMB [4]	CMB [3]	CMB [2]	CMB [1]	CMB [0]	00		
	This cor	nmand is	s used to	set the mir	imum brig	htness val	ue of the	display for	CABC fur	nction.					
	CMB[7:0	0]: CABC	minimum	n brightnes	s control,	this param	eter is use	ed to avoic	too much	brightne	ss reduction	on.			
	When C	ABC is a	active, CA	BC canno	t reduce t	he display	brightnes	s to less t	han CABO	minimur	n brightne	ss setting	. Image		
	process	ing funct	ion is wor	ked as nor	mal, even	if the brigh	ntness car	nnot be cha	anged.						
Description	This fur	nction do	es not af	ect to the	other fun	ction, mar	nual bright	tness setti	ng. Manu	al brightn	ess can b	e set the	display		
Bosonption	brightne	ess to les	s than CA	BC minim	C minimum brightness. Smooth transition and dimming function can be worked as normal.										
	When d	lisplay br	rightness	ntness is turned off (BCTRL=0 of "Write CTRL Display (53h)"), CABC minimum brightness setting is											
	ignored.														
In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means								eans the	highest						
	brightne	ss for CA	ABC.												
						Status	3		Availab	oility					
				Nor	mal Mode	On, Idle M	lode Off, S	Sleep Out	Yes	i					
Register				Nor	mal Mode	On, Idle M	lode On, S	Sleep Out	Yes	i					
Availability				Par	tial Mode	On, Idle M	ode Off, S	Sleep Out	Yes						
				Par	tial Mode	On, Idle M	ode On, S	Sleep Out	Yes						
				Sleep In Yes											
					Stat	us		Default Va							
				CMB [7:0]											
Default				<u> </u>	Power On Sequence 8'h00h										
	SW Reset No Change HW Reset 8'h00h														
					HW F	eset		8'h00h	1						





8.2.45. Read CABC Minimum Brightness (5Fh)

5Fh				Backlight Control 1										
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	XX	0	1	0	1	1	1	1	1	5Fh	
1 st Parameter	1	1	1	XX	X	Χ	Χ	X	Х	Х	X	Х	Χ	
2 nd Parameter	1	↑	1	XX	CMB	CMB	CMB	CMB	CMB	CMB	CMB	CMB	00	
		'			[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]		
	This cor	nmand re	eturns the	minimum	brightnes	s value of	CABC fur	nction.						
1	In princi	ple the re	elationshi	p is that 00)h value m	eans the	lowest briç	ghtness ar	nd FFh va	lue mean	s the high	est brightr	iess.	
Description	CMB[7:	D] is CA	3C minim	ium bright	ness spec	ified with	"Write CA	ABC minin	num brigh	itness (5l	∃h)" comn	nand. In p	rinciple	
	relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for													
CABC.														
						Status	3		Availab	oility				
				Norr	nal Mode	On, Idle M	lode Off, S	Sleep Out	Yes	3				
Register				Norr	nal Mode	On, Idle M	lode On, S	Sleep Out	Yes	S				
Availability				Part	ial Mode (On, Idle M	ode Off, S	leep Out	Yes	3				
				Part	ial Mode (On, Idle M	ode On, S	leep Out	Yes	3				
ı				Slee	p In				Yes	S				
					Sta	tus		Default V	alue					
					Jiu			CMB [7]	:0]					
Default				<u>_ F</u>	Power On	Sequence)	8'h00h	1					
					SW F	Reset		No Char	ige					
					HW F	Reset		8'h00h	1					





8.2.46. Read ID1 (DAh)

DAh					RDID1 (Read ID1)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX				
Command	0	1	1	XX	1	1	0	1	1	0	1	0	DAh				
1 st Parameter	1	1	1	XX	Χ	Х	Χ	Χ	Х	Χ	Χ	Х	Х				
2 nd Parameter	1	1	1	XX				ID1	[7:0]				00				
Description	The 1 st pa	aramete aramete	r is dum	he LCD module's r my data. I module's manufa			nd it is s	pecified	by User								
Restriction																	
Register Availability				Normal Mo Normal Mo Partial Mo Partial Mo	de On, de On, de On, de On,	ldle Mode dle Mode	On, Sle	ep Out ep Out	Availabi Yes Yes Yes Yes	lity							
Default			-	Status Power On Sequel SW Reset HW Reset		Before MT 8'h 8'h	00h 00h	am) (A		program alue alue)						
Flow Chart	SW Reset 8'h00h MTP value											Legend Command Carameter Display Action Mode					





8.2.47. Read ID2 (DBh)

DBh						RDID2	(Read ID	(2)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	0	1	1	0	1	1	DBh
1 st Parameter	1	1	1	XX	Х	Х	Х	Х	Х	Х	Х	Χ	Х
2 nd Parameter	1	1	1	XX				ID	2 [7:0]				00
Description	changes The 1 st pa	each tim aramete aramete can be p	ne a revis r is dumi er is LCD	rack the LCD m sion is made to t my data. module/driver v ned by MTP fund	he displa	ay, materia	al or const	ruction	specification	ons.		greement) and
Restriction													
Register Availability				Normal Partial	Mode O Mode O	Status n, Idle Mo n, Idle Mo n, Idle Mo n, Idle Mo Sleep In	de On, Sle de Off, Sle de On, Sle	eep Out	t Yes Yes	ility			
Default				Status Power On Sec SW Rese	et	(Before I	ault Value MTP progr 3'h80h 3'h80h		Default (After MTP MTP v MTP v	program) value value			
Flow Chart						ummy Reac					Pa D	egend mmand rameter isplay Action Mode	





8.2.48. Read ID3 (DCh)

DCh		RDID3 (Read ID3)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	XX	1	1	0	1	1	1	0	0	DCh	
1 st Parameter	1	1	1	XX	Χ	Χ	Χ	Х	X	Χ	Х	Х	Х	
2 nd Parameter	1	1	1	XX				ID	3 [7:0]				00	
	This re	ad byte	identifies	the LCD modu	le/driver a	nd It is sp	ecified by	User.						
	The 1 st	parame	eter is dun	nmy data.										
Description	The 2 nd	^a parame	eter is LC	D module/drive	r ID.									
	The ID	3 can be	e program	nmed by MTP fu	ınction.									
	X = Do	n't care												
Restriction														
						Status			Availat	oility				
				Norm	al Mode C		ode Off, S	Sleep O						
Register							ode On, S							
Availability							ode Off, S			3				
,				Partia	al Mode C	n, Idle M	ode On, S	leep Ou	ıt Yes	S				
						Sleep l	n		Yes	3				
				Statu	IS		fault Valu MTP pro		Defaul (After MTF	t Value P program)				
Default				Power On S			8'h00h			value				
				SW Re			8'h00h			value	_			
				HW Re	eset		8'h00h		MTP	value				
Flow Chart					RDID3(Dummy Rea					P P	egend command arameter Display Action Mode		



8.3. Description of Level 2 Command

8.3.1. RGB Interface Signal Control (B0h)

B0h	IFMODE (Interface Mode Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HE
Command	0	1	1	XX	1	0	1	1	0	0	0	0	B0ł
Parameter	1	1	1	xx	ByPass_MODE	RCM [1]	RCM [0]	0	VSPL	HSPL	DPL	EPL	40
	Sets th	e operat	ion statı	us of the display	interface. The sett	ing beco	mes effe	ective as	soon as	the comn	nand is	received	
	EPL: D	E polari	ty ("0"= I	High enable for I	RGB interface, "1"=	Low en	able for	RGB inte	erface)				
	DPL: D	OTCLK	polarity	set ("0"= data fe	tched at the rising	time, "1"	'= data fe	etched at	the fallin	ng time)			
	HSPL:	HSYNC	polarity	("0"= Low level	sync clock, "1"= Hi	gh level	sync clo	ck)					
	VSPL:	VSYNC	polarity	("0"= Low level	sync clock, "1"= Hi	gh level :	sync clo	ck)					
December	RCM [1:0]: RG	B interfa	ace selection (re	fer to the RGB inte	rface se	ction).						
Description													
	ByPas	s_MODI	E: Selec	t display data pa	th whether Memor	y or Dire	ect to Shi	ift registe	er when F	RGB Inter	face is ι	used.	
				ByPass_MODE		Disp	olay Data	a Path					
				0	Di	rect to SI	hift Regis	ster (def	ault)				
				1			Memor	у					
Restriction	EXTC	should b	e high to	o enable this cor	nmand								
					Status				vailability				
				Mormal				MIT I	Yes				
Register					Mode ON, Idle Mo								
_				Norma	Mode ON, Idle Me	ode ON,	Sleep O	UT	Yes Yes				
Register Availability				Norma Partial	Mode ON, Idle Mo Mode ON, Idle Mo Mode ON, Idle Mo	ode ON, de OFF, ode ON,	Sleep O Sleep O	UT	Yes Yes Yes				
_				Norma Partial	Mode ON, Idle Mo Mode ON, Idle Mo	ode ON, de OFF, ode ON,	Sleep O Sleep O	UT	Yes Yes				
-				Norma Partial	Mode ON, Idle Mo Mode ON, Idle Mo Mode ON, Idle Mo	ode ON, de OFF, ode ON,	Sleep O Sleep O Sleep Ol	UT UT UT	Yes Yes Yes				
-				Norma Partial	Mode ON, Idle Mo Mode ON, Idle Mo Mode ON, Idle Mo Sleep I	ode ON, de OFF, ode ON, s	Sleep O Sleep Ol Sleep Ol	UT UT UT Value	Yes Yes Yes Yes		- FDI		
Availability			Power	Norma Partial Partial	Mode ON, Idle Mo Mode ON, Idle Mo Mode ON, Idle Mo Sleep I	ode ON, de OFF, ode ON, N	Sleep O Sleep Ol Sleep Ol Default [1:0] V	UT UT UT Value	Yes Yes Yes Yes HSPL	DPL 1'h0	EPL 1'h1		
_				Norma Partial Partial	Mode ON, Idle Mo Mode ON, Idle Mo Mode ON, Idle Mo Sleep I	ode ON, de OFF, ode ON, s	Sleep O Sleep O Sleep Ol Default [1:0] V	Value (SPL 1'b0	Yes Yes Yes Yes	DPL 1'b0 1'b0	EPL 1'b1 1'b1		





8.3.2. Frame Rate Control (In Normal Mode/Full Colors) (B1h)

B1h		FRMCTR1 (Frame Rate Control (In Normal Mode / Full colors))											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	0	1	1	0	0	0	1	B1h
1 st Parameter	1	1	1	XX	0	0	0	0	0	0	DIVA	· [1:0]	00
2 nd Parameter									1B				

Formula to calculate frame frequency:

Frame Rate= $\frac{}{\text{Clocks per line } x \text{ Division ratio } x \text{ (Lines} + \text{VBP} + \text{VFP)}}$

Sets the division ratio for internal clocks of Normal mode at MCU interface.

fosc: internal oscillator frequency Clocks per line: RTNA setting Division ratio: DIVA setting Lines: total driving line number VBP: back porch line number VFP: front porch line number

	RTI	NA [4:0]		Frame Rate (Hz)
1	0	0	0	0	119
1	0	0	0	1	112
1	0	0	1	0	106
1	0	0	1	1	100
1	0	1	0	0	95
1	0	1	0	1	90
1	0	1	1	0	86
1	0	1	1	1	83

	RTI	NA [4:0]		Frame Rate (Hz)
1	1	0	0	0	79
1	1	0	0	1	76
1	1	0	1	0	73
1	1	0	1	1	70(default)
1	1	1	0	0	68
1	1	1	0	1	65
1	1	1	0	1	63
1	1	1	1	1	61

Description

DIVA [1:0]: division ratio for internal clocks when Normal mode.

DIVA	[1:0]	Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNA [4:0]: RTNA[4:0] is used to set 1H (line) period of Normal mode at MCU interface.

	RTI	NA [4:0]	Clock per Line	
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

	RTI	NA [4:0]	Clock per Line	
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

	KII	VA [4	4:0]	Clock per Line	
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks





Restriction	EXTC should be high to enabl	igh to enable this command				
	ſ		Status			Availability
		Nor	mal Mode ON, Idle Mode	OFF, Sleep	OUT	Yes
Register		Nor	mal Mode ON, Idle Mode	e ON, Sleep (TUC	Yes
Availability		Par	tial Mode ON, Idle Mode	OFF, Sleep (TUC	Yes
		Pai	rtial Mode ON, Idle Mode	ON, Sleep C	DUT	Yes
			Sleep IN			Yes
				Defe	l± \ / = l	
			Status	Defau DIVA [1:0]		e A [4:0]
Default			Power ON Sequence	2'b00		11Bh
			SW Reset	2'b00		11Bh
			HW Reset	2'b00		n1Bh
					<u> </u>	





8.3.3. Frame Rate Control (In Idle Mode/8 colors) (B2h)

B2h		FRMCTR2 (Frame Rate Control (In Idle Mode / 8I colors))											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	1	0	B2h
1 st Parameter	1	1 ↑ XX 0 0 0 0 0 DIVB[1:0] 00											
2 nd Parameter	1	1 ↑ XX 0 0 0 RTNB [4:0] 1B											

Formula to calculate frame frequency

Frame Rate= $\frac{\text{fosc}}{\text{Clocks per line } \text{x Division ratio x (Lines + VBP + VFP)}}$

Sets the division ratio for internal clocks of Idle mode at MCU interface.

fosc: internal oscillator frequency
Clocks per line: RTNB setting
Division ratio: DIVB setting
Lines: total driving line number
VBP: back porch line number
VFP: front porch line number

	RT	NB [4:0]	Frame Rate (Hz)	
1	0	0	0	0	119
1	0	0	0	1	112
1	0	0	1	0	106
1	0	0	1	1	100
1	0	1	0	0	95
1	0	1	0	1	90
1	0	1	1	0	86
1	0	1	1	1	83

	D.T.			5 . (1)	
	RII	NB [4:0]		Frame Rate (Hz)
1	1	0	0	0	79
1	1	0	0	1	76
1	1	0	1	0	73
1	1	0	1	1	70(default)
1	1	1	0	0	68
1	1	1	0	1	65
1	1	1	0	1	63
1	1	1	1	1	61

Description

DIVB [1:0]: division ratio for internal clocks when Idle mode.

DIVB	[1:0]	Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNB [4:0]: RTNB[4:0] is used to set 1H (line) period of Idle mode at MCU interface.

	RTI	NB [4:0]	Clock per Line	
				LITIE	
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

	RTI	NB [4:0]	Clock per Line	
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

	RTI	NB [4:0]	Clock per Line	
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks





Restriction	EXTC should be high to enable this command							
			Status			Availability		
		Nor	mal Mode ON, Idle Mode	e OFF. Sleep	OUT	Yes		
Register			rmal Mode ON, Idle Mod			Yes		
Availability		Par	tial Mode ON, Idle Mode	OFF, Sleep (TUC	Yes		
		Pa	rtial Mode ON, Idle Mode	e ON, Sleep C	DUT	Yes		
			Sleep IN			Yes		
			0	Defau	lt Valu	е		
			Status	DIVB [1:0]	RTN	IB [4:0]		
Default			Power ON Sequence	2'b00	5'l	n1Bh		
			SW Reset	2'b00	5'ł	n1Bh		
			HW Reset	2'b00	5'l	n1Bh		





8.3.4. Frame Rate control (In Partial Mode/Full Colors) (B3h)

B3h		FRMCTR3 (Frame Rate Control (In Partial Mode / Full colors))											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	0	1	1	0	0	1	1	B3h
1 st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVC	[1:0]	00
2 nd Parameter	1	1	1	XX	0	0	0		F	RTNC [4:0)]		1B

Formula to calculate frame frequency:

Frame Rate= $\frac{\text{fosc}}{\text{Clocks per line } \text{x Division ratio x (Lines + VBP + VFP)}}$

Sets the division ratio for internal clocks of Partial mode (Idle mode off) at MCU interface.

fosc: internal oscillator frequency
Clocks per line: RTNC setting
Division ratio: DIVC setting
Lines: total driving line number
VBP: back porch line number
VFP: front porch line number

	RTI	NC [4:0]	Frame Rate (Hz)	
1	0	0	0	0	119
1	0	0	0	1	112
1	0	0	1	0	106
1	0	0	1	1	100
1	0	1	0	0	95
1	0	1	0	1	90
1	0	1	1	0	86
1	0	1	1	1	83

	RTI	NC [4:0]	Frame Rate (Hz)	
1	1	0	0	0	79
1	1	0	0	1	76
1	1	0	1	0	73
1	1	0	1	1	70(default)
1	1	1	0	0	68
1	1	1	0	1	65
1	1	1	0	1	63
1	1	1	1	1	61

Description

DIVC [1:0]: division ratio for internal clocks when Partial mode.

DIVC	[1:0]	Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

Note: 1clock unit=1.625u sec

RTNC [4:0]: RTNC [4:0] is used to set 1H (line) period of Partial mode at MCU interface.

	RTI	NC [4:0]		Clock per Line			
0	0	0	0	0	Setting prohibited			
0	0	0	0	1	Setting prohibited			
0	0	0	1	0	Setting prohibited			
0	0	0	1	1	Setting prohibited			
0	0	1	0	0	Setting prohibited			
0	0	1	0	1	Setting prohibited			
0	0	1	1	0	Setting prohibited			
0	0	1	1	1	Setting prohibited			
0	1	0	0	0	Setting prohibited			
0	1	0	0	1	Setting prohibited			
0	1	0	1	0	Setting prohibited			

	RTI	NC [4:0]		Clock per Line				
					LITIE				
0	1	0	1	1	Setting prohibited				
0	1	1	0	0	Setting prohibited				
0	1	1	0	1	Setting prohibited				
0	1	1	1	0	Setting prohibited				
0	1	1	1	1	Setting prohibited				
1	0	0	0	0	16 clocks				
1	0	0	0	1	17 clocks				
1	0	0	1	0	18 clocks				
1	0	0	1	1	19 clocks				
1	0	1	0	0	20 clocks				
1	0	1	0	1	21 clocks				

	RTI	NC [4:0]	Clock per Line	
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks





Restriction	EXTC should be high to enable this command										
			Status			Availability					
		Nor	mal Mode ON, Idle Mode	e OFF, Sleep	OUT	Yes					
Register		Noi	rmal Mode ON, Idle Mod	e ON, Sleep (TUC	Yes					
Availability		Par	rtial Mode ON, Idle Mode	OFF, Sleep (TUC	Yes					
		Pa	rtial Mode ON, Idle Mode	e ON, Sleep C	DUT	Yes					
			Sleep IN			Yes					
			Status	Defau	lt Valu	е					
			Status	DIVC [1:0]	RTN	IC [4:0]					
Default			Power ON Sequence	2'b00	5'l	n1Bh					
		SW Reset 2'b00 5'h1Bh									
			HW Reset	2'b00	5'h	n1Bh					





8.3.5. Display Inversion Control (B4h)

B4h		INVTR (Display Inversion Control)											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h
1 st Parameter	1	1	↑	XX	0	0	0	0	0	NLA	NLB	NLC	02
	NLA: Ir	Display inversion mode set NLA: Inversion setting in full colors normal mode (Normal mode on) NLB: Inversion setting in Idle mode (Idle mode on)											
			_	full colors parti			do on / ld	la mada d	\ff\				
Description	NEG. II	iversion	setting iii	tuii colors parti		NLB / NLC 0 1	Line	version inversion e inversio					
Restriction	EXTC :	should be	e high to e	nable this com	mand								
Register Availability				Normal Partial N	Mode ON, Mode ON, Mode ON,	ldle Mode	ON, Sle	ep OUT	Availab Yes Yes Yes Yes	5 5			
Default				1	Sta Power ON SW F H/W I	Sequence Reset	NLA	Principle of the state of the s	NLC 1'b0 1'b0 1'b0				





8.3.6. Blanking Porch Control (B5h)

B5h	PRCTR (Blanking Porch)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
1 st Parameter	1	1	↑	XX	0				VFP [6:0]				02
2 nd Parameter	1	1	↑	XX	0				VBP [6:0]				02
3 rd Parameter	1	1	↑	XX	0	0	0			HFP [4:0]			0A
4 th Parameter	1	1	↑	XX	0	0	0			HBP [4:0]			14

VFP [6:0] / **VBP [6:0]:** The VFP [6:0] and VBP [6:0] bits specify the line number of vertical front and back porch period respectively.

VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch	VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch
0000000	Setting inhibited	1000000	64
0000001	Setting inhibited	1000001	65
0000010	2	1000010	66
0000011	3	1000011	67
0000100	4	1000100	68
0000101	5	1000101	69
0000110	6	1000110	70
0000111	7	1000111	71
0001000	8	1001000	72
0001001	9	1001001	73
0001010	10	1001010	74
0001011	11	1001011	75
0001100	12	1001100	76
0001101	13	1001101	77
:	:	:	:
:	:	:	:
0111101	61	1111101	125
0111110	62	1111110	126
0111111	63	1111111	127

Description

Note: VFP + VBP ≤ 254 HSYNC signals

HFP [4:0] / **HBP [4:0]:** The HFP [4:0] and HBP [4:0] bits specify the line number of horizontal front and back porch period respectively.

HFP [4:0] HBP [4:0]	Number of DOTCLK of the front/back porch
00000	Setting prohibited
00001	Setting prohibited
00010	2
00011	3
00100	4
00101	5
00110	6
00111	7
01000	8
01001	9
01010	10
01011	11
01100	12
01101	13
01110	14
01111	15

HFP [4:0] HBP [4:0]	Number of DOTCLK of front/back porch
10000	16
10001	17
10010	18
10011	19
10100	20
10101	21
10110	22
10111	23
11000	24
11001	25
11010	26
11011	27
11100	28
11101	29
11110	30
11111	31

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Restriction	EXTC should be high to enable this command								
				Status			Availabil	ity	
			Normal Mode	ON, Idle Mode	OFF, Sleep O	UT	Yes		
Register	Register			ON, Idle Mode	e ON, Sleep Ol	UT	Yes		
Availability			Partial Mode	ON, Idle Mode	OFF, Sleep OI	UT	Yes		
-			Partial Mode ON, Idle Mode ON, Sleep OUT						
			Sleep IN						
					Default	Value]
		S	tatus	VFP [6:0]	VBP [6:0]	HFF	P [4:0]	HBP [4:0]	
Default		Power O	N Sequence	7'h02h	7'h02h	5'h	ı0Ah	5'h14h	
		SW	Reset	7'h02h	7'h02h	5'h	ı0Ah	5'h14h	
		HW	Reset	7'h02h	7'h02h	5'h	ı0Ah	5'h14h	





8.3.7. Display Function Control (B6h)

B6h	DISCTRL (Display Function Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	0	1	1	0	1	1	0	B6h
1 st Parameter	1	1	1	XX	0	0	0	0	PTG	[1:0]	PT	[1:0]	0A
2 nd Parameter	1	1	1	XX	REV	GS	SS	SM		ISC	[3:0]		82
3 rd Parameter	1	1	1	XX	0	0			NL	[5:0]			27
4 th Parameter	1	1	1	XX	0	0		•	PCDI	V [5:0]			XX

PTG [1:0]: Set the scan mode in non-display area.

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	VCOM output
0	0	Normal scan	Set with the PT [2:0] bits	VCOMH/VCOML
0	1	Setting prohibited		
1	0	Interval scan	Set with the PT [2:0] bits	
1	1	Setting prohibited		

PT [1:0]: Determine source/VCOM output in a non-display area in the partial display mode.

ОТ	[4.0]	Source output or	non-display area	VCOM output on non-display area		
PT [1:0]		Positive polarity Negative polarity		Positive polarity	Negative polarity	
0	0	V63	V0	VCOML	VCOMH	
0	1	V0	V63	VCOML	VCOMH	
1	0	AGND	AGND	AGND	AGND	
1	1	Hi-Z	Hi-Z	AGND	AGND	

SS: Select the shift direction of outputs from the source driver.

SS	Source Output Scan Direction
0	S1 → S720
1	S720 → S1

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, and B dots to the source driver pins.

Description

To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0.

To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1.

REV: Select whether the liquid crystal type is normally white type or normally black type.

REV	Liquid crystal type
0	Normally black
1	Normally white

ISC [3:0]: Specify the scan cycle interval of gate driver in non-display area when PTG [1:0] ="10" to select interval scan.

Then scan cycle is set as odd number from 0~29 frame periods. The polarity is inverted every scan cycle.

ISC [3:0]	Scan Cycle	f _{FLM} = 60Hz
0000	1 frame	17ms
0001	3 frames	51ms
0010	5 frames	85ms
0011	7 frames	119ms
0100	9 frames	153ms
0101	11 frames	187ms
0110	13 frames	221ms
0111	15 frames	255ms



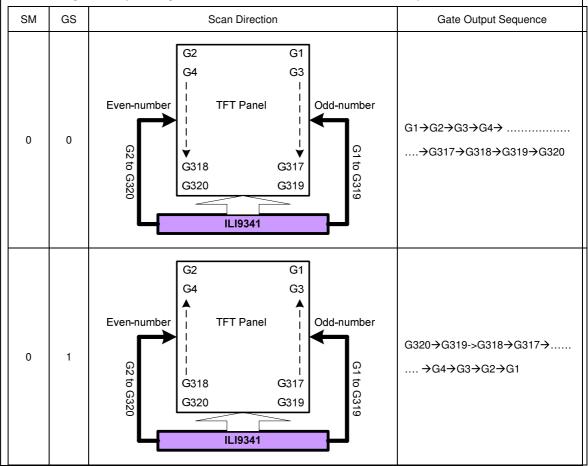


1000	17 frames	289ms
1001	19 frames	323ms
1010	21 frames	357ms
1011	23 frames	391ms
1100	25 frames	425ms
1101	27 frames	459ms
1110	29 frames	493ms
1111	31 frames	527ms

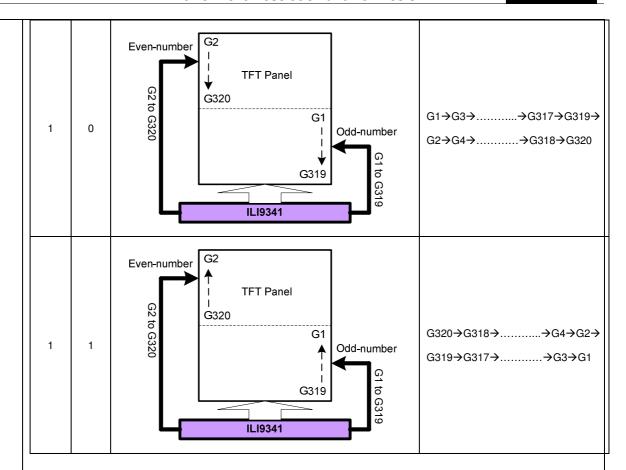
GS: Sets the direction of scan by the gate driver in the range determined by SCN [4:0] and NL [4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

GS	Gate Output Scan Direction			
0	G1 → G320			
1	G320 → G1			

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.







NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL [5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

		NL J	[5:0]	LCD Drive Line		
0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	1	16 lines
0	0	0	0	1	0	24 lines
0	0	0	0	1	1	32 lines
0	0	0	1	0	0	40 lines
0	0	0	1	0	1	48 lines
0	0	0	1	1	0	56 lines
0	0	0	1	1	1	64 lines
0	0	1	0	0	0	72 lines
0	0	1	0	0	1	80 lines
0	0	1	0	1	0	88 lines
0	0	1	0	1	1	96 lines
0	0	1	1	0	0	104 lines
0	0	1	1	0	1	112 lines
0	0	1	1	1	0	120 lines
0	0	1	1	1	1	128 lines
0	1	0	0	0	0	136 lines
0	1	0	0	0	1	144 lines
0	1	0	0	1	0	152 lines
0	1	0	0	1	1	160 lines
0	1	0	1	0	0	168 lines

		NL	[5:0]			LCD Driver Line
0	1	0	1	0	1	176 lines
0	1	0	1	1	0	184 lines
0	1	0	1	1	1	192 lines
0	1	1	0	0	0	200 lines
0	1	1	0	0	1	208 lines
0	1	1	0	1	0	216 lines
0	1	1	0	1	1	224 lines
0	1	1	1	0	0	232 lines
0	1	1	1	0	1	240 lines
0	1	1	1	1	0	248 lines
0	1	1	1	1	1	256 lines
1	0	0	0	0	0	264 lines
1	0	0	0	0	1	272 lines
1	0	0	0	1	0	280 lines
1	0	0	0	1	1	288 lines
1	0	0	1	0	0	296 lines
1	0	0	1	0	1	304 lines
1	0	0	1	1	0	312 lines
1	0	0	1	1	1	320 lines
		Oth	ers			Setting inhibited

PCDIV [5:0]:





	external fosc= $\frac{DOTCLK}{2 \times (PCDIV + 1)}$											
Restriction	EXTC should be high to ena	able thi	s command									
				Status				Availabi	lity			
Register			nal Mode ON					Yes				
Availability			nal Mode ON ial Mode ON					Yes Yes				
Availability			ial Mode ON					Yes				
				Sleep IN				Yes				
	Status		PTG [1:0]	PT [1:0]	REV	Default GS	Value SS	SM	10.01 0.01	NII [5:0]		
Default	Power ON Sequ	ence	2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	ISC [3:0] 4'b0010	NL [5:0] 6'h27h		
	SW Reset		2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'b0010	6'h27h		
	HW Reset		2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'b0010	6'h27h		





B7h					E	TMOD (E	ntry Mode	e Set)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HE
Command	0	1	1	XX	1	0	1	1	0	1	1	1	B7l
Parameter	1	1	1	XX	0	0	0	0	0	GON	DTE	GAS	06
	GAS: I	_ow volta	age detect	ion control.	GAS 0 1	Lo	w voltage (Enab Disab	le					
								-					
Description	GON/F	NTE: Sat	the output	t level of gate	a driver G1	~ G330 a	followe						
	GON/L	TE. Set	trie outpu	l level of gat				2-1- 0-1					
					GON 0	DTE C	61~G320 (out				
		0 0 VGH 0 1 VGH											
					1	0		GL					
					1	1		display					
Restriction	EXTC	should b	e high to e	enable this co	ommand								
						Ctatus			A.,-!!-	hilit:			
				Norma	al Mode ON	Status Idle Mod	e OFF SI	en OHT	Availa Ye				
Register					al Mode ON				Ye				
					I Mode ON,				Ye				
Availability									Ye				
		Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes											
						efault Val	ue						
					Sta	itus	GON	DTE	GAS				
Default					Power ON	Segueno		1'b1	1'b0				
						Reset	1'b1	1'b1	1'b0				
	1							1	. 23				

1'b1 1'b1 1'b0

HW Reset





8.3.9. Backlight Control 1 (B8h)

B8h				•		Ва	acklig	ht Cor	ntrol 1				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	0	1	1	1	0	0	0	B8h
Parameter		1	1	XX	0	0	0	0	TH_UI [3]	TH_UI [2]	TH_UI [1]	TH_UI [0]	0C
	TH_UI [3	(UI) m		atio of max	dimum	_	_	-		umulate histo isplay image			
			[3:0]		Descr	iption		TH_UI	[3:0]	Description			
Description			4'0h	99%					4'8		84%		
	4'1h				98%					h	82%		
			4'2h	1	96%				4'A	h	80%		
1			4'3h	1	94%				4'B	4'Bh			
			4'4h	1		92	%		4'C	h	76%		
			4'5h		90%				4'D		74%		
			4'6h		88%				4'E		72%		
			4'7h	1	86%				4'F	h	70%		
						St	atus			Availability			
									Sleep Out	Yes			
Register									Sleep Out	Yes			
Availability									Sleep Out	Yes	_		
						On, Idle	e Mod	e On,	Sleep Out	Yes			
				Sleep In	1					Yes			
				Status					Default Va				
Default				P	ower (On Sec	quence	е	4'b0110				
					SV	V Res	et		No chang	je			
					Н۱	V Res	et		4'b0110				





8.3.10. Backlight Control 2 (B9h)

B9h		Backlight Control 2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	XX	1	0	1	1	1	0	0	1	B9h	
Parameter	1	1	↑	XX	TH_MV [3]	TH_MV [2]	TH_MV [1]	TH_MV [0]	TH_ST [3]	TH_ST [2]	TH_ST [1]	TH_ST [0]	СС	

TH_ST [3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the still picture mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

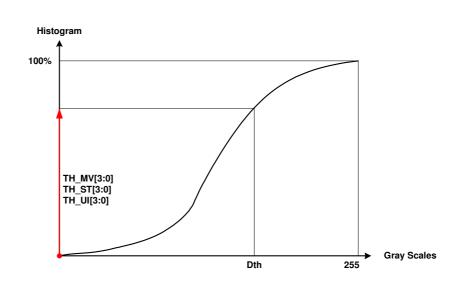
TH_ST [3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

TH_ST [3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%

TH_MV [3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the moving image mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

TH_MV [3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

TH_MV [3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%







		Status	Availability
	Normal Mode On	n, Idle Mode Off, Sleep Out	Yes
Register	Normal Mode On	n, Idle Mode On, Sleep Out	Yes
Availability	Partial Mode On.	, Idle Mode Off, Sleep Out	Yes
	Partial Mode On.	, Idle Mode On, Sleep Out	Yes
	Sleep In		Yes
	Ctatus	Default Va	llue
	Status	TH_MV [3:0]	TH_ST [3:0
Default	Power On Sequence	4'b1100	4'b1100
	SW Reset	No change	No change
	HW Reset	4'b1100	4'b1100





8.3.11. Backlight Control 3 (BAh)

BAh	Backlight Control 3												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	0	1	1	1	0	1	0	BAh
Parameter	1 1 ↑ XX 0 0 0 0 DTH_UI DTH_UI DTH_UI DTH_UI DTH_UI [0]										DTH_UI [0]	04	
	DTH_UI		•						0,		value in User I	, ,	

	DTH_UI [3:0]	Description
Description	4'0h	252
·	4'1h	248
	4'2h	244
	4'3h	240
	4'4h	236
	4'5h	232
	4'6h	228
	4'7h	224

the display quality is not acceptable.

DTH_UI [3:0]	Description
4'8h	220
4'9h	216
4'Ah	212
4'Bh	208
4'Ch	204
4'Dh	200
4'Eh	196
4'Fh	192

	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Register	Normal Mode On, Idle Mode On, Sleep Out	Yes
Availability	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Status	Default Value DTH_UI [3:0]
Power On Sequence	4'b0100
SW Reset	No change
HW Reset	4'b0100





8.3.12. Backlight Control 4 (BBh)

BBh						Bacl	klight Con	trol 4					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	0	1	1	1	0	1	1	BBh
Parameter	1	1	1	XX	DTH_MV [3]	DTH_MV [2]	DTH_MV [1]	DTH_MV [0]	DTH_ST [3]	DTH_ST [2]	DTH_ST [1]	DTH_ST [0]	65

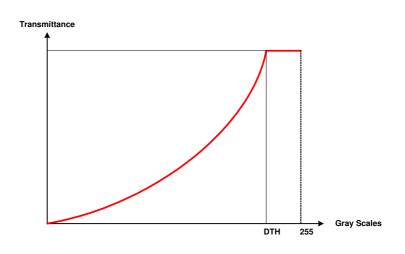
DTH_ST [3:0]/DTH_MV [3:0]: This parameter is used set the minimum limitation of grayscale threshold value. This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not acceptable.

DTH_ST [3:0]	Description
4'0h	224
4'1h	220
4'2h	216
4'3h	212
4'4h	208
4'5h	204
4'6h	200
4'7h	196

DTH_ST [3:0]	Description
4'8h	192
4'9h	188
4'Ah	184
4'Bh	180
4'Ch	176
4'Dh	172
4'Eh	168
4'Fh	164

DTH_MV [3:0]	Description
4'0h	224
4'1h	220
4'2h	216
4'3h	212
4'4h	208
4'5h	204
4'6h	200
4'7h	196

Description
192
188
184
180
176
172
168
164



Register
Availability

Description

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes





		Otatasa	Default Value		
	Status	DTH_MV [3:0]	DTH_ST [3:0]		
Default		Power On Sequence	4'b0110	4'b0101	
		SW Reset	No change	No change	
		HW Reset	4'b0110	4'b0101	





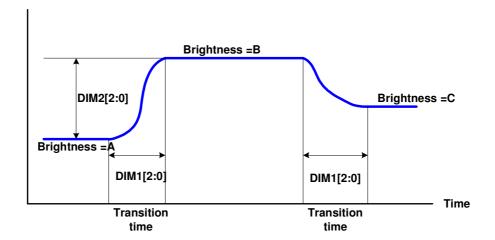
8.3.13. Backlight Control 5 (BCh)

BCh						Backl	ight Contr	ol 5					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	0	1	1	1	1	0	0	BCh
Parameter	1	1	1	XX	DIM2 [3]	DIM2 [2]	DIM2 [1]	DIM2 [0]	0	DIM1 [2]	DIM1 [1]	DIM1 [0]	44

DIM1 [2:0]: This parameter is used to set the transition time of brightness level to avoid the sharp brightness transition on vision.

DIM1 [2:0]	Description
3'0h	1 frame
3'1h	1 frame
3'2h	2 frames
3'3h	4 frames
3'4h	8 frames
3'5h	16 frames
3'6h	32 frames
3'7h	64 frames

Description



DIM2 [3:0]: This parameter is used to set the threshold of brightness change.

When the brightness transition difference is smaller than DIM2 [3:0], the brightness transition will be ignored.

For example:

If | brightness B - brightness A| < DIM2 [2:0], the brightness transition will be ignored and keep the brightness A.

	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Register	Normal Mode On, Idle Mode On, Sleep Out	Yes
Availability	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

	Chahua	Default	: Value
	Status	DIM2 [3:0]	DIM1 [2:0]
Default	Power On Sequence	4'b0100	4'b0100
	SW Reset	No change	No change
	HW Reset	4'b0100	4'b0100





8.3.14. Backlight Control 7 (BEh)

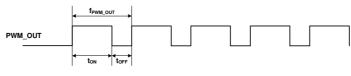
BEh		Backlight Control 7													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	XX	1	0	1	1	1	1	1	0	BEh		
Parameter	1	1	1	XX	PWM_ DIV[7]	PWM_ DIV[6]	PWM_ DIV[5]	PWM_ DIV[4]	PWM_ DIV[3]	PWM_ DIV[2]	PWM_ DIV[1]	PWM_ DIV[0]	0F		

PWM_DIV [7:0]: PWM_OUT output frequency control. This command is used to adjust the PWM waveform frequency of

PWM_OUT. The PWM frequency can be calculated by using the following equation.

$$f_{PWM_OUT} = \frac{16MHz}{(PWM_DIV[7:0]+1)\times255}$$

PWM_DIV [7:0]	f _{PWM_OUT}
8'h0	62.74 KHz
8'h1	31.38 KHz
8'h2	20.915KHz
8'h3	15.686KHz
8'h4	12.549 KHz
8'hFB	249Hz
8'hFC	248Hz
8'hFD	247Hz
8'hFE	246Hz
8'hFF	245Hz



Note: The output frequency tolerance of internal frequency divider in CABC is ±10%

Register
Availability

Description

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Default Value
PWM_DIV [7:0]=0Fh
No change
PWM_DIV [7:0]=0Fh





8.3.15. Backlight Control 8 (BFh)

BFh		,		JI U (L	,		Rad	sklight Co	ntro	al 2					
DFII														D0	HEX
Command	0	1	VV \\ \^	XX	1	0	1	1		1	1	-	1	1	BFh
Parameter	1	1	<u> </u>	XX									EDONPOL	LEDPWMPOL	00
)I:The			efine polarit			signa						1
]	BL	LEDPWMI				EDPW	Main				
					0	0	FUL		L	0	и ри				
					0	1				1					
					1	0		Origin	al po	olarity (of PWM	signa	I		
					1	1		Invers	ed p	olarity	of PWM	signa	ıl		
	LEDO	NPOL	: This b	t is used	to co	ntrol LEDON	l pin.								
					BL	LEDONP	OL		L	EDON	pin				
Description					0	0				0					
Description					0	1				1					
	1 0 LEDONR														
		1 1 Inversed LEDONR													
	LEDO	NR: T	his bit is	used to	contro	l LEDON pi	n.								
					LEDONR			D		ription					
					F	0			Lo						
					L	1			Hiç	gh					
							Sta	itue			Δν	ailabili	tv		
					Nori	mal Mode O			f. Sle	еер Оц	_	Yes	i.y		
Register						mal Mode O						Yes			
Availability						tial Mode O						Yes			
					Par	tial Mode O	n, Idle	Mode On	ı, Sle	eep Ou	t	Yes			
					Slee	p In						Yes			
					0	tatue			D	efault '	Value				
					Status			EDONR	LE	DONP	OL LI	EDPW	/MPOL		
Default				Po		n Sequence		1'b0		1'b0		1'k			
						Reset	No	change	No	o chan	ge		ange		
					HW	Reset		1'b0		1'b0		1't	00		
]														





8.3.16. Power Control 1 (C0h)

C0h	PWCTRL 1 (Power Control 1)																		
	D/CX	RDX	WRX	D	17-8			07 D6	D5)4		D3		D2	D1	D0	HEX
Command	0	1	↑		XX			1 1	0			0		0		0	0	0	C0h
1 st Parameter	1	1	↑		XX		(0 0						VRI	H [5:	0]			21
	VRH [5	::0]: Set	the GVD	D leve	, whi	ch is	a re	eference level	for the	VC	ОΜΙ	evel	and	the	gray	/scale	e voltage l	evel.	
				VRH	l [5:0]		GVDD		[V	RH	[5:0			GVDD		
			0	0 0	0	0	0	Setting prohi			1		0	0	0	0	4.45 V		
			0	0 0	0	1	0	Setting prohi			1		0	0	1	0	4.50 V 4.55 V		
			0	0 0	0	1	1	3.00 V	biteu		1		0	0	1	1	4.60 V		
			0	0 0	1	0	0	3.05 V			1	0	0	1	0	0	4.65 V		
			0	0 0	1	0	1	3.10 V			1		0	1	0	1	4.70 V		
			0	0 0	1	1	1	3.15 V 3.20 V			1		0	1	1	0	4.75 V 4.80 V		
			0	0 1	0	0	0	3.25 V			1	0	1	0	0	0	4.85 V		
			0	0 1	0	0	1	3.30 V			1	0	1	0	0	1	4.90 V		
			0	0 1	0	1	1	3.35 V 3.40 V			1	0	1	0	1	0	4.95 V 5.00 V		
			0	0 1	1	0	0	3.45 V			1	0	1	1	0	0	5.05 V		
			0	0 1	1	0	1	3.50 V			1	0	1	1	0	1	5.10 V		
			0	0 1	1	1	1	3.55 V 3.60 V			1	0	1	1	1	0	5.15 V 5.20 V		
Description			0	1 0	0	0	0	3.65 V			1		0	0	0	0	5.25 V		
			0	1 0	0	0	1	3.70 V			1		0	0	0	1	5.30 V		
			0	1 0	0	1	0	3.75 V			1		0	0	1	0	5.35 V		
			0	1 0 1 0	1	0	0	3.80 V 3.85 V			1		0	0	0	0	5.40 V 5.45 V		
			0	1 0	1	0	1	3.90 V			1		0	1	0	1	5.50 V		
			0	1 0	1	1	0	3.95 V			1		0	1	1	0	5.55 V		
			0	1 0 1 1	0	0	0	4.00 V 4.05 V			1	1	0	0	0	0	5.60 V 5.65 V		
			0	1 1	0	0	1	4.10 V		•	1		1	0	0	1	5.70 V		
			0	1 1	0	1	0	4.15 V			1	1	1	0	1	0	5.75 V		
			0	1 1	1			4.20 V 4.25 V			1	1	1	1	0	0	5.80 V 5.85 V		
			0	1 1	1	0	1	4.23 V 4.30 V			1		1	1	0	1	5.90 V		
			0	1 1	1	1	0	4.35 V			1	1	1	1	1	0	5.95 V		
			0	1 1	1	1	1	4.40 V			1	1	1	1	1	1	6.00 V		
	Note1:	Make sı	ure that \	/C and	VRH	sett	ting r	estriction: GVI	$DD \leq ($	DD	VDF	l - 0.2	2) V.						
Restriction	EXTC :	should b	e high to	enable	this	com	ıman	d											
								Status					Α	vaila	abilit	y			
Deviates					Norr	nal I	Mode	ON, Idle Mod	le OFF,	, Sle	еер (TUC		Ye	es				
Register				-	Nor	mal	Mode	e ON, Idle Mod	de ON,	Sle	ер (DUT	_	Ye	es				
Availability				L				ON, Idle Mod						Ye					
				-	Par	tial N	Mode	ON, Idle Mod		Sle	ep C	UT		Ye					
				L				Sleep IN						Ye	es				
										_	,								
								Status				t Valu	ıe						
Default		VRH [5:0] Power ON Sequence 6'h21h																	
Delault							10	ower ON Sequ SW Reset				<u>21h</u> 21h							
								HW Reset				21n 21h							
	Ī						Щ	TIVV TICSEL			UII	<u>- 111</u>							





8.3.17. Power Control 2 (C1h)

C1h	PWCTRL 2 (Power Control 2)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h
Parameter	1	1	1	XX	0	0	0	0	0		BT [2:0]		10
Description	BT [2:0]: Sets the factor used in the step-up circuits. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.												
Restriction	EXTC s	should b	e high to	enable this con	nmand								
Register Availability				Normal Partial N	Mode ON, Mode ON, Mode ON,	, Idle Mod Idle Mode	e ON, Sle OFF, Sle	eep OUT eep OUT	Availal Yes Yes Yes Yes	6			
Default					Power	Status ON Seque W Reset W Reset		efault Val BT [2:0] 3'b000 3'b000 3'b000	ue				





0010001

0010010

0010011

-2.075

-2.050

-2.025

C5h	VMCTRL1 (VCOM Control 1)														
	D/CX	RDX	WRX	D.	17-8	D7	' D6		05 D4	D3	D2	2	D1	D0	HEX
Command	0	1	↑	X		1	1		0 0	0	1	1	0	1	C5ł
1 st Parameter	1	1	<u> </u>		XX	0				VMH [6:0]					31
2 nd Parameter	1 1		1		XX	0				VML [6:0]					3C
	VMH [6:0]: Set the VCOMH voltage.														
	VMH [6:0]		VCOMH(V)		VMH [6	6:0]	VCOMH(V)		VMH [6:0]	VCOMH(V)		VMH [6:0]	VCOM	IH(V)
		00000	2.700		01000	_	3.500		1000000	4.300	ŕ		1100000	5.1	_ ` _
	0000001		2.725		01000		3.525	-	1000001	4.325		L	1100001	5.1	
		0010	2.750 2.775		01000		3.550 3.575	-	1000010 1000011	4.350 4.375		-	1100010	5.1 5.1	
	0000011 0000100		2.775		0100011		3.600		1000011	4.400			1100110	5.2	
		0101	2.825		0100101		3.625		1000101	4.425			1100101	5.2	
		0110	2.850		0100110		3.650		1000110	4.450			1100110	5.2	
	l -	0111	2.875 2.900		0100111		3.675	-	1000111	4.475		-	1100111	5.2	
	0001000 0001001		2.900		0101000		3.700 3.725		1001000 1001001	4.500 4.525			1101000	5.3 5.3	
Description	l -	1010	2.950		01010		3.750		1001001	4.550		-	1101010	5.3	
	0001011		2.975		01010	11	3.775		1001011	4.575			1101011	5.3	
		1100	3.000		01011		3.800	1	1001100	4.600			1101100	5.4	
		11101	3.025		01011		3.825		1001101	4.625			1101101	5.4 5.4	
)1110)1111	3.050 3.075		01011		3.850 3.875	1	1001110 1001111	4.650 4.675		-	1101111	5.4	
		0000	3.100	1	01100		3.900	1	1010000	4.700		-	1110000	5.5	
		0001	3.125		01100		3.925		1010001	4.725			1110001	5.5	25
		0010	3.150		01100		3.950		1010010	4.750		-	1110010	5.5	
	l -	0011 0100	3.175 3.200	-	01100		3.975 4.000	-	1010011 1010100	4.775 4.800		-	1110011 1110100	5.5 5.6	
		0101	3.225	1	01101		4.000	1	1010100	4.825		-	1110101	5.6	
		0110	3.250		01101		4.050		1010110	4.850			1110110	5.6	
		0111	3.275		01101		4.075		1010111	4.875			1110111	5.6	
		1000	3.300	-	01110		4.100	1	1011000	4.900		-	1111000	5.7	
		1001 1010	3.325 3.350	1	01110		4.125 4.150	1	1011001 1011010	4.925 4.950		-	1111001	5.7 5.7	
		1011	3.375	1	01110		4.175		1011011	4.975		-	1111011	5.7	
	001	1100	3.400		01111		4.200		1011100	5.000			1111100	5.8	
		1101	3.425	1	01111		4.225	-	1011101	5.025			1111101	5.8	
		1110 1111	3.450 3.475	1	01111		4.250 4.275		1011110 1011111	5.050 5.075		-	11111111	5.8 5.8	
	001		0.470		01111	,	7.275	j	1011111	3.073		L		3.0	7.5
	VML [6:0] : Set the VCOML voltage														
		/IL [6:0]	VCOML(V)		VML [VCOML(V)		VML [6:0]	VCOML(V	/)		VML [6:0]	VCOM	
		000000	-2.500	\dashv	01000		-1.700	-	1000000	-0.900			1100000	-0.10	
		00001	-2.475 -2.450	\dashv	01000		-1.675 -1.650	-	1000001 1000010	-0.875 -0.850			1100001 1100010	-0.07 -0.05	
		00011	-2.425)11	-1.625		1000010	-0.825			1100010	-0.03	
	00	00100	-2.400		0100		-1.600		1000100	-0.800			1100100	0	
		00101	-2.375		0100		-1.575	-	1000101	-0.775		_	1100101	Reserv	
		00110	-2.350	4	0100		-1.550 1.525	-	1000110	-0.750 -0.725		_	1100110	Reserv	
		00111	-2.325 -2.300	\exists	0100		-1.525 -1.500	1	1000111 1001000	-0.725	=		1100111 1101000	Reserv	
		01001	-2.275	1	01010		-1.475	1	1001000	-0.675			1101000	Reserv	
	00	01010	-2.250		01010)10	-1.450		1001010	-0.650			1101010	Reserv	ed_
		01011	-2.225	4	01010		-1.425	-	1001011	-0.625	_		1101011	Reserv	
		01100	-2.200 -2.175	\dashv	0101		-1.400 -1.375	1	1001100	-0.600 -0.575	_		1101100	Reserv	
		01101 01110	-2.175 -2.150	-	0101		-1.375 -1.350	1	1001101 1001110	-0.575 -0.550	=		1101101 1101110	Reserv Reserv	
		01111	-2.125		0101		-1.325		1001111	-0.525			1101111	Reserv	
	00	10000	-2.100		01100		-1.300		1010000	-0.500		_	1110000	Reserv	
	1 00	10001	-2 075		01100	nn 1	-1 275	1	1010001	-0 475	1	1	1110001	Resen	٠,٠٠

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-1.275

-1.250

-1.225

1010001

1010010

1010011

-0.475

-0.450

-0.425

1110001

1110010

1110011

Reserved

Reserved

Reserved

0110001

0110010

0110011





	0010100	-2.000	0110100	-1.200		1010100		0.400		1110100	Dogonical	7 7
											Reserved	-
	0010101	-1.975 -1.950	0110101	-1.175	-	1010101		0.375 0.350	-	1110101	Reserved	-
	0010110		0110110	-1.150 -1.125	-	1010110		0.350		1110110	Reserved	_
	0010111	-1.925	0110111		_	1010111				1110111	Reserved	-
	0011000 0011001	-1.900 -1.875	0111000 0111001	-1.100 -1.075	_	1011000	_	0.300		1111000 1111001	Reserved	-
	0011001	-1.850			_					1111001	Reserved	-
	0011010	-1.825	0111010	-1.050 -1.025		1011010		0.250		1111010	Reserved Reserved	
	0011011	-1.825	0111100	-1.025		10111011		0.200		11111011	Reserved	
	0011101	-1.775	0111101	-0.975		1011101	_	0.200		1111100	Reserved	
	0011101	-1.750	0111110	-0.975		1011110		0.175		1111110	Reserved	
	0011110	-1.725	0111111	-0.930		1011111		0.125		11111111		
	0011111	-1.725	0111111	-0.925		1011111		0.125		11111111	Reserved	_
5	=\/=0 ! !!!											
Restriction	EXTC should be	high to enabl	le this comman	d								
				Status		Availabili	tv					
			Normal Mode			EE Sloop O		Yes	Ly			
Register												
1109.010.			Normal Mode		Yes							
Availability			Partial Mode	ON, Idle Mo	de OF	F, Sleep Ol	UT	Yes				
			Partial Mode	ON, Idle Mo	de O	N, Sleep OL	JT	Yes				
				Sleep I	N			Yes				
									l			
			Sta	Value								
			Status VMH [6:0]					[6:0]				
Default			Power ON Sequence 7'h31				7'h	3C				
			· · · · · · · · · · · · · · · · · · ·					3C				
			SW Reset 7'h31 HW Rest 7'h31									
			HW	nest	/	1131	<i>i</i> r	3C				



Description

a-Si TFT LCD Single Chip Driver 240RGBx320 Resolution and 262K color



8.3.19. VCOM Control 2(C7h)

C7h					VM	CTRL1 (VCOM Co	ontrol 1)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	1	1	C7h
Parameter	1	1	1	XX	nVM	VMF [6:0]							

nVM: nVM equals to "0" after power on reset and VCOM offset equals to program MTP value. When nVM set to "1", setting of VMF [6:0] becomes valid and VCOMH/VCOML can be adjusted.

VMF [6:0]: Set the VCOM offset voltage.

F [6:0]: Set the \	COM offset	voltage.				
	VMF[6:0]	VCOMH	VCOML	VMF[6:0]	VCOMH	VCOML
	0000000	VMH	VML	1000000	VMH	VML
	0000001	VMH - 63	VML - 63	1000001	VMH + 1	VML + 1
	0000010	VMH - 62	VML - 62	1000010	VMH + 2	VML + 2
	0000011	VMH - 61	VML - 61	1000011	VMH + 3	VML + 3
	0000100	VMH - 60	VML - 60	1000100	VMH + 4	VML + 4
	0000101	VMH – 58	VML – 58	1000101	VMH + 5	VML + 5
	0000110	VMH – 58	VML – 58	1000110	VMH + 6	VML + 6
	0000111	VMH – 57	VML – 57	1000111	VMH + 7	VML + 7
	0001000	VMH – 56	VML – 56	1001000	VMH + 8	VML + 8
	0001001	VMH – 55	VML – 55	1001001	VMH + 9	VML + 9
	0001010	VMH – 54	VML – 54	1001010	VMH + 10	VML + 10
	0001011	VMH – 53	VML – 53	1001011	VMH + 11	VML + 11
	0001100	VMH – 52	VML – 52	1001100	VMH + 12	VML + 12
	0001101	VMH – 51	VML -51	1001101	VMH + 13	VML + 13
	0001110	VMH – 50	VML – 50	1001110	VMH + 14	VML + 14
	0001111	VMH – 49	VML – 49	1001111	VMH + 15	VML + 15
	0010000	VMH – 48	VML – 48	1010000	VMH + 16	VML + 16
	0010001	VMH – 47	VML – 47	1010001	VMH + 17	VML + 17
	0010010	VMH – 46	VML – 46	1010010	VMH + 18	VML + 18
	0010011	VMH – 45	VML – 45	1010011	VMH + 19	VML + 19
	0010100	VMH – 44	VML – 44	1010100	VMH + 20	VML + 20
	0010101	VMH – 43	VML – 43	1010101	VMH + 21	VML + 21
	0010110	VMH – 42	VML – 42	1010110	VMH + 22	VML + 22
	0010111	VMH – 41	VML – 41	1010111	VMH + 23	VML + 23
	0011000	VMH – 40	VML – 40	1011000	VMH + 24	VML + 24
	0011001	VMH – 39	VML – 39	1011001	VMH + 25	VML + 25
	0011010	VMH – 38	VML – 38	1011010	VMH + 26	VML + 26
	0011011	VMH – 37	VML – 37	1011011	VMH + 27	VML + 27
	0011100	VMH – 36	VML – 36	1011100	VMH + 28	VML + 28
	0011101	VMH – 35	VML – 35	1011101	VMH + 29	VML + 29
	0011110	VMH – 34	VML – 34	1011110	VMH + 30	VML + 30
	0011111	VMH – 33	VML – 33	1011111	VMH + 31	VML + 31
	0100000	VMH – 32	VML – 32	1100000	VMH + 32	VML + 32
	0100001	VMH – 31	VML – 31	1100001	VMH + 33	VML + 33
	0100010	VMH – 30	VML – 30	1100010	VMH + 34	VML + 34
	0100011	VMH – 29	VML – 29	1100011	VMH + 35	VML + 35
	0100100	VMH – 28 VMH – 27	VML - 28	1100100	VMH + 36	VML + 36
	0100101		VML - 27	1100101	VMH + 37	VML + 37
	0100110	VMH - 26	VML – 26 VML – 25	1100110	VMH + 38	VML + 38
	0100111	VMH – 25 VMH – 24		1100111	VMH + 39	VML + 39 VML + 40
	0101000 0101001	VMH – 24 VMH – 23	VML – 24 VML – 23	1101000 1101001	VMH + 40 VMH + 41	VML + 40 VML + 41
	0101001	VMH – 23	VML – 23		VMH + 42	VML + 41
	0101010	VMH – 21	VML – 22	1101010	VMH + 43	VML + 42
	01011100	VMH – 20	VML – 21	1101011 1101100	VMH + 44	VML + 44
	0101100	VMH – 20	VML – 20	1101101	VMH + 45	VML + 45
	0101110	VMH – 18	VML – 19	1101110	VMH + 46	VML + 45
	0101111	VMH – 17	VML – 17	1101111	VMH + 47	VML + 47
	0110000	VMH – 16	VML – 17	1110000	VMH + 48	VML + 47
	0110000	VMH – 15	VML – 15	1110000	VMH + 49	VML + 49
	0110001	VMH – 14	VML – 13	1110001	VMH + 50	VML + 50
	0110010	VMH – 13	VML – 14	1110010	VMH + 51	VML + 51
	0110100	VMH – 12	VML – 12	1110100	VMH + 52	VML + 51
	00100	7.17.1. 12	7 1VIL 12		*	*

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	0110101 0110110 0110111 0111000 0111001 0111010 0111011 0111100 0111101 0111110	VMH - 10 VMH - 9 VMH - 8 VMH - 7 VMH - 6 VMH - 5 VMH - 4 VMH - 3 VMH - 2	VML - 11 VML - 10 VML - 9 VML - 8 VML - 7 VML - 6 VML - 5 VML - 4 VML - 3 VML - 2		1110101 1110110 1110111 1111000 1111001 1111010 1111101 1111100 1111101	VM VM VM VM	IH + 53 IH + 54 IH + 55 IH + 56 IH + 57 IH + 58 IH + 59	VML + 53 VML + 54 VML + 55 VML + 56 VML + 57 VML + 58 VML + 59		
	0110111 0111000 0111001 0111010 0111011 0111100 0111101	VMH - 9 VMH - 8 VMH - 7 VMH - 6 VMH - 5 VMH - 4 VMH - 3 VMH - 2	VML - 9 VML - 8 VML - 7 VML - 6 VML - 5 VML - 4 VML - 3		1110111 1111000 1111001 1111010 1111011 1111100	VM VM VM VM	IH + 55 IH + 56 IH + 57 IH + 58 IH + 59	VML + 55 VML + 56 VML + 57 VML + 58		
	0111000 0111001 0111010 0111011 0111100 0111101	VMH – 8 VMH – 7 VMH – 6 VMH – 5 VMH – 4 VMH – 3 VMH – 2	VML - 8 VML - 7 VML - 6 VML - 5 VML - 4 VML - 3		1111000 1111001 1111010 1111011 1111100	VM VM VM	IH + 56 IH + 57 IH + 58 IH + 59	VML + 56 VML + 57 VML + 58		
	0111001 0111010 0111011 0111100 0111101 0111110	VMH – 7 VMH – 6 VMH – 5 VMH – 4 VMH – 3 VMH – 2	VML - 7 VML - 6 VML - 5 VML - 4 VML - 3		1111001 1111010 1111011 1111100	VM VM VM	IH + 57 IH + 58 IH + 59	VML + 57 VML + 58		
	0111010 0111011 0111100 0111101 0111110	VMH - 6 VMH - 5 VMH - 4 VMH - 3 VMH - 2	VML - 6 VML - 5 VML - 4 VML - 3		1111010 1111011 1111100	VM VM	IH + 58 IH + 59	VML + 58		
	0111011 0111100 0111101 0111110	VMH – 5 VMH – 4 VMH – 3 VMH – 2	VML - 5 VML - 4 VML - 3	_	1111011 1111100	VM	IH + 59		-	
	0111100 0111101 0111110	VMH – 4 VMH – 3 VMH – 2	VML – 4 VML – 3	_	1111100			VML + 59		
	0111101 0111110	VMH – 3 VMH – 2	VML – 3	-		VM	11			
	0111110	VMH – 2		-	1111101		IH + 60	VML + 60		
			VML – 2				IH + 61	VML + 61		
	0111111	VMH – 1		-	1111110		IH + 62	VML + 62		
		•	VML – 1	╛╘	1111111	VM	IH + 63	VML + 63]	
	EXTC should be high to enable	this command								
			Status				Availabili	24		
	-					O		.y		
Dogictor	<u> </u>	Normal Mode Of					Yes			
Register		Normal Mode O	N, Idle Mo	ode (DN, Sleep C	DUT	Yes			
Availability		Partial Mode ON	N, Idle Mo	de O	FF, Sleep C	DUT	Yes			
		Partial Mode Of	N. Idle Mo	de C	N. Sleep O	UT	Yes			
			Sleep II		,		Yes			
	L		Sieep ii	IN			163			
-										
					Defect	4 \ /~ l	_			
		Status	_		Defaul			_		
				r	ıVM	VN	1F [6:0]			
Default		Power ON Sec	quence	-	l'b1	7	'h40h			
		SW Rese	et T		l'b1	7	'h40h			
					l'b1		'h40h	1		
		HW Rese	-:							
Default			et	•	l'b1	7	'h40h	-		





8.3.20. NV Memory Write (D0h)

D0h					NV	MWR (I	NV Memor	y Write)							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	↑	XX	1	1	0	1	0	0	0	0	D0h		
1 st Parameter	1	1	↑	XX	0	0	0	0	0	PG	M_ADR [2:0]	00		
2 nd Parameter	1	1	↑	XX				PGM_	DATA [7:0]				XX		
	This co	mmand	is used to	program the	NV memor	y data. A	After a succ	cessful M	ITP operat	ion, the in	formation	of PGM_	_DATA		
	[7:0] wi	ill progra	ımmed to	NV memory.											
	PGM_A	ADR [2:0	0] : The se	lect bits of ID1	, ID2, ID3	and VM	F [6:0] prog	gramming	g.						
				PGM	_ADR [2:0	Prog	grammed N	IV Memo	ry Selection	n					
Description				0	0 0		ID1 pr	ogramm	ing						
				0	0 1			ogramm							
				0	1 0		ID3 pr	ogramm	ing						
				1	0 0		VMF [6:0] prograr	nming						
l					Others		Re	eserved							
Restriction		PGM_DATA [7:0]: The programmed data. EXTC should be high to enable this command													
						Ctatus			A! a	.:!!!					
				Normal	Mada ON	Status			Availat						
Register							de OFF, Sl ode ON, Sl	· ·							
Avoilability							de OFF, Sl								
Availability							de ON, Sle								
						Sleep I		ж с	Yes						
							D	efault Va	alue						
					Status	P	 GM_ADR [2		GM_DATA	[7:0]					
Default				Power (ON Sequen		3'b000		MTP valu						
				SI	V Reset		3'b000		MTP valu	е					
				H\	V Reset		3'b000		MTP valu	е					





8.3.21. NV Memory Protection Key (D1h)

D1h					NVMPI	KEY (NV	Memory I	Protection I	(ey)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	XX	1	1	0	1	0	0	0	1	D1h		
1 st Parameter	1	1	1	XX				KEY [2	3:16]				55h		
2 nd Parameter	1	1	1	XX				KEY [15:8]				AAh		
3 rd Parameter	1	1	↑	XX				KEY [7:0]				66h		
Description	_	- A66h to		y programming /ITP programmi	•	•		•	•	Ü			ning will		
Restriction	EXTC	should b	e high to	enable this co	mmand										
Register Availability				Norma Partial	Status Availability Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Normal Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes										
Default					Power O SW	tatus N Sequer Reset ' Reset	KE'	Default Valu Y [23:0]=55A Y [23:0]=55A Y [23:0]=55A	AA66h AA66h						





8.3.22. NV Memory Status Read (D2h)

D2h					RDNVM	(NV I	Memory St	tatus Read)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	1	0	D2h
1 st Parameter	1	1	1	XX	Х	Х	Х	Х	Х	Χ	Х	Х	Х
2 nd Parameter	1	↑	1	XX	0		ID2_CNT [[2:0]	0		D1_CNT	[2:0]	XX
3 rd Parameter	1	↑	1	XX	BUSY	'	VMF_CNT	[2:0]	0	I	D3_CNT	[2:0]	XX
Description	automa	 itically aft	er writing		T [2:0] to N T [2:0] / II T [2:0] / V Statu 0 0 1	D2_CI	emory. NT [2:0] CNT [2:0] 0 1 1 1	Avai No Programi Programn Programn	ription ability grammed ned 1 time ned 2 time ned 3 time	e ess	. The bits	will increa	se "+1"
Restriction	EXTC s	should be	high to e	nable this comm	and								
						Status	3		Availabi	ility			
				Normal Mo				leep OUT	Yes				
Register							ode ON, SI		Yes				
Availability							de OFF, SI		Yes				
,				Partial Mo	de ON, lo	dle Mo	ode ON, Sl	eep OUT	Yes				
					S	Sleep I	IN		Yes				
				0				Default Valu	е				
				Status	ID3_C	NT	ID2_CNT	ID1_CNT		CNT	BUSY		
Default			Powe	er ON Sequence	Х		Χ	Х	Х		Χ		
				SW Reset	Х		Χ	Х	Х		Χ		
ı				HW Reset	Х		Χ	Х	Х		Χ		





8.3.23. Read ID4 (D3h)

D3h						RDID4	(Read ID	04)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	XX	1	1	0	1	0	0	1	1	D3h	
1 st Parameter	1	1	1	XX	X	Х	Х	Χ	Χ	Х	Х	Х	Х	
2 nd Parameter	1	1	1	XX	0	0	0	0	0	0	0	0	00h	
3 rd Parameter	1	1	1	XX	1	0	0	1	0	0	1	1	93h	
4 th Parameter	1	1	1	XX	0	1	0	0	0	0	0	1	41h	
Description	The 1 st	parame	eter is dun	nmy read period s the IC version or mean the IC n	ı.	ne.								
Restriction	EXTC :	TC should be high to enable this command Status Availability												
		Status Availability												
				Normal I	Mode ON	, Idle Mod	e OFF, S	leep OUT						
Register				Normal	Mode ON	, Idle Mod	de ON, SI	eep OUT	Yes	S				
Availability				Partial N	lode ON,	Idle Mod	e OFF, SI	eep OUT	Yes	S				
-				Partial I	Mode ON	Idle Mod	e ON, Sle	eep OUT	Yes	S				
						Sleep IN			Yes	S				
Default							ence 2	4'h00934	lh					
		Status Availability Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Normal Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes												





8.3.24. Positive Gamma Correction (E0h)

E0h					PGAM	CTRL (Po	sitive Ga	amma Con	trol)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	1	0	0	0	0	0	E0h
1 st Parameter	1	1	↑	XX	0	0	0	0		VP63	[3:0]		08
2 nd Parameter	1	1	1	XX	0	0			VP62	[5:0]			
3 rd Parameter	1	1	1	XX	0	0			VP61	[5:0]			
4 th Parameter	1	1	1	X	0	0	0	0		VP59	[3:0]		05
5 th Parameter	1	1	1	XX	0	0	0		V	P57 [4:0]			
6 th Parameter	1	1	1	XX	0	0	0	0		VP50	[3:0]		09
7 th Parameter	1	1	1	XX	0			\	/P43 [6:0]				
8 th Parameter	1	1	1	XX		VP2	7 [3:0]			VP36	[3:0]		
9 th Parameter	1	1	1	XX	0			١	/P20 [6:0]				
10 th Parameter	1	1	1	XX	0	0	0	0		VP13	[3:0]		0B
11 th Parameter	1	1	1	XX	0	0	0		\	/P6 [4:0]			
12 th Parameter	1	1	1	XX	0	0	0	0		VP4	[3:0]		00
13 th Parameter	1	1	1	XX	0	0			VP2	[5:0]			
14 th Parameter	1	1	1	XX	0	0			VP1	[5:0]			
15 th Parameter	1	1	↑	XX	0	0	0	0		VP0	[3:0]		00
Description	Set the	gray so	cale volta	ige to adjust the	e gamma	character	istics of th	he TFT par	nel.				
Restriction	EXTC	should l	oe high to	enable this co	mmand								
						Status			Availab	oility			
				Norma	I Mode Of			Sleep OUT					
Register								Sleep OUT		;			
Availability								Sleep OUT	Yes	5			
7								Sleep OUT	Yes				
						Sleep I		•	Yes				
Default													





8.3.25. Negative Gamma Correction (E1h)

E1h					NGAMCT	RL (Neg	ative Gar	nma Corre	ection)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	1	0	0	0	0	1	E1h
1 st Parameter	1	1	1	XX	0	0	0	0		VN63	[3:0]		08
2 nd Parameter	1	1	1	XX	0	0			VN62	[5:0]			
3 rd Parameter	1	1	↑	XX	0	0			VN61	[5:0]			
4 th Parameter	1	1	↑	XX	0	0	0	0		VN59	[3:0]		07
5 th Parameter	1	1	1	XX	0	0	0		V	'N57 [4:0]			
6 th Parameter	1	1	1	XX	0	0	0	0		VN50	[3:0]		05
7 th Parameter	1	1	1	XX	0			,	/N43 [6:0]				
8 th Parameter	1	1	1	XX		VN3	6 [3:0]			VN27	[3:0]		
9 th Parameter	1	1	1	XX	0			,	/N20 [6:0]				
10 th Parameter	1	1	↑	XX	0	0	0	0		VN13	[3:0]		04
11 th Parameter	1	1	↑	XX	0	0	0		\	VN6 [4:0]			
12 th Parameter	1	1	1	XX	0	0	0	0		VN4	[3:0]		0F
13 th Parameter	1	1	↑	XX	0	0			VN2	[5:0]			
14 th Parameter	1	1	↑	XX	0	0			VN1	[5:0]			
15 th Parameter	1	1	1	XX	0	0	0	0		VN0	[3:0]		0F
Description	Set the	et the gray scale voltage to adjust the gamma characteristics of the TFT panel.											
Restriction	EXTC	XTC should be high to enable this command											
						Status			Availal	oility			
				Normal	Mode Of			Sleep OUT	_				
Register								Sleep OUT					
Availability								Sleep OUT					
Atvailability								leep OUT	Yes				
						Sleep I		'	Yes				
Default													





8.3.26. Digital Gamma Control 1 (E2h)

D/CX				20, 111	O I UL (DI	gital Gam	ma Co	ontro	I 1)				
	RDX	WRX	D17-8	D7	D6	D5	D4		D3	D2	D1	D0	HEX
0	1	1	XX	1	1	1	0		0	0	1	0	E2h
1	1	1	XX		RCA	0 [3:0]				BCA	0:8]		XX
1	1	1	XX		RCA	x [3:0]				BCA	x [3:0]		XX
1	1	1	XX		RCA1	5 [3:0]				BCA	15 [3:0]		XX
			-	_		_							
EXTC s	should b	e high to	enable this	command									
	Status Availability Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Normal Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes												
			-	Power ON :	Sequence	RCAx TB	[3:0] D D	BCA	Ax [3:0] ГВD ГВD				
	1 1 RCAx	1 1 1 1 1 1 1 1 1 RCAx [3:0]: Ga	1 1 ↑ 1 1 ↑ 1 1 ↑ RCAx [3:0]: Gamma M BCAx [3:0]: Gamma M	1 1 ↑ XX 1 1 ↑ XX 1 1 ↑ XX RCAx [3:0]: Gamma Macro-adjustn BCAx [3:0]: Gamma Macro-adjustn EXTC should be high to enable this Norm Norm Parti Part	1 1 ↑ XX 1 1 ↑ XX 1 1 ↑ XX RCAx [3:0]: Gamma Macro-adjustment registe BCAx [3:0]: Gamma Macro-adjustment registe EXTC should be high to enable this command Normal Mode Of Normal Mode Of Partial Mode Of Partial Mode Of Partial Mode Of SW R	1 1 ↑ XX RCA(1	1 1 ↑ XX RCA0 [3:0] 1 1 ↑ XX RCA15 [3:0] 1 1 ↑ XX RCA15 [3:0] RCAx [3:0]: Gamma Macro-adjustment registers for red gamma of BCAx [3:0]: Gamma Macro-adjustment registers for blue gamma of EXTC should be high to enable this command Status Normal Mode ON, Idle Mode OFF, Son Normal Mode ON, Idle Mode OFF, Son Normal Mode ON, Idle Mode ON, Son Partial Mode ON, Idle Mode ON, Son Son Son Son Son Son Son Son Son Son	1 1 ↑ XX RCA0 [3:0] 1 1 ↑ XX RCAx [3:0] 1 1 ↑ XX RCA15 [3:0] RCAx [3:0]: Gamma Macro-adjustment registers for red gamma curve. BCAx [3:0]: Gamma Macro-adjustment registers for blue gamma curve. EXTC should be high to enable this command Status Normal Mode ON, Idle Mode OFF, Sleep OF Partial Mode ON, Idle Mode OFF, Sleep OF Partial Mode ON, Idle Mode ON, Sleep OF Sleep IN Status Status Partial Mode ON, Idle Mode ON, Sleep OF Sleep IN Status Status Poefaul RCAx [3:0] Power ON Sequence TBD SW Reset TBD	1 1 ↑ XX RCA0 [3:0] 1 1 ↑ XX RCA15 [3:0] RCAx [3:0]: Gamma Macro-adjustment registers for red gamma curve. BCAx [3:0]: Gamma Macro-adjustment registers for blue gamma curve. EXTC should be high to enable this command Status Normal Mode ON, Idle Mode OFF, Sleep OUT Normal Mode ON, Idle Mode OFF, Sleep OUT Partial Mode ON, Idle Mode ON, Sleep OUT Partial Mode ON, Idle Mode ON, Sleep OUT Sleep IN Status Default Value RCAx [3:0] BCA Power ON Sequence TBD SW Reset TBD	1 1 ↑ XX RCA0 [3:0] 1 1 ↑ XX RCAx [3:0] 1 1 ↑ XX RCAx [3:0] RCAx [3:0]: Gamma Macro-adjustment registers for red gamma curve. BCAx [3:0]: Gamma Macro-adjustment registers for blue gamma curve. EXTC should be high to enable this command Status	1 1 ↑ XX RCA0 [3:0] BCA 1 1 ↑ XX RCA15 [3:0] BCA 1 1 ↑ XX RCA15 [3:0] BCA RCAX [3:0]: Gamma Macro-adjustment registers for red gamma curve. BCAX [3:0]: Gamma Macro-adjustment registers for blue gamma curve. EXTC should be high to enable this command Status Availability Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Normal Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes Status Default Value RCAX [3:0] BCAX [3:0] Power ON Sequence TBD TBD SW Reset TBD TBD	1 1 ↑ XX RCA0 [3:0] BCA0 [3:0] 1 1 ↑ XX RCA15 [3:0] BCA15 [3:0] RCAx [3:0]: Gamma Macro-adjustment registers for red gamma curve. BCAx [3:0]: Gamma Macro-adjustment registers for blue gamma curve. EXTC should be high to enable this command Status Availability Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Sleep IN Yes Status Default Value RCAx [3:0] BCAx [3:0] Power ON Sequence TBD TBD SW Reset TBD TBD	1 1 ↑ XX RCA0 [3:0] BCA0 [3:0] 1 1 ↑ XX RCAx [3:0] BCAx [3:0] 1 1 ↑ XX RCA15 [3:0] BCA15 [3:0] RCAx [3:0]: Gamma Macro-adjustment registers for red gamma curve. EXTC should be high to enable this command Status Availability Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes Status Default Value RCAx [3:0] BCAx [3:0] Power ON Sequence TBD TBD SW Reset TBD TBD





8.3.27. Digital Gamma Control 2(E3h)

E3h					DGAM	CTRL (Dig	ital Gan	nma C	ontro	l 2)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	ļ.	D3	D2	D1	D0	HEX	
Command	0	1	1	XX	1	1	1	0		0	0	1	1	E3h	
1 st Parameter	1	1	1	XX		RFA0	[3:0]				BF	A0 [3:0]		XX	
:	1	1	1	XX		RFAx	[3:0]				BF	Ax [3:0]		XX	
64 rd Parameter	1	1	1	XX		RFA6	3 [3:0]				BFA	(63 [3:0]		XX	
Description				icro-adjustm icro-adjustm											
Restriction	EXTC s	should b	e high to	enable this	command										
						Status				Availa	ability				
Register					Normal Mode ON, Idle Mode OFF, Sleep OUT Yes										
negistei					Normal Mode ON, Idle Mode ON, Sleep OUT Yes										
Availability					al Mode ON						es				
				Part	ial Mode ON	•		leep C	UT	Ye					
						Sleep IN	<u> </u>			Y€	es				
								Defaul	t Valu	е					
				j	Status RFAx [3:0] BFAx [3:0]										
Default				Ī	Power ON	Sequence				TBD					
				Ī	SW F		TE	BD.	Т	ΓBD					
					HW F	Reset	TE	3D	1	ΓBD					





8.3.28. Interface Control (F6h)

F6h	IFCTL (16bits Data Format Selection)														
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	XX	1	1	1	1	0	1	1	0	F6h		
1 st Parameter	1	1	1	XX	MY_ EOR	MX_ EOR	MV_ EOR	0	BGR_ EOR	0	0	WE MODE	01		
2 nd Parameter	1	1	1	XX	0	0	EPF [1]	EPF [0]	0	0	MDT [1]	MDT [0]	00		
3 rd Parameter	1	1	1	XX	0	0	ENDIAN	0	DM [1]	DM [0]	RM	RIM	00		

MY_EOR / MX_EOR / MV_EOR / BGR_EOR:

The set value of MADCTL is used in the IC is derived as exclusive OR between 1st Parameter of IFCTL and MADCTL Parameter.

MDT [1:0]: Select the method of display data transferring.

WEMODE: Memory write control

WEMODE=0: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.

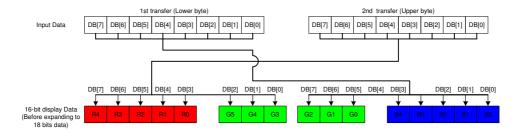
WEMODE=1: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

ENDIAN: Select Little Endian Interface bit. At Little Endian mode, the host sends LSB data first.

ENDIAN	Data transfer Mode
0	Normal (MSB first, default)
1	Little Endian (LSB first)

Note: Little Endian is valid on only 65K 8-bit and 9-bit MCU interface mode.

Description



DM [1:0]: Select the display operation mode.

[OM [1]	DM [0]	Display Operation Mode
	0	0	Internal clock operation
	0	1	RGB Interface Mode
	1	0	VSYNC interface mode
	1	1	Setting disabled

The DM [1:0] setting allows switching between internal clock operation mode and external display interface operation mode.

However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.





RM: Select the interface to access the GRAM.

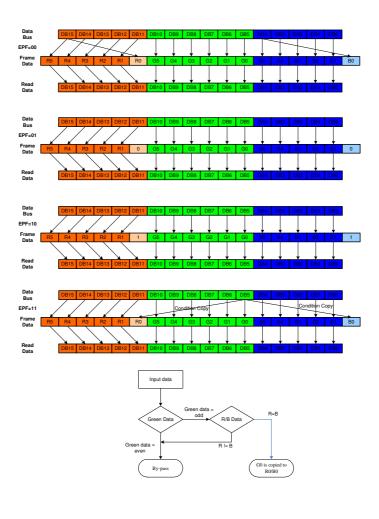
Set RM to "1" when writing display data by the RGB interface.

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

RIM: Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through the RGB interface and should not be set during operation.

RIM	COLMOD [6:4]	RGB Interface Mode
_	110 (262K color)	18- bit RGB interface (1 transfer/pixel)
0	101 (65K color)	16- bit RGB interface (1 transfer/pixel)
	110 (262K color)	6- bit RGB interface (3 transfer/pixel)
l	101 (65K color)	6- bit RGB interface (3 transfer/pixel)

EPF [1:0]: 65K color mode data format.







ŀ										
	EP	PF [1:0]			Expand 16 bb	p (R,G,B) to	18bbp (R,G,E	3)		
		00	$r [5:0] = {\dot{R}}$ $g [5:0] = {G}$	utted to LSB [4:0], R [4]} & [5:0]} & [4:0], B [4]}						
		01	"0" is inputt r [5:0] = {R g [5:0] = {G b [5:0] = {B	ted to LSB [4:0], 0} a [5:0]} a [4:0], 0}		W.O.F.				
		10	"1" is inputt r [5:0] = {R g [5:0] = {G b [5:0] = {B	[4:0], 1} 3 [5:0]}						
		11	Compare F Case 1: R= Case 2: R= Case 3: R=	R [4:0], G [5:1], B =G=B → r [5:0] = =B≠G → r [5:0] = =G≠B → r [5:0] = =G≠R → r [5:0] =	[4:0] case: {R [4:0], G [0]}, {R [4:0], R [4]}, {R [4:0], G [0]},	, g [5:0] = {G , g [5:0] = {G , g [5:0] = {G	[5:0]}, b [5:0] [5:0]}, b [5:0]	= {B [4:0], E = {B [4:0], E	3 [0]} 3 [0]}	
Restriction	EXTC sh	ould be hi	gh to enable	this command						
Restriction	EXTC sh	ould be hi	gh to enable	this command	Statue		Availah	ility		
Restriction	EXTC sh	ould be hi			Status N, Idle Mode O	FF, Sleep O	Availab UT Yes			
Restriction Register	EXTC sho	ould be hi		this command Normal Mode O Normal Mode C	N, Idle Mode O		UT Yes			
Register	EXTC shi	ould be hi		Normal Mode O	N, Idle Mode O N, Idle Mode C	N, Sleep Ol	UT Yes			
Register	EXTC sho	ould be hi		Normal Mode O Normal Mode C	N, Idle Mode O N, Idle Mode C N, Idle Mode O N, Idle Mode O	ON, Sleep Ol FF, Sleep Ol	UT Yes JT Yes JT Yes JT Yes			
Register	EXTC shi	ould be hi		Normal Mode O Normal Mode C Partial Mode Ol	N, Idle Mode O N, Idle Mode O N, Idle Mode Ol	ON, Sleep Ol FF, Sleep Ol	UT Yes JT Yes JT Yes			
Restriction Register Availability	EXTC shi	ould be hi		Normal Mode O Normal Mode C Partial Mode Ol	N, Idle Mode O N, Idle Mode C N, Idle Mode O N, Idle Mode O	DN, Sleep OI FF, Sleep OI N, Sleep OI	UT Yes JT Yes JT Yes JT Yes Yes			
Register	EXTC she			Normal Mode O Normal Mode C Partial Mode OI Partial Mode O	N, Idle Mode O N, Idle Mode O N, Idle Mode O N, Idle Mode O Sleep IN	DN, Sleep OI FF, Sleep OI N, Sleep OL Defaul	UT Yes JT Yes JT Yes JT Yes Ves JT Yes TYes		DM	DIM
Register Availability		St	ratus	Normal Mode O Normal Mode O Partial Mode OI Partial Mode O	N, Idle Mode O N, Idle Mode O N, Idle Mode O N, Idle Mode O Sleep IN MDT [1:0]	DN, Sleep OI FF, Sleep OI N, Sleep OL Defaul	UT Yes JT Yes JT Yes JT Yes Ves t Value WEMODE	DM [1:0]	RM	RIM
Register		St. Power ON	atus	Normal Mode O Normal Mode C Partial Mode O Partial Mode O EPF [1:0] 2'b00	N, Idle Mode O N, Idle Mode O N, Idle Mode O N, Idle Mode O Sleep IN MDT [1:0] 2'b00	DN, Sleep OI FF, Sleep OI N, Sleep OI Defaul	UT Yes JT Yes JT Yes JT Yes t Value WEMODE	DM [1:0] 2'b00	1'b0	1'b0
Register Availability		St. Power ON	ratus	Normal Mode O Normal Mode O Partial Mode OI Partial Mode O	N, Idle Mode O N, Idle Mode O N, Idle Mode O N, Idle Mode O Sleep IN MDT [1:0]	DN, Sleep OI FF, Sleep OI N, Sleep OL Defaul	UT Yes JT Yes JT Yes JT Yes Ves t Value WEMODE	DM [1:0]		





8.4 Description of Extend register command

8.4.1 Power control A (CBh)

	CBh	Power control A D/CX RDX WRX D17-8 D7 D6 D5 D4 D3 D2 D1 D0 HEX													
Command		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D	2	D1	D0	HEX
Parameter	Command	0	1	1	XX	1	1	1	1	0	1		1	0	CBh
3	1 st Parameter	1	1	1	XX	0	0	1	1	1	C)	0	1	39
### Availability A Parameter		1	1	1	XX	0	0	1	0	1	1		0	0	2C
Segister Availability Parameter Pa		1	1	1	XX	0	0	0	0	0	C			1	00
REG_VD[2:0]: vcore control		1	1	1								R		0]	
Description	^{5rd} Parameter	11	1	1	XX	0	0	0	0	0			VBC[2:0]		02
Status	Description	REG_VD[2:0] Vcore(V) 000 1.55 001 1.4 010 1.5 011 1.65 100 1.6 101 1.7 110 reserved VBC[2:0]: ddvdh control VBC[2:0] DDVDH(V) 000 5.8 001 5.7 010 5.6 011 5.5 100 5.4 101 5.3 110 5.2 111 Reserved													
Normal Mode ON, Idle Mode OFF, Sleep OUT Yes	Restriction	EXTC s	should b	e high to	enable t	his cor	nmand								
Normal Mode ON, Idle Mode ON, Sleep OUT Yes								Status			Availabi	lity			
Availability Partial Mode ON, Idle Mode OFF, Sleep OUT Yes	Dogistor														
Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes															
Sleep IN Yes Sleep IN Yes Default Value Parameter1 Parameter2 Parameter3 Parameter4 Parameter5 Power ON Sequence 39 2C 00 34 02 SW Reset 39 2C 00 34 02	Availability											_			
Status Default Value Parameter1 Parameter2 Parameter3 Parameter4 Parameter5						<u> Partial</u>			UN, Slee	p OUT		_			
Default Status Parameter1 Parameter2 Parameter3 Parameter4 Parameter5 Power ON Sequence 39 2C 00 34 02 SW Reset 39 2C 00 34 02								Pieeb IIV			Yes				
Default Parameter Paramete		Default Value											1		
Default Power ON Sequence 39 2C 00 34 02 SW Reset 39 2C 00 34 02				Status		Par	ameter1	Paramet				ramet	er4 Pa	arameter5	1
	Default	-	Powe	r ON Se	quence										
HW Reset 39 2C 00 34 02				SW Res	et		39	2C 00 34 02					02		
				HW Res	et		39	2C		00		34		02	





8.4.2 Power control B (CFh)

CFh	Power control B																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	0	1	1	XX	1	1	0	0	1	1	1	1	CFh											
1 st Parameter	1	1	1	XX	0	0	0	0	0	0	0	0	00											
2 nd Parameter	1	1	1	XX	1	0	0	Power con	rol[1:0]	0	0	1	81											
3 rd Parameter	1	1	1	XX	0	0	1	DC_ena	0	0	0	0	30											
Description	Only se BT [2 0 0 0 0 0 1 0 1 0 1	0 0 1 0 VCI x 2 VCI x 3 VCI x 4 VCI x 6																						
Restriction	EXTC	should b	e high to	o enable	this com	mand																		
							Status		Ava	ilability														
5				1	Normal N	Mode ON	Idle Mode C	FF, Sleep Ol	JT	Yes														
Register										Yes														
Availability								FF, Sleep OU	T				Normal Mode ON, Idle Mode ON, Sleep OUT Yes											
					Partial N			Partial Mode ON, Idle Mode OFF, Sleep OUT Yes																
	Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes																							
					T ditial i	Mode ON.		N, Sleep OU		Yes Yes														
					T dittair	Mode ON																		
					Status	Mode ON		Default	Value		er3													
Default							Sleep IN	Default	Value eter2	Yes	er3													
Default				Power	Status	uence	Sleep IN Parameter	Default 1 Param	Value eter2	Yes Paramet	er3													





8.4.3 Driver timing control A (E8h)

C.T.S DIIVE		,		,		vor tim.		wal A					
F6h					1	ver timi		1	ı				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	1	0	1	0	0	0	E8h
1 st Parameter	1	1	1	XX	1	0	0	0	0	1	0	NOW	84
2 nd Parameter	1	1	1	XX	0	0	0	EQ	0	0	0	CR	11
3 rd Parameter	1	1	↑	XX	0	1	1	1	1	0	PC[1:	0]	7A
Description	1st parameter:gate driver non-overlap timing control 0:default non-overlap time 1:default + 1 unit 2nd parameter:EQ timing control 0: default = 1 unit 1:default EQ timing parameter:CR timing control 0: default = 1 unit 1:default CR timing 3rd parameter:pre-charge timing control 11: reserved 10: default pre-charge timing 01:default = 1 unit												
Restriction	EXTC sho	ould be higl	n to enable	this comma	nd								
					0:					•	L = 1 - 122		
		F	KI -	rmal Mada		tus Mada O	EE Ola	n OUT			lability		
Register		-		rmal Mode ormal Mode				•			'es 'es	\dashv	
Availability		-		rtial Mode (es es		
Availability		F		artial Mode							es es	1	
		ľ			Slee		1, 0.000				es es		
									ļ				
							Defa	ult Value					
			Stati	as	Parame	ter1	Para	meter2	ı	Paramet	er3		
Default			Power Seque		84			11		7A			
			SW Re	eset	84			11		7A			
			HW R	eset	84			11		7 A			
				•		Ц					4		





8.4.4 Driver timing control B (EAh)

F6h	Driver timing control B												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	1	0	1	0	1	0	EAh
1 st Parameter	1	1	1	XX	VG_	SW_T4	VG_	W_T2	VG_	SW_T1	66		
2 nd Parameter	1	1	1	XX	Χ	X	Х	X	X	X	0	0	00
Description	VG_SV VG_SV VG_SV	V_T1[1: V_T2[1: V_T3[1: V_T4[1: nit nit	0]:EQ to 0]:EQ to	DDVDH DDVDH	control								
Restriction	EXTC	should b	e high to	o enable t	this com	ımand							
							Status		Ava	lability			
				١	Normal I	Mode ON.		OFF, Sleep O		res			
Register								ON, Sleep O		⁄es			
Availability					Partial N	∕lode ON,	Idle Mode (OFF, Sleep O	UT \	res .			
					Partial I	Mode ON,	Idle Mode	ON, Sleep Ol	JT '	res .			
							Sleep IN		`	⁄es			
Default					5	Status ON Sequ SW Reset	ence	Defaul rarameter1 66 66 66	t Value Parame 00 00				





8.4.5 Power on sequence control (EDh)

F6h	Power on sequence control													
	D/CX	RDX	WRX	D17-	D.		D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	8 XX	1		1	1	0	1	1	0	1	EDh
1 st Parameter	1	1	<u> </u>	XX	X		1	CP1 soft		X	1		soft start	55
2 nd Parameter	1	1	<u> </u>	XX	Х		0	En_v		Х	0		ddvdh	01
3 rd Parameter	1	1	↑	XX	Х		0	En_v		Х	0		_vgl	23
4 th Parameter	1	1	1	XX	DDVDF	I_ENH	0	0	0	0	0	0	1	1
Description	00:soft 01:soft 01:soft 11:disa 2 nd / 3 rd 00:1 st f 01:2 nd 10:3 rd f 11:4 th f 4 th para 0: disa	1st parameter:soft start keep 3 frame 01:soft start keep 2 frame 01:soft start keep 1 frame 11:disable 2nd/ 3rd parameter:power on sequence control 00:1st frame enable 01:2nd frame enable 11:4th frame enable 11:4th frame enable 11:4th parameter:DDVDH enhance mode(only for 8 external capacitors) 0: disable 1: enable												
Restriction	EXTC	should b	e high to	enable t	this comma	and								
						(Status			Availabi	lity			
_				N	Normal Mo			OFF, Sleep	OUT	Yes	.,			
Register				1	Normal Mo	de ON, Id	dle Mode	ON, Sleep	OUT	Yes				
Availability								OFF, Sleep		Yes				
				<u> </u>	Partial Mo			ON, Sleep (TUC	Yes				
						S	leep IN			Yes				
Default				Status		Parame 55	ter1 i	Parameter2 01	ult Val	arameter3 23	3 Par	ameter4		
	l			SW Rese	E	55		01		23		01		
				HW Rese		55	J	01		23		01		





8.4.6 Enable 3G (F2h)

F6h	Enable_3G														
	D/CX	RDX	WRX	D17-8	D7	D6	D5	[D4	D3	D2		D1	D0	HEX
Command	0	1	1	XX	1	1	1		1	0	0		1	0	F2h
1 st Parameter	1	1	↑	XX	0	0	0		0	0	0		1	3G_enb	02
Description				le 3 gam amma co											
Restriction	EXTC	should b	oe high t	o enable t	this con	nmand									
							Status			A	Availability				
					Normal	Mode ON	, Idle Mode	OFF, :	Sleep C	DUT	Yes				
Register					Normal	Mode ON	I, Idle Mode	ON, S	Sleep C	UT	Yes				
Availability							Idle Mode (Yes				
				_	Partial	Mode ON	, Idle Mode	ON, S	Sleep O	UT	Yes				
							Sleep IN				Yes				
Default						S	Status ON Sequent W Reset W Reset	ce	Para	ult Value meter1 02 02 02					





8.4.7 Pump ratio control (F7h)

F6h	Pump ratio control													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4		D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	1	1		0	1	1	0	F7h
1 st Parameter	1	1	1	XX	Χ	Х	Ratio	[1:0]		0	0	0	0	10
Description	00:rese	erved		trol										
Restriction	EXTC should be high to enable this command													
							Status	NEE 01	OUT		lability			
Register							, Idle Mode C , Idle Mode C				′es ′es			
Availability							Idle Mode O				es /es			
Availability				-			Idle Mode C				es/es			
					· artiar		Sleep IN	, 0.005	,		⁄es			
Default						Power (Status ON Sequenc W Reset W Reset	Pa	fault Va aramete 10 10 10					

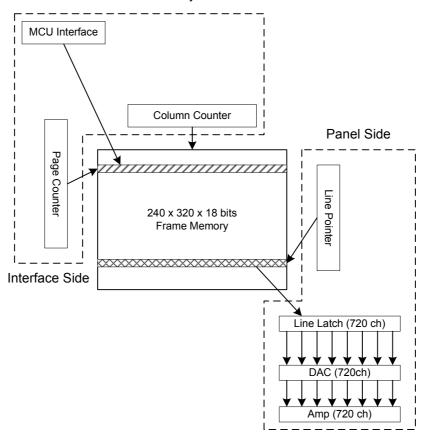




9. Display Data RAM

9.1. Configuration

The display data RAM stores display dots and consists of 1,382,400 bits (240x18x320 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous panel read and interface read or write display data to the same location of the frame memory.





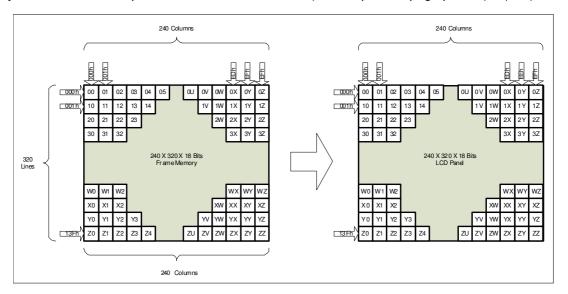


9.2. Memory to Display Address Mapping

9.2.1. Normal Display ON or Partial Mode ON, Vertical Scroll Mode OFF

In this mode, the content of frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 013Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0)





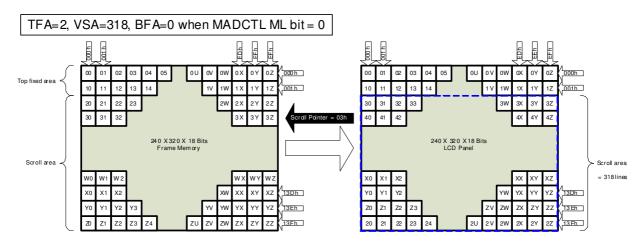


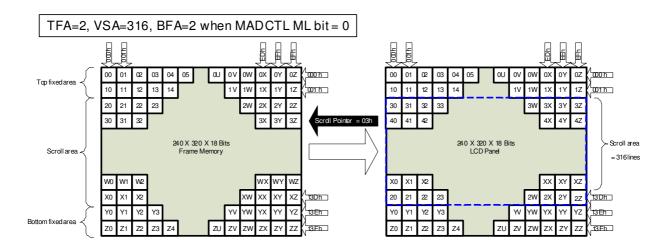


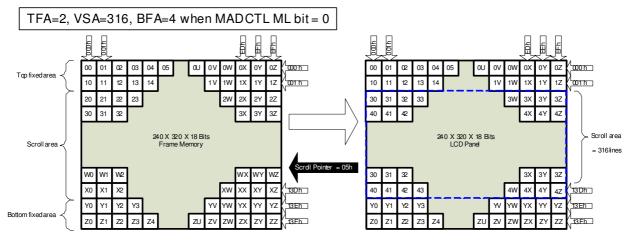
9.2.2. Vertical Scroll Mode

There is a vertical scrolling mode, which is determined by the commands "Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

The Vertical Scroll Mode function is explained by these examples in the following.







Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) ≠ 320, Scrolling Mode is undefined.





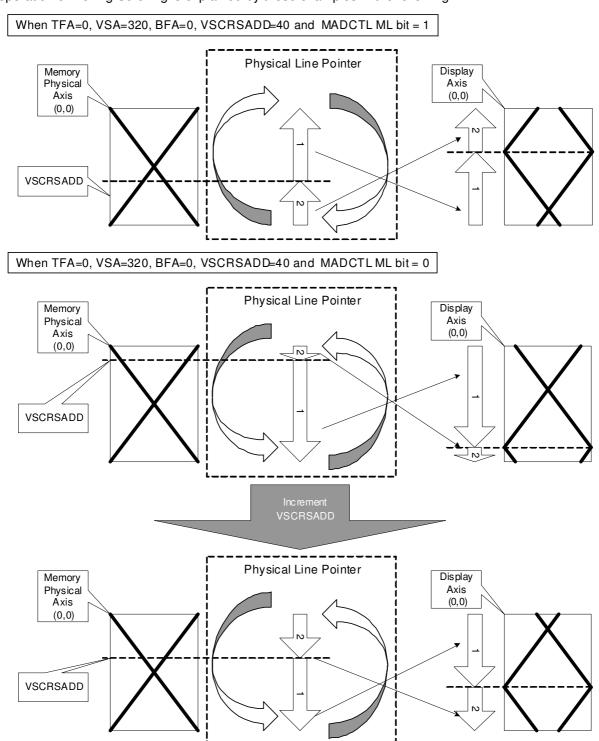
9.2.3. Vertical Scroll Example

9.2.4. Case1: TFA+VSA+BFA < 320

This setting is prohibited, unless unexpected picture will be shown.

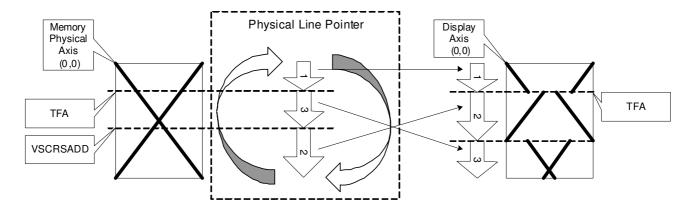
9.2.5. Case2: TFA+VSA+BFA = 320 (Rolling Scrolling)

The operation of Rolling Scrolling is explained by these examples in the following.

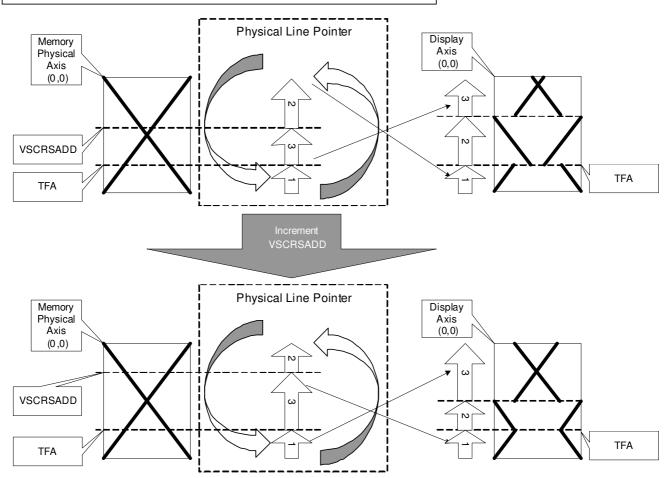








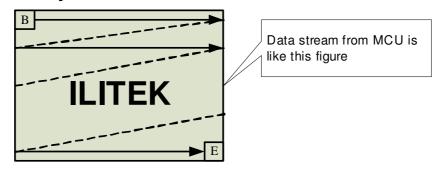
When TFA=30, VSA=290, BFA=0, VSCRSADD=80 and MADCTL ML bit = 1



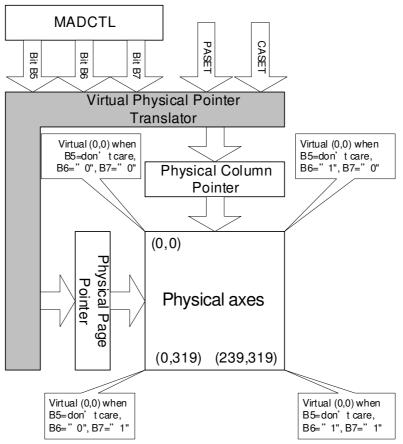




9.3. MCU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by "Memory Data Access Control" Command, Bits B5, B6, and B7 as described below.



B5	B6	B7	CASET			PASET		
0	0	0	Direct to Physical Column F	Pointer	Direct to Physical Page Pointer			
0	0	1	Direct to Physical Column F	Pointer	Direct to (319-Physical Page Pointer)			
0	1	0	Direct to (239-Physical Coli	umn Pointer)	Direct to Physical Page Pointer			
0	1	1	Direct to (239-Physical Coli	umn Pointer)	Direct to (319	P-Physical Page Pointer)		
1	0	0	Direct to Physical Page Poi	nter	Direct to Physical Column Pointer			
1	0	1	Direct to (319-Physical Pag	e Pointer)	Direct to Phy	sical Column Pointer		
1	1	0	Direct to Physical Page Poi	nter	Direct to (239	Physical Column Pointer)		
1	1	1	Direct to (319-Physical Pag	e Pointer)	Direct to (239-Physical Column Pointe			
		Coi	ndition	Column	Counter	Page counter		
Whe	n RAMW	'R/RAMF	RD command is accepted	Return to "Sta	art column"	Return to "Start Page"		
	Comple	ete Pixel	Read/Write action	Increment by	1	No change		
The (Column v	/alues is	large than "End Column"	Return to "Sta	art column"	Increment by 1		
The	e Page c	ounter is	large than "End Page"	Return to "Sta	Return to "Start column" Return to "Start Page"			





Note:

Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5. The write order for each pixel unit is

Γ	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	В3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

Display Data		IADCT aramete		Image in the Memory	Image in the Driver (Frame Memory)
Direction	MV	MX	МҮ	(MPU)	inage in the 21101 (Table Monory)
Normal	0	0	0	B	Counter(0,0)
Y-Mirror	0	0	1	B	Memory(0,0) E Counter(0,0)
X-Mirror	0	1	0	B	Memory(0,0) B Counter(0,0)
X-Mirror Y-Mirror	0	1	1	B	Memory(0,0) E Counter(0,0)
X-Y Exchange	1	0	0	B	Memor(0,0) B Counter(0,0) E E
X-Y Exchange Y-Mirror	1	0	1	B	Memory(0,0) E
XY Exchange X-Mirror	1	1	0	B	Memory(0,0) E Counter(0,0)
XY Exchange XY-Mirror	1	1	1	B E	Memory(0,0) E Counter(0,0)





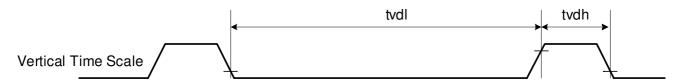
10. Tearing Effect Output

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the parameter of the Tearing Effect Line Off & On commands.

The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

10.1. Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Sync information only:



tvdh = The LCD display is not updated from the Frame Memory.

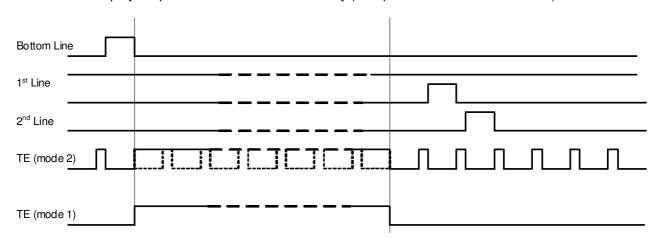
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2, the tearing effect output signal consists of V-Sync and H-Sync information; there is one V-sync and 320 H-sync pulses per field:



thdh = The LCD display is not updated from the Frame Memory.

thdl = The LCD display is updated from the Frame Memory (except Invisible Line - see above).



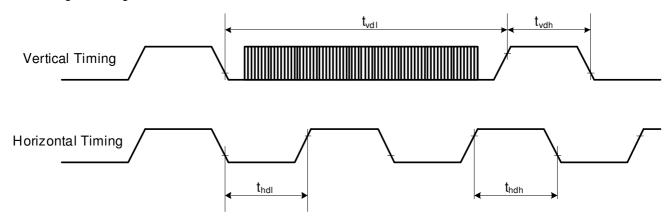
Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.





10.2. Tearing Effect Line Timings

The tearing effect signal is described below:

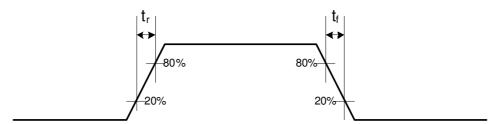


AC characteristics of Tearing Effect Signal (Frame Rate = 60Hz)

Symbol	Parameter	Min.	Тур.	Max.	Unit	Description
t_{vdl}	Vertical timing low duration				ms	
$t_{\rm vdh}$	Vertical timing high duration	1000			us	
t _{hdl}	Horizontal timing low duration				us	
t _{hdh}	Horizontal timing high duration			500	us	

Note:

- 1. The timings in Table as above apply when MADCTL B4=0 and B4=1
- 2. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.





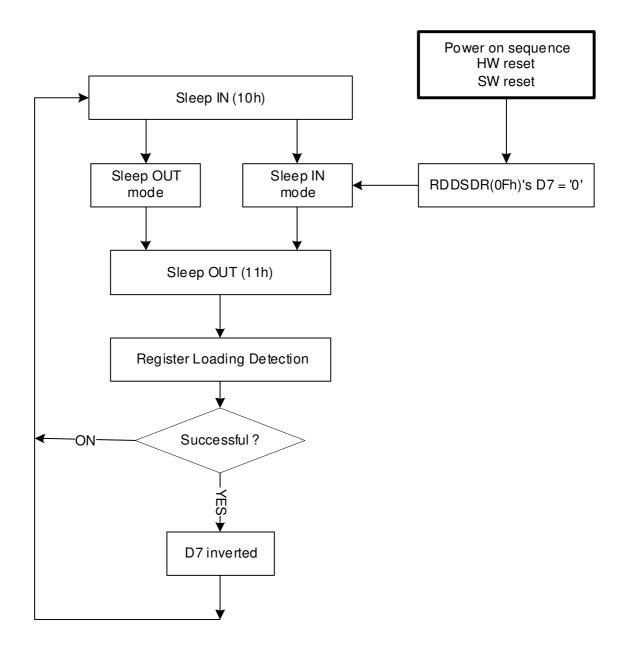
11. Sleep Out – Command and Self-Diagnostic Functions of the Display Module

11.1. Register loading Detection

Sleep Out-command (Command "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EV Memory(or similar device) to registers of the display controller is working properly.

If the register loading detection is successfully, there is inverted (= increased by 1) a bit, which is defined in command "Read Display Self-Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D7). If it is failure, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:





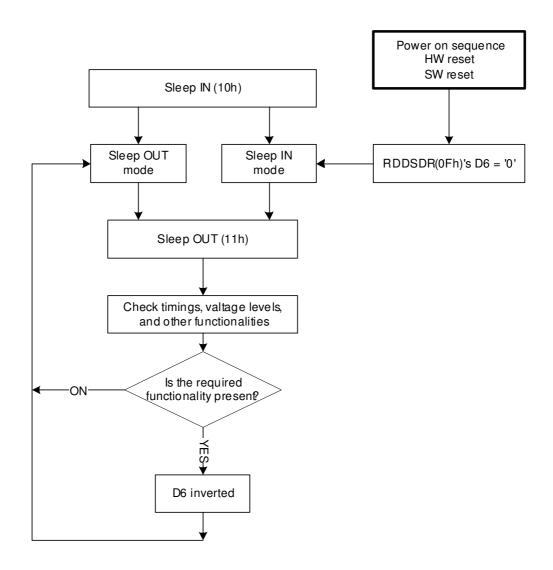


11.2. Functionality Detection

Sleep Out-command (Command "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.) If functionality requirement is met, there is an inverted (= increased by 1) bit, which defined in command "Read Display Self- Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.

The flow chart for this internal function is following:



Note 1: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In -mode to Sleep Out -mode, before there is possible to check if User's functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out -command is sent in Sleep Out -mode.





12. Power ON/OFF Sequence

VDDI and VCI can be applied in any order.

VCI and VDDI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and VDDI must be powered down minimum 120msec after RESX has been released.

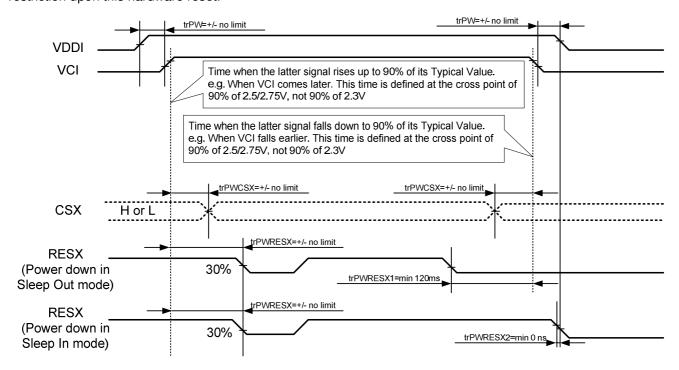
During power off, if LCD is in the Sleep In mode, VDDI or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

- Note 1: There will be no damage to the display module if the power sequences are not met.
- Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
- Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
- Note 4: If RESX line is not held stable by host during Power On Sequence as defined in Sections 12.1 and 12.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

12.1. Case 1 – RESX line is held High or Unstable by Host at Power ON

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode trPWRESX2 is applied to RESX falling in the Sleep In Mode

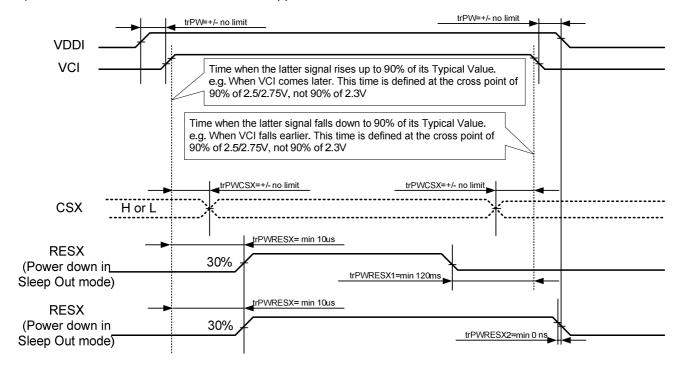
Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.





12.2. Case 2 – RESX line is held Low by Host at Power ON

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VCI and VDDI have been applied.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.





12.3. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, ILI9341 will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until "Power On Sequence" actives.





13. Power Level Definition

13.1. Power Levels

7 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

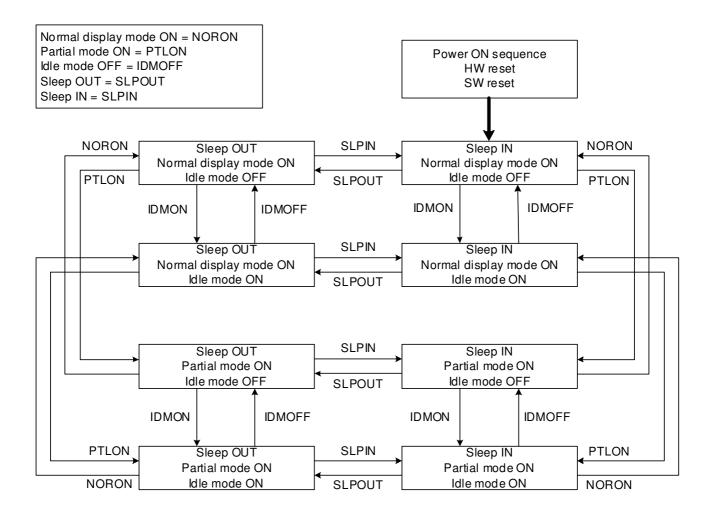
- 1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
 - In this mode, the display is able to show maximum 262,144 colors.
- 2. Partial Mode On, Idle Mode Off, Sleep Out.
 - In this mode part of the display is used with maximum 262,144 colors.
- 3. Normal Mode On (full display), Idle Mode On, Sleep Out.
 - In this mode, the full display area is used but with 8 colors.
- 4. Partial Mode On, Idle Mode On, Sleep Out.
 - In this mode, part of the display is used but with 8 colors.
- 5. Sleep In Mode.
 - In this mode, the DC: DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.
- 6. Power Off Mode.

In this mode, both VCI and VDDI are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands.



13.2. Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.





14. Gamma Curves Selection

ILI9341 provide one gamma curve Gamma2.2. The gamma curve can be selected by the GC0 settings.

14.1. Gamma Default Values (for NW type LC)

	, (101		ypc L	-,
Doto	VCOM		Voltage	Lliada
Data	VCOM :		VCOM =	
_	Gamma	2.2	Gamma	2.2
1	V0P V1P	4.084	V0N V1N	0.277
2	V1P V2P	4.015	V1N V2N	0.346
		3.843	V2N V3N	0.482
3	V3P V4P	3.681	V3N V4N	0.629
5	V4F V5P	3.518	V4N V5N	0.776
6	VSF V6P	3.445 3.371	V6N	1.071
7	Vor V7P	3.285	V7N	1.157
8	V/F V8P	3.199	V8N	1.137
9	V9P	3.128	V9N	1.314
10	V9F V10P	3.056	V10N	1.385
11	V10F V11P	2.985	V10N V11N	1.456
12	V111	2.928	V11N	1.513
13	V12F		V12N	
14	V13F V14P	2.871	V13N V14N	1.570
15	V15P	2.733		
16	V15P	2.733	V15N V16N	1.668
17	V17P	2.615	V17N	1.753
18	V17F V18P	2.557	V17N	1.795
19	V19P	2.508	V19N	1.830
20	V20P	2.458	V20N	1.865
21	V20F V21P	2.425	V20N V21N	1.899
22	V21F V22P	2.391	V21N V22N	1.932
23	V22F V23P	2.357	V23N	1.966
24	V231 V24P	2.323	V23N	2.000
25	V25P	2.289	V25N	2.034
26	V26P	2.256	V26N	2.068
27	V27P	2.222	V27N	2.102
28	V28P	2.193	V28N	2.129
29	V29P	2.165	V29N	2.155
30	V30P	2.136	V30N	2.182
31	V31P	2.108	V31N	2.208
32	V32P	2.080	V32N	2.235
33	V33P	2.051	V33N	2.262
34	V34P	2.023	V34N	2.288
35	V35P	1.994	V35N	2.315
36	V36P	1.966	V36N	2.342
37	V37P	1.942	V37N	2.368
38	V38P	1.917	V38N	2.395
39	V39P	1.893	V39N	2.421
40	V40P	1.869	V40N	2.448
41	V41P	1.845	V41N	2.475
42	V42P	1.820	V42N	2.501
43	V43P	1.796	V43N	2.528
44	V44P	1.776	V44N	2.549
45	V45P	1.755	V45N	2.571
46	V46P	1.730	V46N	2.597
47	V47P	1.706	V47N	2.623
48	V48P	1.681	V48N	2.649
49	V49P	1.653	V49N	2.679
50	V50P	1.624	V50N	2.710
51	V51P	1.598	V51N	2.735
52	V52P	1.573	V52N	2.761
53	V53P	1.541	V53N	2.793
54	V54P	1.508	V54N	2.825
55	V55P	1.476	V55N	2.857
56	V56P	1.438	V56N	2.895
57	V57P	1.400	V57N	2.933
58	V58P	1.359	V58N	2.982
59	V59P	1.319	V59N	3.031
60	V60P	1.246	V60N	3.109
61	V61P	1.173	V61N	3.186
62	V62P	1.070	V62N	3.289
63	V63P	0.279	V63N	4.083

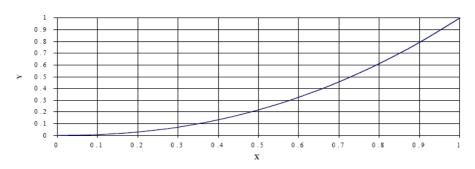




14.2. Gamma Curves

14.2.1. Gamma Curve 1 (GC0), applies the function $y=x^{2.2}$



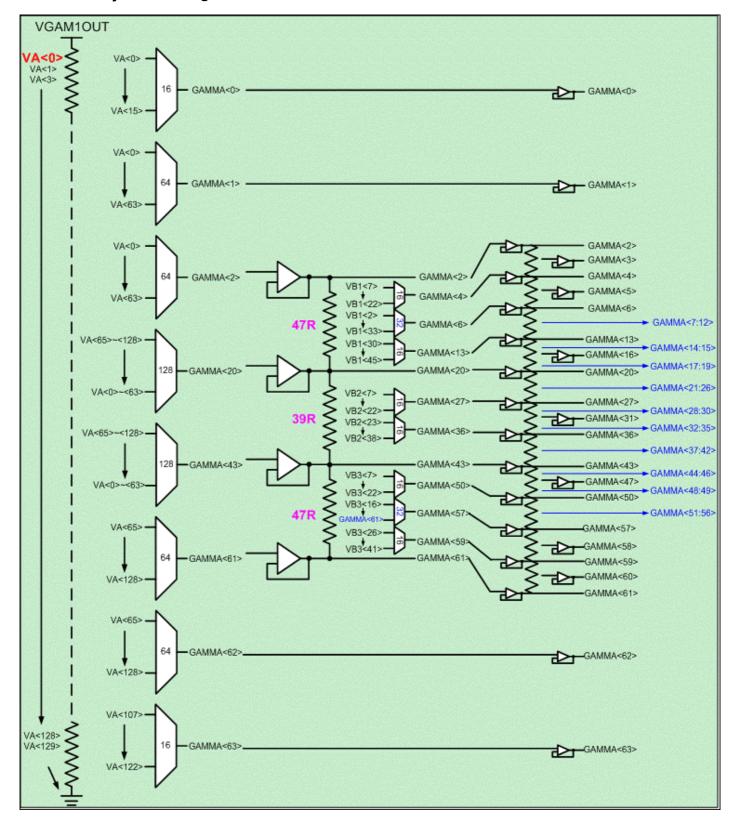






14.3. Gamma Curves

14.3.1. Grayscale Voltage Generation







14.3.2. Positive Gamma Correction

Gamma	Value "X"	Formula
Level VP0	in Formula VP0[3:0]	(VREG1-VGS)*(130R-X*R)/130R
VP1	VP0[3.0] VP1[5:0]	(VREG1-VGS) (130R-X R)/130R (VREG1-VGS)*(130R-X*R)/130R
VP2	VP2[5:0]	(VREG1-VGS)*(130R-X*R)/130R
VP3	— —	(VP2-VP4)*35R/(35R*2)+VP4
VP4	VP4[3:0]	(VP2-VP20)*(47R-X*R-7R)/47R+VP20
VP5		(VP4-VP6)*35R/(35R*2)+VP6
VP6	VP6[4:0]	(VP2-VP20)*(47R-X*R-2R)/47R+VP20
VP7		(VP6-VP13)*(12R+10R*3+8R*2)/(12R*2+10R*3+8R*2)+VP13
VP8		(VP6-VP13)*(10R*3+8R*2)/(12R*2+10R*3+8R*2)+VP13
VP9		(VP6-VP13)*(10R*2+8R*2)/(12R*2+10R*3+8R*2)+VP13
VP10	_	(VP6-VP13)*(10R+8R*2)/(12R*2+10R*3+8R*2)+VP13
VP11	_	(VP6-VP13)*(8R*2)/(12R*2+10R*3+8R*2)+VP13
VP12	_	(VP6-VP13)*8R/(12R*2+10R*3+8R*2)+VP13
VP13	VP13[3:0]	(VP2-VP20)*(47R-X*R-30R)/47R+VP20
VP14		(VP13-VP20)*(14R+12R*3+10R*2)/(14R*2+12R*3+10R*2)+VP20
VP15		(VP13-VP20)*(12R*3+10R*2)/(14R*2+12R*3+10R*2)+VP20
VP16		(VP13-VP20)*(12R*2+10R*2)/(14R*2+12R*3+10R*2)+VP20
VP17	_	(VP13-VP20)*(12R+10R*2)/(14R*2+12R*3+10R*2)+VP20
VP18		(VP13-VP20)*(10R*2)/(14R*2+12R*3+10R*2)+VP20
VP19		(VP13-VP20)*10R/(14R*2+12R*3+10R*2)+VP20
VP20	VP20[6:0]	<64 (VREG1-VGS)*(130R-X*R)/130R
\/D04	. ,	>=64 (VREG1-VGS)*(130R-X*R-1R)/130R
VP21	_	(VP20-VP27)*(12R*6)/(12R*7)+VP27
VP22	_	(VP20-VP27)*(12R*5)/(12R*7)+VP27
VP23	<u> </u>	(VP20-VP27)*(12R*4)/(12R*7)+VP27
VP24	_	(VP20-VP27)*(12R*3)/(12R*7)+VP27
VP25		(VP20-VP27)*(12R*2)/(12R*7)+VP27
VP26 VP27		(VP20-VP27)*12R/(12R*7)+VP27
VP28	VP27[3:0]	(VP20-VP43)*(39R-X*R-7R)/39R+VP43
VP29		(VP27-VP36)*(8R*8)/(8R*9)+VP36 (VP27-VP36)*(8R*7)/(8R*9)+VP36
VP30		(VP27-VP36)*(8R*6)/(8R*9)+VP36
VP31	_	(VP27-VP36)*(8R*5)/(8R*9)+VP36
VP32		(VP27-VP36)*(8R*4)/(8R*9)+VP36
VP33		(VP27-VP36)*(8R*3)/(8R*9)+VP36
VP34	_	(VP27-VP36)*(8R*2)/(8R*9)+VP36
VP35	_	(VP27-VP36)*8R/(8R*9)+VP36
VP36	VP36[3:0]	(VP20-VP43)*(39R-X*R-23R)/39R+VP43
VP37	—	(VP36-VP43)*(12R*6)/(12R*7)+VP43
VP38	_	(VP36-VP43)*(12R*5)/(12R*7)+VP43
VP39	_	(VP36-VP43)*(12R*4)/(12R*7)+VP43
VP40	_	(VP36-VP43)*(12R*3)/(12R*7)+VP43
VP41	_	(VP36-VP43)*(12R*2)/(12R*7)+VP43
VP42	_	(VP36-VP43)*12R/(12R*7)+VP43
VP43	VP43[6:0]	<64 (VREG1-VGS)*(130R-X*R)/130R
VF45	VF45[0.0]	>=64 (VREG1-VGS)*(130R-X*R-1R)/130R
VP44		(VP43-VP50)*(14R*2+12R*3+10R)/(14R*2+12R*3+10R*2)+VP50
VP45		(VP43-VP50)*(14R*2+12R*3)/(14R*2+12R*3+10R*2)+VP50
VP46		(VP43-VP50)*(14R*2+12R*2)/(14R*2+12R*3+10R*2)+VP50
VP47		(VP43-VP50)*(14R*2+12R)/(14R*2+12R*3+10R*2)+VP50
VP48		(VP43-VP50)*(14R*2)/(14R*2+12R*3+10R*2)+VP50
VP49		(VP43-VP50)*14R/(14R*2+12R*3+10R*2)+VP50
VP50	VP50[3:0]	(VP43-VP61)*(47R-X*R-7R)/47R+VP61
VP51	_	(VP50-VP57)*(12R*2+10R*3+8R)/(12R*2+10R*3+8R*2)+VP57
VP52	<u> </u>	(VP50-VP57)*(12R*2+10R*3)/(12R*2+10R*3+8R*2)+VP57
VP53		(VP50-VP57)*(12R*2+10R*2)/(12R*2+10R*3+8R*2)+VP57
VP54	<u> </u>	(VP50-VP57)*(12R*2+10R)/(12R*2+10R*3+8R*2)+VP57
VP55	_	(VP50-VP57)*(12R*2)/(12R*2+10R*3+8R*2)+VP57
VP56	<u> </u>	(VP50-VP57)*12R/(12R*2+10R*3+8R*2)+VP57
VP57	VP57[4:0]	(VP43-VP61)*(47R-X*R-16R)/47R+VP61
VP58	— VD5000:03	(VP57-VP59)*35R/(35R*2)+VP59
VP59 VP60	VP59[3:0]	(VP43-VP61)*(47R-X*R-26R)/47R+VP61
VP60 VP61	— VP61[5:0]	(VP59-VP61)*35R/(35R*2)+VP61
VP62	VP61[5.0] VP62[5:0]	(VREG1-VGS)*(65R-X*R)/130R (VREG1-VGS)*(65R-X*R)/130R
VP63	VP63[3:0]	(VREG1-VGS) (65R-X K)/136R (VREG1-VGS)*(23R-X*R)/130R
	VI 00[0.0]	(Tites 100) (Early 1971001)





14.3.3. Negative Gamma Correction

Gamma Level	Value "X" in Formula	Formula			
VN63	VN63[3:0]	(VREG1-VGS)*(130R-X*R)/130R			
VN62	VN62[5:0]	(VREG1-VGS)*(130R-X*R)/130R			
VN61	VN61[5:0]	(VREG1-VGS)*(130R-X*R)/130R			
VN60	_	(VN61-VN59)*35R/(35R*2)+VN59			
VN59	VN59[3:0]	(VN61-VN43)*(47R-X*R-7R)/47R+VN43			
VN58	_	(VN59-VN57)*35R/(35R*2)+VN57			
VN57	VN57[4:0]	(VN61-VN43)*(47R-X*R-2R)/47R+VN43			
VN56	_	(VN57-VN50)*(12R+10R*3+8R*2)/(12R*2+10R*3+8R*2)+VN50			
VN55	_	(VN57-VN50)*(10R*3+8R*2)/(12R*2+10R*3+8R*2)+VN50			
VN54	_	(VN57-VN50)*(10R*2+8R*2)/(12R*2+10R*3+8R*2)+VN50			
VN53 VN52		(VN57-VN50)*(10R+8R*2)/(12R*2+10R*3+8R*2)+VN50			
VN51	_	(VN57-VN50)*(8R*2)/(12R*2+10R*3+8R*2)+VN50 (VN57-VN50)*8R/(12R*2+10R*3+8R*2)+VN50			
VN50	VN50[3:0]	(VN61-VN43)*(47R-X*R-30R)/47R+VN43			
VN49	- V1430[3.0]	(VN50-VN43)*(14R+12R*3+10R*2)/(14R*2+12R*3+10R*2)+VN43			
VN48	_	(VN50-VN43)*(12R*3+10R*2)/(14R*2+12R*3+10R*2)+VN43			
VN47	_	(VN50-VN43)*(12R*2+10R*2)/(14R*2+12R*3+10R*2)+VN43			
VN46	_	(VN50-VN43)*(12R+10R*2)/(14R*2+12R*3+10R*2)+VN43			
VN45	_	(VN50-VN43)*(10R*2)/(14R*2+12R*3+10R*2)+VN43			
VN44	_	(VN50-VN43)*10R/(14R*2+12R*3+10R*2)+VN43			
VN43	VN43[6:0]	<64 (VREG1-VGS)*(130R-X*R)/130R			
	V1443[0.0]	>=64 (VREG1-VGS)*(130R-X*R-1R)/130R			
VN42	_	(VN43-VN36)*(12R*6)/(12R*7)+VN36			
VN41	_	(VN43-VN36)*(12R*5)/(12R*7)+VN36			
VN40	_	(VN43-VN36)*(12R*4)/(12R*7)+VN36			
VN39	_	(VN43-VN36)*(12R*3)/(12R*7)+VN36			
VN38	<u> </u>	(VN43-VN36)*(12R*2)/(12R*7)+VN36			
VN37		(VN43-VN36)*12R/(12R*7)+VN36			
VN36	VN36[3:0]	(VN43-VN20)*(39R-X*R-7R)/39R+VN20			
VN35 VN34	<u> </u>	(VN36-VN27)*(8R*8)/(8R*9)+VN27			
VN33		(VN36-VN27)*(8R*7)/(8R*9)+VN27			
VN32		(VN36-VN27)*(8R*6)/(8R*9)+VN27 (VN36-VN27)*(8R*5)/(8R*9)+VN27			
VN31	_	(VN36-VN27)*(8R*4)/(8R*9)+VN27			
VN30	_	(VN36-VN27)*(8R*3)/(8R*9)+VN27			
VN29	_	(VN36-VN27)*(8R*2)/(8R*9)+VN27			
VN28	_	(VN36-VN27)*8R/(8R*9)+VN27			
VN27	VN27[3:0]	(VN43-VN20)*(39R-X*R-23R)/39R+VN20			
VN26	_	(VN27-VN20)*(12R*6)/(12R*7)+VN20			
VN25		(VN27-VN20)*(12R*5)/(12R*7)+VN20			
VN24		(VN27-VN20)*(12R*4)/(12R*7)+VN20			
VN23	_	(VN27-VN20)*(12R*3)/(12R*7)+VN20			
VN22	_	(VN27-VN20)*(12R*2)/(12R*7)+VN20			
VN21		(VN27-VN20)*12R/(12R*7)+VN20			
VN20	VN20[6:0]	<64 (VREG1-VGS)*(130R-X*R)/130R >=64 (VREG1-VGS)*(130R-X*R-1R)/130R			
VN19	_	>=64 (VREG1-VGS)*(130R-X*R-1R)/130R (VN20-VN13)*(14R*2+12R*3+10R)/(14R*2+12R*3+10R*2)+VN13			
VN18	_	(VN20-VN13)*(14R*2+12R*3+10R);(14R*2+12R*3+10R*2)+VN13			
VN17	_	(VN20-VN13)*(14R*2+12R*2)/(14R*2+12R*3+10R*2)+VN13			
VN16	_	(VN20-VN13)*(14R*2+12R)/(14R*2+12R*3+10R*2)+VN13			
VN15	_	(VN20-VN13)*(14R*2)/(14R*2+12R*3+10R*2)+VN13			
VN14	_	(VN20-VN13)*14R/(14R*2+12R*3+10R*2)+VN13			
VN13	VN13[3:0]	(VN20-VN2)*(47R-X*R-7R)/47R+VN2			
VN12		(VN13-VN6)*(12R*2+10R*3+8R)/(12R*2+10R*3+8R*2)+VN6			
VN11		(VN13-VN6)*(12R*2+10R*3)/(12R*2+10R*3+8R*2)+VN6			
VN10	_	(VN13-VN6)*(12R*2+10R*2)/(12R*2+10R*3+8R*2)+VN6			
VN9	_	(VN13-VN6)*(12R*2+10R)/(12R*2+10R*3+8R*2)+VN6			
VN8	<u> </u>	(VN13-VN6)*(12R*2)/(12R*2+10R*3+8R*2)+VN6			
VN7	-	(VN13-VN6)*12R/(12R*2+10R*3+8R*2)+VN6			
VN6	VN6[4:0]	(VN20-VN2)*(47R-X*R-16R)/47R+VN2			
VN5 VN4		(VN6-VN4)*35R/(35R*2)+VN4			
VN3	VN4[3:0] —	(VN20-VN2)*(47R-X*R-26R)/47R+VN2 (VN4-VN2)*35R/(35R*2)+VN2			
VN2	VN2[5:0]	(VN44-VN2) 33R((33R-2)+VN2 (VREG1-VGS)*(65R-X*R)/130R			
VN1	VN1[5:0]	(VREG1-VGS)*(65R-X*R)/130R			
VN0	VN0[3:0]	(VREG1-VGS)*(23R-X*R)/130R			
		, (





15. **Reset**

15.1. Registers

The registers that are initialized are listed as below:

	After Powered ON	After Hardware Reset	After Software Reset
Frame Memory	Random	Repair data	No Change
Sleep	In	In	In
Display Mode	Normal	Normal	Normal
Display	Off	Off	Off
ldle	Off	Off	Off
Column Start Address	0000 h	0000 h	0000 h
Column End Address	00EF h	00EF h	If MADCTL's B5=0:00EF h If MADCTL's B5=1:013F h
Page Start Address	0000 h	0000 h	0000 h
Page End Address	013F h	013F h	If MADCTL's B5 = 0:013F h If MADCTL's B5=1:00EF h
Gamma Setting	GC0	GC0	GC0
Partial Area Start	0000 h	0000 h	0000 h
Partial Area End	013F h	013F h	013F h
Memory Data Access Control	00 h	00 h	No Change
RDDPM	08 h	08 h	08 h
RDDMADCTL	00 h	00 h	No Change
RDDCOLMOD	06 h	06 h	06 h
RDDIM	00 h	00 h	00 h
RDDSM	00 h	00 h	00 h
RDDSDR	00 h	00 h	00 h
TE Output Line	Off	Off	Off
TE Line Mode	Mode 1 (Note 3)	Mode 1 (Note 3)	Mode 1 (Note 3)

Note 1: There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.

Note 2: After Powered-On Reset finishes within 10µs after both VCI & VDDI are applied.

Note 3: Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.





15.2. Output Pins, I/O Pins

	After Power ON	After Hardware Reset	After Software Reset	
TE line	Low	Low	Low	
D[17:0] (output driver)	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)	

Note 1: There will be no output from D [17:0] during Power ON/OFF sequence, hardware reset and software reset.

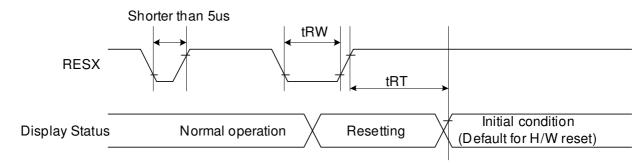
15.3. Input Pins

	During Power ON Process			After Software Reset	During Power OFF Process	
RESX	See Chapter 12	Input valid	Input valid	Input valid	See Chapter 12	
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid	
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid	
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid	
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid	
D[17:0] (input driver)	Input invalid	Input valid	Input valid	Input valid	Input invalid	





15.4. Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Penet cancel		5 (note 1,5)	mS
	IN I	Reset cancel		120 (note 1,6,7)	mS

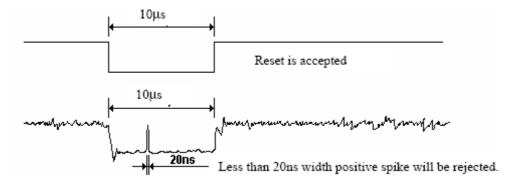
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action		
Shorter than 5us	Reset Rejected		
Longer than 10us	Reset		
Between 5us and 10us	Reset starts		

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



- Note 5: When Reset applied during Sleep In Mode.
- Note 6: When Reset applied during Sleep Out Mode.
- Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

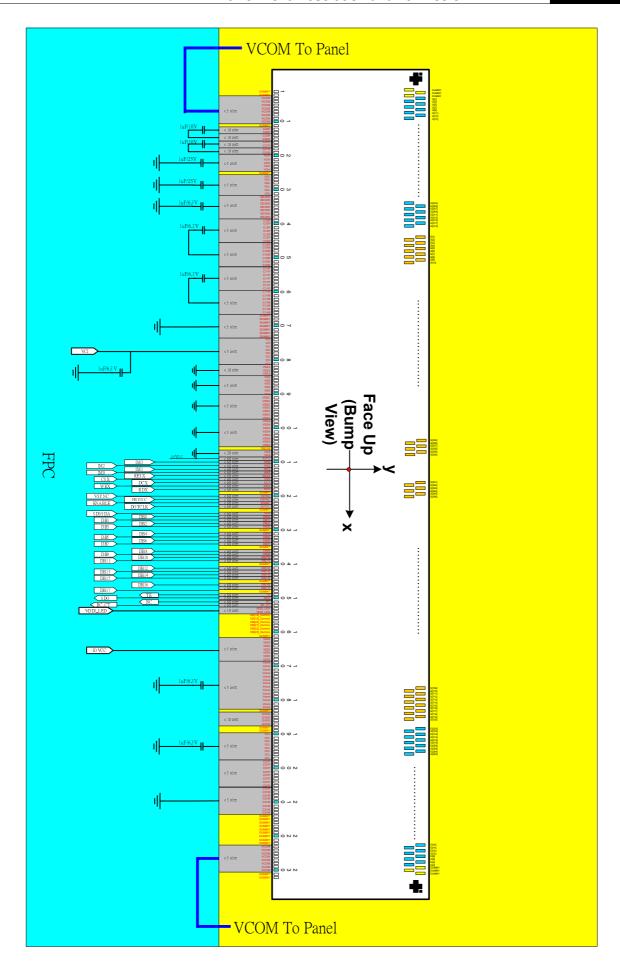






16. Configuration of Power Supply Circuit









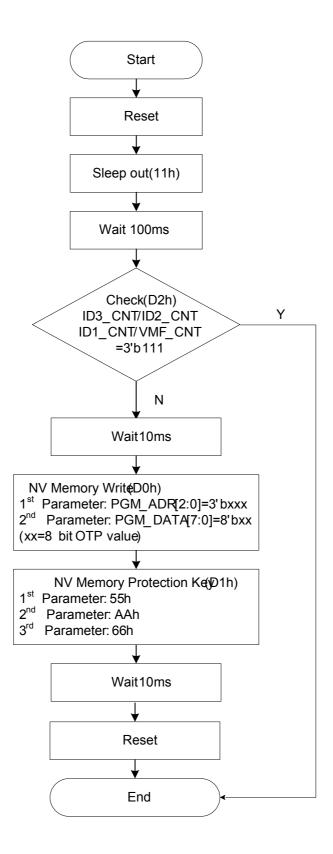
The Following tables shows specifications of external elements connected to the ILI9341's power supply circuit.

Items	Recommended Specification	Pin connection
Capacity 1 µF (B characteristics)	6.3V	DDVDH ,VCL,C11P/M,C12P/M,Vcore,VCI
	10V	C21P/M,C22P/M
	25V	VGL, VGH



ILI9341

17. NV Memory Programming Flow







18. Electrical Characteristics

18.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9341 is used out of the absolute maximum ratings, ILI9341 may be permanently damaged. To use ILI9341 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, ILI9341 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3 ~ +4.6
Supply voltage (Logic)	VDDI	V	-0.3 ~ +4.6
Supply voltage (Digital)	VCORE	V	-0.3 ~ + <mark>2.0</mark>
Driver supply voltage	VGH-VGL	V	-0.3 ~ +32.0
Logic input voltage range	VIN	V	-0.3 ~ VDDI + 0.3
Logic output voltage range	VO	V	-0.3 ~ VDDI + 0.3
Operating temperature	Topr	$^{\circ}\mathbb{C}$	-40 ~ +85
Storage temperature	Tstg	$^{\circ}$	-55 ~ +110

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.





18.2 DC Characteristics

18.2.1 General DC Characteristics

Power and Operating	Item	Symbol	Unit	Condition	Min.	Тур.	Max.	Note
Analog Operating			0	oonanion.		- 7		11010
Voltage								
Voltage		VCI	V	Operating voltage	2.5	2.8	3.3	Note2
Voltage		VDDI	V	I/O cupply voltage	1.65	2.0	2.2	Noto2
voltage VCORE V Digital supply Voltage - 1.3 - Note2 Gate Driver High Voltage VGH V - 10.0 - 16.0 Note3 Gate Driver Low Voltage VGL V - -10.0 - -5.0 Note3 Driver Supply Voltage - V IVGH-VGL 15 - 28 Note3 Current consumption during standby mode Isr μA VCI-2.8V , Ta=25 °C - - 100 - Logic High Level Input Voltage VIL V - 0.7°VDDI - VDDI Note1,2,3 Logic Low Level Input Voltage VOH V IOL=1.0mA 0.8°VDDI - VDDI Note1,2,3 Logic Low Level Input Voltage VOL V IOL=1.0mA VSS - 0.2°VDDI Note1,2,3 Logic Low Level Input Current III uA - - 1 Note1,2,3 Logic Low Level Input Current III uA -		VDDI	v	70 Supply Voltage	1.00	2.0	3.3	Notez
Vorlage		VCORE	V	Digital supply voltage	-	1.5	-	Note2
Voltage	Ü			0 117				
Gate Driver Low Voltage	<u> </u>	VGH	V	-	10.0	-	16.0	Note3
Voltage) (O)	.,		40.0			
Current consumption during standby mode I _{ST} μA VCI=2.8V , Ta=25 °C - - 100 - Input and Output Logic High Level Input Voltage VIH V - 0.7*VDDI - VDDI Note1,2,3 Logic Low Level Input Voltage VOH V IOL=1.0mA 0.8*VDDI - VDDI Note1,2,3 Logic Low Level Output Voltage VOL V IOL=1.0mA VSS - 0.2*VDDI Note1,2,3 Logic Low Level Output Voltage VOL V IOL=1.0mA VSS - 0.2*VDDI Note1,2,3 Logic Low Level Input Current IIH uA - - - 1 Note1,2,3 Logic Low Level input Current IIL uA VIN=VDDI or VSS - 0.2*VDDI Note1,2,3 Logic Input Leakage Current ILEA uA VIN=VDDI or VSS - 0.1 +0.1 Note1,2,3 VCOM High Voltage VCOME VOMA V Ccom=12nF 2.5 - 5.0 Note3		VGL	V	-	-10.0	ı	-5.0	Note3
Input and Output Input and Output VIH	Driver Supply Voltage	-	V	VGH-VGL	15	-	28	Note3
Input and Output Input and Output VIH	Current concumption							
Input and Output		I _{ST}	μΑ	VCI=2.8V , Ta=25 ℃	-	-	100	-
Logic High Level Input Voltage	daning standby mode							
Voltage		_						
Voltage		VIH	V	-	0.7*VDDI	_	VDDI	Note1.2.3
Voltage					0 122.			
Description Logic High Level Output Voltage VOH V IOL=1.0mA 0.8*VDDI - VDDI Note1,2,3		VIL	V	-	VSS	-	0.3*VDDI	Note1,2,3
Output Voltage VOH V IOL=1.0mA U.8*VDDI - VDDI Note1,2,3 Logic Low Level Output Voltage VOL V IOL=1.0mA VSS - 0.2*VDDI Note1,2,3 Logic High Level Input Current IIH uA - - - 1 Note1,2,3 Logic Low Level input Current IILEA uA VIN=VDDI or VSS -0.1 - +0.1 Note1,2,3 Logic Input Leakage Current ILEA uA VIN=VDDI or VSS -0.1 - +0.1 Note1,2,3 VCOM Operation VCOM Meligh Voltage VCOMH V Ccom=12nF 2.5 - 5.0 Note3 VCOM Low Voltage VCOMA V VCOMH-VCOML 4.0 - 5.5 Note3 VCOM Amplitude Voltage VCOMA V VCOMH-VCOML 4.0 - 5.5 Note3 Source Driver Source Output Range Vsout V - 0.1 - DDVDH-0.1 Note4 Gamma Re	<u> </u>							
Logic Low Level Output Voltage	5 5	VOH	V	IOL=-1.0mA	0.8*VDDI	-	VDDI	Note1,2,3
Courent Current Curr		VOI	W	IOI 1 0m A	Vee		0.0*\/DDI	Noted 2.2
Current	,	VOL	V	IOL=1.0IIIA	VSS	-	0.2 VDDI	100te 1,2,3
Current Logic Low Level input Current IIL uA - -1 - - Note1,2,3 Current Logic Input Leakage Current ILEA uA VIN=VDDI or VSS -0.1 - +0.1 Note1,2,3 VCOM Operation VCOM High Voltage VCOMH V Ccom=12nF 2.5 - 5.0 Note3 VCOM Low Voltage VCOMA V IVCOMH-VCOMLI 4.0 - 5.5 Note3 VCOM Amplitude Voltage VCOMA V IVCOMH-VCOMLI 4.0 - 5.5 Note3 Source Driver Source Output Range Vsout V - 0.1 - DDVDH-0.1 Note4 Gamma Reference Voltage GVDD V - 3.0 - 5.0 Note3 Output Deviation Voltage (Source Output Channel) Vdev mV Sout<		IIH	uA	-	-	-	1	Note1.2.3
Current								, ,-
Logic Input Leakage Current		IIL	uA	-	-1	-	-	Note1,2,3
Current Curr								
VCOM High Voltage VCOMH V Ccom=12nF 2.5 - 5.0 Note3 VCOM Low Voltage VCOML V Ccom=12nF -2.5 - 0.0 Note3 VCOM Amplitude Voltage VCOMA V VCOMH-VCOML 4.0 - 5.5 Note3 Source Driver Source Output Range Vsout V - 0.1 - DDVDH-0.1 Note4 Gamma Reference Voltage GVDD V - 3.0 - 5.0 Note3 Output Deviation Voltage (Source Output channel) Vdev mV Sout>=4.2V Sout>0.8V - - - 20 Note4 Output Offset Voltage VOFSET mV - - - - 35 Note7 Booster Operation 1st Booster (VCIx2) Voltage DDVDH V - 4.95 (Note 5) - 5.8 (Note 6) Note3 1st Booster (VCIx2 Drop Voltage Voltage % loading=1mA - - - 5 Note3		ILEA	uA	VIN=VDDI or VSS	-0.1	-	+0.1	Note1,2,3
VCOM Low Voltage VCOML V Ccom=12nF -2.5 - 0.0 Note3 VCOM Amplitude Voltage VCOMA V VCOMH-VCOML 4.0 - 5.5 Note3 Source Driver Source Output Range Vsout V - 0.1 - DDVDH-0.1 Note4 Gamma Reference Voltage GVDD V - 3.0 - 5.0 Note3 Output Deviation Voltage (Source Output channel) Vdev mV Sout>=4.2V Sout>=0.8V - - 20 Note4 Output Offset Voltage VOFSET mV - - - 35 Note7 Booster Operation 1st Booster (VCIx2) Voltage DDVDH V - 4.95 (Note 5) - 5.8 (Note 6) Note3 1st Booster (VCIx2 Drop Voltage VCIx2 drop % loading=1mA - - - 5 Note3	VCOM Operation							
VCOM Amplitude Voltage VCOMA V VCOMH-VCOML 4.0 - 5.5 Note3 Source Driver Source Output Range Vsout V - 0.1 - DDVDH-0.1 Note4 Gamma Reference Voltage GVDD V - 3.0 - 5.0 Note3 Output Deviation Voltage (Source Output channel) Vdev mV Sout<=4.2V Sout<>0.8V - - 20 Note4 Output Offset Voltage VOFSET mV - - - 15 - Booster Operation 1st Booster (VClx2) Voltage DDVDH V - 4.95 (Note 5) - 5.8 (Note 6) Note3 1st Booster (VClx2 Drop Voltage VClx2 drop % loading=1mA - - 5 Note3	VCOM High Voltage	VCOMH	V	Ccom=12nF	2.5	-	5.0	Note3
Voltage		VCOML	V	Ccom=12nF	-2.5	-	0.0	Note3
Source Driver Source Output Range Vsout V -	•	VCOMA	V	VCOMH-VCOML	4.0	-	5.5	Note3
Source Output Range	•			'				
Gamma Reference Voltage GVDD V - 3.0 - 5.0 Note3 Output Deviation Voltage (Source Voltage (Source Output channel) Vdev mV Sout >= 4.2 V Sout >= 0.8 V - - - 20 Note4 Output Offset Voltage VOFSET mV 4.2 V > Sout >= 0.8 V - - - 15 - Booster Operation 1st Booster (VCIx2) Voltage DDVDH V - 4.95 (Note 5) - 5.8 (Note 6) Note3 1st Booster (VCIx2 Drop Voltage VCIx2 drop % loading=1mA - - 5 Note3		Vocut	\/		0.1			Noto 4
Voltage GVDD V - 3.0 - 5.0 Note3 Output Deviation Voltage (Source Output channel) Vdev mV Sout>=4.2V Sout>= - - - 20 Note4 Output channel) 4.2V>Sout>=0.8V - - - 15 - Output Offset Voltage VOFSET mV - - - 35 Note7 Booster Operation 1st Booster (VCIx2) Voltage DDVDH V - 4.95 (Note 5) - 5.8 (Note 6) Note3 1st Booster (VCIx2 Drop Voltage VCIx2 drop % loading=1mA - - 5 Note3				-		-		
Output Deviation Voltage (Source Voltage (Source Output channel) Vdev mV Sout>=4.2V Sout - - 20 Note4 Output Offset Voltage VOFSET mV 4.2V>Sout>0.8V - - - 15 - Booster Operation 1st Booster (VCIx2) Voltage DDVDH V - 4.95 (Note 5) - 5.8 (Note 6) Note3 1st Booster (VCIx2) Voltage VCIx2 drop % loading=1mA - - 5 Note3		GVDD	V	-	3.0	-	5.0	Note3
Voltage (Source Output channel) Vdev MV MV Sout<=0.8V - - - 20 Note4 Output channel) 4.2V>Sout>0.8V - - - 15 - Output Offset Voltage VOFSET MV - - - 35 Note7 Booster Operation 1st Booster (VCIx2) Voltage DDVDH V - 4.95 (Note 5) - 5.8 (Note 6) Note3 1st Booster (VCIx2 Drop Voltage VCIx2 drop % loading=1mA - - - 5 Note3				Sout>=4.2V			00	Note 4
Output Offset Voltage VOFSET mV - - - 35 Note7 Booster Operation 1st Booster (VCIx2) Voltage DDVDH V - 4.95 (Note 5) - 5.8 (Note 6) Note3 1st Booster (VCIx2 Drop Voltage VCIx2 drop % loading=1mA - - - 5 Note3		Vdev	mV		-	-	20	Note4
Booster Operation				4.2V>Sout>0.8V	-	-		-
1st Booster (VCIx2) DDVDH V - 4.95 (Note 5) - 5.8 (Note 6) Note3 1st Booster (VCIx2 Drop Voltage VCIx2 drop % loading=1mA - - 5 Note3		VOFSET	mV	-	-	-	35	Note7
Voltage DDVDH V - (Note 5) - (Note 6) Note3 1 st Booster (VCIx2 VCIx2 drop % loading=1mA - - 5 Note3		ı			4.5-			<u> </u>
Voltage (Note 5) (Note 6) 1st Booster (VCIx2 VCIx2 drop % loading=1mA - 5 Note3	· · ·	DDVDH	٧	-		-		Note3
Drop Voltage drop % loading=TitiA 5 Notes		VClv2	-		(INO(6 2)			
			%	loading=1mA	-	-	5	Note3
	Liner Range		٧	-	0.2	-	DDVDH-0.2	





Note 1: VDDI=1.65 to 3.3V, VCI=2.5 to 3.3V, AGND=VSS=0V, Ta=-30 to 70 (to +85 no damage) \mathcal{C} .

Note2: Please supply digital VDDI voltage equal or less than analog VCI voltage.

Note3: CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, SCL, IM3, IM2, IM1, IM0, and Test pins.

Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

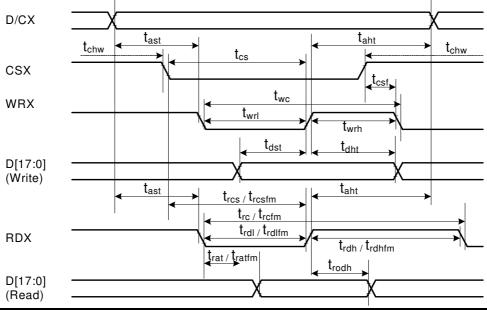
Note5: VCI=2.6V Note6: VCI=3.3V

Note7: The Max. Value is between with Note 4 measure point and Gamma setting value



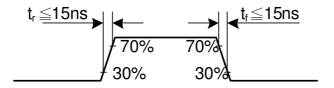
18.3 AC Characteristics

18.3.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- I system)



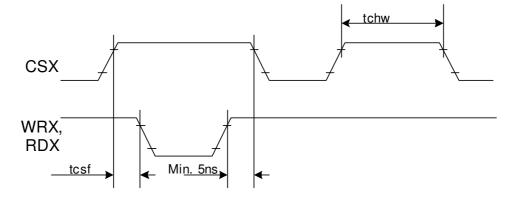
Signal	Symbol	Parameter	min	max	Unit	Description
DCX tast		Address setup time	0	-	ns	
DCX	taht	Address hold time (Write/Read)	0	-	ns	
	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
CSX	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
	twc	Write cycle	66	-	ns	
WRX	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
	trcfm	Read Cycle (FM)	450	-	ns	
RDX (FM)	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
	trc	Read cycle (ID)	160	-	ns	
RDX (ID)	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[47.0]	tdst	Write data setup time	10	-	ns	
D[17:0],	tdht	Write data hold time	10	-	ns	For maximum CL 20nF
D[15:0], D[8:0],	trat	Read access time	-	40	ns	For maximum CL=30pF For minimum CL=8pF
D[8:0], D[7:0]	tratfm	Read access time	-	340	ns	I of millimum GL=opr
D[7.0]	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V



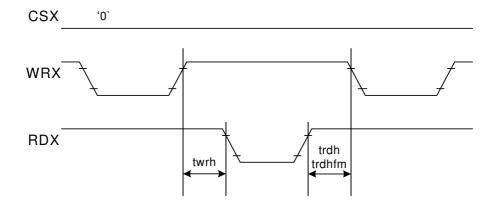


CSX timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

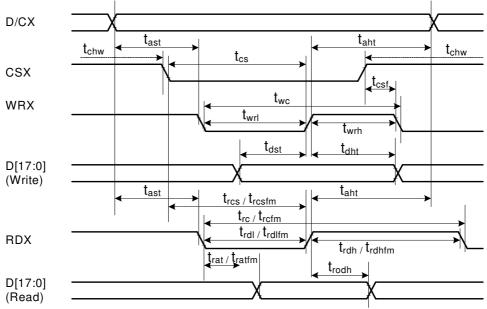
Write to read or read to write timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

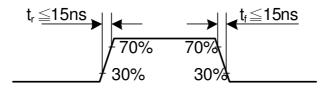


18.3.2 Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080- II system)



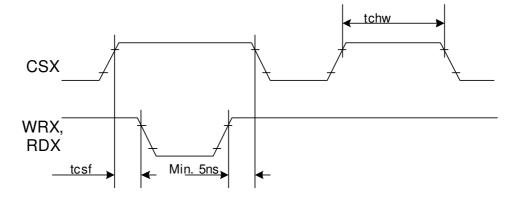
Signal	Symbo	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
DCX	taht	Address hold time (Write/Read)	0	-	ns	
	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
CSX	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
	twc	Write cycle	66	-	ns	
WRX	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
	trcfm	Read Cycle (FM)	450	-	ns	
RDX (FM)	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
	trc	Read cycle (ID)	160	-	ns	
RDX (ID)	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1],	tdst	Write data setup time	10	-	ns	
	tdht	Write data hold time	10	-	ns	For maximum CL 2055
	trat	Read access time	-	40	ns	For maximum CL=30pF For minimum CL=8pF
D[17:10], D[17:9]	tratfm	Read access time	ı	340	ns	For minimum CL=opF
D[17.3]	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.



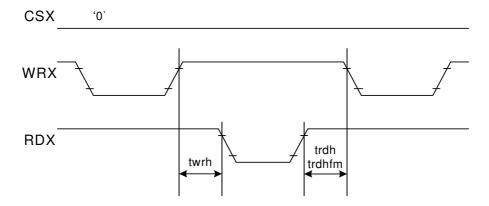


CSX timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:

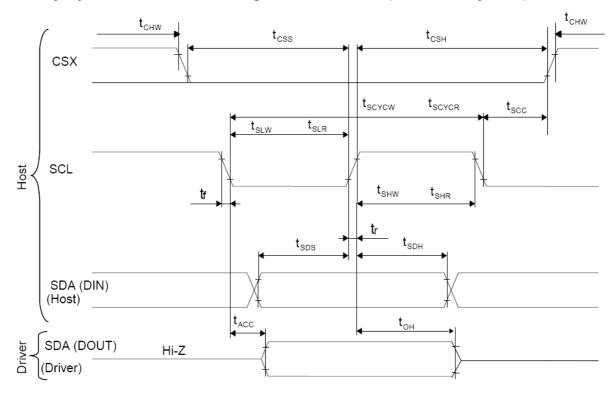


Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.



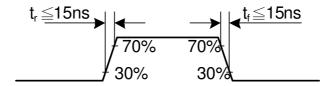


18.3.3 Display Serial Interface Timing Characteristics (3-line SPI system)



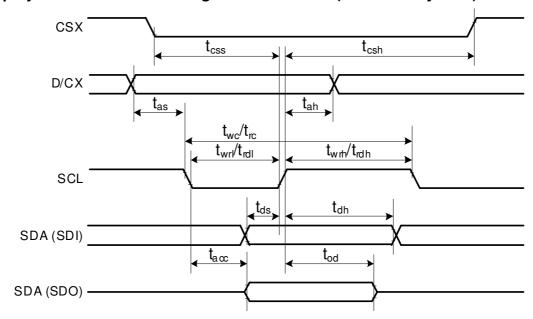
Signal	Symbol	Parameter	min	max	Unit	Description
	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
SCL	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
SCL	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI	SDA / SDI tsds Data setup time (Write)		30	-	ns	
(Input)	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO	tacc	Access time (Read)	10	1	ns	
(Output) toh		Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	ı	ns	
	tchw	CSX "H" Pulse Width	40	ı	ns	
	tcss	CCV CCL Time	60	1	ns	
	tcsh	CSX-SCL Time	65	-	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V



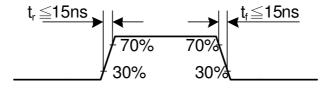


18.3.4 Display Serial Interface Timing Characteristics (4-line SPI system)



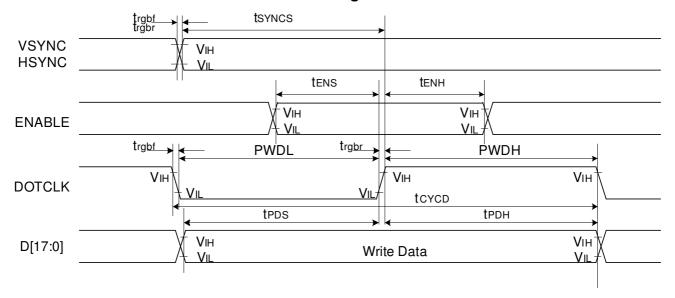
Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL "H" pulse width (Write)	40	-	ns	
SCL	twrl	SCL "L" pulse width (Write)	40	-	ns	
SCL	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
D/GX	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI	tds	Data setup time (Write)	30	-	ns	
(Input) tdh		Data hold time (Write)	30	-	ns	
SDA/SDO	tacc	Access time (Read) 10 - ns		ns	For maximum CL=30pF	
(Output)	(Output) tod Output disable time (Read)		10	50	ns	For minimum CL=8pF

Note: $Ta = 25 \, ^{\circ}$ C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V



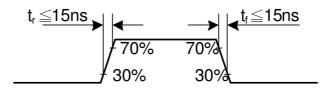


18.3.5 Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter min max				Description	
VSYNC /	tsyncs	VSYNC/HSYNC setup time		-	ns		
HSYNC	tsynch	VSYNC/HSYNC hold time	15	-	ns		
DE	t _{ENS}	DE setup time	15	-	ns		
DE	t _{ENH}	DE hold time	-	ns			
D[17:0]	t _{POS}	Data setup time	15	-	ns	18/16-bit bus RGB	
D[17.0]	t _{PDH}	Data hold time	15	-	ns	interface mode	
	PWDH	DOTCLK high-level period	15	-	ns		
DOTCLK	PWDL	DL DOTCLK low-level period		-	ns		
DOTOLK	t _{CYCD}	DOTCLK cycle time	100	-	ns		
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	15	ns			
VSYNC /	t _{SYNCS}	VSYNC/HSYNC setup time	15	-	ns		
HSYNC	tsynch	VSYNC/HSYNC hold time	15	-	ns		
DE	t _{ENS}	DE setup time	15	-	ns		
DE	t _{ENH}	DE hold time	15	-	ns		
D[17:0]	t _{POS}	Data setup time	15	-	ns	6-bit bus RGB	
	t _{PDH}	Data hold time	15	-	ns	interface mode	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns		
	PWDL	DOTCLK low-level pulse period	15	-	ns		
	t _{CYCD}	DOTCLK cycle time	100	-	ns		
	t _{rgbr} , t _{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns		

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V







19 Revision History

Version No.	Date	Page	Description			
V1.00	2010/10/12	All	New Created.			
V1.01	2010/10/12	179	Update charge pump ratio			
V1.02	2010/12/17	35,195~200	Add description of extend register command			
V1.03	2010/12/20	196	Modify description of pumping			
V1.04	2010/12/24	All	Update extend register and OTP flow			
V1.05	2011/01/05	All	Update extend register			
V1.06	2011/01/20	16,230	No.75 pad location, DC Characteristics			
V1.07	2011/02/24	199,226,227	Modify register, external element.			
V1.08	2011/03/04	179,196,227,228	Analog supply voltage naming, external element, DDVDH Max, Modify C1h,CFh			
			default setting			
V1.09	2011/03/15	9,159,197,199,226	Update clock timing, IC Configuration, E8h, EDh			
V1.10	2011/04/15	226	Update for general FPC application			