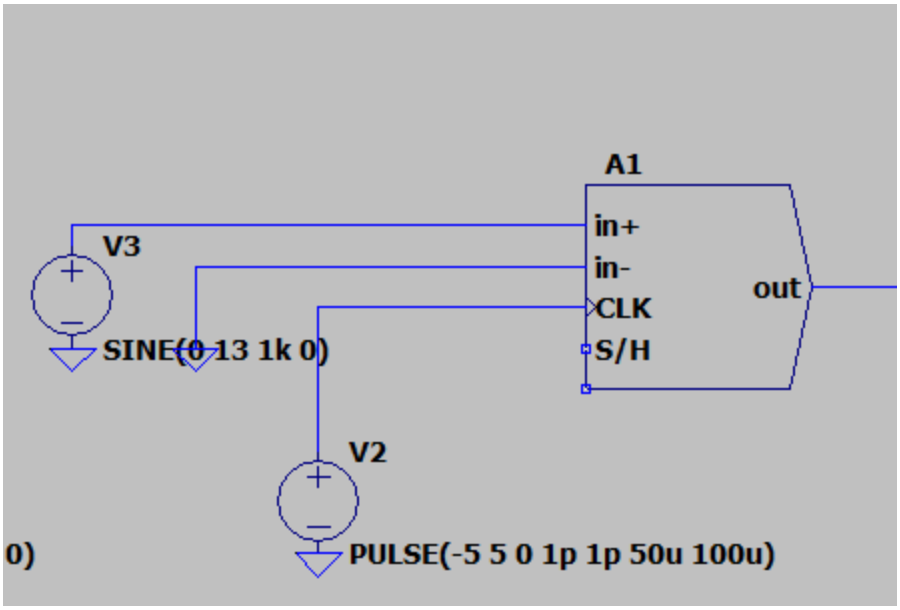
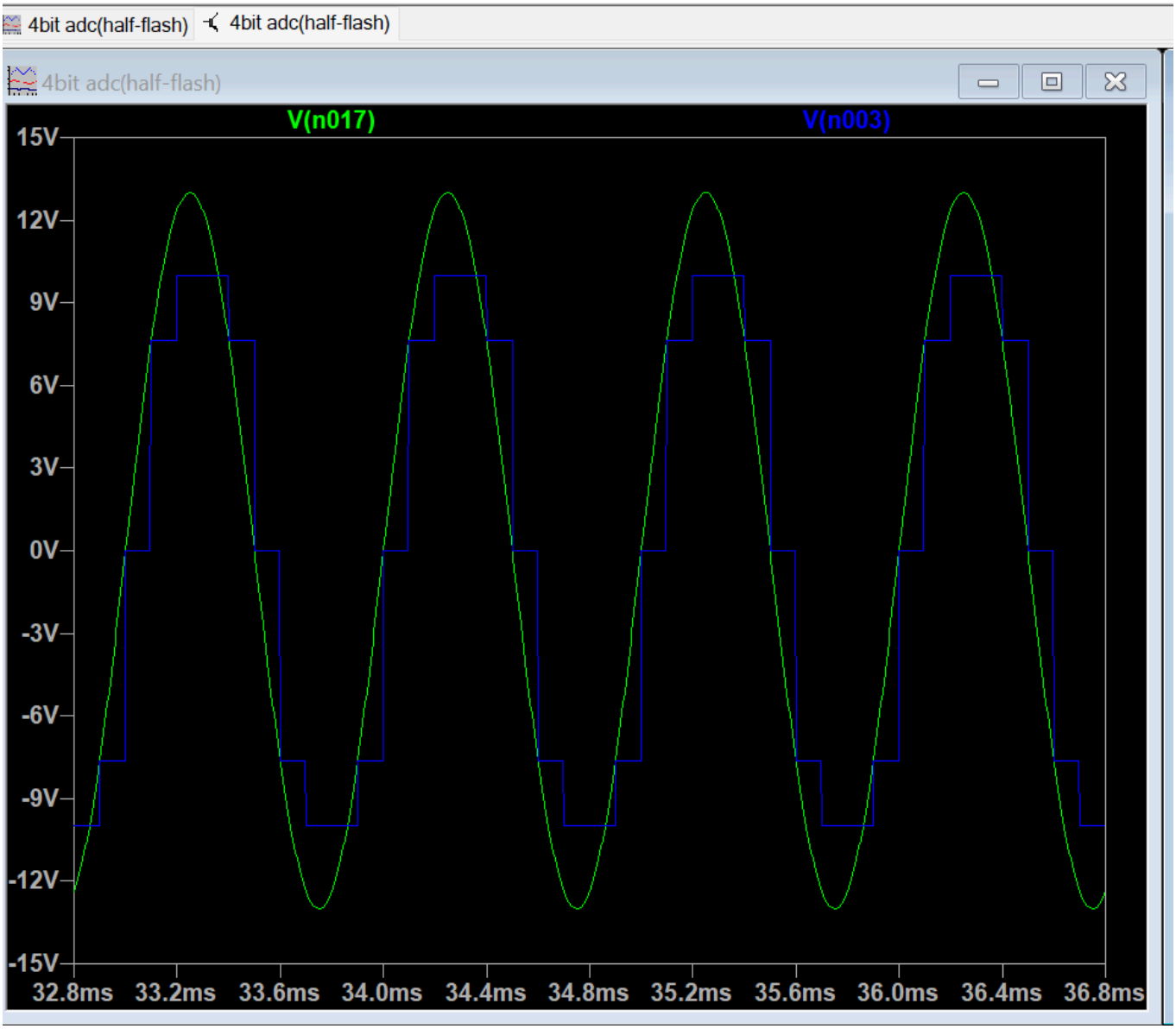
AIM: Construction of half flash ADC, its working and advantages over flash ADC

In this report, we shall analyze how half flash ADC is made and will see working of each component. We are giving an analog input at one of its terminals and then we are trying to count digital output through latches.



The very first part of the circuit contains a sample and hold circuit which internally uses a mosfet for switching technique and whenever this switch is closed, current passes through the capacitor and it gets charged which is also sampling and after getting charged, the capacitor voltage is high and it holds that value because clock is negative for some duration and this cycle continues.

$$let's \quad see \quad the \quad output \quad waveform \quad for \quad a \quad sine \quad wave$$



the green one is input waveform and blue one is the output waveform. we can see that output has been saturated at +/- 10 V because an opamp is ensuring its saturation.

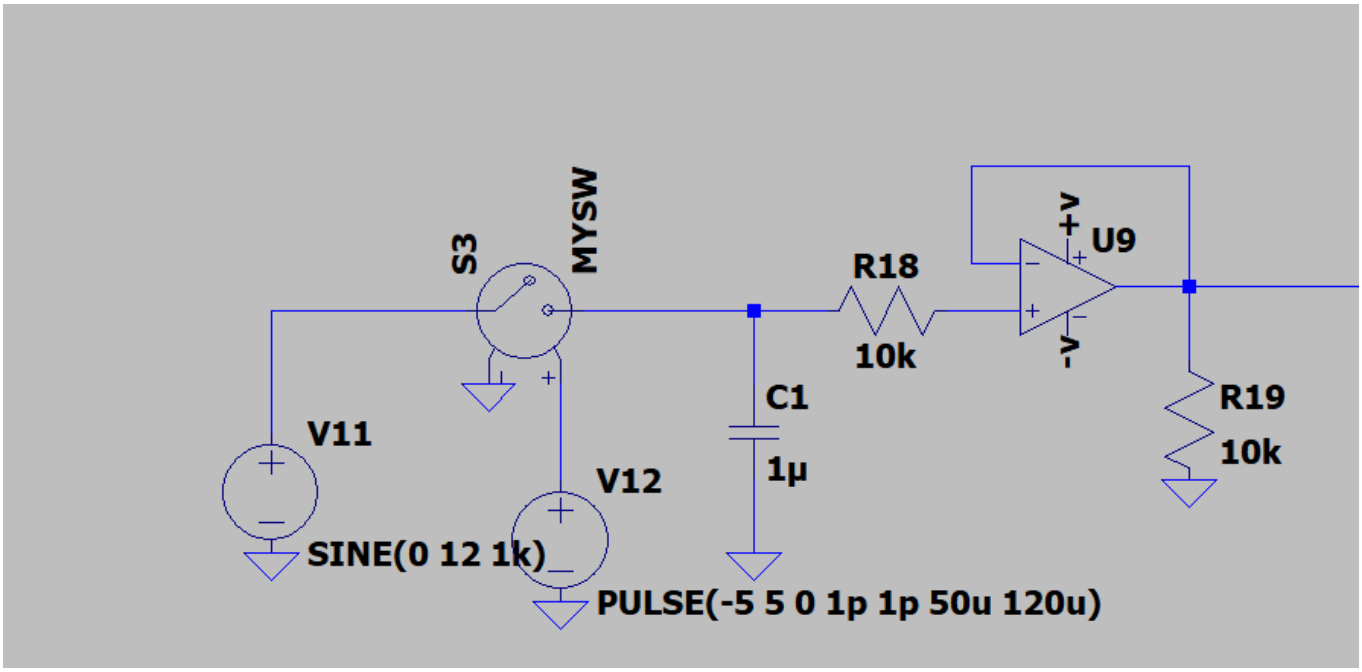
for a D.C. voltage the output waveform and input waveform will look like this:

output and input voltages are same and they are overlapping.

we can overcome this saturation or exceed this saturation to the point where we want to measure by mosfet switching technique or using an ideal switch. I am rectifying here through an ideal switch whose model is:

$$R_{on} = 1, R_{off} = 1Meg, V_t = 0.5, V - h = 0.4$$

the circuit looks like this:



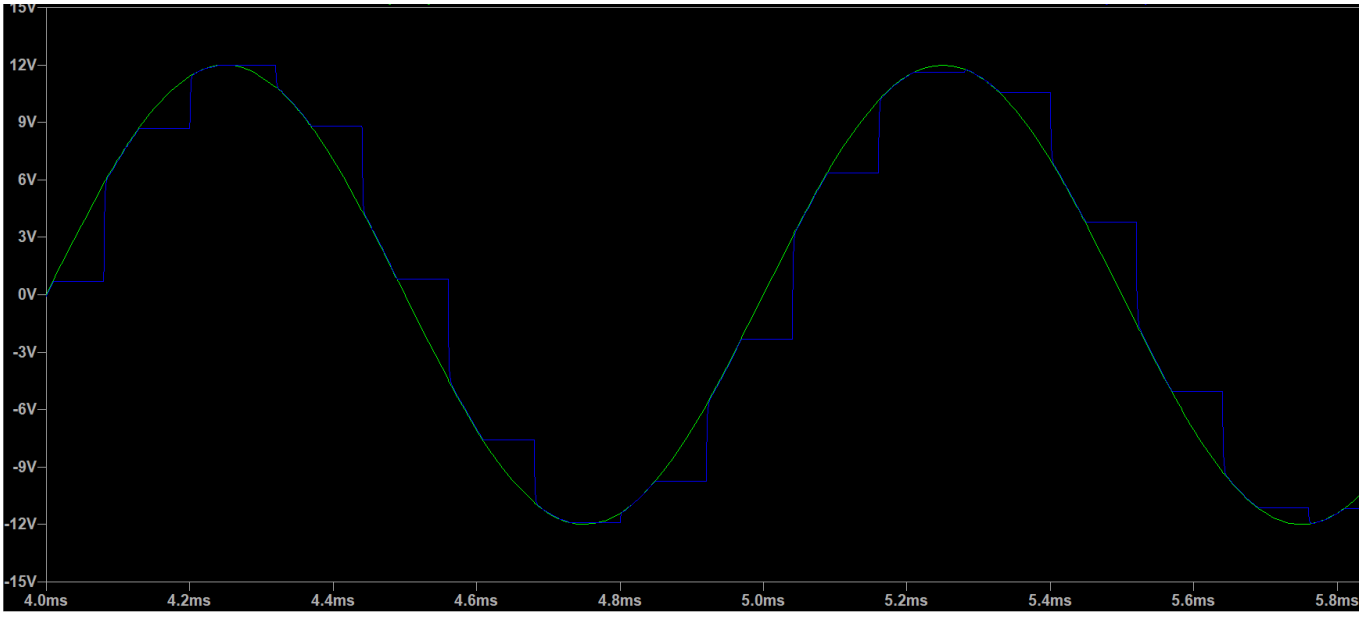
The sampling frequency is kept greater than twice of input frequency to ensure nyquist rate is followed.

$$\omega_s > 2\omega_m$$

One more correction needed in order to simulate the circuit wholly. we shall be doing transient analysis with

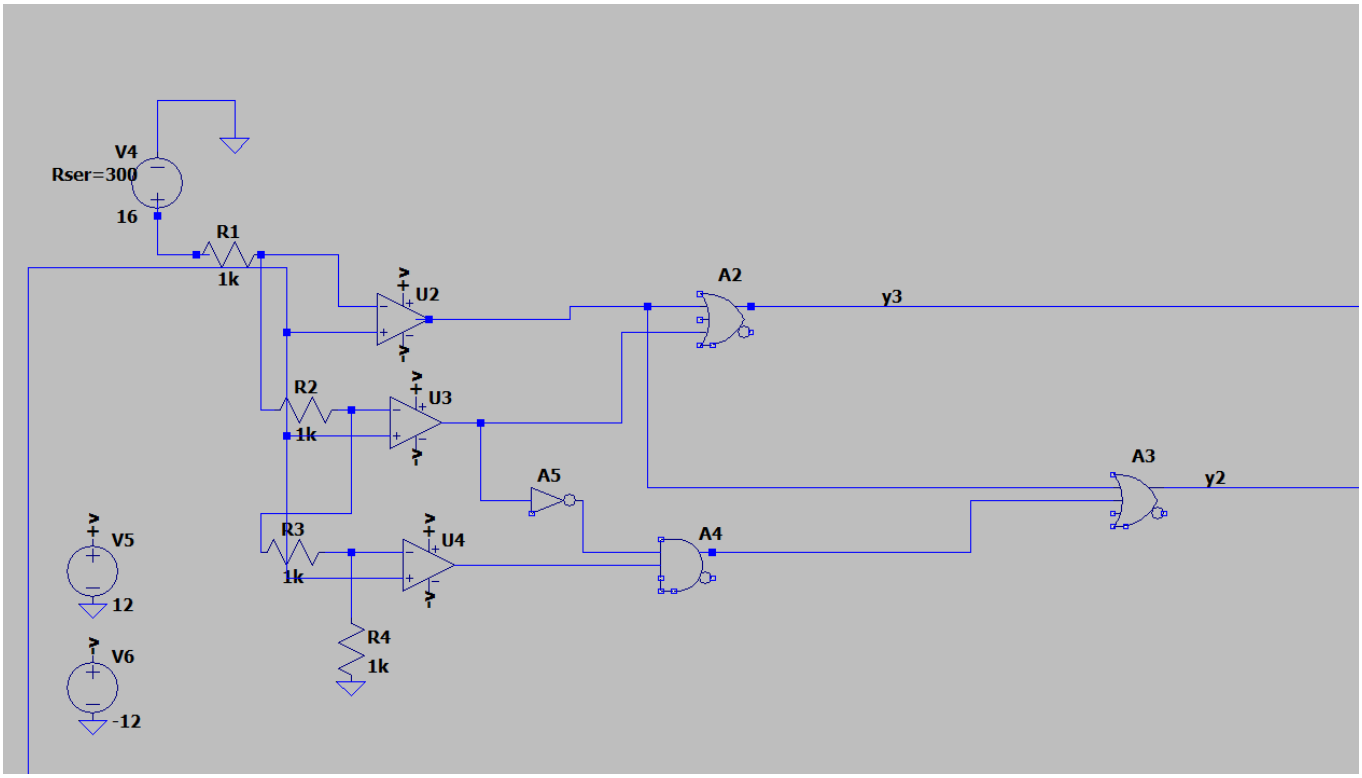
$$timestep = 1us, stoptime = 0.1ms$$

let's now look at the waveform for a sinusodial signal:



The output of the sample and hold circuit is given to ADC and a comparator. let's see what ADC is doing. our ADC at the upper part is responsible for 2 MSBs. This is a flash adc which has 4

resistor each having value equal to 1k which is acting as voltage divider circuit. there are three comparators and each one of them are given two inputs i.e; input voltage and voltage coming after drop at resistor(example; for comparator 1 ,12V for comparator 2, 8V ...).It compares between these two voltages. it saturates at -12v if input voltage is less than voltage at non-inverting terminals and saturates at +12V for the other case.



A series resistance is added with reference voltage so that -ve saturation can be avoided for the input voltages greater than 8v. y3 and y2 are our MSBs. A priority encoder is giving output for two most significant bits whose logic can be observed as following:

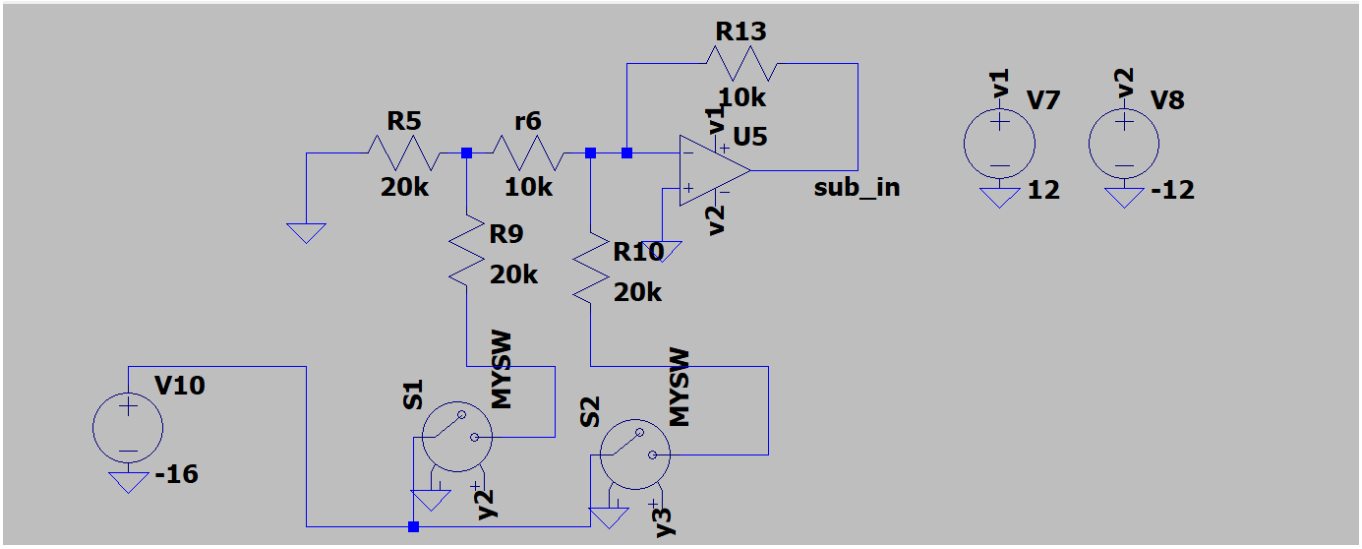
$$y_3 = I_2 + I_3$$

$$y_2 = I_{20}I_1 + I_3$$

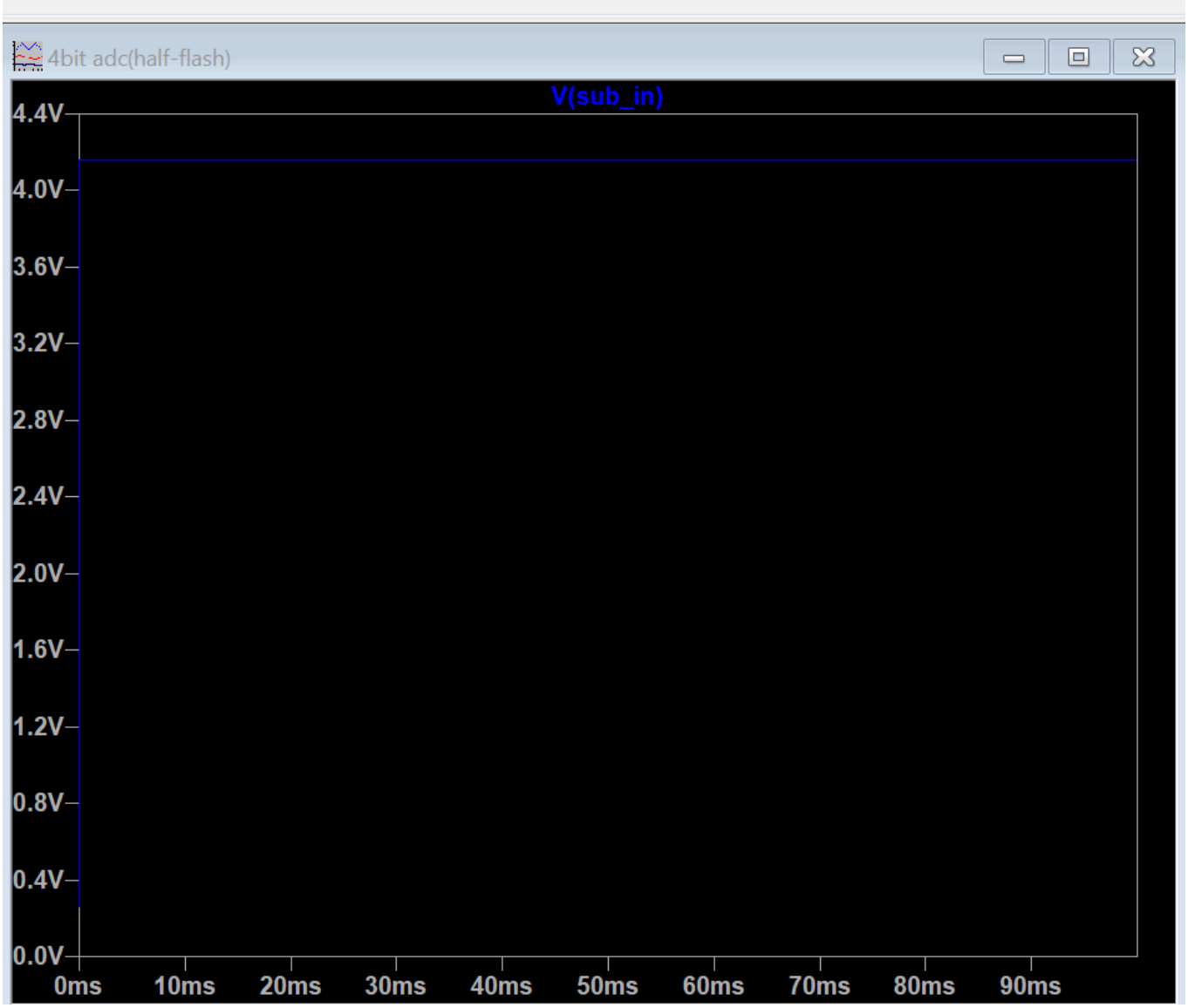
For 7v, y2 should be high and y3 should be low. let's see.

it is clear that y2 is high and y3 which is also d3 is low for input voltage 7v.

Now these inputs are being given to DAC which will convert this signal to analog and this analog voltage will be given to subtractor circuit which will give us a voltage which will be accountable for 2 LSBs. Here, i have used a R-2R ladder DAC .

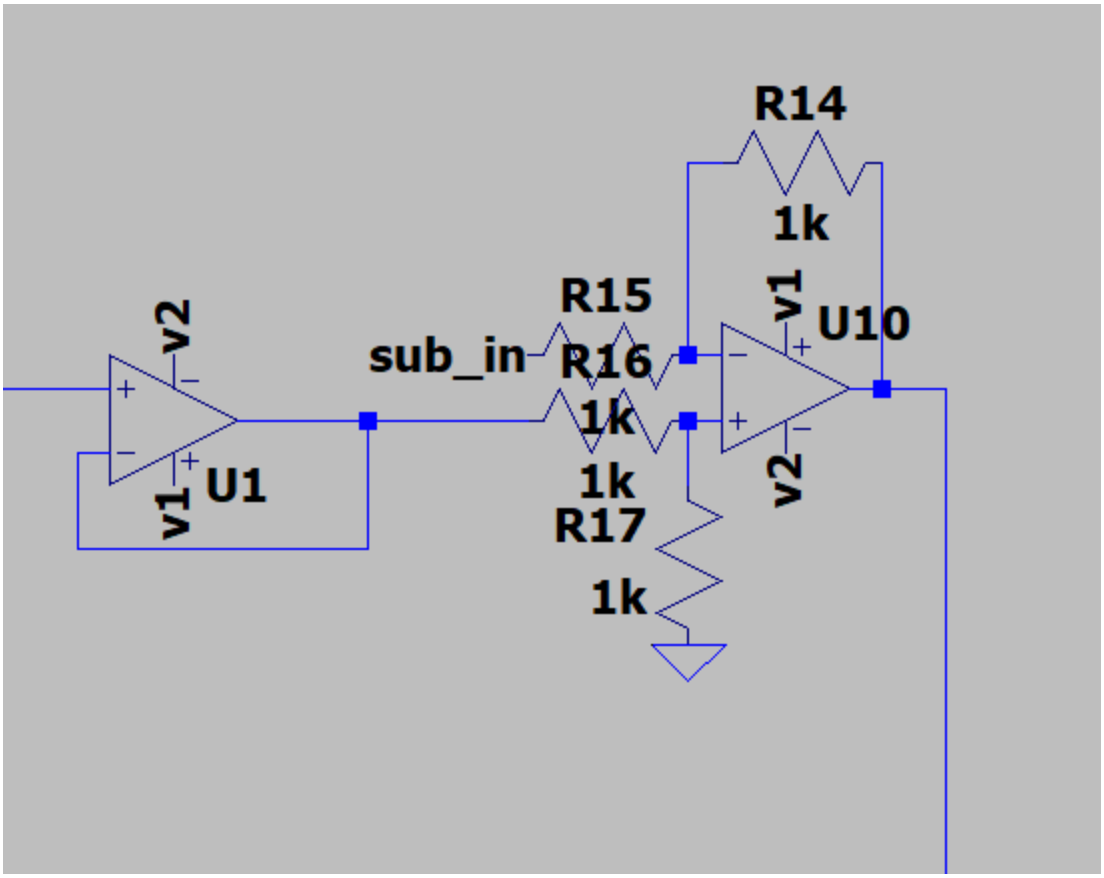


Maintaining the same reference voltage as above ADC we are able to convert the 2 MSBs into desired voltage. In this case DAC output should be +4v. let' see what we are getting.

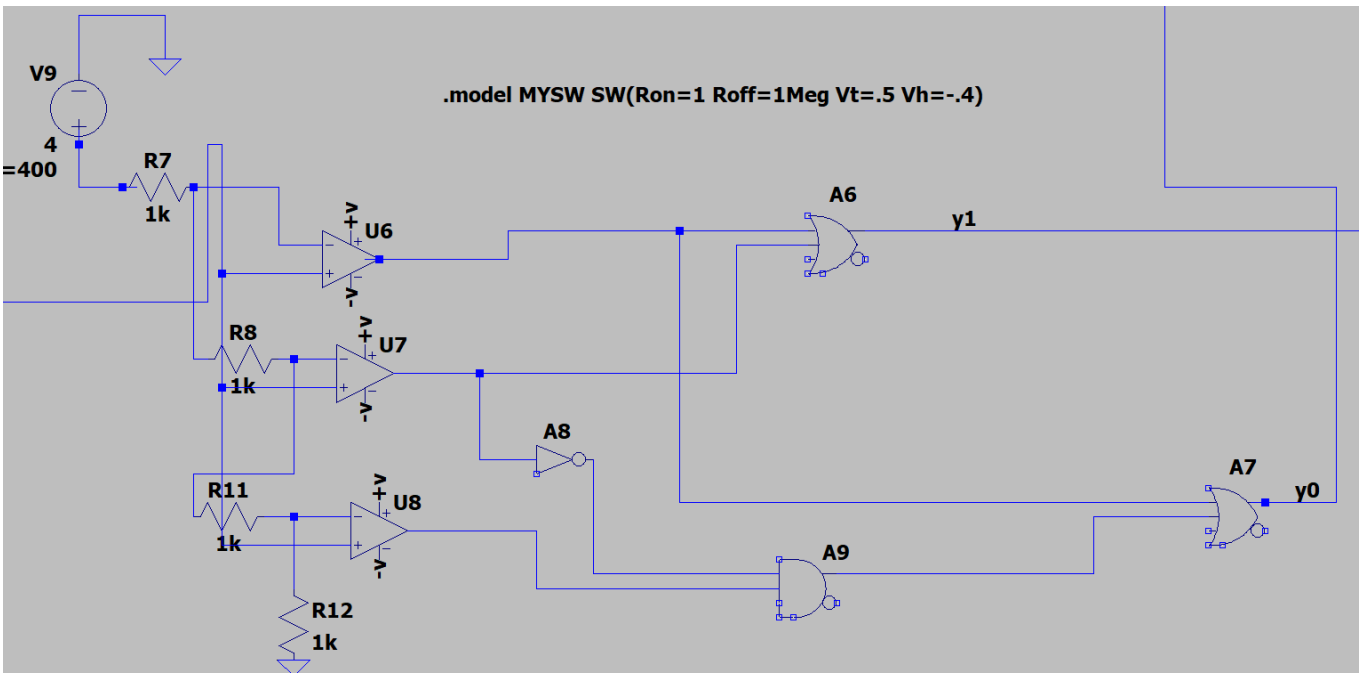


as expected, we are getting an output voltage nearly equal to 4v.

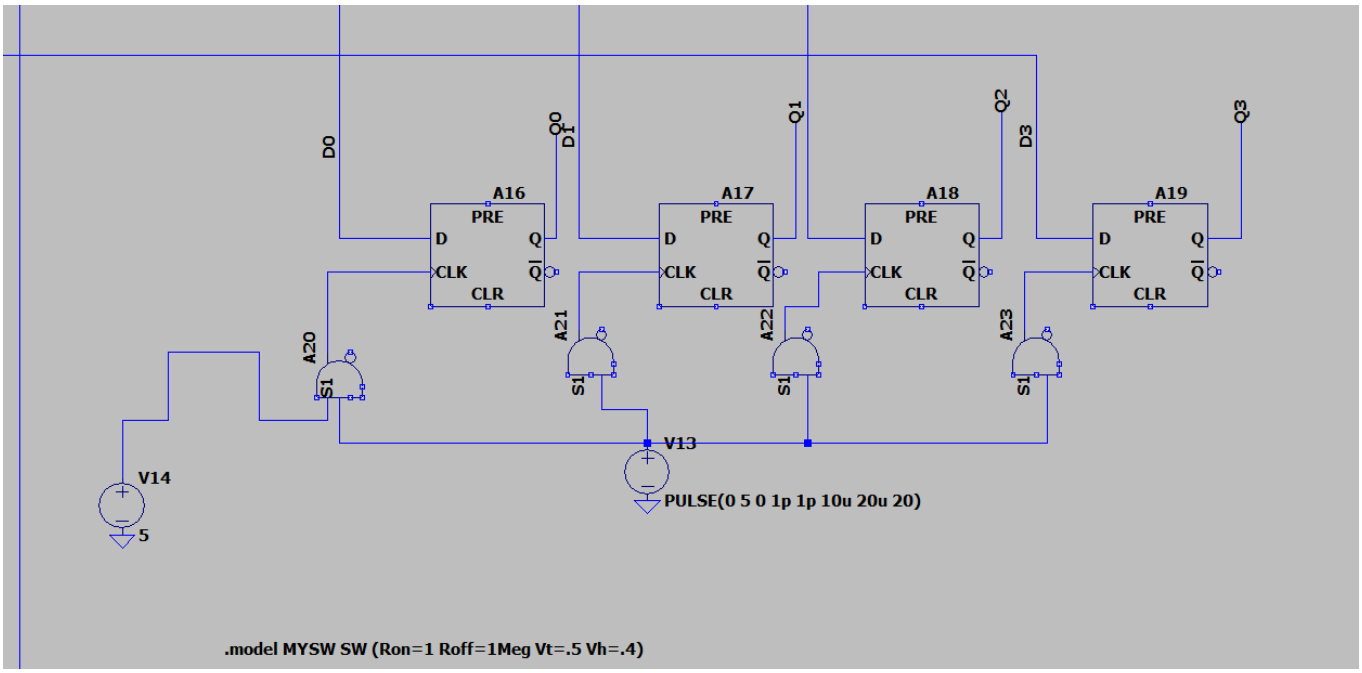
Now, this 4v and input 7v will be given to subtractor circuit which will return an output voltage equal to 3v.



as expected, we are getting a difference nearly equal to 3v. Now this 3v is again given to a 2-bit ADC and we expect that both of output of priority encoder for lower ADC is high.



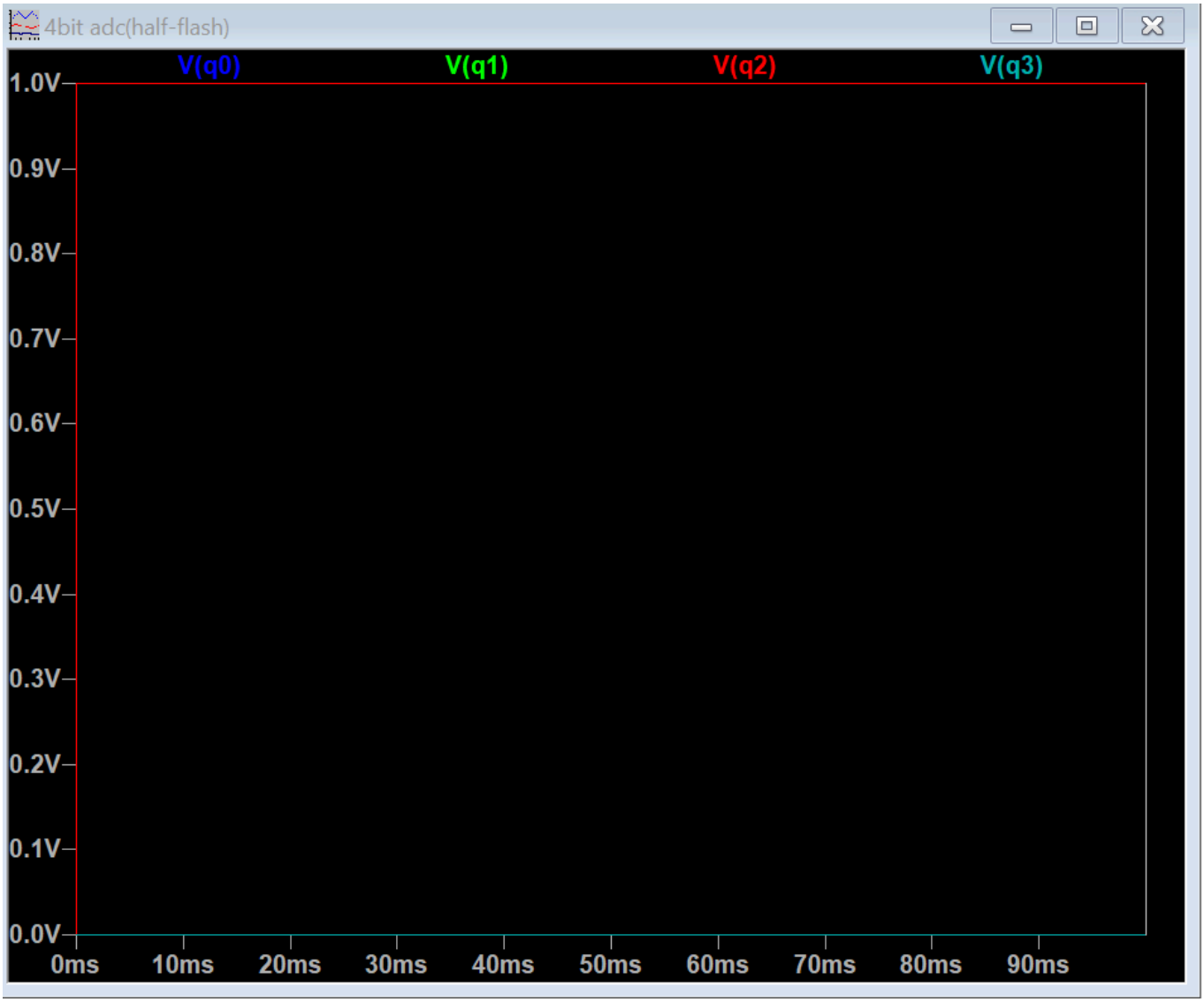
We can see that both of them are high. now, all these y0,y1,y2 and y3 are given to a 4-bit latch which stores the 4 bit output.



this is a synchronous latch made by using four D- flip flop. enable is always high because i don't want it to store the previous output here. we expect the output of this latch should be

$$y_0 = 1, y_1 = 1, y_2 = 1, y_3 = 0$$

let's see we are getting the same or not.



clearly, we are getting the same. hence, this can be used anywhere where we need to use a 4-bit ADC.

ADVANTAGES:

1. half-flash ADC uses less number of comparators than flash ADC which makes it less bulkier.
2. it uses less complex encoder for n-bit ADC.
3. it is almost as fast as flash ADC.
4. while comparing bit resolution both offers the same resolution :

$$2^4 = 16$$

5. it can sample at very high sampling rate.
6. it is commonly used in digital oscilloscopes.