C-33 Jwalamukhi Hostel, IIT Delhi
Hauz Khas, Delhi-110016
Website: shashank-varshney.github.io

SHASHANK VARSHNEY

+91 9458608825
shashankvarshney94@gmail.com

EDUCATION

Master's in technology (VDTT) Expected June 2019
Indian Institute of Technology, Delhi
CGPA: 9.62/10 (Batch topper)

Bachelor of Electronics Engineering 2017
Zakir Husain College of engineering and technology, AMU
CGPA: 9.08/10

COURSES

MOS VLSI Design, Synthesis of digital system, Digital system design lab, Micro Nanoelectronics, Advance digital signal processing, Semiconductor memory design, Neural s/s and learning m/c, Physical design lab, Digital IC design, Analog electronics, Computer Architecture.

PROJECTS

NanoTherm: A Computationally Efficient EDA Tool for Thermal Simulations May 2018-June-2019
- An efficient and accurate analytical solution for architectural thermal simulations and device simulations. The solution simultaneously solves the Fourier and the gray Boltzmann transport equation to accurately predict the thermal profile at both levels.

High speed 1Mb SRAM Jan-May 2018
- Layout and PEX analysis of the memory core, pre-charge circuit and write buffers.

A module of constrained based scheduling with common subexpression elimination technique in C++. Oct-Nov 2017
- Module for LLVM

A fast serial-parallel n-bit multiplier Sep-Nov 2017
- Designed a hardware efficient latch based serial-parallel multiplier for the 130 nm technology node.

RF smart meter: An IOT based smart energy meter for the remote monitoring and control. 2017
- Developed a firmware for the power management and the communication unit of the meter using STM's STMP33 and 6LowPAN APIs.

I2C and SPI memory shield July-Dec 2016
- Developed the memory management firmware for I2C and SPI memory chips for the STM's Nucleo platform.

SmartAgri May-June 2016
- Smart agriculture data acquisition system based on the STMicroelectronics Nucleo platform.
  Web Link: http://www.soilhealthcard.pe.hu

Advance cane system for assisting visually impaired 2015
- An ultra-low cost portable indoor/outdoor smart cane system for visually impaired.
  YouTube link: https://www.youtube.com/watch?v=Z2SqeYoWMk0

EXPERIENCE

Intern, **STMicroelectronics**, Greater Noida, Uttar Pradesh June-July 2016
- Firmware development on the Nucleo platform for the project of IOT based Agriculture.

POSITIONS OF RESPONSIBILITY

Teaching Assistant at NPTEL July-Nov 2018
- Coordinating and providing expert answers on a forum of over 6000+ students
- Setting Assignments for undergraduate students

Joint Co-ordinator (Technical), AMURoboclub 2014-2015
- Assisted coordinators in carrying out technical activities of the club.
- Tasked to guide the 100+ members of the club.

ACCOMPLISHMENTS

- GATE 2017(Electronics): AIR-187, GATE score: 829/1000
- Best paper award "A Novel Advance Cane System for Assisting Visually Impaired". ITPC-2015, Aligarh

PUBLICATIONS

- Varshney, S., Sultan, H., Jain, P., Sarangi, S. R. "NanoTherm: An Analytical Fourier-Boltzmann Framework for Full Chip Thermal Simulations", International Conference on Computer Aided Design (ICCAD-2019), Westminister, USA
- Sultan, H., Varshney, S., Sarangi, S. R. "Is leakage power a linear of temperature?", arXiv:1809.03147 (2018)
- A. Na, W. Isaac, S. Varshney and E. Khan, "An IoT based system for remote monitoring of soil characteristics," *2016 InCITe - The Next Generation IT Summit on the Theme - Internet of Things: Connect your Worlds*, Noida, 2016.
- Abhinandan Jain, Shashank Varshney, "A Novel Advance Cane System for Assisting Visually Impaired", *Workshop on Information Technology –Prospects and Challenges (ITPC-2015)*, Aligarh.

TECHNICAL SKILLS

- Language: C/C++, VHDL, Python, R
- Software: MATLAB, COMSOL, Ansys Icepak, Mathematica, Virtuoso, Innovus, Encounter, Xilinx Vivado, Eagle, PSPICE.

WORKSHOPS/CONFERENCES ATTENDED

- VLSI Design conference 2019, Delhi, India. Jan 2019
- One-day Workshop on Emerging RF technologies: A Design Perspective at Dept. of Electronics Engg, AMU. Feb 2016
- Two days' Workshop on IC Design for Industry: Analog, Mixed-Signal and Memory Chips at Department of Electronics Engineering, AMU, Aligarh February 2016

FIELD OF INTEREST

CAD for VLSI, Application specific RTL design, Embedded systems

REFEREES

Prof. Smruti Ranjan Sarangi	Mr. Raunaque Quaiser
Dept. of Computer Science and Eng.	Senior manager
IIT Delhi	STMicroelectronics Pvt Ltd, Noida, UP