

Course: EE787 – Memory Design and Testing  
Department of Electrical Engineering  
Indian Institute of Technology, Delhi

Major Test, Winter Semester, Session 2012-2013

Date: 10<sup>th</sup> May, 2013

Max Marks: 40

*All 4 questions are to be answered* Time allowed: 90 mins.

- 1) Following questions are to be answered in brief, preferably in point form. Verbose answers will possibly attract penalty.
- What are the main differences between the following two possibilities of embedded DRAM on a logic chip:
    - Case 1: Use a trench capable process. (3)
    - Case 2: Use a regular process with poly-caps as storage capacitors.
  - You have two memories:
    - Memory A is a DDR SDRAM with 32 bit data bus, an access pattern of 5-1-1-1 (block select – row decode – column decode – burst cycle, burst length restricted to a total of four word accesses), running at a bus frequency of 100 MHz.
    - Memory B is a single port SRAM with 32 bit data bus running at 100MHz.
    - What is the maximum data access bandwidth of memory A and B?
    - What access bandwidth do memory A and B provide when you read/write data in blocks of 4 Bytes at a time? <sup>Word</sup> (3)
  - What is the maximum memory access bandwidth of a 64bit wide, 200MHz DDR SDRAM with the following access latencies: 3-2-2.5-0.5 (block select – row decode – column decode – burst cycle)? What is the typical memory access bandwidth when a new random address is periodically applied after 4 words read? (3)
  - Which RAM-type do you select for
    - a network processor with 4GByte of memory?
    - a single-chip search engine with a table size of 1024x1024 bit, access freq. of 300MHz required? (3)
  - Fig. 1 shows a wordline driver design. State why you think this design is not acceptable? (3)

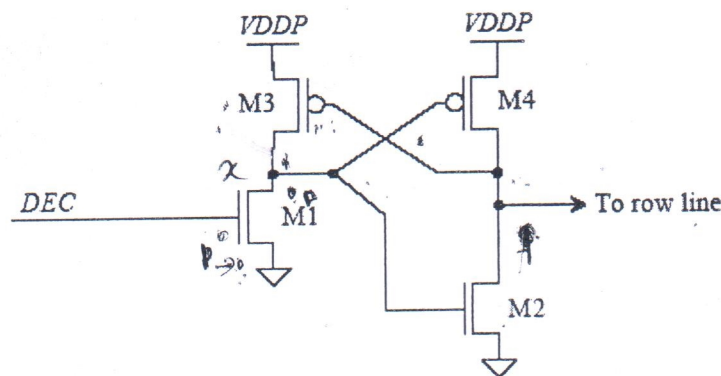


Figure 1

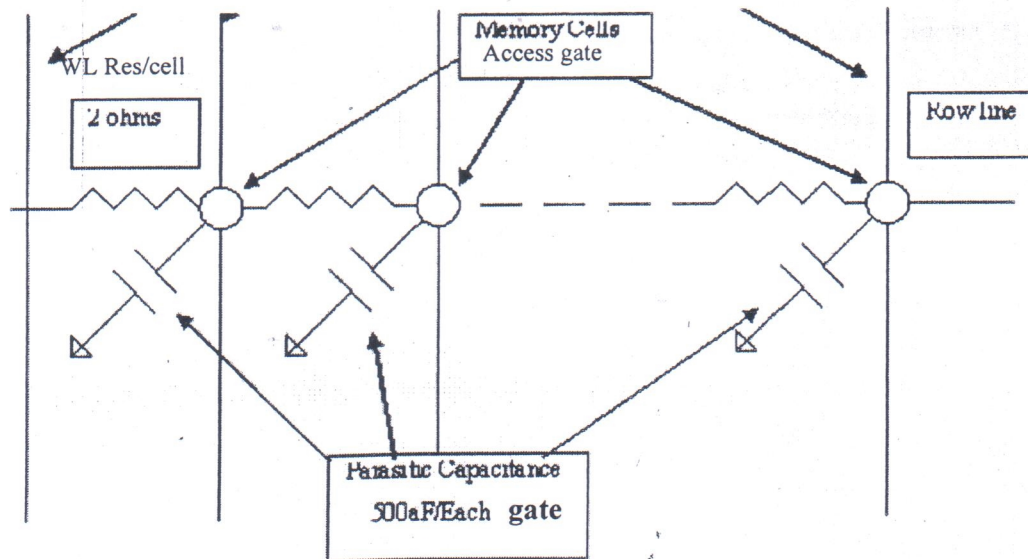


Figure 2

- 2) For a static ram subarray block of 1024 rows x 512 columns, the wordline parasitic model is shown above in fig.2.
  - a. Find the Elmore delay considering the wordline as a distributed RC line. (2)
  - b. Find the RC delay considering a lumped model. (1)
  - c. Comment briefly on the reason for the difference between the two results. Which of the two values is would you use for a practical design and why? (2)
  
- 3) Consider a DRAM with 2Mb storage and data I/O DQ x2. The array is configured as 8 blocks of 256Kb each. (1024 rows, 512 columns, folded bitline)
  - a. How many I/O lines are needed the array? (1)
  - b. How big is a page of data? (Recall the definition of a page from NAND flash context) (1)
  - c. Sketch a decoding scheme. Show only the block schematic with bus widths etc. (2)
  - d. Assume 3 bits is globally decoded and others are locally decoded. How many these bit needed to be routed to each array? (1)
  - e. Draw the floorplan of the array and show the routing of the address, data and key control signals. (3)
  - f. Draw the gate level schematic of the block address decoder. (2)

Handwritten calculations and diagrams:

$$2 \text{ Mb} = 2 \times 10^6 \text{ bytes}$$

$$256 \text{ Kb} = 256 \times 10^3 \text{ bytes}$$

$$256 \text{ Kb} = 256 \times 10^3 \times 8 \text{ bits}$$

$$256 \text{ Kb} = 2048 \text{ Kbits}$$

$$2048 \text{ Kbits} = 2048 \times 1024 \text{ bits}$$

$$2048 \times 1024 = 2109824 \text{ bits}$$

$$2109824 \text{ bits} = 263728 \text{ bytes}$$

$$263728 \text{ bytes} = 263728 \times 8 \text{ bits}$$

$$263728 \times 8 = 2109824 \text{ bits}$$

Diagram showing a grid of memory cells with address lines  $\bar{a} \bar{b} \bar{c}$  and data lines  $a b c$ .