Course: EE787 – Memory Design and Testing
Department of Electrical Engineering
Indian Institute of Technology, Delhi

Major Test, Winter Semester, Session 2010-2011
Date: 7th May, 2011

Max Marks: 40

All 4 questions are to be answered **Time allowed: 90 mins.**

1) Following questions are to be answered in brief, preferably in point form. Verbose answers will possibly attract penalty.
   a. Why are sense amplifiers located between memory array and column decoder but not between row decoder and memory array? (2)
   b. What are the main differences between the following two possibilities of embedded DRAM on a logic chip:
      i. Case 1: Use a trench capable process. (2)
      ii. Case 2: Use a regular process with poly-caps as storage capacitors.
   c. Imagine the part of a cache controller that is responsible for transferring data from the main DRAM to a local SRAM cache line. The cache line width is a multiple of the memory bus width. Which property of SDRAMs (SDR or DDR) helps in this situation and why? (2)
   d. What is the maximum memory access bandwidth of a 64bit wide, 200MHz DDR SDRAM with the following access latencies:(3-2-2.5-0.5)(block select – row decode – column decode – burst cycle)? What is the typical memory access bandwidth when a new random address is periodically applied after 4 words read? (2)
   e. Which RAM-type do you select for
      i. a network processor with 4GByte of memory
      ii. a single-chip search engine with a table size of 1024x1024 bit, access freq. of 300MHz required? (2)

2) Consider a DRAM with 2Mb storage and data I/O DQ x2. The array is configured as 8 blocks of 256Kb each. (1024 rows, 512 columns, folded bitline)
   a. How many I/O lines are needed the array? (1)
   b. How big is a page of data? (Recall the definition of a page from NAND flash context) (1)
   c. Sketch a decoding scheme. Show only the block schematic with bus widths etc. (2)
   d. Assume 3 bits is globally decoded and others are locally decoded. How many these bit needed to be routed to each array? (1)
   e. Draw the floorplan of the array and show the routing of the address, data and key control signals. (3)
   f. Draw the gate level schematic of the block address decoder. (2)

3) Consider the folded-area DRAM core architecture in figure 1.
   a. What problems do you foresee in the sensing scheme? Would the problem the mitigated if we put many sense enable transistors instead of one (3)
   b. Provide the gate level design of the column decoder (4)
   c. Outline any problems you see in the signal levels on the I/O and I/O complement lines. Provide a solution to the problem (3)