A New Lateral PNM Schottky Collector Bipolar Transistor (SCBT) on SOI for Nonsaturating VLSI Logic Design

M. Jagadesh Kumar and D. Venkatesh Rao

***Abstract*—The novel characteristics of a new lateral PNM Schottky collector bipolar transistor (SCBT) on silicon-on-insulator (SOI) are explored using two-dimensional (2-D) simulation. The collector-base junction of the proposed lateral PNM transistor consists of a Schottky junction between n-base (N) and metal (M). The characteristics of this structure are compared with that of lateral PNP transistors on SOI. We demonstrate that the proposed structure has a superior performance in terms of reduced collector resistance, high current gain, negligible base widening, and very low reverse recovery time compared to the compatible lateral PNP transistors. A simple fabrication procedure is also suggested providing the incentive for experimental verification.**

***Index Terms*—Bipolar transistor, lateral PNM, numerical simulation, Schottky collector, silicon-on-insulator (SOI).**

I. Introduction

Because of their well controllable characteristics, the bipolar transistors exhibit significant advantages over those of CMOS transistors in various critical applications such as bandgap voltage references, accurate current mirrors, variable gain amplifiers and other high speed analog and mixed signal circuit designs [1]. This advantage of the BJT coupled with the inherent isolation available for the SOI devices led to the emergence of SOI based BiCMOS technologies where both BJTs and MOSFETs are fabricated on the same chip. However, to reduce the complexity of BiCMOS processes, which employ expensive double polysilicon complementary technologies, and also to minimize the disadvantages associated with the conventional vertical current concept [2], lateral bipolar transistors are being studied extensively [3]–[8].

In many BiCMOS applications such as the push-pull amplifiers, a PNP transistor with performance identical to that of an NPN transistor is frequently required. But, due to the low hole mobility, PNP transistors are known for their poor speed and high collector resistance. However, it has been shown experimentally that if a metal is used for the collector, not only is the collector resistance less but also are the majority carriers collected more efficiently without the back injection of the minority carriers from the Schottky collector junction [9]. This is highly useful because it permits the design of high performance nonsaturating inverter logic circuits. Such Schottky collector junction transistors, based on vertical current concept, have been demonstrated earlier for VLSI applications [10]. However, a fascinating question which so far has not received any critical attention is the study of lateral PNM Schottky collector bipolar transistors on SOI. To the best of our knowledge such an investigation has not been reported in literature.

The objective of this work is therefore to present for the first time the design and characteristics of a lateral PNM Schottky collector bipolar transistor (SCBT) on SOI using two dimensional simulation. We demonstrate that the proposed lateral PNM SCBT is superior in performance compared to an equivalent lateral PNP BJT on SOI in terms of high current gain, high switching speed and the ability to operate at high collector current densities with suppressed base widening. We have also proposed a simple method of fabricating this lateral PNM SCBT on SOI.

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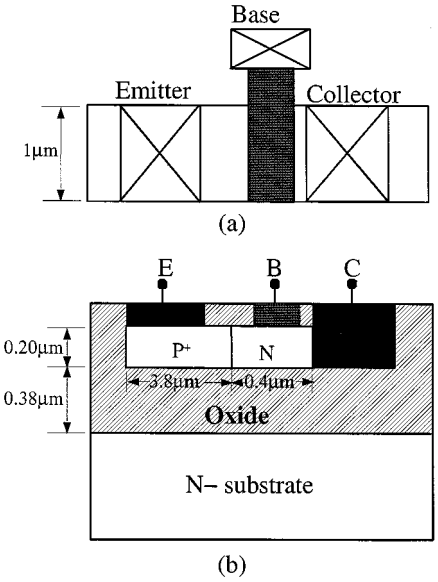

Fig. 1. Top layout and schematic cross-section of the SCBT structure.

II. Device Structure and Parameters

The top layout and the schematic cross-section of the lateral PNM SCBT is shown in Fig. 1, as implemented in the two-dimensional (2-D) device simulator ATLAS [11]. The epitaxial silicon film thickness is chosen to be 0.2 μm and the buried oxide thickness is 1 μm. The emitter is a p^+-region doped at $5 \times 10^{19}/\text{cm}^3$, the metallurgical n-base width is 0.4 μm and is doped at $5 \times 10^{17}/\text{cm}^3$. These parameters are the same as those used in the lateral NPN experimental structure of [6]. The collector region of the SCBT structure is chosen to be platinum silicide due to its pertinent barrier height of 0.85 eV, high conductivity, and process selectivity [9]. The lateral PNP transistor with which we have compared our results is also an SOI structure and has precisely the same parameters as that of SCBT except that the collector is p-type silicon with a doping of $5 \times 10^{17}/\text{cm}^3$ so that both the transistors have approximately identical collector breakdown voltage.

III. SCBT Fabrication Process

Fig. 2 shows the fabrication sequence for the proposed lateral PNM SCBT [2], [6]. After mesa isolation by epi-etching, a thick CVD oxide (LTO) is deposited and patterned as shown in Fig. 2(a). A CVD nitride film is deposited [Fig. 2(b)] and an unmasked RIE etch is performed to retain a silicon nitride spacer at the edge of the CVD oxide [Fig. 2(c)] [6]. The lateral p^+ emitter is next formed by implanting boron at wafer tilt angle of 15°. The implantation energy is 30 KeV at a dose of 7×10^{14} cm^{-2}. If proper tilt angle is not chosen, the p^+ emitter will be too close to the n^+-poly base contact resulting in a tunneling current between emitter and base. We have arrived at the above tilt angle based on our implantation simulations using the process simulator ATHENA [12]. Following the p^+ emitter formation, a thick CVD oxide is deposited [Fig. 2(d)] and planarized by CMP process as shown in Fig. 2(e). After etching the nitride film, an n^+-polysilicon film is deposited and the wafer is again planarized using CMP leaving n^+-poly in the place where the nitride film was present [Fig. 2(f)]. Using a mask, the field oxide and the silicon are etched in the window as shown in Fig. 2(g). Similarly, a contact window [Fig. 2(h)] is now opened on top of the p^+ emitter using a mask. Following this, platinum silicide is deposited and patterned to form the Schottky collector contact and

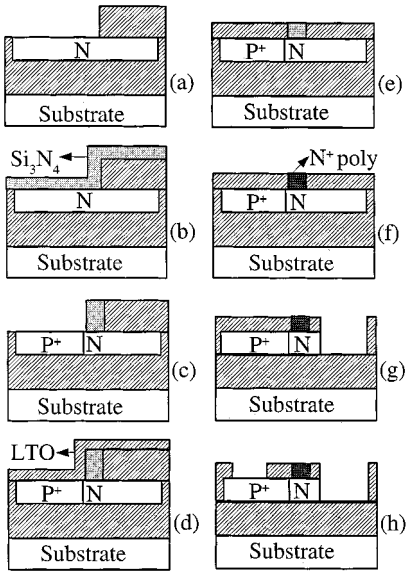

Fig. 2. Process steps for the SCBT structure.

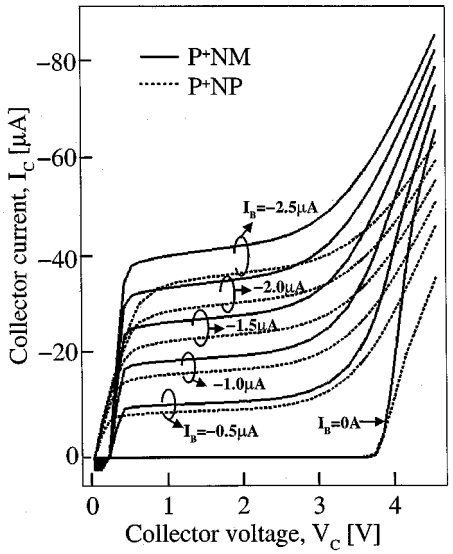

Fig. 3. Simulated I–V characteristics of lateral SCBT and lateral PNP structures.

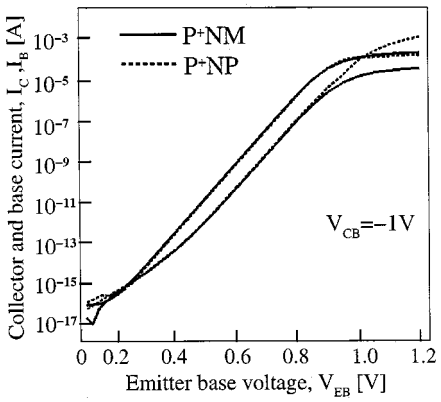

Fig. 4. Gummel plots of lateral SCBT and lateral PNP structures.

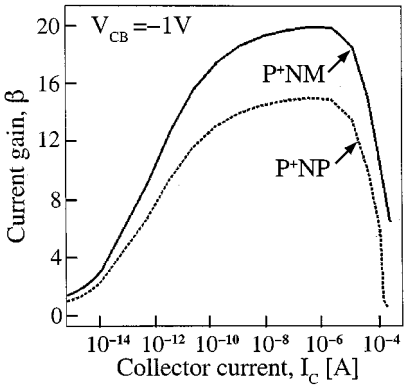

Fig. 5. Beta versus collector current of lateral SCBT and lateral PNP structures.

the emitter and the base ohmic contacts. The final structure is as shown in Fig. 1. It may be pointed out here that the base-collector junction in the above process is not self-aligned to the base contact. Therefore, the base width is defined by the collector window etching and thus it depends on mask alignment tolerance. This conceptual problem has to be overcome in order to obtain a more viable fabrication procedure.

IV. Performance of Lateral SCBT Structure

In our simulations using ATLAS [11], we have used suitable models for the bandgap narrowing, SRH and Auger recombination and the concentration and field dependent mobility. Breakdown voltage is calculated including nonlocal impact ionization [13]. For simulating the Schottky junction properties, standard thermionic emission model is used including the image force barrier lowering effects [14]. The simulated current–voltage (I–V) characteristics of the lateral SCBT and lateral PNP transistor are shown in Fig. 3. As can be seen, the current-voltage characteristics of the SCBT structure are superior to those of the PNP transistor in terms of reduced collector resistance. The $V_{\rm CE}$ off-set voltage ($\approx$ 0.2 V) is typical of any Schottky collector transistor [9] and should be taken into account while designing the digital logic circuits.

The Gummel plot shown in Fig. 4 indicates that the base current in the SCBT device is smaller than that of the PNP transistor. This is because in the case of PNM transistor, when the base-collector (n-M) junction is reverse biased, there is a finite electron current $I_{\rm nM}$ caused by the electron flow from metal into the n-base [15]. Since the electron current from emitter to base is fixed by the emitter-base forward voltage, the electron current $I_{\rm nM}$ from metal to n-base flows into the base terminal [16] reducing the total base current. As a result, the current gain of the SCBT is larger than that of the PNP transistor, as shown in Fig. 5. We further note from Fig. 4 that for $V_{\rm EB} > 0.8$ V, there is a substantial increase in the base current of the PNP transistor due to the base widening into the collector. To maintain charge-neutrality in the widened base region, the base terminal is forced to supply additional electrons, increasing the base current. However, in the case SCBT, there is no such increase in base current even at a high collector current. This is a clear indication of the suppressed base widening in the case of SCBT. This can further be confirmed from Fig. 6 in which the cut-off frequency f_T is plotted as a function of the collector current. At $I_C = 10^{-4}$ A, the f_T of the SCBT is 2 GHz while the comparable lateral PNP transistor has a negligible cut-off frequency at this current. In spite of a large collector doping used in the lateral PNP transistor, it is clear that base widening due to Kirk effect [13] limits its high-frequency performance, while the lateral SCBT does not suffer from this shortcoming because of the metal collector. The presence of the Schottky collector also has the added advantage that the SCBT will

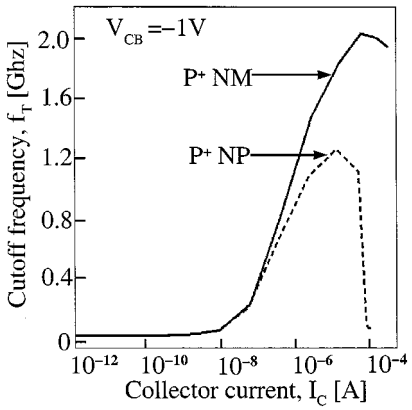

Fig. 6. Cutoff frequency versus collector current of lateral SCBT and lateral PNP structures.

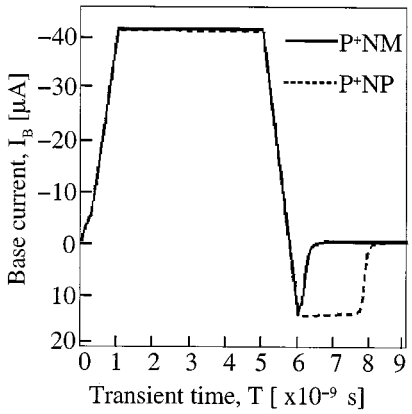

Fig. 7. Switching performance of lateral SCBT and lateral PNP structures.

not suffer from storage charge effects when the transistor is in saturation. This is clearly evident from Fig. 7 in which the reverse recovery characteristics of SCBT are compared to that of the PNP transistor. The lateral SCBT has zero storage time permitting its application in the design of nonsaturating inverter logic with significantly fast response.

V. Conclusions

The concept of the lateral SCBT structure on SOI has been successfully demonstrated using 2-D simulation. The proposed SCBT is shown to be superior to that of the conventional lateral PNP transistor on SOI in terms of improved current gain, reduced collector resistance, suppressed base widening, and fast switching response. A simple fabrication procedure is also discussed. If this structure is implemented in the design of bipolar logic circuits, a significant performance leverage can be expected.

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On the Applicability of Nonself-Consistent Monte Carlo Device Simulations

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***Abstract*—Recently, nonself-consistent (with respect to the electric field) Monte Carlo (NSC-MC) simulations have been proposed for the estimation of the noise and expected value of stationary terminal currents without examining the accuracy of the NSC approximation for these kinds of simulations. Comparison with self-consistent (SC) simulations reveals that NSC simulations of quantities like the drain current of a MOSFET or collector current of a BJT tend to reproduce the results of the momentum-based model used to calculate the electric field without improving the accuracy. In case of terminal current noise it is found that under nonequilibrium conditions the NSC results can substantially overestimate the SC results.**

***Index Terms*—Device simulation, Monte Carlo method, silicon.**

I. Introduction

Many hot-carrier phenomena can be described adequately only by self-consistent (SC) Monte Carlo (MC) device simulation [1], [2]. Unfortunately, this method is very CPU intensive and approximations have been developed like the nonself-consistent (NSC) MC method for the steady-state where the electric field is calculated by a momentum-based

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