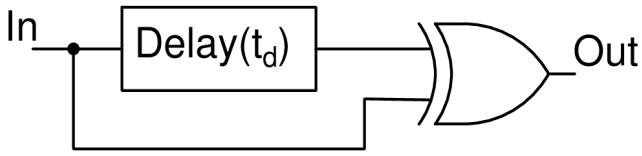
IEC LAB 1

ASSIGNMENT-1

Deadline : 27th September 2017

An address transition detection(ATD) circuit is used in asynchronous memories for producing a pulse by detecting a transition at any of its address lines . This pulse acts as clock signal for subsequent circuitry.

A typical ATD circuit is shown below:



Use V_{DD}=1.2V, UMC 130nm SP 1.2V transistors.

(Library Path:/tools/public/asiclib/umcoa/L130/process/umc130/umc13mmrf)

* Make an XOR gate using standard CMOS logic with a maximum delay of 50ps in the tt corner at 27^{o} C. A delay lower than this would also be fine.
* Make a delay element of 150ps(+- 10%) for ATD in tt. Run a parametric analysis on the sizes to obtain the appropriate delay. Choose appropriate sweep limits based on Elmore Delay calculations.
* Make ATD circuit using the delay made earlier and calculate the pulse width. Perform corner analysis and tabulate the value of pulse width in following format.

Process Corner	-40^{o}C	27^{o}C	85^{o}C
tt			
ss			
ff			

Bonus Question : Can you acheive nanoseconds of delay using this circuit? If not, could you suggest any other circuit to do so?