Thin-Film Bipolar Transistors on Recrystallized Polycrystalline Silicon Without Impurity Doped Junctions: Proposal and Investigation

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***Abstract*—A lateral polysilicon Bipolar Charge Plasma Transistor (poly-Si BCPT) on undoped recrystallized polycrystalline silicon which is compatible with the thin-film field effect transistor (TFT) fabrication is reported in this paper. Using calibrated two-dimensional device simulation, the electrical performance of the poly-Si BCPT is evaluated in detail by considering the position of the single grain boundary. Our simulation results demonstrate that the poly-Si BCPT has the potential to realize low-cost thin-film polycrystalline silicon bipolar transistors with large current gain and cut-off frequency making it suitable for a number of applications including the driver circuits of the displays.**

***Index Terms*—Bipolar charge plasma transistor (BCPT), bipolar transistor, current gain, glass substrates, poly-Si, simulation, thin-film transistors (TFTs).**

I. Introduction

LOW temperature polycrystalline silicon (Poly-Si) thin-film transistors (TFTs) on insulating substrates such as glass and plastics, even at sub-100 nm channel lengths, are aggressively investigated in the literature [1]–[9]. The use of low thermal budget ($<$ 600 ° C), and less expensive substrate materials such as plastic and glass makes TFTs a low-cost choice for a wide range of applications such as active matrix liquid crystal displays (AMLCDs) [1], and memory devices [2]. With the possibility of monolithic integration of CMOS drivers and other peripheral circuit elements, poly-Si TFTs have paved the way for system on-panel device integration [4]. Fabrication of the drivers directly on glass substrates eliminates the additional driver attachment and packaging steps and in turn significantly brings down the overall cost. More recently, poly-Si TFTs have also been suggested as promising devices for RF modules in system-on-panel applications [5], [6] and 3D IC designs [7]. Although poly-Si exhibits a large field-effect mobility in both n- and p-channel devices compared to that of the amorphous silicon (a-Si), significant improvements are required in the thin-film transistor performance for increasing the level of integration of peripheral functions in the active matrix displays [10]. TFT performance is still limited when compared to the operational speed and the current driving capability of the bipolar transistors. The use of poly-Si as the device material for poly-Si TFTs has dominated so far. However, the lateral poly-Si bipolar transistors on insulating substrates can extend the scope of thin film devices beyond AMLCDs. In the past, there have been very few poly-Si bipolar transistor studies (often with poor current gain) [11]–[13]. The primary reason why BJTs on polycrystalline silicon have not become attractive is because of their low current gain and the high thermal budgets ($\sim 1000°\mathrm{C}$) required for the post ion-implantation annealing of the highly doped emitter and the base regions of the bipolar transistors. However, the upper limit of the thermal budget of the TFTs on glass substrates is limited to 600 ° C with solid phase crystallization of the polycrystalline silicon [14], [15]. To overcome the above problems, in this paper, we demonstrate the possibility of making bipolar transistors on intrinsic recrystallized polycrystalline thin-film silicon without the need for impurity diffusion. Using two-dimensional simulations, similar to that of Walker's approach [16]–[23] for TFTs, we demonstrate the possibility of realizing a polysilicon Bipolar Charge Plasma Transistor (poly-Si BCPT). The proposed device could be suitable for different applications such as the driver circuits of the displays. In the poly-Si BCPT, which is compatible with the poly-Si TFT fabrication steps, neither ion-implantation nor the diffusion of impurity dopants into the poly-Si is required to form the emitter, base and the collector regions. Rather, metal electrodes with different work functions ($\varnothing_{m,E}, \varnothing_{m,C} < \varnothing_{\mathrm{Si}}$ and $\varnothing_{m,B} > \varnothing_{\mathrm{Si}}$) [24]–[28] are employed to create the n-type emitter and the collector regions by inducing electron plasma into the undoped poly-Si and hole plasma to form the p-type base region. No complicated thermal budgets are, therefore, required for: 1) the electrical activation of the implanted impurity atoms and 2) to repair the damage caused by the bombardment of high energy impurity atoms into the poly-Si.

II. Device Structure and Parameters

The cross-sectional view of the poly-Si BCPT is shown in Fig. 1. In the poly-Si BCPT, the emitter region is created by employing Hafnium (work function $\varphi_{m,E} = 3.9$ eV) as the emitter electrode metal to induce the electron plasma in the undoped poly-Si film. Holes are induced to create the base region by using Platinum (work function $\varphi_{m,B} = 5.65$ eV) as the base electrode. Since we need a lower electron concentration in the collector region compared to what is required in the emitter region of the transistor, Aluminum (work function $\varphi_{m,C} = 4.28$ eV) is used as the collector electrode. To make sure that the induced carrier concentration at the top and the

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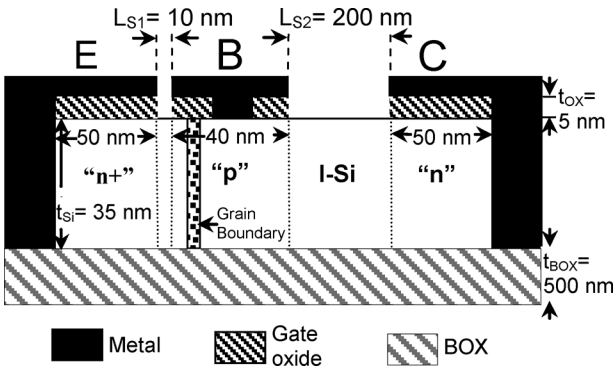


Fig. 1. Schematic cross-sectional view of the poly-Si BCPT.

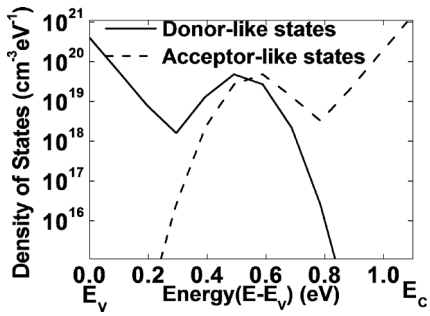


Fig. 2. Distribution of donor/acceptor-like trap states across the forbidden energy gap of the poly-Si [16].

bottom of the poly-Si film is not significantly different, we have kept the intrinsic poly-Si film thickness within the Debye length [24]. Hence, the thickness of the poly-Si film chosen in our simulations is 35 nm. The metallurgical base contact length is 10 nm long. Although the poly-Si film is intrinsic, we have assumed it to be un-intentionally doped with $\mathrm{N_A} = 1 \times 10^{14}/\mathrm{cm}^3$ [29], [30]. The simulations are performed for 1 μm width. Intrinsic gap $\mathrm{L_{S1}}$ of 10 nm separates the emitter and the base field electrodes and a gap ($\mathrm{L_{S2}}$) of 200 nm is present between the base and the collector field electrodes. To realize an emitter-base gap of 10 nm in a fabricated device, one could use overleaping yet insulated emitter and base electrodes.

Simulations are performed with the ATLAS device simulation tool [31] using the Fermi-Dirac distribution of carrier statistics and Lombardi's model for modeling the effect of electric field and carrier concentration on the mobility [32]. The conventional drift-diffusion (DD) model [31], [33] used for carrier transport has basic semiconductor equations same as those of a single crystal device except that the trapped charges within the grain boundary region are included in Poisson's equation and a modified Shockley–Read–Hall (SRH) recombination term is used in the carrier continuity equations. To account for the impact ionization, Selberherr's model is invoked [34]. We have calibrated our models by first reproducing the results for a short channel TFT with a single grain boundary in the channel region as given in [16]. As the TFTs are scaled down to the nano-scale regime, channel length of the TFTs approaches the grain size and it is possible to have a single GB in the re-crystallized silicon film. However, controlling the location of the single GB in the device is difficult [9], [16]. Contact resistances are considered to be zero at all the contacts. SRH carrier lifetimes $\mathrm{taun0} = \mathrm{taup0} = 0.5$ μs are used in our simulations.

In our model, trap states are located only in the grain boundary (GB) region. We have considered a 4 nm long GB in the base region of the poly-Si BCPT just as in the case of the poly-Si TFT [16], [35]. As is done in Walker's approach [16], we have assumed the GB to be oriented perpendicular to the semiconductor surface for its maximum impact on carrier transport, although, in a real film the GB orientation would be random.

The placement of the single GB in the base region will affect the performance of the poy-Si BCPT. To analyze this effect we have varied the GB postion among three locations in the base region of the poly-Si BCPT – Device A: grain boundary is close to the emitter-base junction (6 nm away from the left edge of the base region), Device B: grain boundary is in the middle of the base region, Device C: grain boundary is close to the base-collector junction (6 nm before the right edge of the base region) of the poly-Si BCPT. In the GB, we have considered both acceptor-like and donor-like traps and have defined the density of defect states as a combination of four bands [16], [29]. Two exponential tail bands that have a large density of defect states near the conduction band (acceptor like traps) and valence band (donor like traps) edges, respectively, are specified. Two deep-level bands (acceptor-like and donor-like) with Gaussian distribution are also defined. The trap density distributions used in our simulations are as shown in Fig. 2 and all the associated simulation parameters are given in Table I. For the three GB positions as described above, the carrier concentration along the length of the device (cutline is taken 2 nm away from the top poly-Si-SiO_2 interface) is as shown in Fig. 3. As can be seen in Fig. 3, the carrier concentration is maintained in the device under thermal equilibrium ($\mathrm{V_{CE}} = \mathrm{V_{BE}} = 0$ V) as well as under forward active bias ($\mathrm{V_{CE}} = 1.0$ V and $\mathrm{V_{BE}} = 0.7$ V) conditions.

TABLE I
SIMULATION PARAMETERS

Parameters	Poly-Si BCPT
Capture cross section of (i) electrons in acceptor-like states σ_{ae} and (ii) holes in donor-like states σ_{dh}	1×10^{-16} cm^2
Capture cross section of (i) electrons in donor-like states σ_{de} and (ii) holes in acceptor-like states σ_{ah}	1×10^{-14} cm^2
Density of acceptor-like tail states N_{TA}	1×10^{21} cm^{-3} eV^{-1}
Density of donor-like tail states N_{TD}	4×10^{20} cm^{-3} eV^{-1}
Density of acceptor-like Gaussian states N_{GA}	5×10^{19} cm^{-3} eV^{-1}
Density of donor-like Gaussian states N_{GD}	5×10^{19} cm^{-3} eV^{-1}
Decay energy for acceptor-like tail states W_{TA}	0.05 eV
Decay energy for donor-like tail states W_{TD}	0.05 eV
Decay energy for acceptor-like Gaussian W_{GA}	0.1 eV
Decay energy for donor-like Gaussian W_{GD}	0.1 eV
Energy of Gaussian for acceptor-like states E_{GA}	0.51 eV
Energy of Gaussian for donor-like states E_{GD}	0.51 eV

III. RESULTS AND DISCUSSION

The Gummel plots in Fig. 4 for the three GB positions indicate that for a lower base-emitter voltage ($\mathrm{V_{BE}} < 0.6$ V), the collector current (I_C) increases as the GB position is varied across the base and it is highest for the Device C when the GB is nearer to the collector-base junction. To explain the rise in collector current as the GB is moved across the base region, the

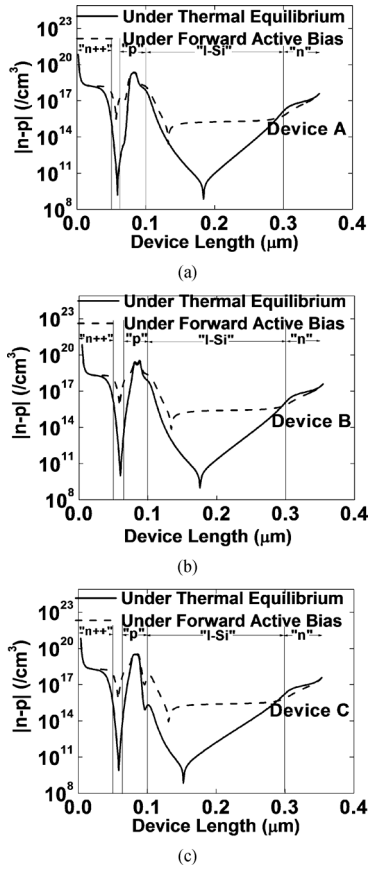


Fig. 3. Simulated net carrier concentrations for different bias conditions in the poly-Si BCPT for the three GB positions.

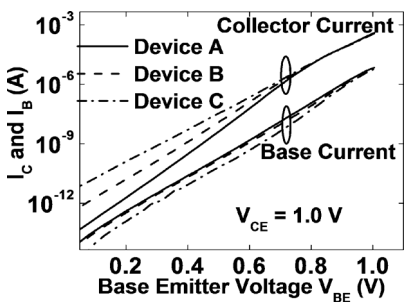


Fig. 4. Gummel plots of the poly-Si BCPT for the three GB positions.

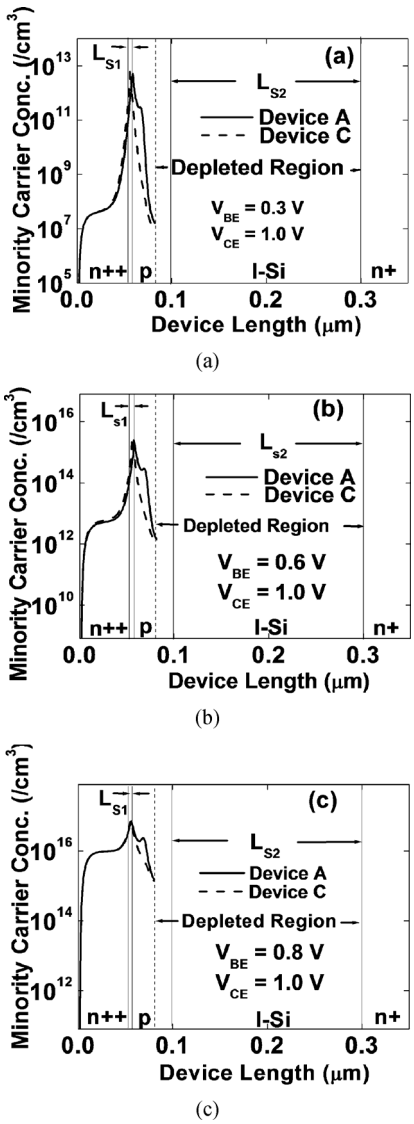


Fig. 5. The minority carrier profile for (a) $\mathrm{V_{BE}} = 0.3$ V (b) $\mathrm{V_{BE}} = 0.6$ V and (c) $\mathrm{V_{BE}} = 0.8$ V keeping $\mathrm{V_{CE}} = 1.0$ V for Device A and Device C.

minority carrier profile for Device A and Device C for different base-emitter voltages ($\mathrm{V_{BE}} = \{0.3\ \mathrm{V}, 0,6\ \mathrm{V}\ \mathrm{and}\ 0.8\mathrm{V}\}$) with collector–emitter voltage kept as constant ($\mathrm{V_{CE}} = 1.0$ V) is shown in Fig. 5. For lower $\mathrm{V_{BE}}$ values ($\mathrm{V_{BE}} = 0.3$ V and 0.6 V), the defect states present in the GB of the Device A trap the electrons injected from the emitter into the base, and lower the concentration gradient of the electrons in the base as shown in Fig. 5 compared to that for Device C. For Device C, GB lies out of the neutral base width region and hence, has the least recombination of the electrons in the base region and as a result, it has the highest concentration gradient of the electrons in the base and consequently, Device C exhibits the highest collector current among the three device structures. For $\mathrm{V_{BE}} = 0.8$ V almost all the trap states in the GB of the Device A are filled and the concentration gradient of the minority carriers in the base region is almost similar for all the devices causing the collector current of all the devices to be almost equal. For even higher $\mathrm{V_{BE}}$ values, high injection effect crops in and the slope of the collector current changes for all the devices.

The base current of Device A and Device B is more or less same, whereas, it is least for Device C. Since, the GB in Device C lies in the depleted region of the base, there is a significant enhancement in the generation current for Device C. Therefore, its base current is less as can be seen in Fig. 4. Consequently, Device C exhibits the highest peak current gain compared to the other two devices as seen in Fig. 6. The observed large current gain in the poly-BCPT structure is because of the surface layer accumulation of electrons at the metal-semiconductor interface on the emitter side. As explained in [24], [36], [37], the electron accumulate when a low work function metal is contacted to the n-type emitter forming a retarding electric field to the holes injected from the base region. This will lead to a reduction in the base current which enhances the current gain.

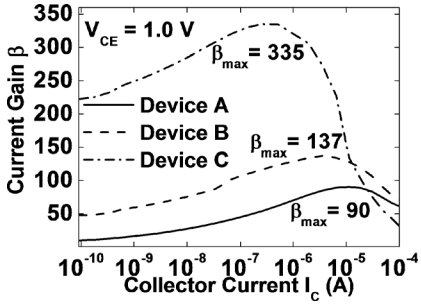


Fig. 6. Current gain variation of the poly-Si BCPT for the three GB positions.

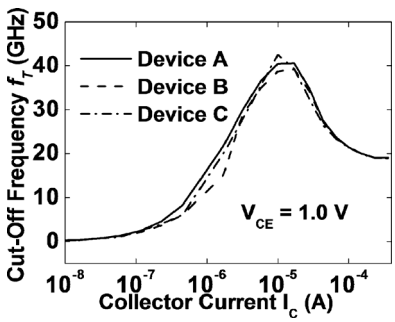
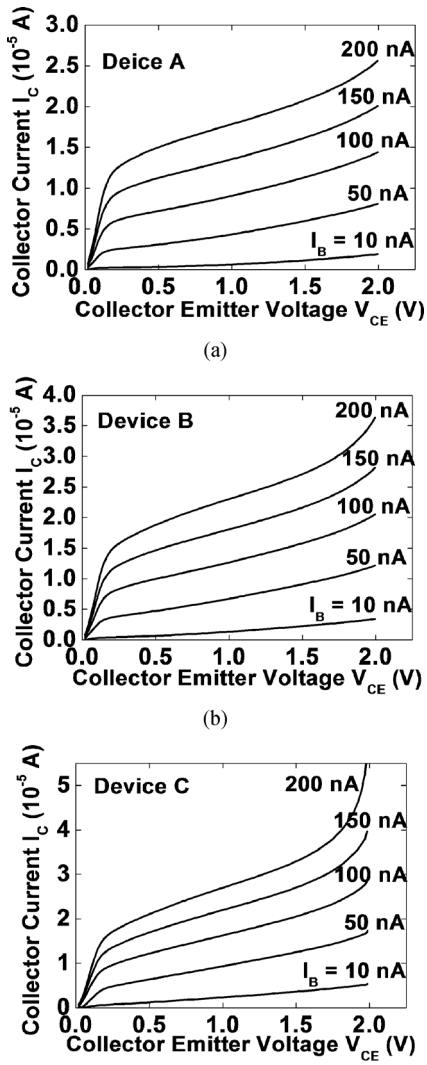


Fig. 7. Cut-Off frequency f_T variation of the poly-Si BCPT for the three GB positions.

By performing the AC analysis, the simulator gives the cut-off frequency of the device for the given bias conditions. The cut-off frequency f_T of the poly-Si BCPT, an important RF design parameter, is found to be around 40 GHz as shown in Fig. 7. The GB position in the base region does not cause the f_T to change drastically. Therefore, it makes the poly-Si BCPT an attractive device for the RF modules implemented in system-on-panel applications. Fig. 8 shows the output characteristics of the poly-Si BCPT for the three GB positions. The $\mathrm{BV_{CEO}}$ of the poly-Si BCPT is around 2.4 V for all the three GB positions.

IV. Conclusion

In this paper, using two-dimensional device simulations, the prospects of realizing a low-cost, undoped bipolar transistor with poly-Si on insulating substrates is reported. The fact that the poly-Si BCPT is not limited by the high thermal budgets that concerns the conventional BJTs makes it ideal for thin-film structures. Our simulation results reveal the efficacy of the poly-Si BCPT with high current gain and cut-off frequency in the range of tens of GHz for different GB positions across the base region. BJTs typically suffer from high input base current as compared to a TFT. However, the low operating voltage ($\mathrm{V_{CE}}$) of BJTs makes them particularly power efficient. Apart from the driver circuits of the AMLCDs, poly-Si BCPT can have potential applications in RF modules for system-on-panel and low-cost RF IDs. Measurement data of real physical device will prove the feasibility of this new structure. However, since we do not have the fabrication facilities, we believe that our simulation results may provide the incentive for further experimental demonstration as well as lay the foundation for system on glass substrate topology. However, it may be pointed out that one of the challenging issues in the fabrication



(a)

(b)

(c)

Fig. 8. Output characteristics of the poly-Si BCPT with $\mathrm{V_{BE}} = 0.7$ V for Device A (Grain boundary is 6 nm away from the left edge of the base region), Device B (Grain boundary is in the middle of the base region) and Device C (Grain boundary is 6 nm before the right edge of the base region).

of poly-Si BCPT is the control of metal work function and metal/undoped-silicon contact properties. Also, the uniformity in the device performance of the Poly-Si BCPT with a single GB under the base region has a strong dependence on the GB position. As in the case of the TFTs where the GB has to be located away from the drain edge [16], if high current gain is to be obtained, it is also desirable to control the GB position in the Poly-Si BCPT so that it is not near the emitter-base junction. The circuits designed with these devices should assume the worst case scenario (Device A with low current gain) since the GB position is not under the designer's control.

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