Bipolar Charge-Plasma Transistor: A Novel Three Terminal Device

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***Abstract*—A distinctive approach for forming a lateral bipolar charge-plasma transistor (BCPT) is explored using 2-D simulations. Different metal work-function electrodes are used to induce n- and p-type charge-plasma layers on undoped silicon-on-insulator (SOI) to form the emitter, base, and collector regions of a lateral n-p-n transistor. Electrical characteristics of the proposed device are simulated and compared with that of a conventionally doped lateral bipolar junction transistor (BJT) with identical dimensions. Our simulation results demonstrate that the BCPT concept will help us realize a superior bipolar transistor in terms of a high current gain, as compared with a conventional BJT. This BCPT concept is suitable in overcoming doping issues such as dopant activation and high-thermal budgets, which are serious issues in ultrathin SOI structures.**

***Index Terms*—Bipolar charge-plasma transistor (BCPT), complementary metal–oxide–semiconductor (CMOS) technology, current gain, silicon-on-insulator (SOI), simulation.**

I. Introduction

BIPOLAR transistors exhibit a number of significant advantages such as well-controllable characteristics, high speed, high gain, and low output resistance. These are excellent properties for mixed-signal circuit design and analog amplifiers. An emergent trend in modern high-density very large scale integrated circuits is the integration of bipolar transistors with complementary metal–oxide–semiconductor (CMOS) technology on thin silicon-on-insulator (SOI) films.

However, CMOS fabrication favors lateral bipolar transistor concepts [1]–[6] on SOI since it is easier to tune the SOI layer properties to optimize the CMOS devices without degrading the performance of the bipolar devices [2]. The realization of a true low-cost BiCMOS process is possible only when the lateral bipolar transistors can be fabricated on CMOS using simple fabrication steps with low thermal budgets. High-temperature cycles, required for post ion-implantation annealing of emitter and base regions of a bipolar transistor, can create complications while integrating the bipolar process with the CMOS process.

To overcome the aforementioned problems, we propose for the first time a new device concept designated as a bipolar charge-plasma transistor (BCPT), as shown in Fig. 1. In this structure, no ion implantation is done on silicon; rather, the p- and n-type regions are formed in the undoped silicon layer by employing metal electrodes with different work functions [7]–[9] to induce an electron plasma for forming the emitter and collector regions, and a hole plasma to form the base region. The most important advantage of the proposed BCPT is the absence of doped regions. This avoids the necessity of complicated thermal budgets using expensive annealing equipment.

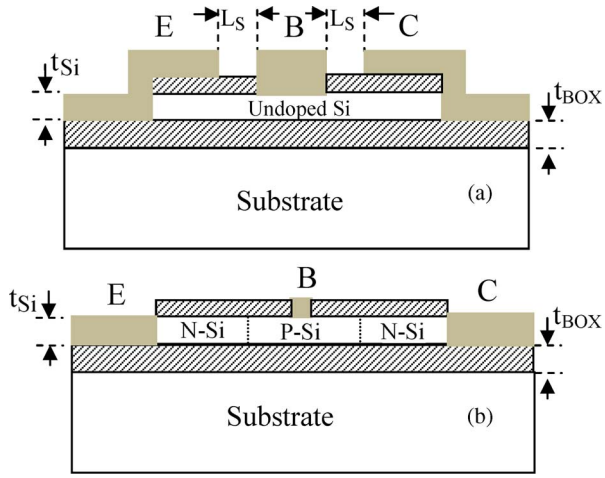

Fig. 1. Schematic cross-sectional view of (a) the BCPT and (b) the conventional BJT.

Using 2-D simulations, we describe in this paper the unique electrical characteristics of the BCPT on an undoped SOI. Our results show that the BCPT exhibits a good transistor action with a significantly larger current gain, as compared with a conventional bipolar junction transistor (BJT) with the same device geometry. Our results may provide the incentive for further experimental exploration of the BCPT concept since a charge-plasma p-n junction has been already experimentally demonstrated [7].

II. Device Structure and Simulation Parameters

The schematic views of the lateral n-p-n BCPT and the conventional lateral BJT are shown in Fig. 1. The parameters of the devices used in our simulation are: the background doping $N = 1 \times 10^{13}/\text{cm}^3$, the buried-oxide layer thickness $t_{\text{BOX}} =$ 375 nm, the separation between the electrodes ($L_S = 100$ nm), the gate-oxide layer thickness $t_{\text{ox}} = 5$ nm, and the undoped-silicon layer thickness $t_{\text{Si}} = 15$ nm. In the BCPT, the electrode length of the emitter, base, and collector regions is chosen to be 0.2, 0.1, and 0.4 μm, respectively. For creating the emitter, by

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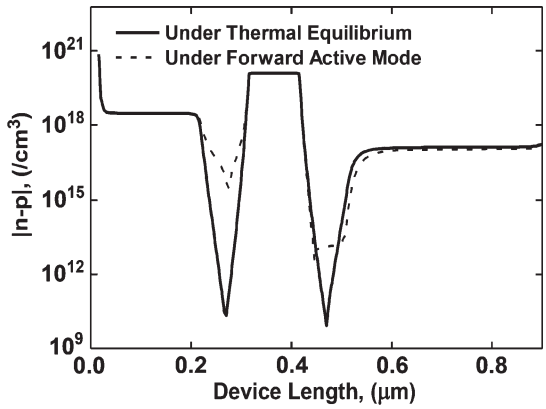

Fig. 2. Simulated net carrier concentrations in the BCPT for different bias conditions.

inducing electrons in the undoped silicon body, hafnium (work function $\varphi_{m,E} = 3.9$ eV) is employed as the emitter electrode metal. For inducing holes to create the base region, platinum (work function $\varphi_{m,B} = 5.65$ eV) is used. As the collector of an n-p-n transistor needs to have a lower carrier concentration than the base region, to induce electrons to create the collector region, Al (work function $\varphi_{m,C}$ of 4.28 eV) is used. It is also important to choose an appropriate thickness for the silicon film. To maintain uniform induced carrier distribution throughout the silicon thickness, from the oxide–Si interface to the Si–buried-oxide interface, the silicon film thickness has to be kept within the Debye length, i.e., $L_D = \sqrt{((\varepsilon_{\rm Si} \cdot v_T)/(q.N))}$ where $\varepsilon_{\rm Si}$ is the dielectric constant of silicon, V_T is the thermal voltage, and N is the carrier concentration in the body [8]. For the BCPT structure shown in Fig. 1, the simulated net carrier concentrations (taken at 2 nm away from the Si–oxide interface) for zero bias and typical forward active conditions are shown in Fig. 2. Either under thermal equilibrium condition ($V_{\rm BE} = 0$ V and $V_{\rm CE} = 0$ V) or under forward active bias condition ($V_{\rm BE} = 0.7$ V and $V_{\rm CE} = 1$ V), the electron and hole charge-plasma concentrations are maintained in the emitter ($n_E = 2 \times 10^{18}$ /cm^3), base ($p_B = 1 \times 10^{20}$ /cm^3), and collector ($n_C = 2 \times 10^{17}$ /cm^3) regions due to the choice of work functions of the metal electrodes with respect to that of silicon, e.g., low value of $\varphi_{m,E}$ and $\varphi_{m,C}$ for the emitter and collector electrodes, and higher $\varphi_{m,B}$ for the base electrode. This presence of charge-plasma (electron/hole) concentrations in the undoped silicon film permits the formation of a BCPT.

Quasi-Fermi levels (QFLs) of the BCPT under thermal equilibrium and under forward active bias conditions are shown in Fig. 3. Under thermal equilibrium, the QFLs for electrons and holes align with each other as in the conventional BJTs, as shown in Fig. 3(a). Since excess carriers are present on either side of the forward-biased emitter–base junction, the QFLs are different for holes and electrons in this case. In the reverse-biased base–collector region, the minority carrier concentration in the collector region does not reach its thermal equilibrium value because of the presence of the field electrode. This is why the QFLs do not merge throughout the collector region, as shown in Fig. 3(b).

The current in the BCPT is strongly controlled by the electrodes. The lateral n-p-n transistor with which we have

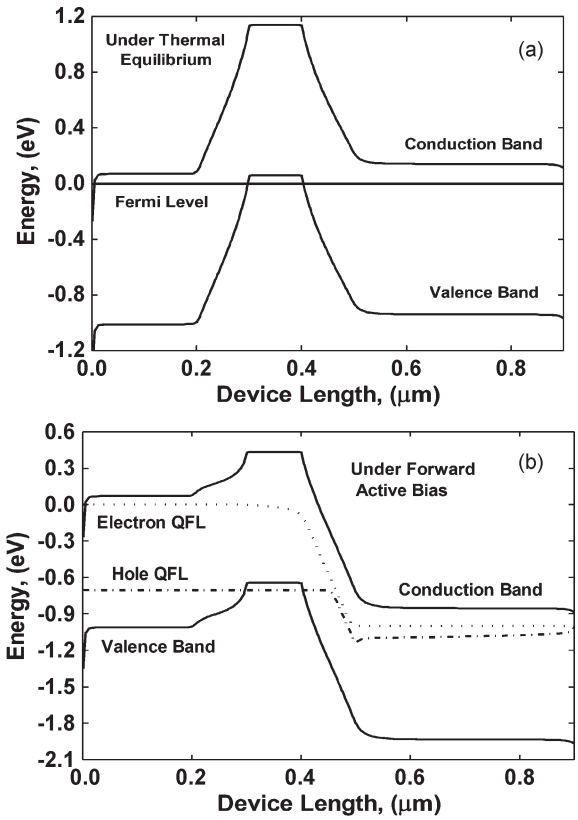

Fig. 3. Simulated energy band diagram (a) under thermal equilibrium and (b) under forward-active bias conditions for the BCPT.

compared our results is also an SOI structure and has the same device parameters as that of the BCPT except that the emitter, base, and collector regions have a length of 0.25, 0.2, and 0.45 μm, and a typical doping of $N_D = 1 \times 10^{20}$ /cm^3, $N_A = 9 \times 10^{17}$ /cm^3, and $N_D = 2 \times 10^{17}$ /cm^3, respectively. The lengths are chosen so as to have an equal neutral base width for both the transistors. The doping profile is chosen similar to that of a practical bipolar transistor. We could not choose the emitter doping and the base doping of the BJT same as the charge-plasma concentrations in the BCPT since this would make the current gain of the BJT extremely low (less than 1) due to the larger base Gummel number, as compared with the emitter Gummel number in the BCPT.

Simulations have been performed with the ATLAS device simulation tool [10] using the Fermi–Dirac distribution for carrier statistics, with Philip's unified mobility model [11], and with doping-induced band-gap narrowing model [12], all with default silicon parameters. The standard thermionic emission model [9] is invoked for the emitter contact of the BCPT with a work function of 3.9 eV and a surface recombination velocity of 2.2×10^6 and 1.6×10^6 cm/s for electrons and holes, respectively. The same base metal, i.e., platinum, is used at the base contact of the BCPT and the BJT to ensure that the base contact properties are identical in both the transistors. This ensures that the lower base current in the BCPT is not due to a difference in the base contact properties. Ohmic contact conditions are assumed at all other contacts. The metal–semiconductor contact resistances are assumed to be negligible in both the transistors. For recombination, we have

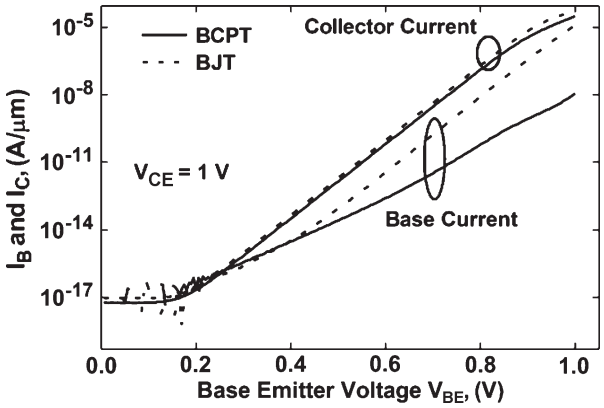

Fig. 4. Gummel plots of the BCPT and conventional BJT structures.

enabled Klassen's model for concentration-dependent lifetimes for Shockley-Read-Hall (SRH) recombination with intrinsic carrier lifetimes $n_{\rm ie} = n_{\rm ih} = 0.2\ \mu$s [13]. High electric-field velocity saturation is modeled through the field-dependent mobility model [10]. The screening effects in the inversion layer are also considered by invoking the Shirahata mobility model [14]. Selberherr impact ionization model is used for calculating $B_{\rm VCEO}$ [15]. To ensure that our simulations are accurate, we have first reproduced the simulation results of the charge-plasma diode characteristics [8] using the aforementioned models and ensured that the current–voltage characteristics predicted by our simulation match with those reported in [8].

III. Results and Discussion

The Gummel plot for the BCPT is compared with that of the BJT, as shown in Fig. 4. While the BCPT exhibits almost the same collector current, as compared with the conventionally doped BJT, the base current of the BCPT is much lower than that of the BJT due to the Surface Accumulation Layer Transistor (SALTran) effect [5], [16]. When a lightly doped emitter is contacted with a metal whose work function is less than that of silicon, it results in a surface accumulation of electrons at the metal contact, as shown in Fig. 5. However, no such electron accumulation is observed in the case of the BJT since its emitter is heavily doped. In the case of the BCPT, the accumulation of electrons results in an electric field due to the electron concentration gradient from the metal–semiconductor interface toward the emitter–base junction. The direction of this field is such that it repels the minority holes injected from the base into the emitter, resulting in a reduced hole concentration gradient in the emitter region. As a consequence, there is a reduction in the base current, leading to a significant improvement in the current gain, as explained in [5] and [16]. Hence, the peak current gain of the BCPT (4532) is several orders higher compared with the peak current gain of the conventional BJT (26.5), as shown in Fig. 6. As discussed in [8] and [17], the metal work functions strongly control the current in the charge-plasma diode. Likewise, the work functions of the emitter and base electrode metals strongly control the emitter and base currents. By appropriately choosing the metal electrode work functions, the BCPT characteristics can be effectively controlled. The output current drive of the BCPT is in agreement with the

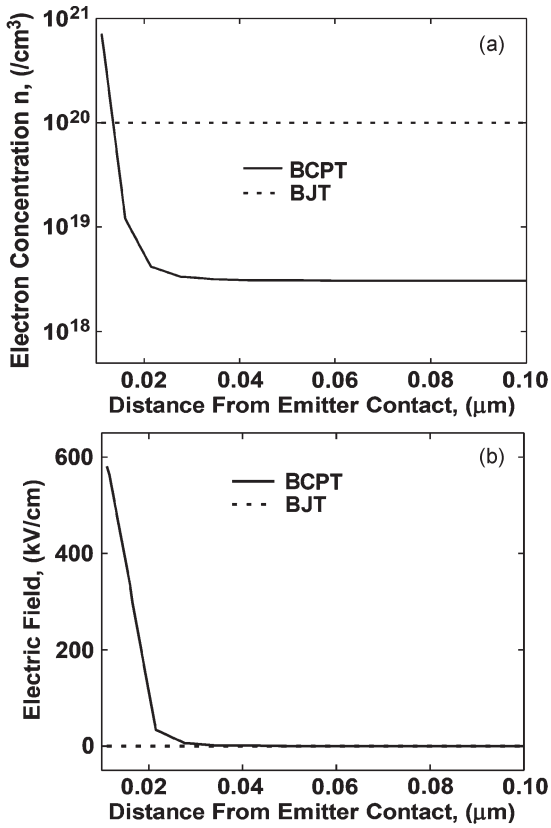

Fig. 5. (a) Electron concentration and (b) electric-field distribution in the emitter region of the BCPT and conventional BJT structures.

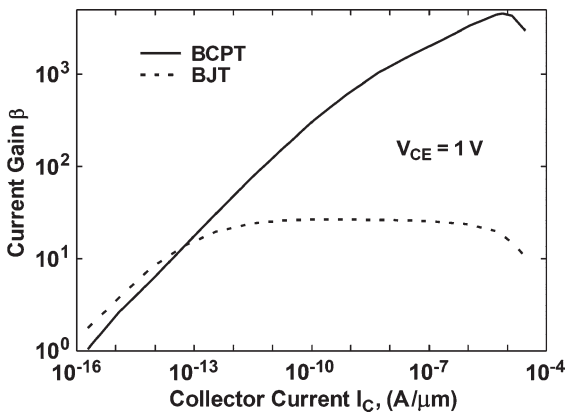

Fig. 6. Current gain variation of the BCPT and the conventional BJT.

forward current levels of the charge-plasma diode reported in [7] and [8]. However, further work needs to be done to increase the current levels by optimizing the device dimensions and the choice of metals.

The output characteristics of the BCPT are compared with that of the conventional BJT in Fig. 7. Due to its larger current gain, the BCPT exhibits a slightly lower collector breakdown voltage compared with the conventional BJT. However, we observe negligible base width modulation in the BCPT due to a higher concentration of induced holes in the base region of the BCPT.

The saturation voltage $[V_{\rm CE(sat)}]$ is marginally higher for the BCPT due to the lower electron concentration in the emitter

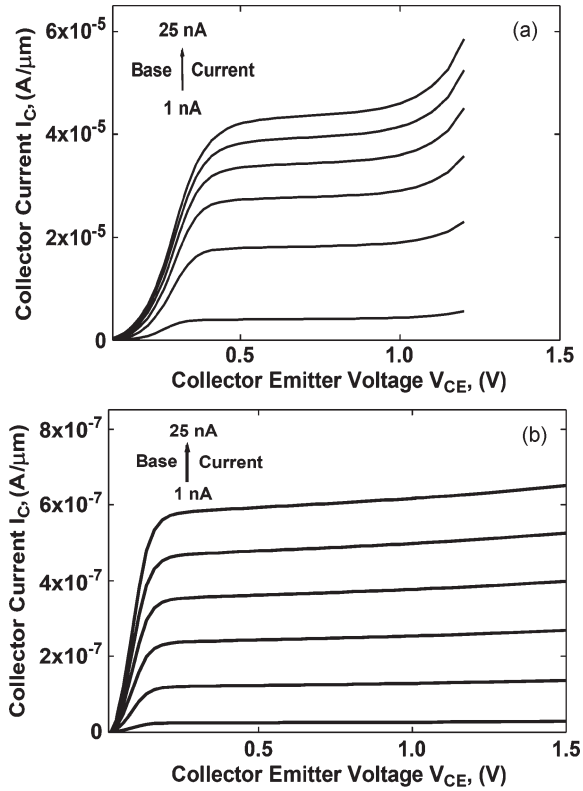

Fig. 7. Output characteristics of (a) the BCPT and (b) the conventional BJT.

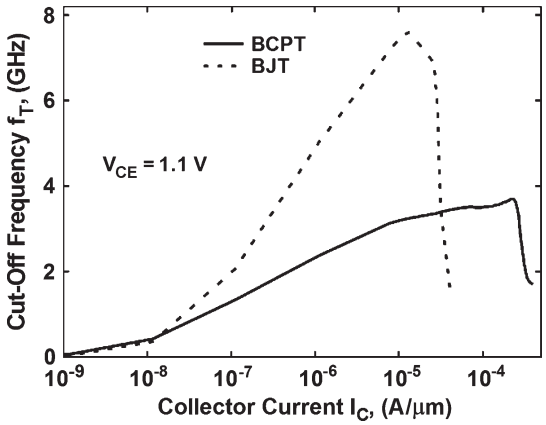

Fig. 8. Cutoff frequency of (a) the BCPT and (b) the conventional BJT.

compared with the BJT. If the emitter doping in the BJT structure is made similar to the electron concentration in the emitter of the BCPT, we have observed a similar increase in $V_{\mathrm{CE(sat)}}$ even for the BJT. For bipolar transistors to be useful in high-frequency applications, their f_T should be higher than 1 GHz. Fig. 8 shows that the simulated cutoff frequency f_T of the BCPT (3.7 GHz) and BJT (7.5 GHz) structures. However, the presence of intrinsic gaps ($L_S = 100$ nm) between the emitter–base and collector–base junctions, which are larger than in the BJT, will lower the cutoff frequency of the BCPT compared with that of the BJT structure. Our simulation results show that the speed of the BCPT is lower than that of the conventional lateral BJTs, and further work needs to be done to optimize the speed of the BCPT.

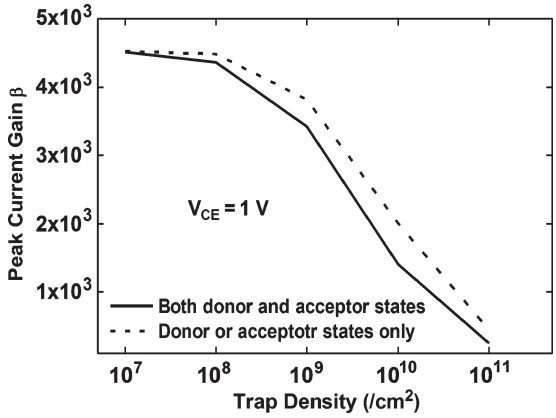

Fig. 9. Peak current gain versus trap density for the BCPT structure.

IV. Effect of Interface Traps on Current Gain

A key feature of the BCPT structure is the low work-function metal electrode employed at the emitter contact forming a metal–semiconductor junction (hafnium–silicon). Depending on the surface preparation and metal deposition methods, there is a definite possibility of the presence of traps at the hafnium–silicon interface due to lattice discontinuity and the dangling bonds, not to mention interdiffusion. These traps are very likely to affect the electron distribution and the electric field in this area, which in turn would affect the SALTran effect [18]. Both the acceptor and donor types of interface traps can affect the accumulation of electrons at the interface and, thus, the current gain of the BCPT.

To simulate the influence of interface traps on the device characteristics, we have considered a typical range of interface traps, which may be present at the interface. In our simulations, both the acceptor and donor types of traps are introduced with the trap energy level (E.level) at 0.49 eV from the conduction (or valance) band [5]. The degeneracy factor (degen) for the trap level is chosen to be 12, and the capture cross sections for electrons (sign) and holes (sigp) are taken to be 2.85×10^{-15} and 2.85×10^{-14} cm^{-2}, respectively.

Peak current gain reduces when the trap density of the acceptor (or donor) type of interface traps increases at the interface, as shown in Fig. 9, and the effect is even more severe when both types of traps are present at the interface. This effect is also observed for a conventional SALTran [5]. However, even with a trap density of 1×10^{11} cm^{-2}, the BCPT still maintains a substantially high peak current gain, as observed in Fig. 9.

V. Conclusion

In conclusion, we have reported the possibility of realizing a unique BCPT made of electron and hole plasmas on undoped silicon making it immune to thermal budget concerns faced by doped transistors and CMOS devices. The efficacy of the proposed concept is verified using 2-D numerical simulations. Our simulation results demonstrate that the BCPT exhibits a significantly large current gain, as compared with a conventional BJT with doped regions of similar geometry. The BCPT concept can be also applied for materials such as SiC in which doping is an issue or for heterojunction bipolar transistors.

This idea can be extended to an undoped silicon nanowire with surround gate electrodes to induce the emitter, base, and collector regions making it compatible with the future nanowire and fin-shaped field-effect transistor-based CMOS technology [19], [20]. Since the charge-plasma-based diode concept has been already experimentally demonstrated [7], we believe that our results will provide the incentive for further experimental verification of the BCPT concept. However, it remains to be seen whether the fabrication of the BCPT will be cost effective, since three different metals are required for the emitter, base, and collector electrodes. The device also needs to be optimized to match the speed performance of the commercially available lateral bipolar transistor technology.

REFERENCES

[1] S. D. Roy and M. J. Kumar, "Enhanced breakdown voltage, diminished quasi-saturation and self-heating effects in SOI thin-film bipolar transistors for improved reliability: A TCAD simulation study," *IEEE Trans. Device Mater. Rel.*, vol. 6, no. 6, pp. 306–314, Jun. 2006.

[2] I. S. M. Sun, W. T. Ng, K. Kanekiyo, T. Kobayashi, H. Mochizuki, M. Toita, H. Imai, A. Ishikawa, S. Tamura, and K. Takasuka, "Lateral high-speed bipolar transistors on SOI for RF SoC applications," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1376–1383, Jul. 2005.

[3] H. Nii, T. Yamada, K. Inoh, T. Shino, S. Kawanaka, M. Yoshimi, and Y. Katsumata, "A novel lateral bipolar transistor with 67 GHz $f_{(\max)}$ on thin-film SOI for RF analog applications," *IEEE Trans. Electron Devices*, vol. 47, no. 7, pp. 1536–1541, Jul. 2000.

[4] M. J. Kumar and D. V. Rao, "A new lateral PNM Schottky collector bipolar transistor (SCBT) on SOI for non-saturating VLSI logic design," *IEEE Trans. Electron Devices*, vol. 49, no. 6, pp. 1070–1072, Jun. 2002.

[5] M. J. Kumar and V. Parihar, "Surface Accumulation Layer Transistor (SALTran): A new bipolar transistor for enhanced current gain and reduced hot-carrier degradation," *IEEE Trans. Device Mater. Rel.*, vol. 4, no. 3, pp. 509–515, Sep. 2004.

[6] S. A. Loan, S. Qureshi, and S. S. K. Iyer, "A novel high breakdown voltage lateral bipolar transistor on SOI with multizone doping and multistep oxide," *Semicond. Sci. Technol.*, vol. 24, no. 2, p. 025017, Feb. 2009.

[7] B. Rajasekharan, R. J. E. Hueting, C. Salm, T. van Hemert, R. A. M. Wolters, and J. Schmitz, "Fabrication and characterization of the charge-plasma diode," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 528–530, Jun. 2010.

[8] B. Rajasekharan, C. Salm, R. J. E. Hueting, T. Hoang, and J. Schmitz, "The charge plasma p-n diode," *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1367–1369, Dec. 2008.

[9] K. Nadda and M. J. Kumar, "A novel doping-less bipolar transistor with Schottky collector," in *Proc. Int. Semicond. Device Res. Symp.*, College Park, MD, Dec. 2011.

[10] *ATLAS Device Simulation Software*, Silvaco Int., Santa Clara, CA, 2010.

[11] D. B. M. Klassen, "A unified mobility model for device simulation—I: Model equations and concentration dependence," *Solid State Electron.*, vol. 35, no. 7, pp. 953–959, Jul. 1992.

[12] D. B. M. Klaassen, J. W. Slotboom, and H. C. De Graaff, "Unified apparent band-gap narrowing in n- and p- type silicon," *Solid State Electron.*, vol. 35, no. 2, pp. 125–129, Feb. 1992.

[13] D. B. M. Klassen, "A unified mobility model for device simulation—II: Temperature dependence of carrier mobility and lifetime," *Solid State Electron.*, vol. 35, no. 7, pp. 961–967, Jul. 1992.

[14] M. Shirahata, H. Kusano, N. Kotani, S. Kusanoki, and Y. Akasaka, "A mobility model including the screening effect in MOS inversion layer," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 11, no. 9, pp. 1114–1119, Sep. 1992.

[15] S. Selberherr, *Analysis and Simulation of Semiconductor Devices*. Wien, NY: Springer-Verlag, 1984.

[16] M. J. Kumar and P. Singh, "A super beta bipolar transistor using SiGe-base surface accumulation layer transistor (SALTran) concept: A simulation study," *IEEE Trans. Electron Devices*, vol. 53, no. 3, pp. 577–579, Mar. 2006.

[17] T. van Hemert, R. J. E. Hueting, B. Rajasekharan, C. Salm, and J. Schmitz, "On the modelling and optimization of a novel Schottky based silicon rectifier," in *Proc. of ESSDERC*, 2010, pp. 460–463.

[18] K. Ziegler, "Distinction between donor and acceptor character of surface states in the Si-SiO interface," *Appl. Phys. Lett.*, vol. 32, no. 4, pp. 249–251, Feb. 1978.

[19] M. J. Kumar, M. A. Reed, G. A. J. Amaratunga, G. M. Cohen, D. B. Janes, C. M. Lieber, M. Meyyappan, L.-E. Wernersson, K. L. Wang, R. S. Chau, T. I. Kamins, M. Lundstrom, B. Yu, and C. Zhou, "Special issue on nanowire transistors: Modelling, device design, and technology," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 2813–2819, Nov. 2008.

[20] M. J. Kumar, M. A. Reed, G. A. J. Amaratunga, G. M. Cohen, D. B. Janes, C. M. Lieber, M. Meyyappan, L.-E. Wernersson, K. L. Wang, R. S. Chau, T. I. Kamins, M. Lundstrom, B. Yu, and C. Zhou, "Special issue on nanowire transistors: Modelling, device design, and technology," *IEEE Trans. Nanotechnol.*, vol. 7, no. 6, pp. 643–650, Nov. 2008.

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