LUND UNIVERSITY

Department of
Electrical and Information
Technology

ETI063 - Analogue IC Design
Laboratory Manual

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Contents

Introduction

This laboratory is designed for students who follow the course Analogue IC Design (ETI063), to have a complete idea of how an analog integrated circuit is implemented. You will get acquainted with the whole cycle of integrated circuit design, starting from a specification followed by designing the circuit in schematic phase using a CAD[1] tool (Cadence, version 5.1.0). The next step is layout design, an another important step of integrated circuit design before submitting the circuit to be fabricated on a semiconductor chip by a foundry.

Laboratory Overview

The four laboratories are listed as followed:

1. Measurement of MOS model parameters.
2. Schematic level simulation of an inverter and current mirror.
3. Schematic drawing and simulation of an operational amplifier.
4. Layout design and parasitics simulation of an amplifier.

In the first laboratory some basic transistor parameters, belonging to a simple MOS transistor model, will be measured. The main purpose of this laboratory is to examine the different working areas of the transistor.

The remaining laboratories will have Cadence in common as a tool for building, verifying, and simulating circuit designs. You will work on a schematic level design of an inverter and a current mirror in the second laboratory. The goals are that you will get familiar with the Cadence and GoldenGate environment and perform different types of simulation analyses.

In the third laboratory, you will learn how to design an amplifier, starting by hand calculation and verifying it through simulations. Finally, the layout of the amplifier will be drawn in the fourth laboratory, followed by verification of the layout and simulation including parasitics.

These laboratories give a good foundation for those of you who want to continue with the course IC-Project & Verification in period 2, where you will have an opportunity to design a chip, get it manufactured and perform measurements.

[1] Computer Aided Design

Requirements to complete a laboratory

Each laboratory will consist of three parts:

- Laboratory preparation and home exercises (expected to be completed before coming to the laboratory).
- Execution of the laboratory tasks.
- Submission of a complete laboratory report.

Notice: A laboratory is not approved until all three requirements are fulfilled.

General Guidelines for a Laboratory Report

A laboratory report should contain solutions to questions of home exercises. The results of the laboratory must be included, as well as an explanation of the results. You may include general discussions on obstacles experienced in the laboratory. Suggestions on how to improve our laboratories are always welcome.

Notice: A laboratory report is to be submitted one week after the laboratory was performed.

Laboratory 1 : Measurement of MOS Model Parameters

The goal of this laboratory is to measure three important model parameters for the MOS transistor. The accuracy and reliability on the measured values of the transistor parameters determine directly the accuracy and reliability of the simulation results. Students who have completed the course Analogue Circuits (ESS020/ESSF01) are not obliged to do this laboratory. [2]

Introduction

You will perform measurements on a discrete n-channel MOSFET, the BS170, and a PMOSFET, the BS250. The pin configuration is shown in the data sheet, which can be found on the course website (see Course material).

The simple transistor model that is used here is called Schichman-Hodges, and exists in SPICE as LEVEL 1. Here the drain current is modeled as:

$$I_D = 0 \quad for \;\; V_{GS} - V_t < 0 \tag{1}$$

$$I_D = k' \frac{W}{L} \left[(V_{GS} - V_t) - \frac{V_{DS}}{2} \right] V_{DS} \quad for \;\; 0 < V_{DS} < V_{GS} - V_t \tag{2}$$

$$I_D = \frac{1}{2} k' \frac{W}{L} (V_{GS} - V_t)^2 [1 + \lambda V_{DS}] \quad for \;\; 0 < V_{GS} - V_t < V_{DS} \tag{3}$$

where

$$k' = \mu C_{\mathrm{OX}} \tag{4}$$

During this laboratory you will take measurements on the transistor, and from the curves so obtained you will graphically extract the parameters $k' \frac{W}{L}$, V_t, g_m, and λ. The parameters will be estimated by local fitting, that is, they will be measured in the working region of the transistor where each of them dominates. It is therefore important to select appropriate voltage levels for the measurement of the different parameters, according to the desired working region.

Homework

1. From the datasheet, assuming room temperature, V_{GS}=5.0V and V_{DS}=10V, estimate r_o and λ, and $k' \frac{W}{L}$.

2. The schematic for measuring the NMOSFET is given in figure 1. You will have at your disposal:

[2] However, approval must be received from the course Laboratory administrator.

- one power supply box with two supplies and a signal ground
- one variable resistor
- one fixed value resistor of 100 Ω
- a multi–meter

3. Design a measurement procedure to extract the parameters mentioned in (1) for the saturation region, and the threshold voltage V_t and on-resistance R_{on} in the linear (triode) region (see Eq. 2.53 in the text book): How do you measure the drain current and regulate the variable voltages V_{GS} and V_{DS}? Decide on suitable voltage ranges (write a table) and how to determine each of the above parameters. Keep the supply voltage below 15V, and the gate-source voltage below 2.4V.

4. Draw the schematic and give the drain current equations for a PMOS transistor.

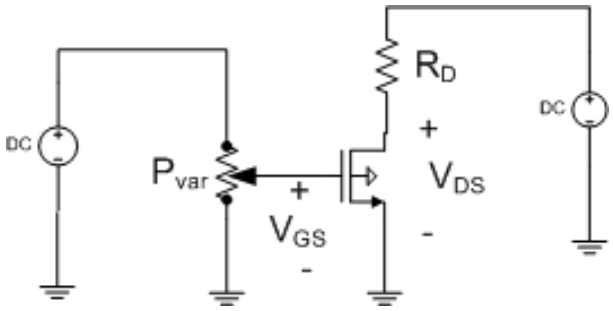

Figure 1: Circuit for biasing the NMOSFET and measuring the current I_D.

Laboratory Exercises

1. Connect the NMOSFET (BS170) and other components as shown in figure 1.

2. Measure the current in the linear region for a small V_{DS} =0.2V, sweeping V_{GS} (see also Eq. (2) above).

3. Reading the section on Parameter extraction, extract V_t and $k' \frac{W}{L}$ from the curve.

4. Measure the current in the linear region sweeping V_{DS}, keeping V_{GS} = 2V.

5. Extract R_{on} from the curve.

6. Measure the current in the saturation region: V_{GS} = 1.8V, sweeping V_{DS} (see also Eq. (3) above). Second, measure I_D while keeping V_{DS} constant (3V) and sweeping V_{GS}.

7. Extract g_m and λ from these measurements.

Notice: Do not connect the power until everything is connected. Turn off the power if you want to change some connections.

Parameter Extraction by Local Fitting Method

The method of local fitting means that each of the model parameters is measured in the working region of the transistor where it dominates. In this way, only a small number of measurements is necessary, which makes the method easy to perform. The main drawback is that it is very model dependent, i.e. a unique measuring program has to be designed for each model.

Let us first have a look at the n-channel transistor in its linear region (small V_{DS}). In the model the drain current is modelled as in equation (2). Here we find that $I_D = 0$ would correspond to the gate-source voltage

$$V_{GS,0} = V_t + \frac{V_{DS}}{2} \; .$$

This means that the threshold voltage can be measured by plotting a $I_D - V_{GS}$ diagram and estimating the intersection with the V_{GS}-axis as in figure 2.[3]

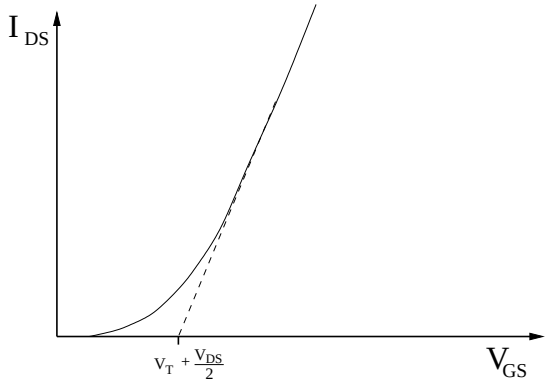

Figure 2: Extraction of the threshold voltage.

In order to determine the value of $k' \frac{W}{L}$ we take the derivative of equation (2) as function of V_{GS}, and get

[3] If the transistor would be used in the active region, the relation between I_D and V_{GS} would be quadratic.

$$\frac{\partial I_D}{\partial V_{GS}} = k' \frac{W}{L} V_{DS} \ ,$$

and since this is the slope of the curve, we can now easily determine $k' \frac{W}{L}$ by analyzing the linear part of the curve. It is adviseable to set a small value for V_{DS} to achieve a wide linear range of operation.

The channel length modulation coefficient (λ) is measured in the saturation region of the transistor. See Eq. 1.164 and 1.165 in the textbook. The drain current in this case is described by equation (3). If we assume a fixed $V_{GS} > V_t$, we can determine λ by looking at the sensitivity of I_D for V_{DS}. The slope of the I_D curve can be determined by interpolating to $I_D = 0$, so we find that

$$V_{DS,0} = -\frac{1}{\lambda} \ .$$

If we plot a $I_D - V_{DS}$ diagram for saturation, with constant V_{GS}, and calculate the intersection with the V_{DS}-axis, as is illustrated in figure 3, we will get the value of λ.

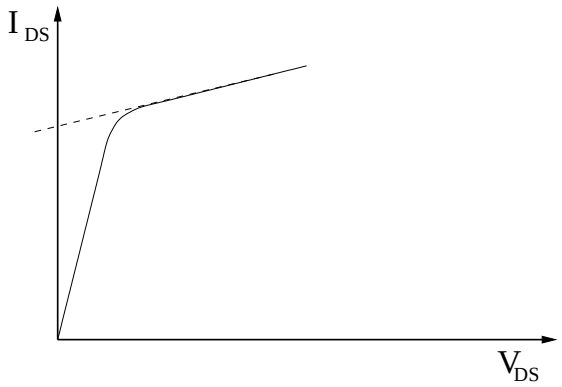

Figure 3: Measuring the channel length modulation factor.

The small-signal transconductance g_m in the saturation region is defined as

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \approx k' \frac{W}{L} (V_{GS} - Vt) \ ,$$

(see Eq. 1.180 in the textbook).

Laboratory Report

Put together a report which shows how the measurements were planned and performed, and which also includes the measurement results for the different parameters.

Laboratory 2 : Schematic Drawing and Simulation

In this laboratory you will be introduced to the Cadence schematic editor and GoldenGate simulation tool. We will focus on two basic circuits: the inverter and the current mirror. A *schematic* and a *symbol* view will be created for each circuit, followed by simulations to verify that they work properly.

Homework

Read through the manual for this laboratory, and read relevant sections of the text book or other sources. Answer the questions below:

Part 1 : The Inverter

1. For an inverter it is often desirable to have equal rise- and falltime. What is a common ratio of the width of the PNOS and NMOS transistor to achieve this?
2. Explain why different widths must be used, that is, explain the physical background.
3. How can one determine the rise- and fall time from a time domain simulation?

Part 2: The Current Mirror

1. Explain in your own words how the current mirror works. How can the current mirror be used?
2. For a DC current $I = 100\mu A$, calculate the expected output resistance r_o.

Laboratory Exercises

Plotting from the Waveform Window

- In the waveform window press: *Window->Hardcopy...*. Unmark *header* and *Mail Log To*.
- Choose *Plotter Name*: *mp*
- Mark *Send Plot Only To File*, and *Fit to page* if you get this option, and type in your filename.ps. The plot will then be saved in your Cadence root directory.

- Then you can open the .ps file with a program such as Gimp.

Part 1: The Inverter

First, a schematic view and symbol view must be generated.

1. Create a catalog, ana2009, in your home directory (**> mkdir ana2009**), to use during this course, and descend into it (*> cd ana2009* in the terminal window).

2. Start the initialization (**> inittde ana2009**), then Cadence (**> icfb &**). If the Library manager does not start automatically, choose *Tools > Library Manager ...* in the CIW to open the Library Manager window.

3. Create a design library and call it **Labs**. Choose *File > New > Library....* Then click OK. Choose
   Attach to an existing techfile - click OK
   Attach To Technology Library = umc13mmrf. Click OK again.

4. Create the inverter schematic: Select library **Labs**, choose *File > New > Cellview ...*, **Cell Name = inverter, View Name = schematic, Tool = Composer-Schematic**.

5. For the inverter you will need the instances *N*_12_*HSL*130*E* and *P*_12_*HSL*130*E* from the design library **umc13mmrf**, and **gnd** and **vdd** from **analogLib**. The transistors have four terminals.
   The instances **vdd** and **gnd** are global. This means that if you connect a voltage source between **vdd** and **gnd**, all of these, on all hierarchical levels, will have the same voltage.

6. In the schematic window, use the command *Add > Instance ...* to create an instance. Browse to find the instances mentioned above, with view *symbol*. Place the instances. Set the transistor width to 0.6u and length to 130n. If you don't do this when the transistors are created, you can change the transistor parameters later on by using the command *Edit > Properties > Objects ...* on a selected transistor.

7. Create the input- and output pins (*Add > Pin ...*). Choose input-output as direction. See Fig.4.
   Connect the instances together by drawing wires (*Add > Wire (narrow)*): Don't forget to connect the PMOS and NMOS bulk to **vdd** and **gnd** respectively. Press ESC if you need to leave the Add wire mode.

8. Verify and save the schematic: *Design > Check and Save*. If any node is floating it will be marked with a blinking cross.

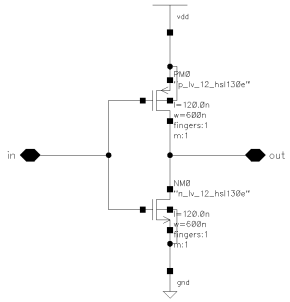

Figure 4: Inverter schematics. Your schematic should look like this.

9. Create a symbolic view for the inverter so it can be used as an instance on a higher level: *Design > Create Cellview > From Cellview ...* in the schematic window. Click *OK*. Change the *Pin Specification* so that your input is located at *left pins* and your output is located at *right pins*. Press **OK**, then save the symbol and close the symbol window.

10. Create a new schematic **inverter_tb** in the library manager. In this schematic you will apply the necessary signals (voltage and current sources) to simulate the inverter. The suffix *tb* stands for *test bench*.

11. In the **inverter_tb** the inverter should be placed as a symbol (*Add > Instance ...*, browse to your inverter symbol). You will also need a power supply and a signal source. They are called **vdc** and **vpulse** in library **analogLib**. A capacitor (**cap**) is used as a load for the inverter. The global power terminals **vdd** and **gnd** are also needed.

12. Connect **vdc** between **vdd** and **gnd**; **vpulse** connects to the inverter input. Place the load capacitor on the output. Your schematic should look something like figure 5.

13. Set the power source (**vdc**) to 1.2 volts (**DC voltage** = 1.2) and the signal source (**vpulse**) like this:

Voltage 1	0
Voltage 2	1.2
Delay time	0
Rise time	10p
Fall time	10p
Pulse width	2.5n
Period	5n

    The capacitor should have the value 30f.

    The different units are set automatically but it is important not to leave a space between the number and the prefix.

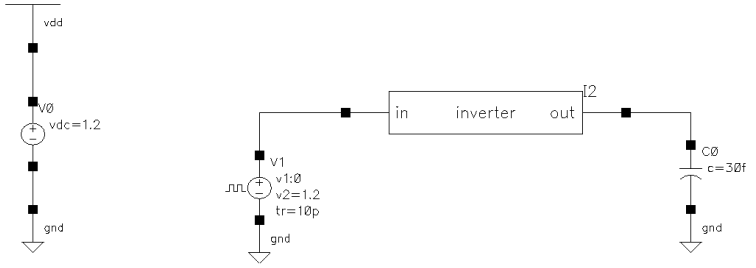

Figure 5: Schematic of the test bench with inverter.

14. Feel free to place a text string on your schematic (*Add* > *Note*) and some labels on the input and output wires (*Add* > *Wire Name*). These labels can then be used during the simulation.

15. *Check and save* the schematic.

Simulations

The function of the inverter can be verified with the help of simulations. You will only check its step response.

1. Start the Analog Environment simulation environment from the **inverter_tb** schematic window (*Tools* > *Analog Environment*).

2. In the Analog Design Environment (ADE) window, make sure that Golden-Gate is your default simulator.

3. Set up for **DC** analysis (*Analyses* > *Choose* ... in the ADE window) by checking 'enabled' in the DC analysis form.

4. Set up for transient analysis (**TR**) (*Analyses* > *Choose* ...) from 0 to 10ns (**Stop Time (s)** = 10n). Set **Max Time Step (s)** = 0.05n.

5. Set up **Probes** for viewing the different signals in the circuit: Press *Vir Probe* in the ADE window,

Probe type	V-meter
Probe name	Vin
Pos. node	*select* (then click the input node in schematic)

Then click *Add*. Do the same for a Probe Vout. The negative node should default be */gnd!*.

6. Start the simulation with the command *Simulation > Netlist and Run* in the ADE window, or by pressing the green traffic light button.

7. Examine the result by choosing *Results > GoldenGate Results > Inverter_tb_TR* . In the Transient Analysis Result window, choose

Plot type	waveform
Probes	Vin
Plot mode	Append

Then click *Plot*. Do the same for Probes = Vout.

8. Zoom in and measure the rise time. Use the markers (*Marker > Crosshair Marker A > Horizontal marker*, put two markers at 10% and 90% of the rise time of the output signal). Check the marker values (*Display Intercept Data* in the marker window), and determine the rise time. Do the same for the fall time.

9. Start the waveform calculator, *Tools > Calculator* ....

10. Analyze the output with the calculator. In the calculator, press *Wave*. Select a curve in the waveform window. Under special functions, select rise time. The settings for rise time should be:

y	0
y	1.2
multiple	

Then click plot. For fall time, reverse the *y* values. Feed the values into the calculator buffer by clicking on the **vt**-button (**vt** stands for voltage transient) and select the wire in the schematic. By selecting **Special Functions** you can measure rise time and fall time for the output. Compare with the results you measured previously.

11. Now change the NMOS transistor size: In the inverter_tb_schematic, select the inverter and choose *Design > Hierarchy > Descend Edit*. Select the NMOS transistor, and change its width to 0.2u (*Edit > Properties > Object*). *Check and save* the inverter, *Design > Hierarchy > Return*, *Check and save* the test bench, and rerun the simulation (*Simulation > Netlist and Run*, or the green traffic light, in the ADE window). Redo the rise- and fall time measurements.

Part 2: The Current Mirror

In this part you will, with the help of simulation, estimate the output resistance of a current mirror. To do this, you will place a voltage source at the output of the current mirror, sweep it between 0V and 1.2V (DC-analysis) and measure the current through it. This is done for different input currents.

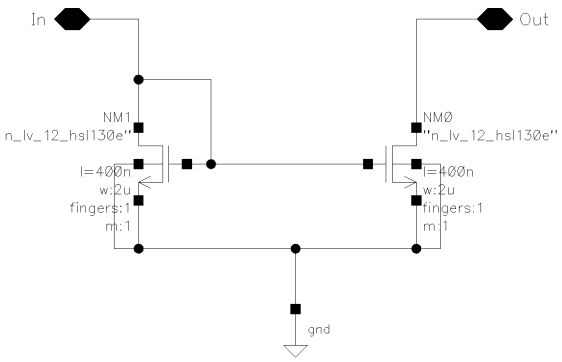

Figure 6: Current Mirror with N-type MOSFETs.

Generate schematic and symbol views:

1. Create a schematic of the current mirror in the same way as for the inverter. A suitable name is *currentmirror*. The transistors should be of n-type and have the size $W/L = 2\mu m/0.4\mu m$. Put pins of *inputOutput* type on the drain nodes of the transistors, as in figure 6.

2. *Check and save* the schematic, and create a symbol view.

3. Create a test bench, *currentmirror_tb*, and add the current mirror as an instance.

4. Add the current source (**idc**), the voltage source (**vdc**) and **gnd**. Connect the current source to the input and make sure that the direction is right, see Fig. 7. The voltage source to be swept is placed between output and ground.

5. Set a variable as value for the current (i.e., **DC current = ibias**) and a numeric value on **DC voltage** of the voltage source, e.g. 1.2V.

Simulate the current mirror:

1. Start Analog Environment.

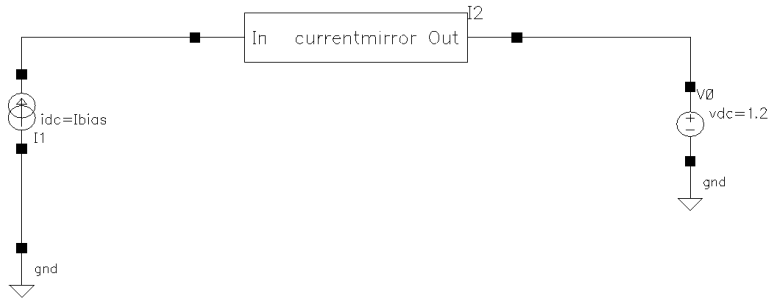

Figure 7: Current Mirror testbench.

2. Add a probe in the ADE window: Click on *Vir probe*, choose *c-meter*, name it Iout, select the output node of the mirror symbol (the red square) and click **Add**.

3. Choose *Variables > Copy From Cellview*, to include the variable **ibias** in the simulator. Set **ibias** to 1m (mA), through *Variables > edit* (or double-click on it). The value does not matter in this case since we are sweeping **ibias**, nevertheless it must be set to a value, see the next two points.

4. Select **> Analyses > Choose**, pick **DC** and click on **Specification Variable**. Write *ibias* as variable, choose the **range** from 20μ to 100μ in linear steps of 20μ. In the Task field choose **sweep**, click on **> Select Device ....** In the new Device Parameters window click **Select**, and then select **vdc** in the schematic. Define the range from 0 to 1.2 in 0.1 volt steps. Click **Add**, and close the window. Finally, click **OK** in the Choose Analyses window.

5. Start the simulation with the command *Simulation > Netlist and Run* in the ADE window, or by pressing the green traffic light button.

6. After the simulation is finished, select **Results > GoldenGate Results > currentmirror_tb_DC** in the ADE window. Select the probe *Iout*, choose *V0_v_p_dc* as the x-axis variable and **Select All** ibias values. Click **Plot**.

7. Now select one curve in the waveform window, and choose **Tools > Calculator ....** How can you measure the output resistance r_o? Plot the conductance

and resistance in the same window by adding subwindows [4]. Repeat for a different *Iout* curve, by adding the relevant curves to the correct subwindow.

Laboratory Report

Compile a report according to the guidelines in the Introduction.

[4]Hint: Use derivative in special functions.

Laboratory 3 : Simulation of an operational amplifier

During this laboratory you will verify that a two-stage operational amplifier is correctly designed. The amplifier is used in the non-inverting configuration shown in fig.8. Capacitors C_1 and C_2 implement a capacitive feedback, typical of SC-circuits; R_1 is used in closed-loop simulations to provide a DC-feedback for the amplifier.

The following data are of interest when simulating the amplifier:

- the bias point
- the loop gain, $T = f_b a(s)$ [5]
- the unity-gain frequency of the loop gain, ω_0 [6]
- the phase margin, ϕ_m
- the closed-loop transfer function, $V_{out}/V_{in} = A(s)$
- the slew rate, *SR*

The bias point is studied with the help of DC-analysis.

$f_b a(s)$, ω_0 and ϕ_m are measured in an open-loop linearized frequency (AC) simulation, with the positive input signal connected to a DC voltage [7] and an AC-voltage source connected to the negative input.

Since in AC simulations only the linearized models of the components at a certain bias point are used, non-linear phenomena like distortion, clipping, and slewing can not be captured with AC simulation. The value of **AC magnitude** in the AC source definition only works as a scaling factor.

SR is best measured with a closed-loop transient simulation. A step of 0.5V is applied at the input (pay attention to the DC-level and the vpulse source voltages), and a transient analysis is performed.

Homework

Read through the manual for this laboratory, including the design example, and read relevant sections of the text book or other sources. Work on the schematic as

[5] In this manual f_b is used instead of f as used in the book (e.g. section 8.1). *a(s)* is the open-loop amplifier gain, *A(s)* is the closed-loop gain.

[6] See e.g. fig. 9.9 in the textbook

[7] If the amplifier is supplied with 0V and 1.2V, a signal ground at around 0.6V would be suitable. However, this DC voltage also sets the common node voltage at the drain of Q_5; Thus, it is more suitable to choose V_{DC} = 0.5 V so Q_5 operates in saturation.

much as possible before the lab; This will save you time. Answer the questions below:

Twostage Operational Amplifier

1. Give the equation for the gain *A(s)* in a non-inverting feedback amplifier with capacitive feedback (see fig.8), and show that $A(s) = 2$ for $C_1 = C_2$.

2. Draw a schematic of the twostage amplifier, as in fig. 10. Follow the design example and calculate all bias currents and device sizes. Make sure the following specifications are met:

$V_{out}/V_{in} = A(s)$	2 (in-band)
$\omega_{-3dB,CL}$	$2\pi \times 18 \times 10^6$ rad/s
SR	$25\, V/\mu$ s
ϕ_m	$> 60^\circ$

   For the capacitors in the loop and the load, the following specification can be used: $C_L = 2$pF, $C_1 = C_2 = 2$pF. Choose Q_{16} so that the zero introduced by C_C is at infinity, and choose C_C to be 1pF, 2pF, or 3pF. The supply voltage $V_{DD} = 1.2V$.

3. What is the order of magnitude of the input offset voltage, and how does it impact open-loop simulations and measurements?

4. How can the loop gain be measured? Indicate this in fig. 9.

Laboratory Exercises

Twostage Operational Amplifier

1. Create a cell with the necessary views for the twostage amplifier you designed in the homework exercise (fig. 10). Pick the compensation capacitor,

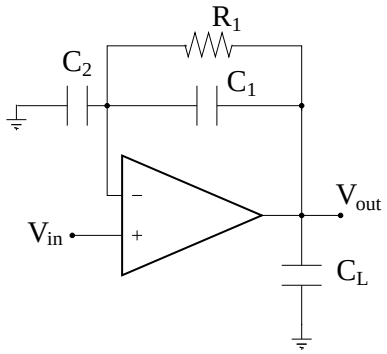

Figure 8: Non-inverting amplifier.

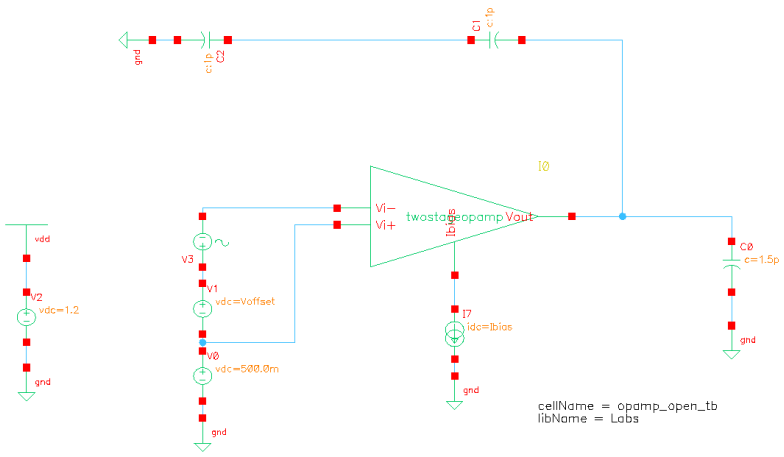

Figure 9: Open loop configuration.

MIMCAPS_MML130E, from the library **umc13mmrf**. For the transistors use **P_12_HSL130E** and **N_12_HSL130E**. For the capacitors C_1, C_2 and C_L capacitors from the library **analogLib** can be used.

2. Prepare for open-loop simulations by building a suitable test bench (fig. 9).

   Start with a DC-analysis to study the bias points and measure the DC-offset voltage of the input of the amplifier. Connect a DC voltage source, **vdc** from AnalogLib, between the inputs and define the DC voltage as variable *Voffset*. Sweep this voltage in a small range until the output reaches 0.5V (see footnote 7):

   Set up for DC analysis (**DC**) (*Analyses* > *Choose* ...). Choose **Task: sweep**, press *Select variable* and choose *Voffset*. Don't forget to select **Enabled**.

   Set up relevant Probes (see Lab 2).

3. Examine the result by choosing *Results* > *GoldenGate Results* > *opamp_open_tb_DC*. In the DC Analysis Result window, choose

Plot type	waveform
Probes	Vout
Plot mode	Append

   Then click *Plot*. The x axis variable should be *Voffset*.

   It may be necessary to perform several sweeps in order to find a precise enough value.

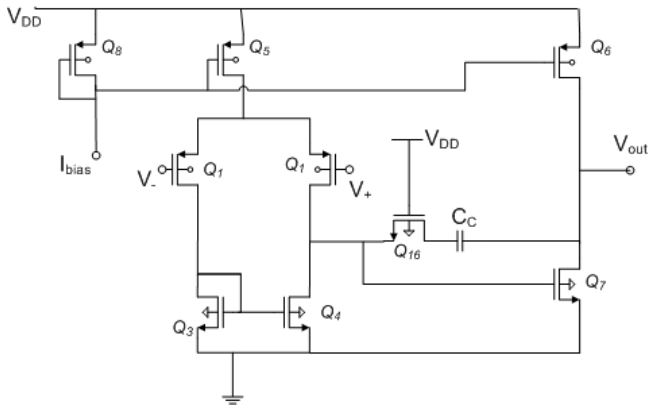

Figure 10: Twostage operational amplifier.

Do the simulated I_5, I_7, $g_{m1,2}$, and g_{m7} match the calculated values? Adjust the dimensions of the transistors if needed.

4. Verify your design by measuring $f_b a(s)$, ω_0 and ϕ_m with an AC measurement. Change your test bench and connect the earlier simulated offset voltage between the inputs. Set *AC Magnitude* to 1V and sweep between 10 Hz and 1 GHz. With the command *Modify* > *Mag* or *Phase* in the AC Analysis Results window you can get a pair of curves from which these data can be extracted.

5. Make a new closed-loop test bench. Close the feedback loop (fig. 11) and find $A(s)$.

6. Now apply a symmetrical 0.5V input step, and check the value of *SR* with a transient analysis. Use *vpulse* from the library *AnalogLib*.

7. Increase and decrease the capacitive load by a factor of 10 and repeat the transient analysis. What happens to the output?

Laboratory Report

Compose a report containing the difference of calculated and simulated values. Include the values of $f_b a(s)$, ω_0, ϕ_m, $A(s)$, and *SR*. The report should also answer the questions in the homework section, and explain the results. Add plots of the interesting curves.

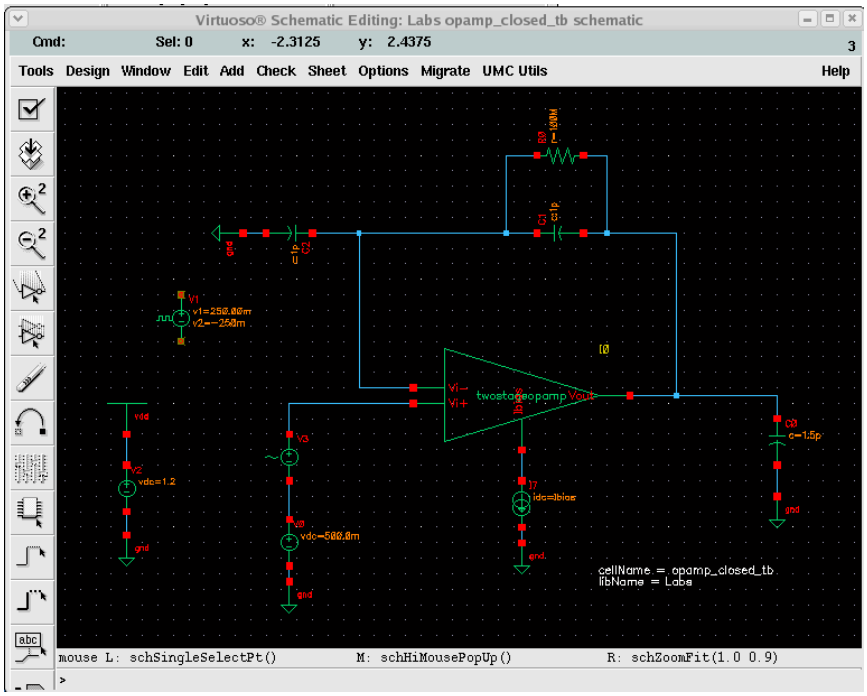

Figure 11: Closed loop configuration.

Laboratory 3: Design example

Below an approach is given to design a two-stage operational amplifier. Besides the text book by Gray, Hurst, Lewis and Meyer ("Analysis and Design of Analog Integrated Circuits"), other useful references are:

- D. A. Johns and K. Martin: "Analog Integrated Circuit Design", John Wiley & Sons, 1997, chapter 5.
- B. Razavi: "Design of Analog CMOS Integrated Circuits", McGraw-Hill, 2001.

Design of a two-stage operational amplifier

For the design example below, the body effect is partly ignored, and it is assumed that $\lambda V_{DS} \ll 1$. Long-channel approximations are used. The specifications for the closed-loop circuit of fig. 12 are the following: [8]

- $A(s) = 2\,(in-band)$
- $\omega_0 = \omega_{-3dB,CL} = 2\pi \cdot 19 \cdot 10^6\, rad/s$
- $SR = 30V/\mu s$
- $\phi_m > 70^\circ$
- $R_1 > 100M\Omega$
- $C_L = 1.5\,pF, C_1 = C_2 = 1pF$

[8] Note: The specifications and resulting values are different from the laboratory assignment.

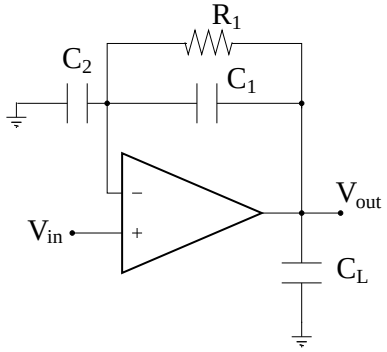

Figure 12: Non-inverting amplifier.

We start by choosing $C_C = 2pF$, which is approximately the same value as the total capacitance between the opamp output and ground.

First, let us look at the current levels in the stages. The slew-rate specifications determine the value of the currents in both the input and output stage: If the first stage is limiting the slew rate, we have

$$SR = I_5/C_C$$

and if the second stage is limiting the slew rate we have

$$SR = I_7/(C_C + C_L + C_1||C_2)$$

.

And thus:

$$I_5 > SRC_C = 30V/\mu s \cdot 2pF = 60\mu A$$
$$I_7 > SR(C_C + C_L + C_1||C_2) = 120\mu A$$

Second, the transconductances are determined by bandwidth, gain and phase margin considerations. For a compensated opamp we can use Eq. 9.47 in the text book, combined with the schematic in fig. 10:

$$p_1 = -\frac{1}{g_{m7}R_2R_1C_C}$$
$$p_2 = -\frac{g_{m7}}{C_{gs7} + C_L + C_1||C_2}$$
$$p_3 = -\frac{1}{R_{16}C_{gs7}}$$
$$z = \frac{1}{(\frac{1}{g_{m7}} - R_{16})C_C}$$

In the above equations some parts have been neglected such as transistor parasitic capacitance other than C_{gs}. Resistances R_1 and R_2 are given by:

$$R_1 = r_{o2}||r_{o4}$$
$$R_2 = r_{o6}||r_{o7}$$

and R_{16} is the resistance of Q_{16} in the linear region (eq. 2.53):

$$R_{16} = \frac{L_{16}}{W_{16}} \cdot \frac{1}{k'_n(V_{GS16} - V_t - V_{DS16})}$$

The opamp should be designed so that the open loop -3dB bandwidth is mainly determined by the first pole. The third pole is usually at such high frequencies that it can be neglected, and the zero should be put at infinity by designing Q_{16} right.

The transconductances of the input differential pair, $g_{m1,2}$ are related to the Gain-Bandwidth product (GWB, or unity-gain frequency, see Eq. 9.49) of the open-loop opamp by the equality

$$GBW[Hz] = a_0 f_{p1} = \frac{g_{m1,2}}{C_C}\frac{1}{2\pi}$$

as well as

$$GBW \approx A_0\frac{\omega_0}{2\pi} \approx \frac{1}{f_b}\frac{\omega_0}{2\pi}$$

(combine Fig. 9.2, Eq. 9.47a and Eq. 9.50 in the book). Thus,

$$g_{m1,2} = \frac{\omega_0 C_C}{f_b} = \frac{2\pi \cdot 19 \cdot 10^6 \times 2 \cdot 10^{-12}}{0.5} \approx 480\mu S.$$

Now we can find the dimensions of $Q_{1,2}$:

$$(W/L)_{1,2} \approx \frac{g_{m1,2}^2}{2k_p' I_5/2} = \frac{(480\mu)^2}{2 \cdot 100 \cdot 10^{-6} \cdot 60 \cdot 10^{-6}/2} = 38.$$

This can be rounded off to $(W/L)_{1,2} \approx 40$. The phase margin [9] is impacted by the second pole:

$$\phi_m(\omega_0) = 180 - \arctan\frac{\omega_0}{\omega_{p1}} - \arctan\frac{\omega_0}{\omega_{p2}}$$

Thus, for a phase margin of at least 70 ° we need to place ω_{p2} at least at $3\omega_0$. We can now derive a relation for g_{m7}. Using the above equation for p_2, and assuming that C_{gs7} is in the range of 100fF, we can derive that

$$g_{m7} = 3\omega_0(C_{gs7} + C_L + C_1||C_2) = 3 \cdot 2\pi \cdot 20 \cdot 10^6 \cdot 2.2 \cdot 10^{-12} = 750\,\mu S.$$

We can now find the dimensions of Q_7:

$$(W/L)_7 \approx \frac{g_{m7}^2}{2k_n' I_7} = \frac{(750\mu)^2}{2 \cdot 400 \cdot 10^{-6} \cdot 120cdot10^{-6}} \approx 6.$$

This is quite a small ratio, and we can afford to increase the above ratios (rather arbitrarily), without loading the output of the differential stage too much: $(W/L)_7 = 50$. The new value for g_{m7} becomes $2.2\,mS$. This will also increase the phase margin.

[9] The phase margin is defined as the phase compared to $-180°$ for the frequency ω_0 where the loop gain $|T(j\omega_0)|$ is 1.

Since the mirror-load transistor pair Q_3, Q_4 ideally has the same gate-source voltage as Q_7, we can write the relation (see also Eq. 6.62, 6.63 in the textbook):

$$\frac{(W/L)_7}{(W/L)_{3,4}} = \frac{I_7}{I_5/2},$$

from which it follows that

$$(W/L)_{3,4} = (W/L)_7 \frac{I_5/2}{I_7} = 50 \cdot \frac{30 \cdot 10^{-6}}{120 \cdot 10^{-6}} = 12.5.$$

Q_{16} is working in the linear region, so we easily can implement a resistance of suitable value.[10] Now that we know the dimensions of Q_7, we set

$$R_{on,16}^{-1} = g_{m7}$$

In the linear region, we have [11] (see Eq. 2.53 in the textbook)

$$R_{on,16}^{-1} = k_n'(W/L)_{16}(V_{GS16} - V_{t16}).$$

Note that

$$V_{S16} = V_{G7} = V_{t7} + \sqrt{\frac{2I_7}{k_n'(W/L)_7}} = 0.3 + 0.11 = 0.41V$$

With V_{G16}=1.2 V we get V_{GS16}=0.79 V. Moreover,

$$V_{t16} = V_{t0n} + \gamma(\sqrt{2\phi_{fn} + V_{S16}} - \sqrt{2\phi_{fn}}) = 0.3 + 0.58(\sqrt{0.7 + 0.41} - \sqrt{0.7}) = 0.43V.$$

Thus,

$$(W/L)_{16} = \frac{g_{m7}}{k_n'(V_{GS16} - V_{t16})} = \frac{2.2 \cdot 10^{-3}}{400 \cdot 10^{-6}(0.79 - 0.43} = 15.$$

Finally, the current sources Q_5 and Q_6 can be made so large that they require a small gate overdrive V_{ov}. If we set V_{ov} to $0.14V$, we obtain

$$(W/L)_5 = \frac{2I_5}{k_p'V_{ov}^2} = 60$$

and

$$(W/L)_6 = \frac{2I_7}{k_p'V_{ov}^2} = 120.$$

[10] Alternatively, the zero can be positioned at a finite frequency (i.e., R_{16} is made somewhat larger), in order to increase the phase margin. This is easier to do after simulating the transfer function of the amplifier, since the location of the zero depends on the position of the non-dominant poles/zeros.

[11] V_{DS16} is ignored; We assume a small AC signal.

For convenience we choose $(W/L)_8$ = $(W/L)_5$ and I_{bias}=I_5. As usual, it is good practice to choose transistor lengths and widths (much) larger then the smallest allowed by the process, since in this way we obtain a better match between transistors, and the transistors behave more in accordance with the long-channel approximation. A possible choice is a common length of $0.5\,\mu m$, resulting in the following dimensions:

Transistor	W	L
Q_1	20	0.5
Q_2	20	0.5
Q_3	6	0.5
Q_4	6	0.5
Q_5	30	0.5
Q_6	60	0.5
Q_7	25	0.5
Q_8	30	0.5
Q_{16}	7.5	0.5

Now we can try to estimate the dc-gain of the opamp:

$$a_o = g_{m1,2}(r_{o2}||r_{o4}) \cdot g_{m7}(r_{o6}||r_{o7}).$$

From the book (Eq. 1.163, 1.164 and 1.194) we see that

$$r_o = \frac{dX_d}{dV_{DS}}^{-1} \frac{L_{eff}}{I_D}$$

where the effective transistor length L_{eff} = L - $2L_d$ - $2X_d$.

Thus,

$$r_{o2} = (0.04 \cdot 10^{-6})^{-1} \cdot \frac{0.485 \cdot 10^{-6}}{30 \cdot 10^{-6}} = 404k\Omega$$

$$r_{o4} = (0.08 \cdot 10^{-6})^{-1} \cdot \frac{0.485 \cdot 10^{-6}}{30 \cdot 10^{-6}} = 202k\Omega$$

$$r_{o6} = (0.04 \cdot 10^{-6})^{-1} \cdot \frac{0.485 \cdot 10^{-6}}{120 \cdot 10^{-6}} = 101k\Omega$$

$$r_{o7} = (0.08 \cdot 10^{-6})^{-1} \cdot \frac{0.485 \cdot 10^{-6}}{120 \cdot 10^{-6}} = 51k\Omega$$

and thus

$$a_o = (480 \cdot 10^{-6} \cdot 135 \cdot 10^3)(2.2 \cdot 10^{-3} \cdot 34 \cdot 10^3) \approx 4.8 \cdot 10^3.$$

Laboratory 4 : Layout of a Twostage Amplifier

The tools Layout Editor and Design Rule Checker from Cadence will be introduced in this laboratory. You will draw the layout for the twostage operational amplifier that you designed in the previous laboratory. You will also verify that it complies with all layout rules, and you will compare it (with LVS, *Layout versus Schematic*, through component and connectivity verification) with the schematic view, in order to detect possible differences. Finally, you will extract a netlist containing parasitic capacitances from the layout view, and run a post-layout simulation.

All layers used to create a layout should have the extension *drw*, drawing. For clarity one can use the *pin*-layer for the connection pins and make sure that the area is completely inside the underlying *drw*-layer. Using a special layer for the pins makes them more visible and makes it possible for the system to treat them differently. However, in order for the LVS to work, labels should be added with the right pin names (*Create* > *Label* ... in the layout window). The following layers will be used for the layout[1]:

ME1	Metal 1 Layer
ME2	Metal 2 Layer
ME3	Metal 3 Layer, etc. (until ME8, metal 8)
DIFF	Diffusion Layer
NPLUS	n^+ Implant Layer
PPLUS	p^+ Implant Layer
PO1	Poly 1 Layer
NWEL	n^-well Layer
CONT	Contact (hole) to ME1 from DIFF & PO1
VI1	Contact Layer, ME1 to ME2
VI2	Contact Layer, ME2 to ME3
VI3	Contact Layer, ME3 to ME4, etc, up till VI7

Homework

Read through the manual for this laboratory, and read relevant sections of the text book or other sources. Work on the layout as much as possible before the lab; This will save you time. Answer the questions below:

1. Calculate the size of a MIM-capacitor, assuming the oxide thickness t_{ox} is 350Å = $350 \cdot 10^{-10}$ m. Use $\varepsilon_{ox} = 3.9 \cdot 8.86 \cdot 10^{-12}$ F/m. The total capacitor value must be 2 pF.

[1] More lithographic masks than the layers specified here will be needed for fabrication. This does not pose any problem, since these extra layers will be generated automatically from the drawn layers and components.

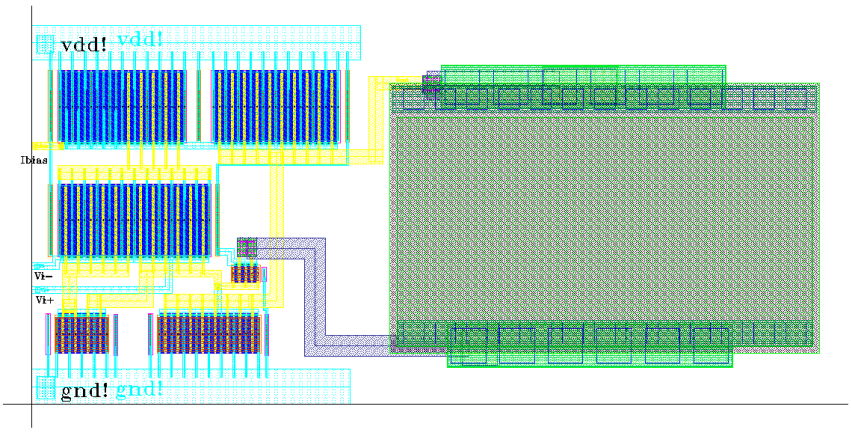

Figure 13: Layout example of a twostage operational amplifier. Remember to add contacts for both the n–well and p–substrate.

2. What is the parasitic capacitance of the bottom plate to substrate, if the bottom plate is formed by metal7 and fringing capacitance can be ignored? Use the technology data sheet.

3. Carefully analyze the layout plot of the amplifier shown in Fig. 13. Identify the components compared to Fig. 10.

Laboratory Exercises

1. Create a layout view for the twostage amplifier (*File* > *New* > *Cellview* ... in the Library Manager), in the same library as the schematic, preferably using the same cell name. The layout editor will start automatically when you set the View Name to *layout*.

   To make all hierarchical levels visible use the command *Options* > *Display* ... **Display levels, Stop** = 20, or toggle between showing all levels or only the top level with **Shift-F** and **Ctrl-F**, respectively.

2. With the help of the layout rules, plan for a compact layout. The layout rules can be found through the website www.es.lth.se/ugradcourses/cadsys/umc130lnx.html [6]. See Fig. 13 for an example of a layout.

3. With the command *Create* > *Instance...* you can import the complete layout for the transistors in the same way that you added the transistor symbol to the schematic. Pick all elements from **umc13mmrf**. For large transistors the number of fingers is often increased, and a maximum finger width may be

defined by the design rules. See the design kit for more information.
If the predefined transistors do not suit your needs, you can always draw one yourself, using rectangles of the appropriate layers, or flattening an existing one and editing it. However, it is not recommended to do this in this laboratory!

4. The capacitor is a so-called MIM-capacitor (metal-insulator-metal) created by overlapping two metal layers. Use **mimcaps_mml130e** from library **umc13mmrf** to include a capacitor with the right capacitance into the layout view. Choose suitable dimensions.

5. Use *Create > Contact...* to make contacts between the layers. They are:

NTAP	contact between n-diffusion and metal1 (n-well)
PTAP	contact between p-diffusion and metal1 (substrate)
M1_POLY	contact between poly and metal1
M2_M1	contact between metal1 and metal2
M3_M2	contact between metal2 and metal3 (.. and so on for the other metal layers)
L2_M8	contact between metal8 and al-2 (for the MIMcap)

6. Use *Create > Path* to draw the connecting wires. Make sure to click the right metal drawing layer in the LSW before choosing this command. Remember to add contacts for the n–well and p–substrate; tied to vdd! and gnd! respectively.

7. Make sure that the pins (*Create > Label...*) are given the same names as in the schematic and that they are drawn in the right metal layer. For the power, use *vdd!* and *gnd!*. The symbol "!" indicates a global node name.

DRC and LVS

Now check the layout with a Design Rule Check, and verify the layout versus the schematic that you designed in laboratory 3.

1. Check that there are no violations of the design rules by running a DRC check: *Assura > Run DRC ....* In the form that appears the *Technology* should be umc130_drc and the *Rules Set* should be ana2009. Select the switches **Skip_Poly_Density_Check** and **Skip_DIFF_Density_Check**.[2] Get detected errors explained through the special tool/window, clicking on the arrows in the right-hand side of the window.

2. If there are DRC errors, change the layout and go through the DRC procedure until your DRC is clean.

[2]This means that the DRC will ignore the fact that the poly or diffusion coverage is too small.

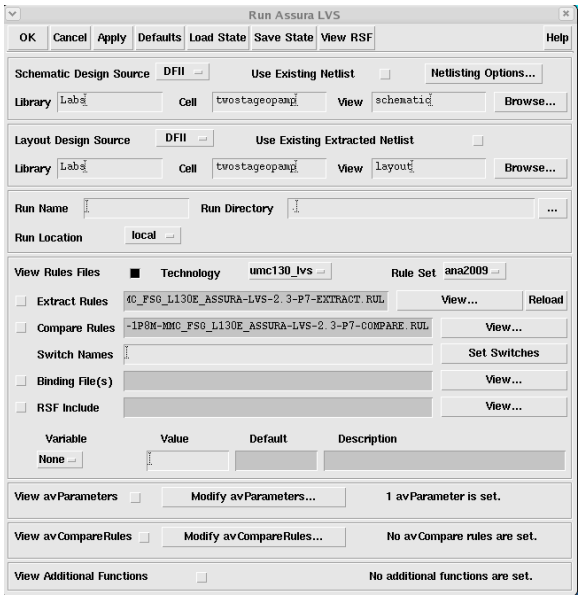

Figure 14: The LVS window.

3. Run an LVS (Layout Versus Schematic) check, in order to verify that the layout view and the schematic view are identical: *Assura > Run LVS ....* In the form that appears the *Technology* should be umc130_lvs and the *Rules Set* should be ana2009. No switches should be set. Check the messages in the tool window (the LVS debug window) to verify that the netlists match.

4. If the netlists match (see Fig 15), and no DRC errors are found, create the **extracted** view: Directly after the LVS (do not close the Assura Run) select *Assura > Run RCX ....* In the RCX window, choose the following:

   In the *Setup* part:

Output	Extracted View

   In the *Extraction* part:

Extraction Type	C only
Cap Coupling Mode	Decoupled
Ref Node	gnd!

   Then click OK. The view *av_extraced* will appear in your Library Manager for the opamp cell.

Simulations

Simulate both the schematic and the layout with parasitic elements, to see if the circuit performance is impacted by the layout.

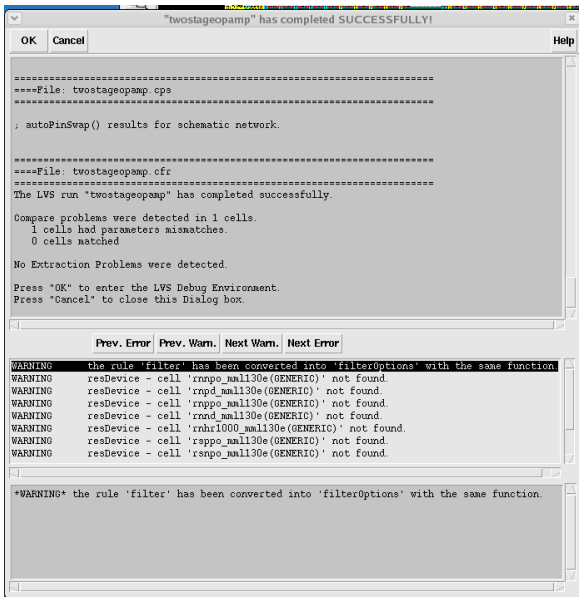

Figure 15: View of a successfull LVS comparison message.

1. In the Library Manager, choose *File* > *New* > *Cellview* ..., and choose the view *config* for your closed-loop opamp test bench (opamp_closed_tb). In the hierarchy editor window (see Fig 16, you must now define your Top Cell as *Labs, opamp_closed_tb, schematic*. Moreover, fill out:

Library List	analogLib umc13mmrf Labs
View List	cmos_sch cmos.sch schematic spectre symbol
Stop list	spectre

2. In the Library Manager, open the *opamp_closed_tb config* view. Click the two yes-checkboxes in the next window to open both the config and the schematic view. Open the simulation tool from the schematic window, and repeat the AC and transient closed-loop simulations. Plot relevant curves.
   Then in the hierarchy editor, change the view of the cell twostageopamp to *av_extracted* by right-clicking in the field 'view to use', and choosing av_extracted in the **Set Cell View** menu that appears. The Hierarchy Browser window should look like the one in Fig 16. Press Update in the top menu!
   Compare the outputs of the amplifier for both simulated views: the closed loop gain ($A(s)$), the AC response, and the transient response to a step signal as in laboratory 3.

Laboratory Report

Compose a report containing the difference of schematic and post-layout values of interest. Submit a plot of the layout, the results from the LVS run, and a plot of

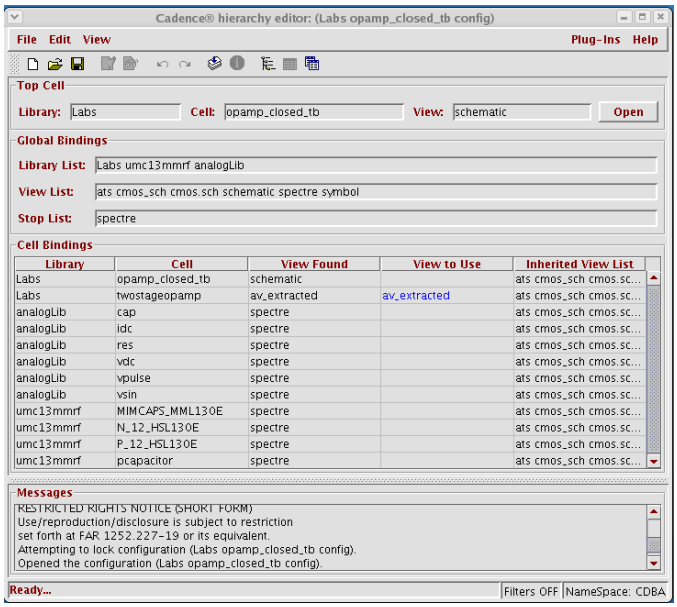

Figure 16: The Config Hierarchy browser window.

the step responses. The report should also answer the questions in the homework section.

References

[1] Gray, Hurst, Lewis and Meyer. *Analysis and Design of Analog Integrated Circuits*, 5^{th} edition. J. Wiley & sons, 2009.

[2] D. A. Johns and K. Martin. *Analog Integrated Circuit Design*. J. Wiley & sons, 1997.

[3] B. Razavi. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, 2001.

[4] *BSIM4 - MOSFET SPICE model.* Department of Electrical Engineering and Computer Science, University of California, Berkeley
http://www-device.eecs.berkeley.edu/ bsim3/bsim4.html

[5] S. Molund. *CAD tools.* Department of Electrical and Information Technology, Lund University 2009.
http://www.es.lth.se/ugradcourses/cadsys/cadtools.html
With links to manuals for GoldenGate, Cadence, etc.

[6] UMC 130 nm manual, design kit and layout rules.
http://www.es.lth.se/ugradcourses/cadsys/umc130lnx.html
Design kit and layout rules.