

Course: EE787 – Memory Design and Testing  
Department of Electrical Engineering  
Indian Institute of Technology, Delhi

Major Test, Winter Semester, Session 2012-2013

Date: 10<sup>th</sup> May, 2013

Max Marks: 40

*All 4 questions are to be answered* Time allowed: 90 mins.

- 1) Following questions are to be answered in brief, preferably in point form. Verbose answers will possibly attract penalty.
- a. What are the main differences between the following two possibilities of embedded DRAM on a logic chip:
    - i. Case 1: Use a trench capable process. (3)
    - ii. Case 2: Use a regular process with poly-caps as storage capacitors.
  - b. You have two memories:
    - Memory A is a DDR SDRAM with 32 bit data bus, an access pattern of 5-1-1-1 (block select – row decode – column decode – burst cycle, burst length restricted to a total of four word accesses), running at a bus frequency of 100 MHz.
    - Memory B is a single port SRAM with 32 bit data bus running at 100MHz.
    - i. What is the maximum data access bandwidth of memory A and B?
    - ii. What access bandwidth do memory A and B provide when you read/write data in blocks of 4 Bytes at a time? <sup>Words</sup> (3)
  - c. What is the maximum memory access bandwidth of a 64bit wide, 200MHz DDR SDRAM with the following access latencies: 3-2-2.5-0.5 (block select – row decode – column decode – burst cycle)? What is the typical memory access bandwidth when a new random address is periodically applied after 4 words read? (3)
  - d. Which RAM-type do you select for
    - i. a network processor with 4GByte of memory?
    - ii. a single-chip search engine with a table size of 1024x1024 bit, access freq. of 300MHz required? (3)
  - e. Fig. 1 shows a wordline driver design. State why you think this design is not acceptable? (3)

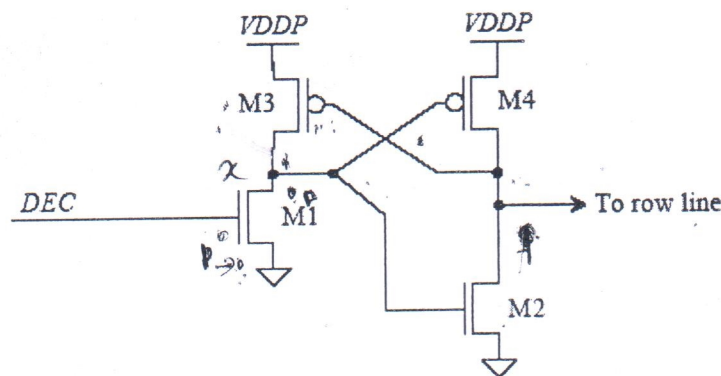


Figure 1