APPENDIX

We propose a solution for the dark-space capacitance at flat bands based on a perturbative approach. The electron wavefunctions at flat bands are given by

$$\phi_n^0 = \sqrt{\frac{2}{L}} \sin\left(\frac{n\pi x}{L}\right) \tag{11}$$

where a fictitious box of length L is considered. The energy levels are the usual $E_n^0 = h^2 n^2/8mL^2$. We now consider that the perturbation introduced by the small signal can be described as a shallow triangular well extending over a distance a, much smaller than L, i.e.,

$$U = \begin{cases} q\Delta V \frac{x-a}{a}, & x < a \\ 0, & x > a \end{cases}. \tag{12}$$

Straightforward perturbation analysis leads then to the expression for the new energy levels

$$E_n - E_n^0 = -\Delta E_n = -\langle \phi_n | U | \phi_n \rangle \approx -q\Delta V \frac{\pi^2 a^3 n^2}{6L^3} \tag{13}$$

where the approximation is valid for a much smaller than the peak of the highest populated wavefunction. This means that this approach is only concerned with the region very close to the semiconductor interface, i.e., it does not consider the re-arrangement of the charge over the classical screening length. The resulting capacitance is then relative only to the dark-space contribution.

From (13), the total semiconductor charge is given by an integration over the bidimensional density of states as

$$Q_s = \sum_n \frac{qm}{\pi\hbar^2} k_B T \ln\left[1 + \exp\left(\frac{E_F - E_n^0 + \Delta E_n}{k_B T}\right)\right]. \tag{14}$$

For a small signal, the varying component of the charge ΔQ can be obtained from a series expansion as

$$\Delta Q = \sum_n \frac{qm}{\pi\hbar^2} k_B T \frac{1}{1 + \exp\left(\frac{E_n^0 - E_F}{k_B T}\right)} \frac{\Delta E_n}{k_B T} \tag{15}$$

which, transforming the discrete sum into a continuous integral (justified when $L \to \infty$), returns

$$\Delta Q = \Delta V \frac{q^2 m a^3 N_D}{6\hbar^2} \tag{16}$$

which is correctly independent of L. At this point, we can note that the perturbation (12) modulates the charge over a distance a. The capacitance can then be written as $C = \epsilon/a$, which finally gives

$$a^4 = \frac{6\hbar^2 \epsilon}{m N_D q^2}. \tag{17}$$

Note that this expression is equivalent to (9) apart from a slight difference in the numerical factor.

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A New Low-Loss Lateral Trench Sidewall Schottky (LTSS) Rectifier on SOI With High and Sharp Breakdown Voltage

M. Jagadesh Kumar and Yashvir Singh

***Abstract*—In this paper, we report a new lateral trench sidewall schottky (LTSS) rectifier on SOI utilizing the sidewall Schottky barrier contact of a trench filled with a metal. Using a two-dimensional (2-D) device simulator (MEDICI), the performance of the proposed device is evaluated in detail by comparing its characteristics with that of the compatible lateral conventional Schottky (LCS) rectifier. Based on our simulation results, we demonstrate that the proposed device provides double the breakdown voltage with reduced reverse leakage current as compared to the LCS rectifier. The forward voltage drop of a 60 V LTSS rectifier is as low as 0.28 V at a current density 100 A/cm^2. An important feature of the proposed Schottky structure is that its reverse breakdown is very sharp similar to that of a PiN diode. Furthermore, at higher operating temperatures, the power losses in the LTSS rectifier are found to be significantly lower as compared to the LCS rectifier.**

***Index Terms*—Barrier lowering, breakdown voltage, lateral Schottky, numerical simulation, silicon-on-insulator (SOI).**

I. INTRODUCTION

In many applications, such as switching mode power supplies for integrated circuits, it is desirable to have a Schottky rectifier with very low forward voltage drop and small reverse leakage current to reduce the power dissipated by the rectifier. In the past, only a few studies have been reported [1]–[3] on vertical Schottky rectifiers with highly doped (e.g., 10^{17} cm^{-3}) epitaxial layers to achieve low forward voltage drop and reduced reverse leakage current by suppressing the barrier lowering effect. In both the trenched junction barrier Schottky (JBS) [1] and the trench MOS barrier Schottky (TMBS) [2] rectifiers, the breakdown voltage capability is limited due to the high value of peak electric field occurring at the bottom corner of the trench. In the case of graded doped trench MOS barrier Schottky (GD-TMBS) rectifier [3], the reverse blocking capability is improved by employing a nonuniform doping in the drift region. Although, the GD-TMBS rectifier is demonstrated to have a low forward voltage drop (e.g., the simulated forward voltage drop of a 60 V GD-TMBS rectifier is 0.37 V at a current density of 180 A/cm^2), the difficulty in realizing the deep trenches with a small mesa width for higher breakdown voltages and the need for nonuniform doping in the drift region may limit the device designer's choice for power ICs. However, lateral power devices are increasingly becoming important because they can be easily integrated in power ICs [4], [5]. An interesting question which so far has not received any serious attention in literature is the study of a lateral Schottky structure on

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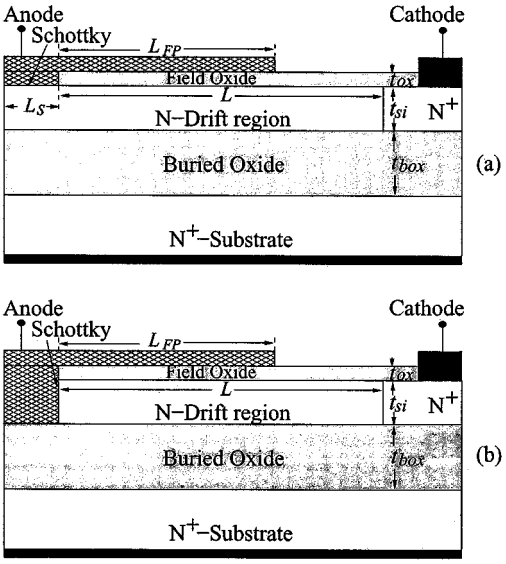

Fig. 1. Schematic cross-sectional view of the (a) LCS and (b) LTSS rectifiers.

SOI using a sidewall Schottky contact. To the best of our knowledge, such a lateral structure has neither been reported nor studied in detail in the literature.

The objective of the present work is therefore to study for the first time, a lateral trench sidewall schottky (LTSS) rectifier utilizing the sidewall Schottky contact of a trench filled with a metal on highly doped SOI epitaxial layers. Using a two-dimensional (2-D) device simulator (MEDICI) [6], the performance of the proposed device is evaluated and compared with that of the compatible lateral conventional Schottky (LCS) rectifier. Based on our simulation results, we demonstrate that for an epitaxial layer doping of 5×10^{16} cm^{-3}, as large as 60 V breakdown voltage with low reverse leakage current and PiN diode-like sharp reverse breakdown can be achieved using the proposed Schottky structure. The proposed structure closely resembles one half of the GD-TMBS rectifier but can be realized easily without the technological difficulties of producing deep trenches with small mesa width.

II. Device Structure and Parameters

The schematic cross-sectional views of the LCS and LTSS rectifiers implemented in MEDICI are shown in Fig. 1. In the LCS structure, the anode is a planar surface Schottky barrier contact whereas in the case of the LTSS structure, the sidewall contact of the trench filled with a metal is utilized to make the Schottky barrier anode. In both the structures, the cathode is an ohmic contact taken from the N^+ region and is at the same potential as the N^+-substrate. A simple metal field-plate termination is used to reduce the electric field crowding at the Schottky contact. Nickel (Ni) is employed for the Schottky barrier (0.57 V) contact [7]. The optimized device parameters used in the simulation for both the LCS and LTSS rectifiers are given in Table I.

TABLE I
MEDICI Input Parameters for the LCS and LTSS Rectifiers

Parameter	Value
N^+ doping for ohmic contact	10^{20} cm^{-3}
Drift region doping, N_D	$2 - 8\text{x}10^{16}$ cm^{-3}
Drift region length, L	2.5 – 5.0 μm
Field–plate length, L_{FP}	2.0 – 4.0 μm
Field oxide thickness, t_{ox}	0.1 – 0.6 μm
Silicon film thickness, t_{si}	0.5 μm
Buried oxide thickness, t_{box}	2.0 μm
Schottky contact length, L_S	0.5 μm
Schottky barrier height (Ni), ϕ_B	0.57 V
Barrier height lowering coefficient	$2\text{x}10^{-7}$ cm

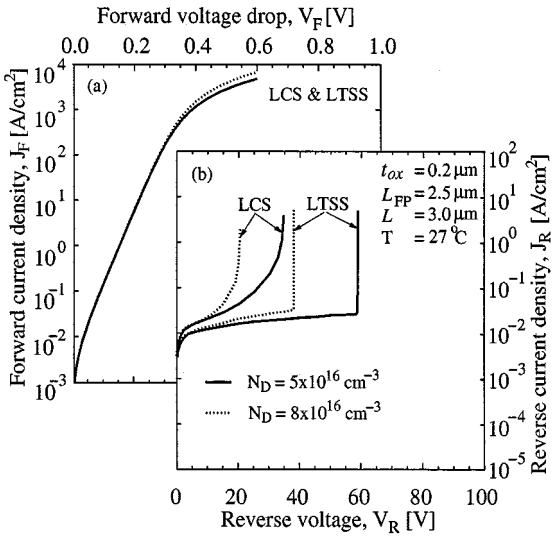

Fig. 2. (a) Forward conduction (b) reverse blocking characteristics of the LCS and LTSS rectifiers.

III. Simulation Results and Discussion

A. I–V Characteristics

Fig. 2 shows the simulated current–voltage characteristics of the LCS and LTSS rectifiers. While both the rectifiers show an identical low forward voltage drop (e.g., 0.28 and 0.31 V at 100 and 200 A/cm^2 respectively), the reverse leakage current of the LCS rectifier increases very rapidly with increasing reverse bias resulting in a relatively low and soft breakdown voltage. On the other hand, the LTSS rectifier has a sharp breakdown similar to that of a PiN diode and gives an improvement of over 1.6 to 1.9 times in breakdown voltage with reduced reverse leakage current as compared to the LCS rectifier.

This significant improvement in the reverse characteristics can be understood by estimating the maximum barrier lowering at the Schottky contact [7], [8] as a function of reverse bias as shown in Fig. 3 for both the LCS and LTSS rectifiers. For the LCS rectifier, the barrier lowering increases very fast with increasing reverse bias causing a rapid increase in the reverse leakage current which results in a soft breakdown characteristic. On the other hand, in the case of the LTSS structure, the reduced barrier lowering suppresses the reverse leakage current and hence eliminates the premature breakdown of the device.

Barrier lowering is strongly influenced by the electric field. Fig. 4 shows the electric field variation along the horizontal line at the field-oxide/silicon interface near breakdown for the LCS and LTSS rectifiers. We observe that for the LCS structure, the presence of a large peak electric field at the Schottky contact results in a significant reverse leakage current due to an increased barrier lowering effect. This gives rise to a low and soft breakdown voltage. Whereas, in the case of the LTSS rectifier, the electric field at the Schottky contact is 54% lower as compared to the LCS rectifier. The lower electric field suppresses the barrier lowering effect leading to a reduced reverse leakage

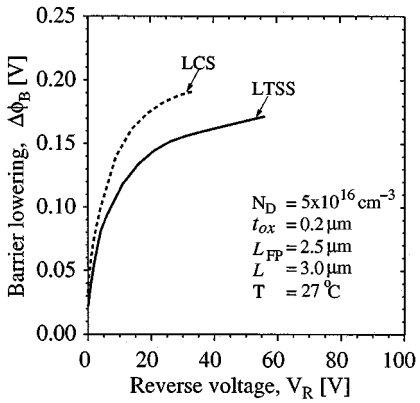

Fig. 3. Barrier lowering as a function of reverse bias voltage for the LCS and LTSS rectifiers.

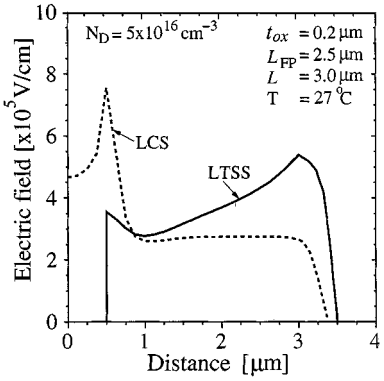

Fig. 4. Electric field variation along the horizontal line at the field-oxide/silicon interface near breakdown voltage of the LCS and LTSS rectifiers.

current. Moreover, in the LTSS structure, the peak electric field occurs at the end of the field-plate (away from the Schottky contact). This makes the device to breakdown at the end of the field-plate resulting in a higher and sharp breakdown voltage.

B. Effect of Drift Region Doping on Device Performance

Fig. 5(a) shows the breakdown voltage as a function of drift region doping for the LCS and LTSS rectifiers. In the given range of drift region doping, the LTSS structure provides an improvement of over 1.4 to 1.9 times in breakdown voltage as compared to the LCS rectifier. As shown in Fig. 5(b), while the forward voltage drop increases only marginally for both the rectifiers from 0.28 V to 0.295 V even when the drift region doping is varied by a wide range, the reverse leakage current for the LCS structure rises very rapidly with increasing drift region doping as shown in Fig. 5(c). On the other hand, the proposed LTSS rectifier exhibits only a marginal increase in the reverse leakage current due to the suppressed barrier lowering at the Schottky contact. This remarkable improvement in the current–voltage characteristics of the proposed device leads to a reduction in power losses as discussed below.

C. Effect of Temperature on Power Dissipation

The maximum static power dissipated (P_D) by a rectifier during the ON and OFF-state per unit area for a 50% duty cycle is given as

$$P_D = \tfrac{1}{2}\,[J_F V_F + J_R V_R]. \tag{1}$$

The power loss calculated using the above equation as a function of temperature is shown in Fig. 6 for the LCS and LTSS rectifiers. It can be

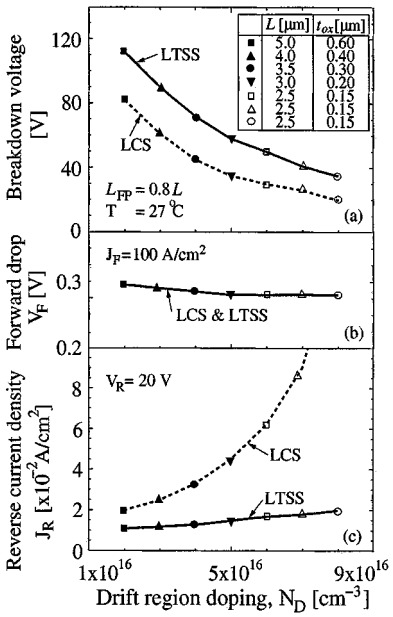

Fig. 5. Effect of variation in drift region doping on (a) breakdown voltage, (b) forward voltage drop, and (c) reverse leakage current for the LCS and LTSS rectifiers.

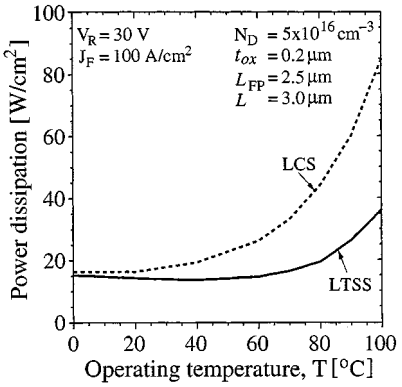

Fig. 6. Power dissipation as a function of temperature for the LCS and LTSS rectifiers.

seen that for low temperatures, the power losses in both the rectifiers are approximately equal because both the devices have identical forward voltage drop which dominates the power losses at these temperatures. At higher temperatures, the reverse leakage current of LCS rectifier dominates the power loss and results in an increased power dissipation with temperature. However, for high temperatures, the power losses in the LTSS rectifier are much lower as compared to the conventional device. For example, even at 80 °C, the power loss in the LTSS rectifier is less than half that of the LCS rectifier.

IV. Conclusions

A novel LTSS rectifier on SOI has been presented. Using 2-D simulation, we have demonstrated that the proposed device provides an improvement of up to 1.9 times in breakdown voltage with reduced reverse leakage current as compared to the LCS rectifier. The forward voltage drop of a 60 V LTSS rectifier is as low as 0.28 V at a current density of 100 A/cm^2. Unlike in the conventional Schottky rectifiers, the reverse breakdown of the proposed Schottky structure is found to be very sharp similar to that of a PiN diode. The ability to produce the proposed LTSS rectifier without the need for deep trenches with small

mesa width makes this device more attractive in applications such as power supplies for integrated circuits requiring low forward voltage drop, excellent reverse blocking capability and low power dissipation.

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Improvement of Polycrystalline Silicon Thin Film Transistor Using Oxygen Plasma Pretreatment Before Laser Crystallization

Kook Chul Moon, Jae-Hoon Lee, and Min-Koo Han

***Abstract*—The device characteristics of the excimer laser recrystallized low temperature poly-Si (polycrystalline silicon) thin-film transistor (TFT) has been improved by employing an oxygen plasma pretreatment on the active amorphous silicon layer prior to the laser crystallization. The oxygen plasma pretreatment has reduced the number of interface traps and increased the field effective mobility in the polysilicon TFT. The device stability of the oxygen plasma pretreated TFTs under the dc stress has been improved due to strong Si–O bond formation during the laser recrystallization.**

***Index Terms*—Interface, laser crystallization, oxygen plasma, Poly-Si TFT.**

I. INTRODUCTION

Polycrystalline silicon thin film transistors (poly-Si TFTs) may be promising devices for various applications such as active matrix liquid crystal displays (AMLCDs) and active matrix organic light-emitting diodes (AMOLEDs). Silicon oxide (SiOx) films prepared by plasma enhanced chemical vapor deposition (PECVD) are widely used as a gate insulator in low temperature polycrystalline silicon (LTPS) thin film transistor [1]. The breakdown filed of low temperature PECVD oxide film is larger than 6 MV/cm [1], [2]. However, the interface trap density of the PECVD silicon oxide films is rather poor (greater than $10^{11}/\text{cm}^2\text{eV}$), while the conventional thermal oxide, of which the typical process temperature is 1000 °C, is about $10^{10}/\text{cm}^2\text{eV}$. It is well known that high quality oxide films for a gate insulator are critical in order to improve a characteristic of TFT [3]. The poor interface property of the low temperature PECVD oxide film may be attributed to both dangling bonds and weak Si–O bonds at the interface [4], [5].

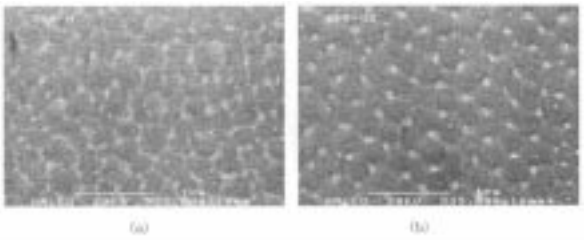

Fig. 1. SEM images of poly-Si (energy density: 380 mJ/cm^2). (a) Nontreated sample. (b) Oxygen plasma pretreated sample.

In this brief, we propose a simple modified thermal oxidation process employing an oxygen plasma pretreatment in order to reduce weak Si–O bonds as well as dangling bonds. Our experimental results show that oxygen plasma pretreatment induces a very thin (about 30 Å) oxide film on the top surface of active silicon prior to the laser recrystallization of which the interface quality is comparable to that of a thermal oxide. We have fabricated LTPS TFTs employing the proposed oxygen plasma pretreatment prior to excimer laser annealing (ELA) and investigated device characteristics of the TFTs. The device characteristics of the proposed TFTs have been considerably improved due to strong Si–O bonds formation in the interface during ELA.

II. DEVICE FABRICATION

A top gate n-channel MOSFET was fabricated on Corning 1737 glass. The fabrication was carried out as follows. A 2000 Å thick silicon oxide film as a buffer oxide was deposited on a glass substrate by PECVD and a 500 Å thick amorphous silicon (a-Si) as a precursor for an ELA was deposited by low pressure chemical vapor deposition (LPCVD) at 450 °C. The a-Si was oxidized in a PECVD chamber for 1 min. The condition of oxygen plasma treatment were RF power density of 0.018 W/cm^2, temperature of 300 °C and 3500 sccm of oxygen flow. The a-Si film was subsequently crystallized by a typical XeCl excimer laser ($\lambda = 308$ nm) annealing in a vacuum chamber. The average grain size of the polycrystalline silicon (poly-Si) film was found to be approximately 0.5 μm. A 1000 Å silicon oxide as a gate insulator was deposited by tetra-ethyl-ortho-silicate (TEOS) in PECVD chamber. The Cr/Al double layer was deposited for the gate electrode and self-align doping mask. The Cr and Al layer could be selectively etched due to a large etching selectivity. A rather long etching time for Al layer was employed to define the 1.1 μm length of the lightly doped drain (LDD) region. Consequently, the upper Cr layer successfully acted as a mask for the LDD. The source and drain regions were doped using an ion shower with PH_3 diluted in H_2. The LDD region was doped by an ion shower after removing the Cr layer. The remained Al layer was utilized for a gate electrode. The impurities in the source, drain and LDD region were activated by an excimer laser annealing. Finally, thermal treatment was performed for the TFT alloy at 400 °C for 30 min in a N_2 ambient. No post treatment such as hydrogenation was employed. We have also fabricated conventional LTPS TFTs (without oxygen plasma pretreatment) for a comparison.

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