UMC 65nm FAQ

G-01-LOGIC_MIXED_MODE65N-LL_LOW_K
G-01-LOGIC_MIXED_MODE65N-SP_LOW_K

UMC FAQ

What is the relationship between UMC and imecICLink ?

ImecICLink is a partner to offer companies, universities and research institutes access to UMC's technologies for prototyping and small volumes through its EUROPRACTICE service

UMC and imecICLink agreed that initial (startup) and small volume customers can be served by imecICLink through the EUROPRACTICE service. Under this agreement customers can get access to the technical documentation of UMC's technologies (0.18um, 0.13um, 90nm, 65nm), access to the MPW runs in these technologies and access to small volumes (up to 1000 wafers per month). Due to UMC's organization and core business it is impossible for them to directly serve small requests.

UMC FAQ
How can I contact UMC for (technical) questions ?

You should NOT contact UMC directly! Probably, your questions will be redirected to imecICLink anyway. UMC can't spend the resources to support universities and startups directly and teamed up with Imec to guarantee first class support to exactly this target group.

Please contact epumc@imec.be if for (technical) questions.

UMC FAQ

Can we access other than MPW technologies ?

Yes, basically all UMC technologies are available, however typically only for fabrication with a dedicated maskset. UMC has more than 200 technology flavors in their portfolio – see also http://www.umc.com/ – but only a few selected technologies are available for MPW prototyping.

Please contact epumc@imec.be if for more information.

UMC FAQ
Can we get wafers from MPW runs ?

No, it is not possible to get wafers from MPW runs.

The reason is that the maskset contains IP from many other customers. For confidentiality reasons, only bare dies are delivered. Wafer-sawing is done at UMCs subcontractor, so we do not have access to wafers either.

UMC FAQ

How many dies can we expect from our MPW/mini@sic participation ?

- **MPW**: We guarantee 40 bare dies, although you will typically receive 60 dies. This depends on the reticle/frame composition and sawing diagram.
- **mini@sic:** We guarantee 20 bare dies, although you will typically receive 30 or 60 dies. This depends on the reticle/frame composition and sawing diagram.

Please contact epumc@imec.be if you need more dies.

UMC FAQ

How can I obtain more than the standard number of dies from an MPW participation ?

Several possibilities exist:

1. If your die is small, and has the correct shape, we can insert it 2x in the applied block. This will add extra dicing cost, which will be charged - typically 1000 €. This would double the amount of dies you can get.
2. From the start you can buy an extra wafer. Cost is to be quoted per case and depends on technology, but typically waferprice is between 1500 € and 5000 €. One MPW wafer yields about 30 dies. Note that this is not standard, it is an extra service offered by imecICLink. UMC may change their policies at any time, which could disable this capability.

3. One could reserve 2 seats (price doubles, number of dies doubles).
4. One could run a minimum batch of 12 wafers with the existing MPW/shuttle maskset. Cost will be dicing cost and 12 x waferprice. You will get around 360 bare dies.
5. One could order an engineering run with dedicated maskset (typically 12 wafers started). Depending on size of your circuit, your circuit is repeated an order of magnitude more on each wafer – eq.: >> 2000 circuits (25sqmm) on a 8" wafer.

Please contact epumc@imec.be if for more information.

UMC FAQ

Do we always get the number of packaged samples as requested ?

Because of packaging-yield, it is possible that you will get less packaged samples than requested. This risk is on the customer's account. Our assembly subcontractors will try to accomplish most of our/your request(s), but cannot give any guarantee. Especially assembly with long bondwires and small pad-pitch is a risk.

Example: If a request for 10 assembled samples results in only 8 completely good IC's, all 10 will be charged.

UMC FAQ
What is an engineering run ?

After MPW prototyping to prove the concept, customers typically engage for an engineering (pilot) run. An engineering run is mandatory before a customer can start volume production. The main importance of the engineering run is the verification of the masks. UMC uses this to fit the technology to your specific circuit, requirements - for example adjust etching receipt to specific metal density.

An engineering run consist of:

- A dedicated maskset for your product.
- 12 wafers started, of which 6 wafers guaranteed to pass WAT criteria.

It is possible to put wafers on hold at a certain processing stage, and run corner wafers.

UMC FAQ
How can I participate on a MPW/mini@sic?

To participate on a MPW/mini@sic, you must perform an **online registration** on following URL:

http://www.europracticeic.com/prototyping_design_registration.php

The reticle is filled up in order of registration, so please register as soon as possible, preferably > 1 month in advance.

If desired, you can sent a Purchase Order (PO) also, although not strictly needed for us.

On our deadline, we expect a final DRC-error-free gds-file. There is some limited time between our deadline and start of maskmaking, so an iteration might be possible, however you should not rely on this.

UMC FAQ

Why is the UMC deadline different from the imecICLink deadline ?

We collect circuits and do framebuild for several customers, before the data is sent for fabrication. To give an idea, on a typical 0.18um mini@sic run, we have >> 30 circuits.

On all circuits we do an extensive incoming inspection:

- Layer integrity.
- Library replacement.
- DRC.
- Antenna rule check.
- ERC (Electrical Rule Check).
- SUB (Substrate Check).
- Visual check.

As a result of these checks - in most cases - modifications are needed.

UMC FAQ
What happens if we miss the deadline ?

If you are unable to send a final layout (gds-file) before the deadline, you should contact epumc@imec.be ASAP to discuss possibilities. Depending on the design and circumstances, we might extend the deadline for a few days, however you should not rely on this.

Cancellations in a later stage are subject to UMC penalties.

If it is decided that you can NOT continue with the design for this particular run, the application will be removed from the run. As a result of this, you will be added to the waiting list for the next similar MPW run.

UMC FAQ
How should I transfer my final gds-file ?

We strongly recommend to compress your gds-file - with for example gzip xxx.gds.

Transfer depends on the filesize.

1. filesize < 5Mb: transfer with @mail to epumc@imec.be.

2. filesize > 5Mb: transfer with FTP. Please contact epumc@imec.be to get FTP details.

If security is of any concern, you can encrypt with symmetric pgp (pgp –c xxx.gds), or gpg/pgp with private/public key. Details on request.

UMC FAQ

Are there any differences between our DRC rulesfile and the sign-off DRC rulesfile used by imecICLink ?

Yes, based on past tapeout experience, we added some extra checks in our Calibre DRC rulesfile.

Extra checks are related to:

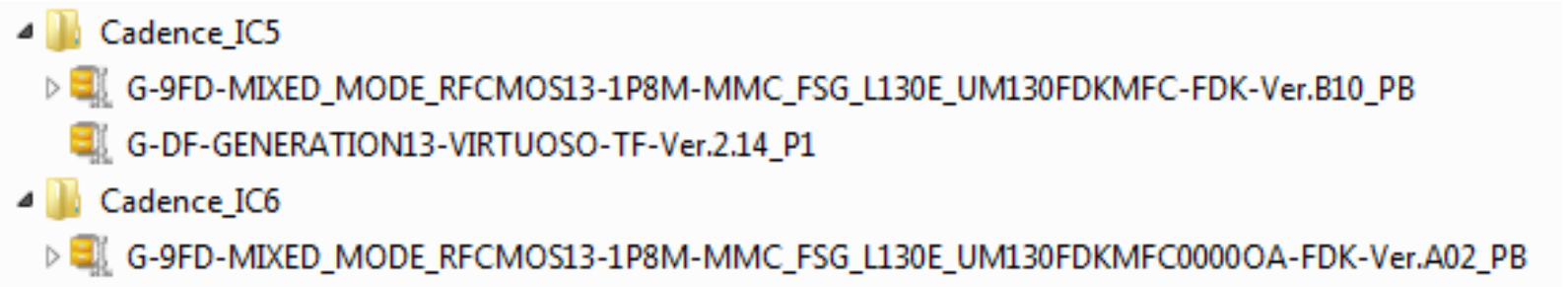
1. Offgrid
2. Metal density
3. Bondpads

Please contact epumc@imec.be for details.

UMC FAQ
Is a designkit for Cadence IC6 available ?

For most UMC technologies, a designkit for both Cadence IC5 (dfwII) and IC6 (Open-Access) is available.

For example for UMC 0.13um MM/RF:



UMC FAQ
What is the thickness of my dies ?

The die thickness depends on wafer-size:

- **8”** wafers -> **29 mil** (approx. 736um)

- **12”** wafers -> **30.5 mil** (approx. 775um)

For MPW there is a possibility to backgrind to **11mil** (approx. 279um) +/-1mil. By default, we backgrind to 11mil, unless you ask us not to do so. Backgrinding is done on wafer-level, and is not possible on die-level. This “11 mil” is chosen carefully, as it fits in the cavity of most plastic packages.

A different thickness is technically possible, but can only be done on an extra wafer.

UMC FAQ
What is the pwell-blockage ?

Most UMC technologies are twin-well – with optional triple-well.

- Nwell – Drawn layer. N-doped.

- Pwell – Generated layer (inverse of Nwell). P-doped.

- Twell – Drawn inside Nwell to create an isolated P-doped area.

Layer "pwell-blockage" blocks the generation of Pwell.

The "masktooling" document describes which layer(s) can be used for pwell-blockage. This is different for every technology. See for example:

P_WELL	91	P_WELL_ONMASK = (((N_WELL_ONMASK OR T_WELL) OR P_WELL_BLOCK) OR NATIVE) OR IND $VARIABLE_START N_WELL_ONMASK = generated by TRO1 T_WELL = a customized_data provided at tape out by customer P_WELL_BLOCK = a customized_data provided at tape out by customer IND = a customized_data provided at tape out by customer NATIVE = a customized_data provided at tape out by customer $VARIABLE_END

UMC FAQ
What is the dummy-blockage ?

For most UMC technologies, a dummy pattern - for diffusion, poly and metals - is generated during maskmaking, to improve planarity during processing. With a "dummy-blockage" layer, this dummy pattern generation is blocked. Please check the layertable for which layer(s) to use.

The dummy pattern (chessboard) is added at a safe distance of existing diffusion/poly/metal structures. For sensitive applications however, this could affect performance or harm matching of the circuit. For example in a sensor, dummy blockage should be added on the pixel.

If a user decides to use dummy-blockage then it becomes his responsibility to fulfill the density rules.

UMC FAQ
Common problem with Calibre (DRC,...) rulefiles?

A common problem with the Calibre (DRC,...) rulefiles is that links to certain files are incorrectly defined in the "INCLUDE" statement.

For example:
INCLUDE ./130nm_layers_v3.6.cal
INCLUDE ./memory_rules_v5.cal

This should be changed to the full path. Typically - when you install the Cadence designkit - the rulefiles are located in the directory <path-to-installation>/Designkit/Ruledecks/Calibre.

UMC FAQ
Calibre (XRC) extraction fails with the error "undefined layer name parameter" ?

It is a common mistake that customers use the ".tec" file as rulesfile. You should run LPE with the LVS rulesfile. In this LVS rulesfile you specify that you want to do LPE (= PEX).

Step 1: modify your LVS ".txt" rulesfile : uncomment the following text and specify the LPE ".tec" rulesfile.

DEFINE PEXRUN
INCLUDE "./RuleDecks/Calibre/LPE/xxx.tec" (or similar version)

Step 2: run LPE
When the LPE window asks for the rule file you need to give the path to the LVS ".txt" rulesfile

UMC FAQ
What is the "antenna" effect ?

A nice and comprehensive explanation can be found on Wikipedia.

http://en.wikipedia.org/wiki/Antenna_effect

It is a common mistake that customers forgot to run an antenna check. This antenna rulefile can be found in the Calibre DRC package.

UMC FAQ
Are DRC violations allowed ?

As a general rule, **design rule check (DRC) violations are not allowed**. The complete circuit - including logos, special structures, polygon-text, ... - must be DRC-error-free. If you suspect there is a false error you should contact epumc@imec.be.

Some rules, related to die-corner, bondpads, assembly/packaging, density,... can be waived for MPW prototyping. A list of "false" errors does not exist however, as this strongly depend on circumstances and the design itself.

UMC FAQ
Which checks should I do before tapeout ?

At least, a DRC and antenna check should be done, prior to sending your gds-file to imecICink. This to make sure your design can be manufactured. This does not guarantee in any way that your design is functionally correct.

DRC. Please be aware that UMC rulesfiles are templates. Appropriate switches should be set according to the exact process flow (For example: IO-voltage, MMC value, metal-stack, topmetal thickness,...).

Antenna check. A separate antenna rulefile is included in the DRC package.

The designer is fully responsible for functionality of the circuit. It is assumed that the appropriate simulations and checks have been done by yourselves. imecICink can and will NOT perform LVS, simulation,... for you, unless clearly agreed otherwise.

UMC FAQ
Are there recommendations for storage of dies/wafers ?

If dies/wafers are not stored properly, assembly might become impossible. It is advised to store dies/wafers in their **original vacuum sealed anti-static plastic bag** or in a **nitrogen cabinet**, to avoid degradation (oxidation, dirt,...) of the bondpads. UMCs guideline is to assemble wafers within **7 days** after opening of their original bags. If these guidelines are not followed, it can not be guaranteed that assembly is possible.

Note: Especially for assembly of bare dies, several months after initial delivery, we often see problems due to wrong storage.

UMC FAQ
Is bumping for flip-chip possible on MPW ?

Yes, this is certainly possible. Some remarks although:

1. Traditional flip-chip bumping balls can only be added on **wafer-level**, thus you need 1 to 2 extra wafers. Further, 3 to 4 dedicated masks are needed (redistribution, UBM, balls itself), depending on exact technique used (printing, plating,...). These wafers and masks are quite expensive – easily 15kEUR.

2. Adding bumping balls is done at UMCs subcontractor. Technical communication is **not straightforward** as many parties are involved. Further, it is difficult to guarantee a fast cycle time. Unfortunately, this has low priority at UMC or the bumping subcontractor.

3. You do not receive wafers because of confidentiality reasons, so logistics are complicated. At the end, just **bare dies with balls are delivered**.

UMC FAQ
Is bumping for flip-chip possible on MPW ?

4. Minimum die-size is 2mm x 2mm, so this is impossible for a UMC 0.18um/0.13um mini@sic block.

5. For aluminum technologies (UMC 0.18um,...), **redistribution** to an array is required in post-processing. This is done at UMC itself, or at their subcontractor. This requires 2 extra masks.

Alternatively, you should consider **stud-bumping**, which can be done on **die-level** for prototyping quantities (MOQ 10 pcs.). This is less expensive (~ 100 EUR/die) and faster (~ 2 weeks). The technique is similar to regular gold ball-bonding, but the wire is cut just after EFO/ball forming. This can be done by virtually any package subcontractor.

Please contact epumc@imec.be for details.

UMC FAQ
Can we divide a 5x5mm MPW block ?

It is possible to divide a 5x5mm MPW block, however there are some technical restrictions:

- Minimum dimension of length/width of a sub-block is 1mm.
- All sub-blocks need to be enclosed by a Die-Seal-Ring.
- Maximum 9 sub-blocks are possible.
- Space between each sub-block is 150um.
- Scribe channels must be continuous and aligned.
- Dicing is done on wafer-level, so maximum 2 different sawing diagrams are possible.

The charge for subdicing requests is 1000 EUR.

Please contact epumc@imec.be for details.

UMC FAQ
How can I run Monte-Carlo (MC) simulations ?

For most UMC technologies, Monte-Carlo (MC) models are available. You should consult your software manual for details.

Please make sure that the "**mismatch**" flag is set for all transistors, and that the "**sigma**" parameter is declared.

UMC FAQ
What is ERC ?

ERC is the abbreviation of Electrical Rule Check.

ERC will not check functionality or connectivity. It works standalone and does not need a netlist - opposite to for example LVS. ERC-check is based on general traceable electrical properties, which are predefined in the ERC deck that is used – for example: check that all Nwells are connected to power.

For most UMC technologies, we have a "self-written" Dracula ERC rule file available. Please contact epumc@imec.be if you want us to run ERC on your design.

UMC FAQ
What yield can I expect for my UMC design ?

Yield is very much dependent of the design itself, the application and the way it has been built. The only yield estimation number that can be given is the pure **processing yield**. This yield is calculated with the Bose-Einstein Model, taking into account the **number of masks** and the **defect density.** An increase in **area** will result in a lower yield. For example, below table specifies the processing yield for UMC L180 Logic GII process, depending on die size.

die size in mm2	6inch wafer #dies	8 inch wafer #dies	12 inch wafer # dies	processing yield %
4	4108	7402	16878	98.5
9	1777	3224	7402	96.6
16	972	1777	4108	94
36	409	758	1777	87
64	217	409	972	78
100	131	250	605	68
225	50	99	250	42.6
400	24	50	131	22.6

Please contact epumc@imec.be for more info.

UMC FAQ
What cycle-time can I expect for my UMC design ?

This depends on the technology, and is significantly affected by the metal-stack, options in the design (MMC, Twell,...) , fab-load, ...

Based on historical data, you can expect cycle-time like:
(from imec deadline to delivery of bare dies):

- UMC 0.18um : 10 - 12 weeks
- UMC 0.13um : 12 - 14 weeks
- UMC 90nm : 14 - 16 weeks
- UMC 65nm : 16 - 18 weeks

UMC FAQ
What are the major assembly constraints ?

Assembly is technology independent, so assembly constraints are valid for all foundries/technologies.

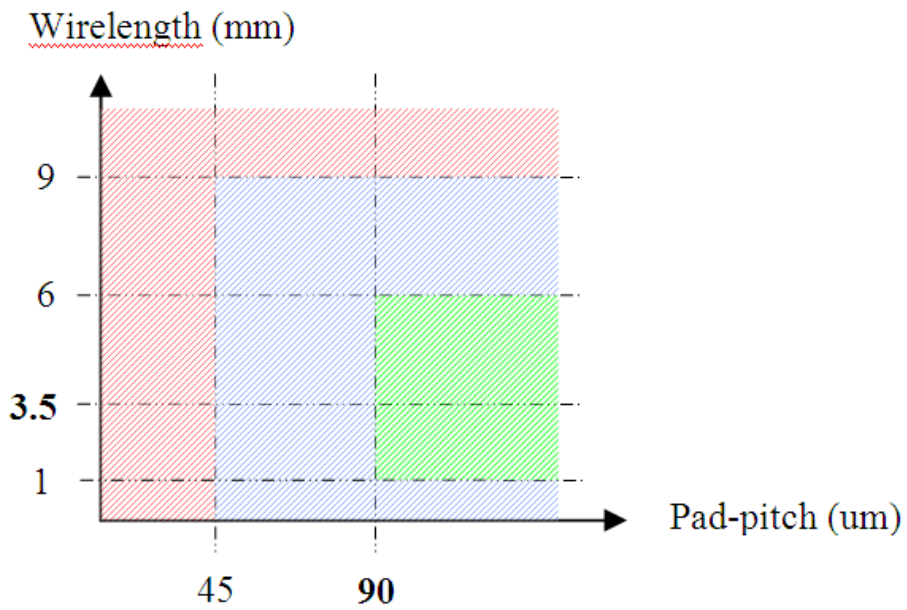
Major assembly constraints for ceramic packages are:

- **Bondwire-length**: Ideal wire-length is 3,5mm. Preferably wire-length is between 1mm and 6mm.

- **Bondpad-pitch**: Preferred bondpad-pitch (= distance between centre of adjacent bondpads) is above 90um. Absolute minimum pad-pitch is 45um (status Q1 2010).

Especially the combination of long wires and small pad-pitch is technically challenging. If pitch is below 90um and/or wire-length above 6mm, it needs to be investigated case-by-case whether assembly is possible. Please contact epumc@imec.be for details.

Wirelength versus Pad-pitch



© Erwin Deumens - 2010

UMC FAQ

What are the assembly-related restrictions to a rectangular design ?

A rectangular design is no problem for fabrication, but special attention is needed for assembly/packaging.

1. Most cavities of ceramic packages are square, so if your design is rectangular, some bond-wires become very long.
Example: A circuit with dimensions 5x10mm (2 seats) in a PGA256 with cavity size 16x16mm. Wire-length on the short side becomes 3mm, but on the long side wire-length is 5,5mm. In the corners of the die, situation is even worse.

2. The circuit side with largest number of bondpads determines the lead quantity of the package.
Example: A rectangular design with 10 - 25 - 10 - 25 bondpads can not be assembled in a 70 pins package, but requires at least 25 x 4 pins = 100 pins.

UMC 65nm FAQ
What flavors are available for UMC 65nm ?

There are basically 2 process flavors:

1. UMC L65 Logic-MM/RF **LL**.
2. UMC L65 Logic-MM/RF **SP.**

These are 2 different processes, so these can not be mixed.

UMC 65nm FAQ
What are the key process & device parameters of the UMC 65nm LL process ?

P-EPI/P-Sub, CMOS Process with Deep N-well option.
193nm Lithography
Four Vt core and Single Thick Gate Devices
Dual Poly Gate with NiSi2
Up to 1P10M Cu process with Low-K (M1~M6) / FSG (M7~M10) or 1P9M2H Cu process with Low-K (M1-M7) / FSG Dielectrics for 6X metal layers(M8;M9) Dielectrics or 1P9M2F Cu process with Low-K (M1-M7) / FSG Dielectrics for 4X metal layers (M8;M9)
Al-Pad / Cu-Pad
Wire Bond / Flip Chip
Split Word Line based on 6T 0.62, 0.499 and 8T 1.158 um^2 dense SRAM Bit Cell

UMC 65nm FAQ
What core devices are possible in UMC 65nm LL technology ?

There are 3 Vt options possible:

- Low Vt (LVT)
- Regular Vt (RVT)
- High Vt (HVT)

UMC 65nm FAQ
Are native devices possible in UMC 65nm LL technology ?

Yes, native devices are possible in UMC 65nm LL technology.

Native devices exist for 1.2V NMOS in Pwell and Ptub (triple well), and for 1.8V/2.5V/3.3V NMOS in Pwell.

UMC 65nm FAQ
What are the key process & device parameters of the UMC 65nm SP process ?

P-EPI/P-Sub, CMOS Process with Deep N-well option.
193nm Lithography
Four Vt core and Single Thick Gate Devices
Dual Poly Gate with NiSi2
Up to 1P10M Cu process with Low-K (M1~M6) / FSG (M7~M10) or 1P9M2H Cu process with Low-K (M1-M7) / FSG Dielectrics for 6X metal layers(M8;M9) Dielectrics or 1P9M2F Cu process with Low-K (M1-M7) / FSG Dielectrics for 4X metal layers (M8;M9)
Al-Pad / Cu-Pad
Wire Bond / Flip Chip
Split Word Line based on 6T 0.62, 0.499 and 8T 1.158 um^2 dense SRAM Bit Cell

Device Type (*1)	LVT	RVT	HVT	SHVT	LVT	RVT	HVT	SHVT	1.8V I/O	2.5V I/O	2.5V Operated at 3.3V	2.5V Operated at 1.8V	3.3V I/O
Vcc (V)	1.0	1.0	1.0	1.0	1.1	1.1	1.1	1.1	1.8	2.5	3.3	1.8	3.3
Electrical Tox (Å)	20/21.5	20/21.5	20/21.5	20/21.5	20/21.5	20/21.5	20/21.5	20/21.5	39/41	62/64.5	62/64.5	62/64.5	72/74.5
Lmin (um)	0.06	0.06	0.06	0.06	0.06	0.06	0.06	0.06	0.18	0.24	0.45/0.38 (N/P)	0.22	0.37
Vt_sat N/P (V)	0.185/0.145	0.23/0.19	0.30/0.265	0.36/0.325	0.175/0.135	0.22/0.18	0.29/0.255	0.350/0.325	0.47/0.40	0.44/0.40	0.597/0.425	0.386/0.395	0.507/0.535
Idsat N/P (uA/um)	900/425	830/390	695/330	585/265	1070/520	1005/480	860/410	730/340	600/255	600/275	582/289	403/161	612/296
Gate Delay (pSec/stage) (*2)	5.1	6.0	7.4	10.5	4.5	5.2	6.3	8.7	20.9	22.5	40.9	26.3	34.4

UMC 65nm FAQ
What core devices are possible in UMC 65nm SP technology ?

There are 4 Vt options possible:

- Low Vt (LVT).
- Regular Vt (RVT).
- High Vt (HVT).
- Super-High Vt (SHVT).

UMC 65nm FAQ
Are native devices possible in UMC 65nm SP technology ?

Yes, native devices are possible in UMC 65nm SP technology.

Native devices exist for 1.0V NMOS in pwell and 1.8V/2.5V/3.3V NMOS in pwell.

UMC 65nm FAQ
What IO devices are possible in UMC 65nm technology ?

You can choose between **1.8V / 2.5V / 3.3V**. These can not co-exist on 1 circuit.

For multiple-voltage applications: The 2.5V device is also modelled for under-drive 1.8V or overdrive 3.3V operation.

UMC 65nmm FAQ
What is the Ft/Fmax of UMC 65nm technology ?

65LL/SP

Type		RF Characteristic	Value
Core	NMOS	Ft for LL/SP @Vd=1.2/1.0V; 0.06umx2umx16x2	160 GHz / 240 GHz
		Fmax for LL/SP @Vd=1.2/1.0V; 0.06umx2umx16x2	120 GHz / 230GHz
		NFmin for LL@Vg=Vd=1.2V; 0.06umx2umx16x2 NFmin for SP@Vg=Vd=1.0V; 0.06umx2umx16x2	<0.3 dB @2.4GHz <0.4dB @5.8GHz
	PMOS	Ft/Fmax for LL@Vd= -1.2V; 0.06umx2umx16x2 Ft/Fmax for SP@Vd= -1.0V; 0.06umx2umx16x2	100 GHz/ 85GHz 125 GHz/ 120GHz
I/O	NMOS	Ft/Fmax@Vd=2.5V; 0.24umx9.8umx8x1	45 GHz/ 57 GHz
	PMOS	Ft/Fmax@Vd= -2.5V; 0.24umx8umx4x4	20 GHz/ 27GHz

UMC 65nm FAQ
What metal-stacks (BEOL) are possible in UMC 65nm ?

The metal-stack (BEOL) is Cu with redistribution to Aluminum.

You can choose between > 50 choices – see TLR document.

Some considerations:

- DRC/LPE rules are different depending on the choice, so please make sure to use the correct DRC/LPE rulesfile.
- Only most common metal-stacks are available in the designkit.
- Not all devices (especially inductor and MOM) for all metal-stacks are available in the designkit.

Note: A mini@sic is always processed with 8M1T0F1U.

UMC 65nm FAQ
What is the thickness of "AL_RDL" in UMC 65nm ?

The default aluminum "AL_RDL" thickness is **12kA**. This is compliant with most assembly/package subcontractor rules for wirebonding.

Optional, 25kA or 36kA is possible. Please contact epumc@imec.be for details.

Note: Please do not mix-up with Cu topmetal thickness – possibilities are: F = 8kA or U = 32.5kA.

UMC 65nm FAQ
What does 1P8M1T0F1U mean ?

The metal-stack 1P8M1T0F1U means:

- **1 P**oly
- **8 M**etals, out of which:
  - Metal 1..6 = normal
  - **1 T**hick metal: Metal 7 (= 2x)
  - No **F**at metal (= 4x)
  - **1 U**ltra-Thick (thickness is 32.5kA)

UMC 65nm FAQ
What MMC values are possible in UMC 65nm ?

MMC value in UMC 65nm is 2fF squm.

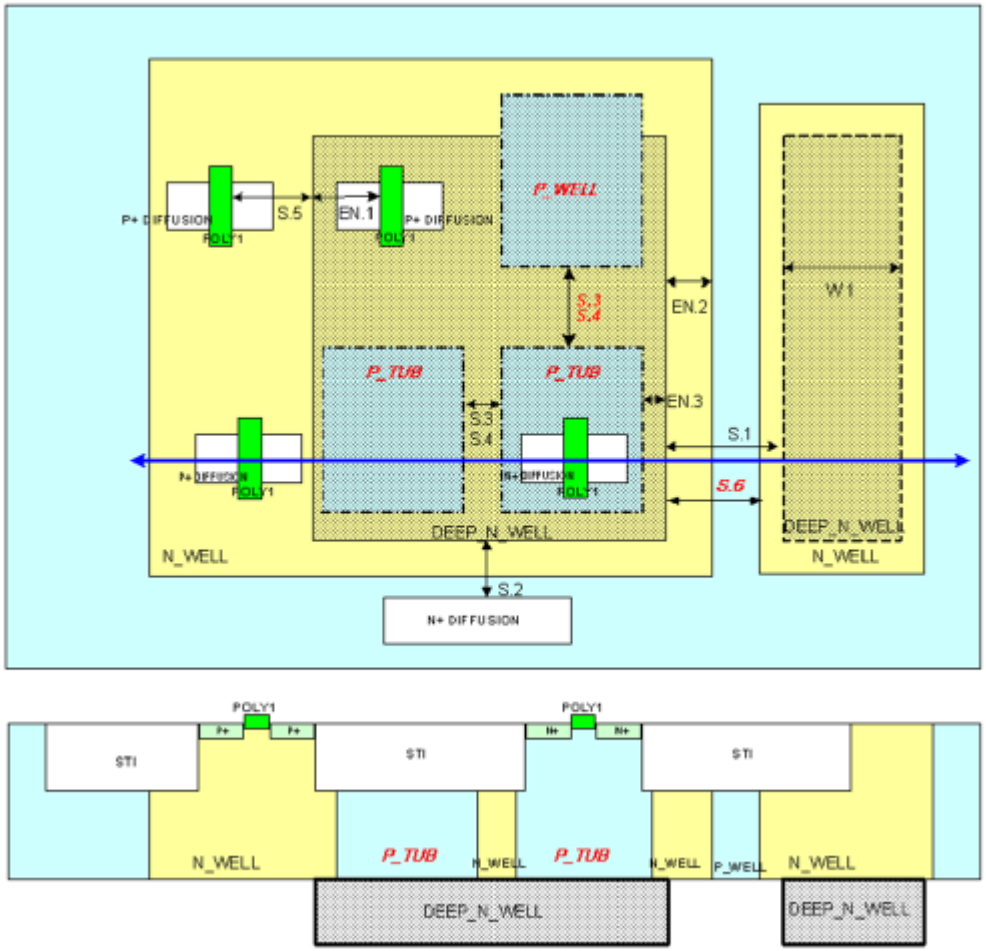
UMC 65nm FAQ
Can I draw an isolated P-doped area in my design ?

Yes, you can draw an isolated P-doped area in your design. You should use layer "**DNW**" for this.

The UMC 65nmm Logic-MM/RF process is Twin-well with optional Tripple-well support:

- Nwell – Drawn layer. N-doped.
- Pwell – Generated layer. P-doped.
- Ptub – DNW (Deep Nwell) should be drawn. Holes in drawn Nwell define the isolated P-doped area. See cross-section on next page.

This is different compared to other technologies (90nm, ...)!



UMC 65nm FAQ
What are the restrictions for a UMC 65nm miniasic ?

Restrictions for a 65nm miniasic are:

- Process flavor is **Low-Leakage** (LL).

  A miniasic circuit must fit in a block with size **1875x1875um**.

  2 blocks (1875x4950) is also possible on request.

- Metal-stack is **8M1T0F1U**.
- MMC value is **2fF**/squm
- IO-devices are **2.5V**. Optional 2.5V_OD_3.3V or 2.5V_UD_1.8V is possible.

UMC 65nm FAQ
The UMC 65nm SP transistor exist for 1.0V and 1.1V. How are these devices different ?

Layout and processing of the 1.0V and 1.1V SP transistor is 100% identical. The only difference is the operation voltage in the model.

Though the process is the same, it is useful for UMC to know the operation voltage, as the WAT (Wafer-Acceptance-Test) measurements can be aligned accordingly.

UMC 65nm FAQ
Which HIPO resistors exist in UMC 65nm technology ?

UMC 65nm technology supports following High-Ohmic Poly (HIPO) resistors:

- **HR** -> Sheet resistance ~ 1kΩ

- **MR** -> This device is available on special request. The sheet resistance will be tuned according to your own needs. This can only be done for circuits with certain production volume potential. Please contact epumc@imec.be for details.

UMC 65nm FAQ
What is layer MOAT used for ?

Layer "MOAT" defines a resistive substrate area, and is typically used in a guard-ring to reduce substrate noise coupling.

UMC 65nm FAQ
Which rulesfiles are supported for LPE ?

Because of practical (filesize) reason, only most used LPE rulesfiles are available on our download-centre.

If you need a specific LPE rulesfile, please contact epumc@imec.be. Not all combinations of metal-stack and software are available, so please specify:

- Exact metal-stack: More than 50 metal-stacks can be used.
- Software used: Calibre XRC, Assura QRC, Fire&Icxe, StarRCXT, BlastFusion,....
- MMC in your design ?

UMC 65nm FAQ
What is the grid for UMC 65nm technology?

The manufacturing grid for UMC 65nm technology is **5nm** (0.005um) for all layers.

For some "high mask-grade" layers (diffusion, poly, P+,N+,contact, metal1,...), a grid of 1nm (0.001um) is allowed.

Exceptionally, offgrids in topmetal from inductor pcells can be waived.