+ Zynq

- The defining feature of Zynq is that it combines a dual-core ARM Cortex-A9 processor with traditional Field Programmable Gate Array (FPGA) logic fabric.
- ARM Cortex-A9 is an application grade processor
- The architecture is completed by industry standard AXI interfaces

System-on-Chip with Zynq

- SoC has usually referred to an Application Specific Integrated Circuit (ASIC)
- The major disadvantages of ASIC-based SoCs are development time and cost, and lack of flexibility.
- The non-recurring engineering effort (and cost) of developing an ASIC are significant, making this type of SoC suitable only for high-volume markets where there is no requirement for future upgrades.
- The limitations of ASIC SoCs render them incompatible with a significant number of applications, particularly where fast time-to-market, flexibility, and upgrade-ability are of key importance.

System on PCB

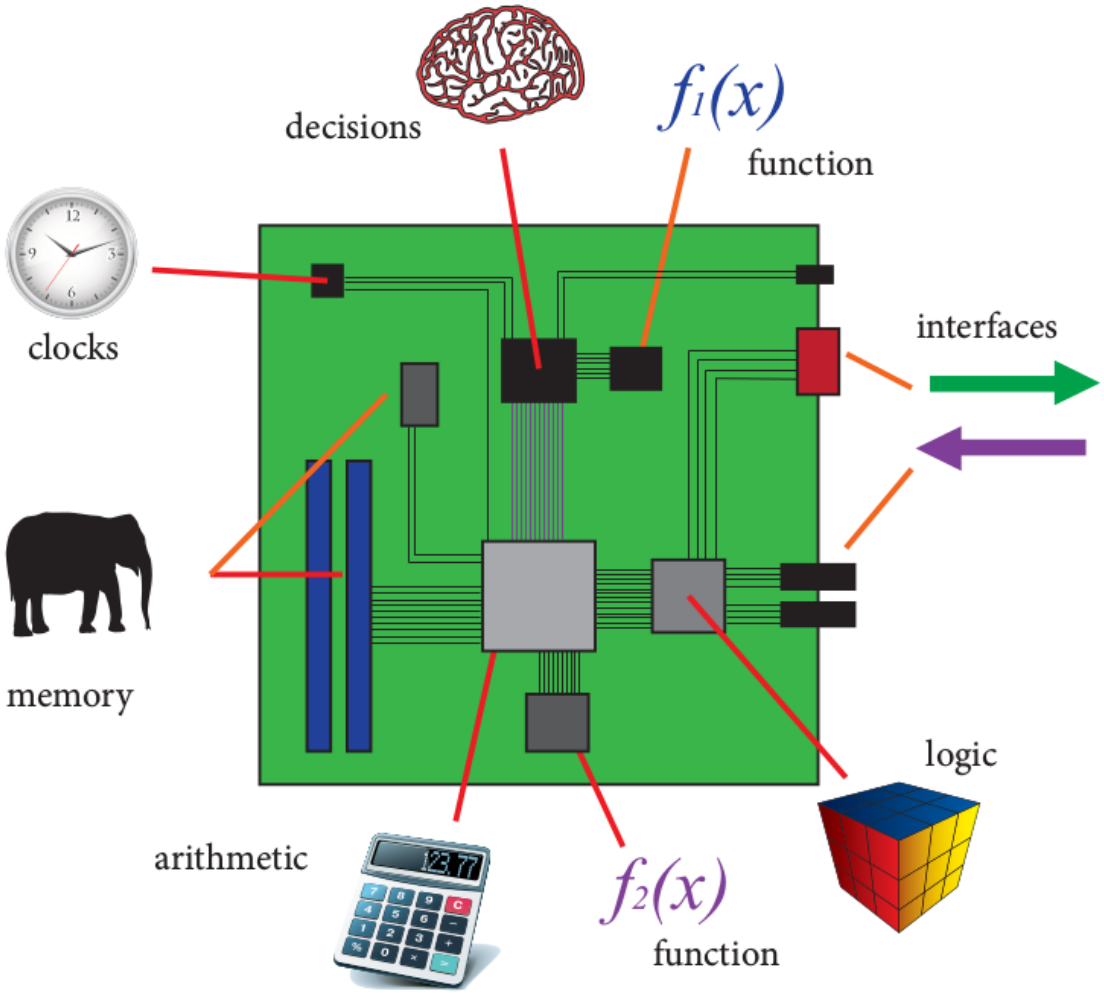


Figure: System on PCB

System on chip

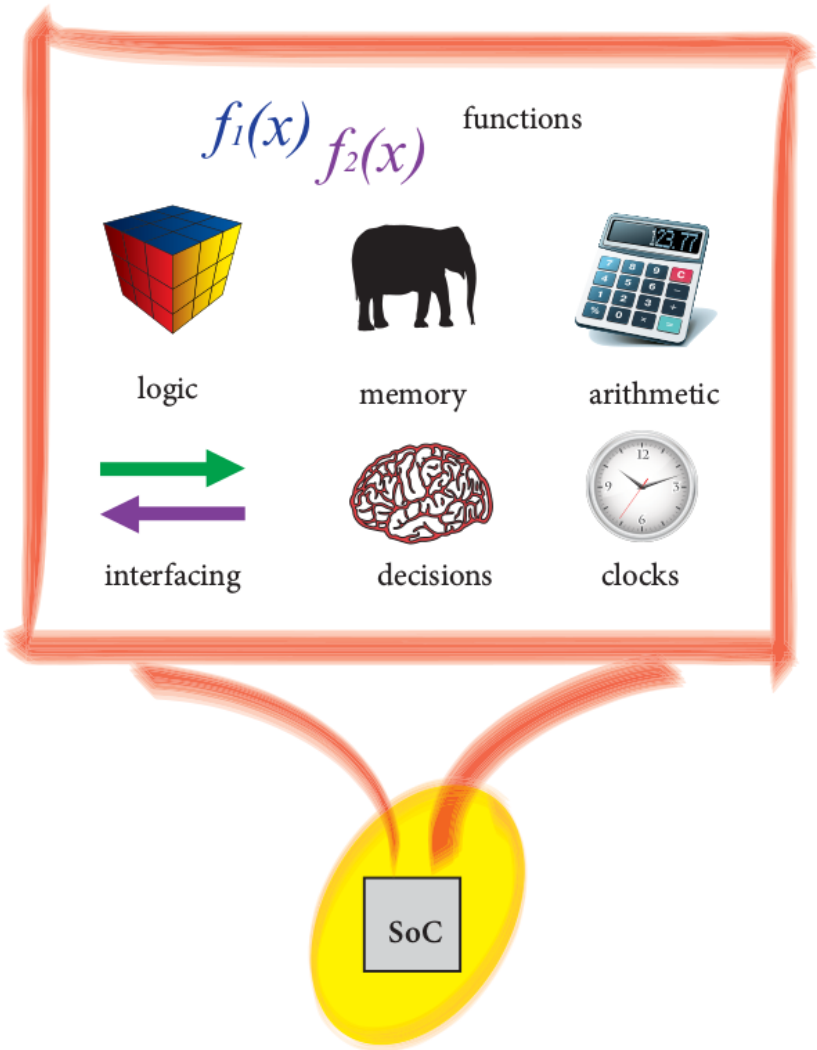


Figure: System on chip

System-on-Chip with Zynq

- Traditional FPGAs are inherently flexible devices that can be configured to implement any arbitrary system, including embedded processors if needed.
- Zynq provides an even more ideal platform for implementing flexible SoCs: Xilinx markets the device as an 'All-Programmable SoC' (APSoC)
- Zynq comprises two main parts:
  - Processing System (PS) formed around a dual-core ARM Cortex-A9 processor
  - Programmable Logic (PL), which is equivalent to that of an FPGA.

Simplified model of the Zynq

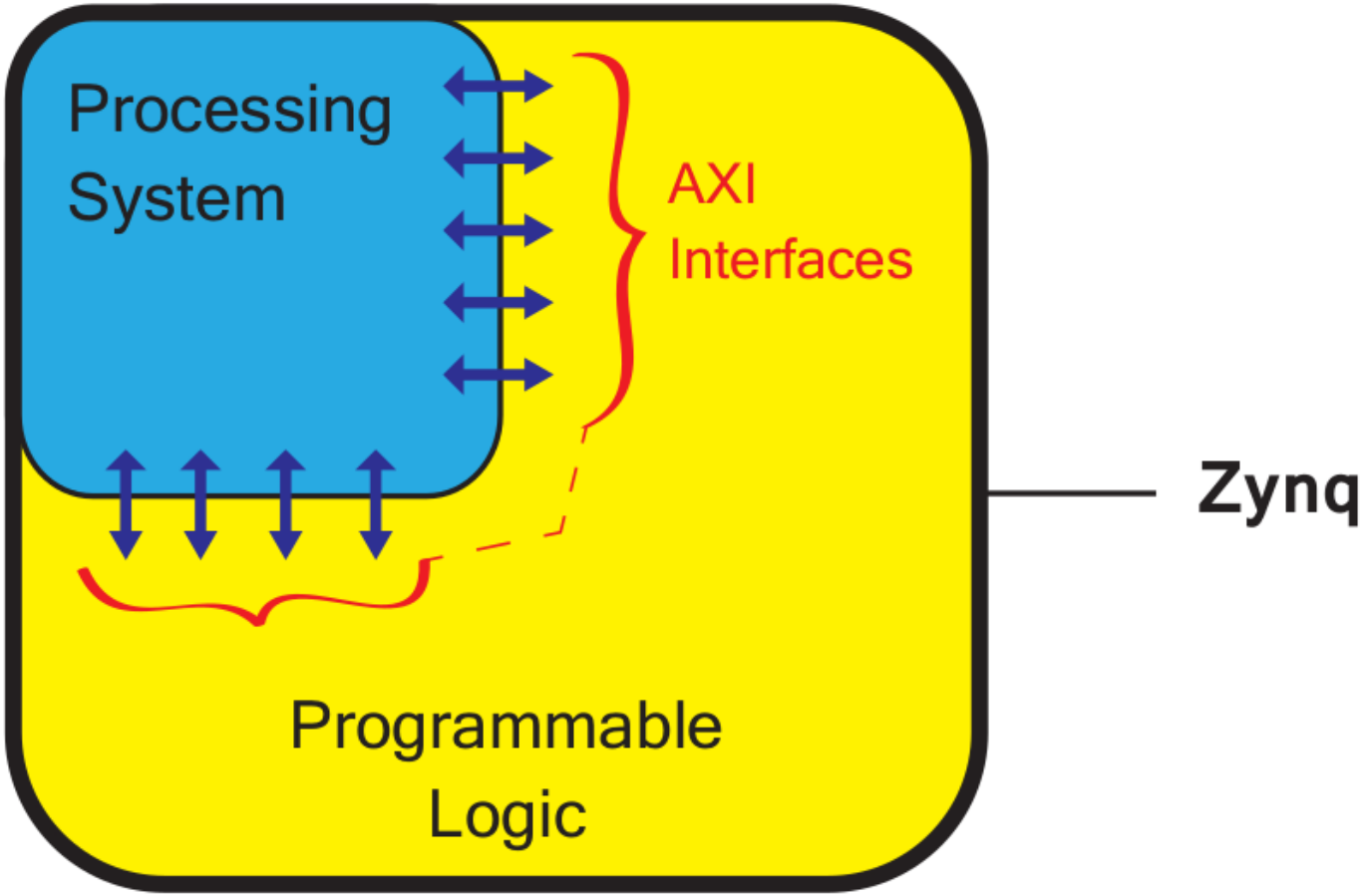


Figure: Simplified model of the Zynq

SoC on Zynq

- The PL section is ideal for implementing high-speed logic, arithmetic and data flow subsystems.
- the PS supports software routines and/or operating systems, meaning that the overall functionality of any designed system can be appropriately partitioned between hardware and software.
- Links between the PL and PS are made using industry standard Advanced eXtensible Interface (AXI) connections

Simple Anatomy of an Embedded SoC

- Embedded SoC is systems incorporating a processor, memories, and peripherals, along with buses connecting the various elements together.

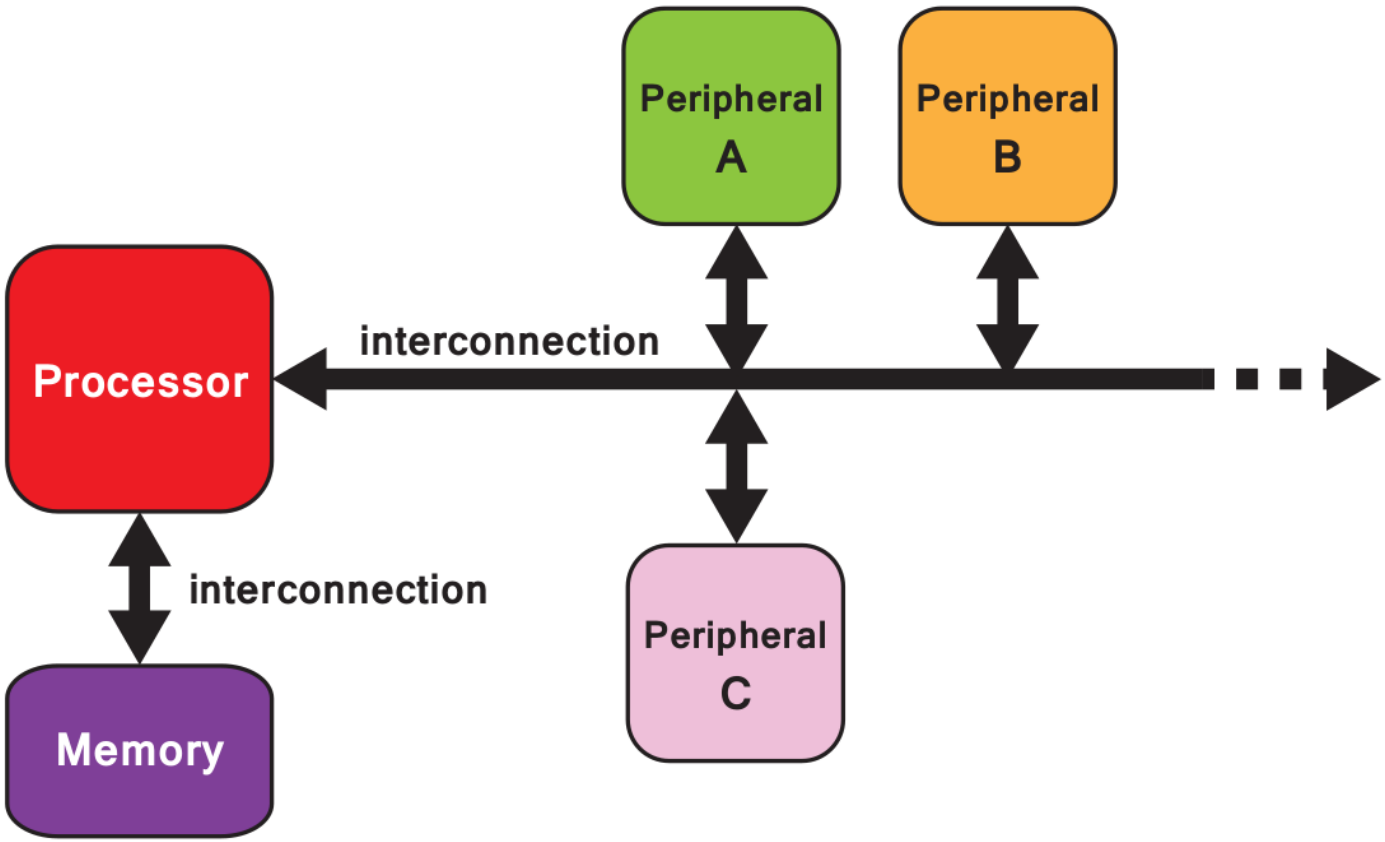


Figure: Embedded SoC

Simple Anatomy of an Embedded SoC - Processor

- The processor can be regarded as the central element of the hardware system.
- The software system (a software 'stack') is run on the processor, comprising applications, and with a lower layer of software functionality for interfacing with the hardware system.
- Communication between system elements takes place via interconnections.
  - point-to-point links
  - buses serving multiple components

Simple Anatomy of an Embedded SoC - Peripherals

- Peripherals are functional components residing away from the processor:
  - coprocessors — elements that supplement the primary processor
  - cores for interacting with external interfaces
  - additional memory elements

Relationship of the software system, hardware system, and Zynq architecture

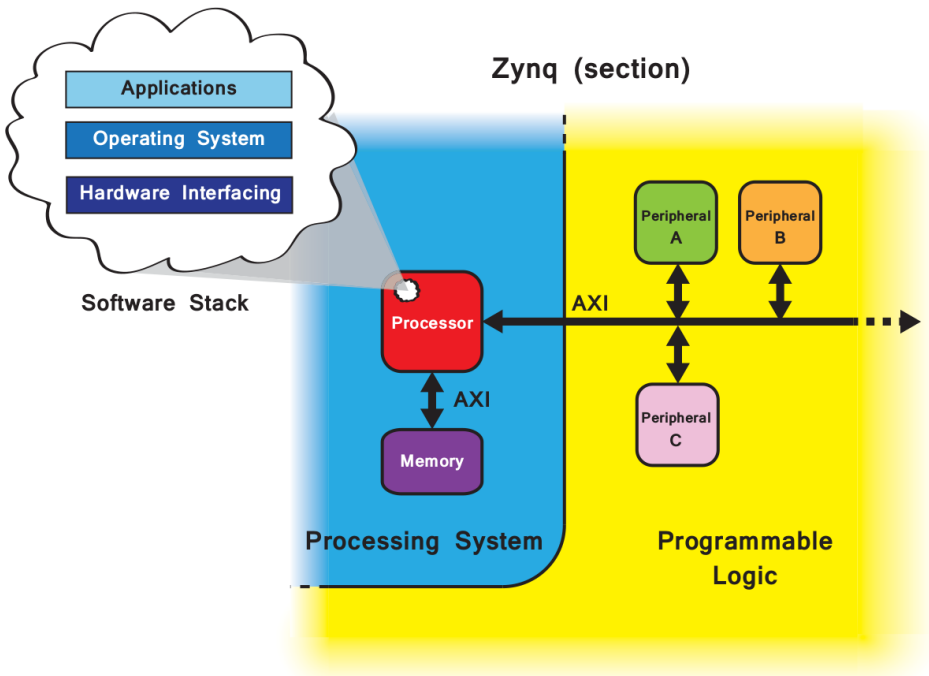


Figure: Relationship of the software system, hardware system, and Zynq architecture

Design Reuse

- The development of a complete embedded system is a significant design task, and there are particular advantages to undertaking the design on a platform such as an FPGA or Zynq device, which make the process more straightforward.
- Intellectual Property (IP) functional blocks can be sourced from Xilinx libraries (provided with the design tools), reused from previous projects, or brought in from third parties or open source repositories, before being integrated together to form the system design.
- Zynq is an SoC, and a wide variety of standard IP is available, meaning that there is no need to redesign these components.

Zedboard

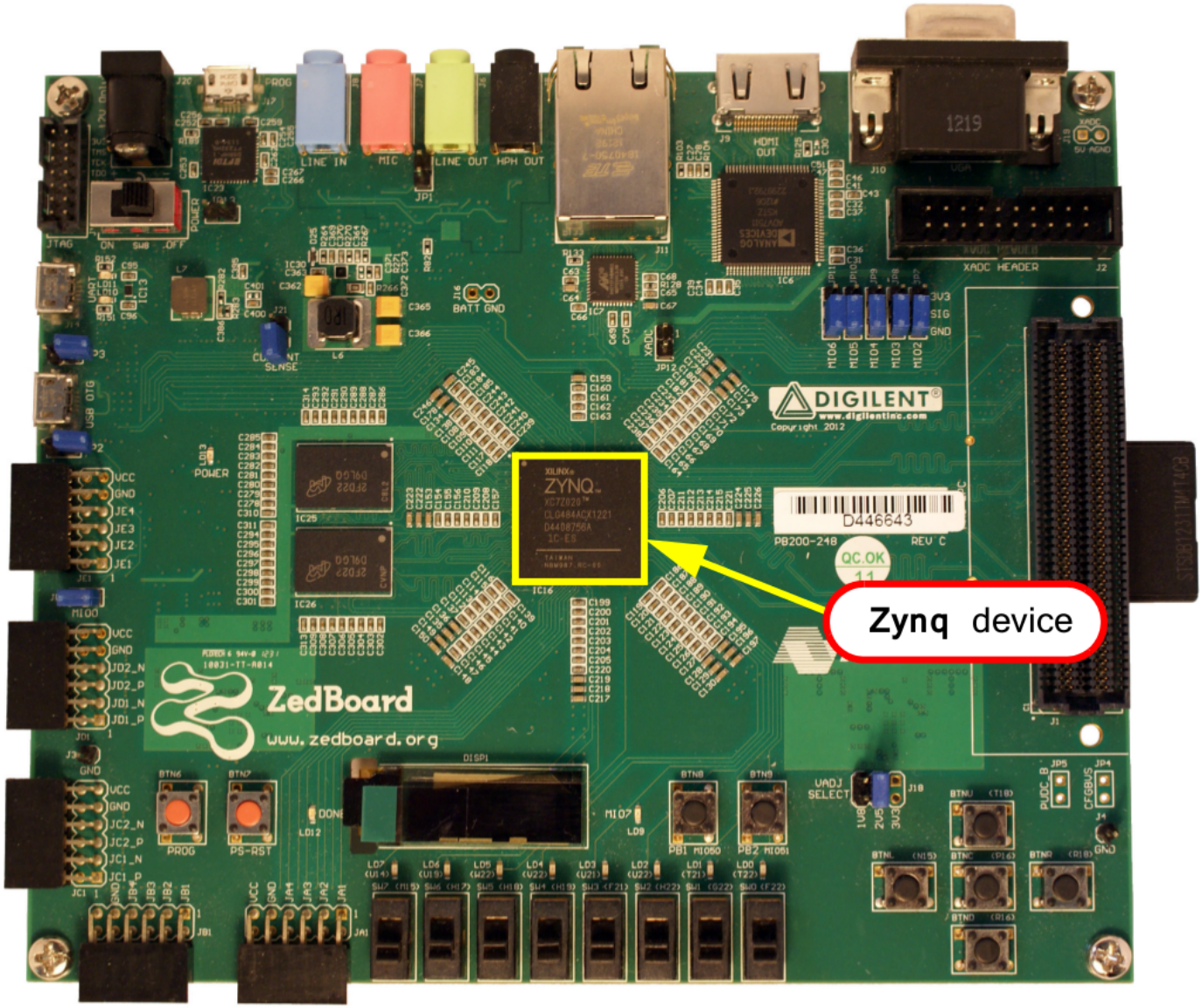


Figure: Zedboard

+ Hard vs Soft Processor

- dual-core ARM Cortex-A9 processor on zynq is a ‘hard’ processor — it exists as a dedicated and optimised silicon element on the device.
- The alternative to a hard processor is a ‘soft’ processor like the Xilinx MicroBlaze.
- The advantage of soft processors is that the number and precise implementation of processor instances is flexible.
- Hard processors can achieve considerably higher performance

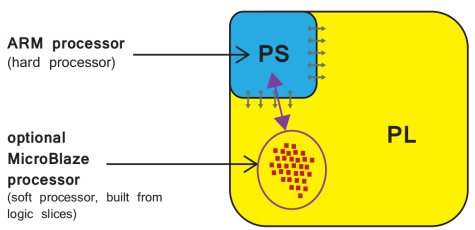


Figure: Hard vs Soft

PS Architecture

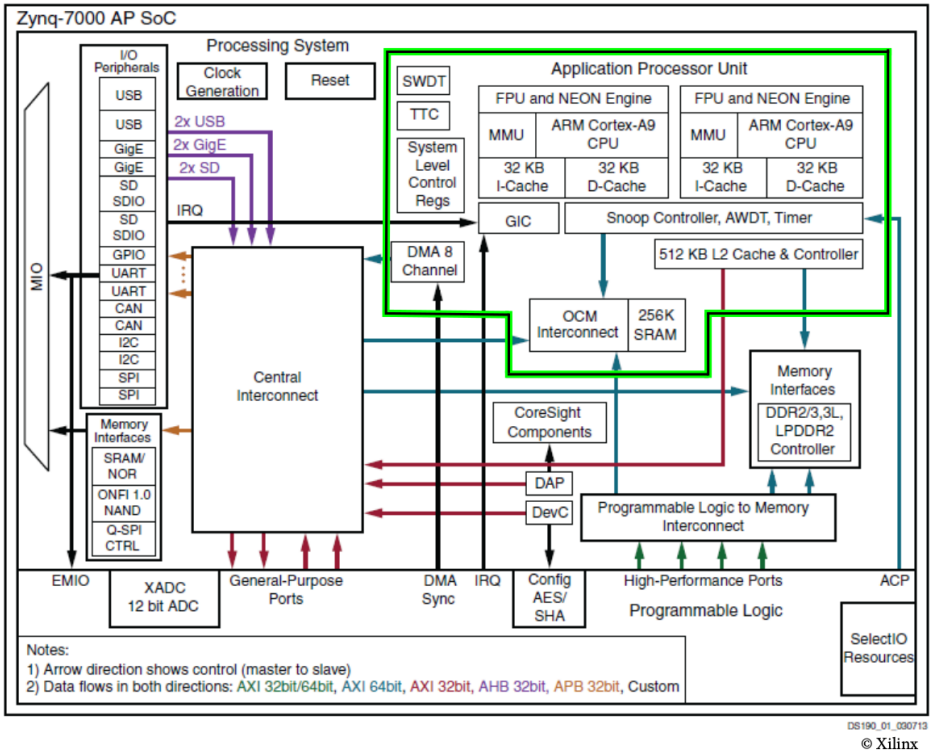


Figure: PS architecture

APU Architecture

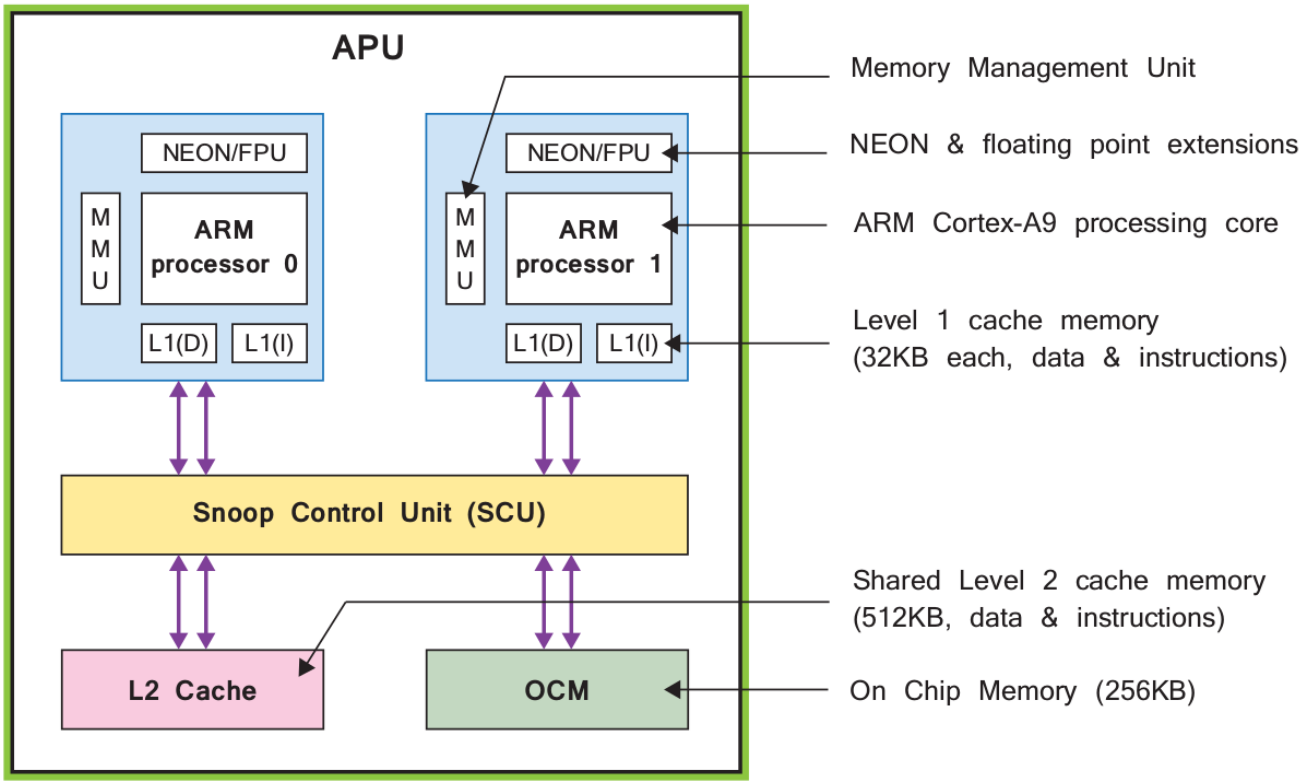


Figure: APU architecture

APU Architecture

- The ARM Cortex-A9 can operate at up to 1GHz, depending on the particular Zynq device.
- Each of the two cores has separate Level 1 caches for data and instructions, both of which are 32KB.
- The two cores additionally share a larger Level 2 cache of 512KB.
- The primary role of the MMU is to translate between virtual and physical addresses.
- The Snoop Control Unit undertakes several tasks relating to interfacing between the processors and Level 1 and 2 cache memories.
  - 'Snooping' is one of several mechanisms for ensuring cache coherency
  - The SCU additionally manages transactions that take place between the PS and PL via the Accelerator Coherency Port (ACP).

APU Architecture

- Timers and an interrupt controller are further functional blocks located in the APU.
- Support for ARM instructions is provided via the Xilinx Software Development Kit (SDK).
- The NEON engine provides Single Instruction Multiple Data (SIMD) facilities to enable strategic acceleration of media and DSP type algorithms
- NEON instructions are an extension to the standard ARM instruction set, and can either be used explicitly, or by ensuring that the C code follows an expected form and thus allows NEON operations to be inferred by the compiler.

NEON Architecture

- The NEON engine can accept multiple sets of input vectors, upon which the same operation is performed simultaneously to provide a corresponding set of output vectors.
- This style of computation caters well to applications like image and video processing, Finite Impulse Response (FIR) filters and Fast Fourier Transforms (FFTs).

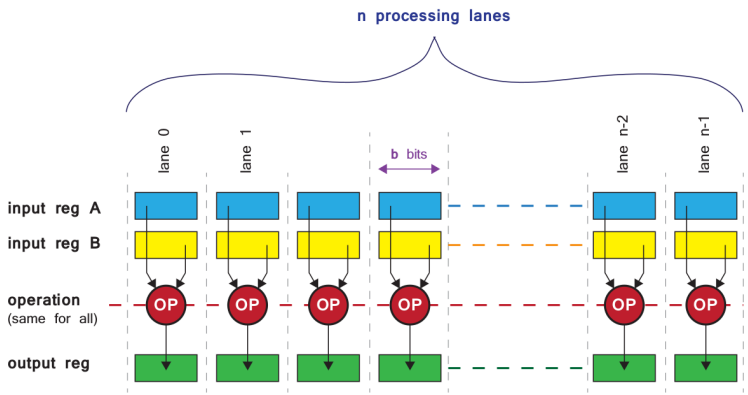


Figure: NEON SIMD

Processing System External Interfaces

- Interfaces between the PS and PL.
- Interfaces between the PS and external components.
- Communication between the PS and external interfaces is achieved primarily via the Multiplexed Input/Output (MIO), which provides 54 pins of flexible connectivity, meaning that the mapping between peripherals and pins can be defined as required.
- Certain connections can also be made via the Extended MIO (EMIO), which is not a direct path from the PS to external connections, but instead passes through and shares the I/O resources of the PL.

Interfaces

I/O Interface	Description
SPI (x2)	Serial Peripheral Interface [10] *De facto standard for serial communications based on a 4-pin interface. Can be used either in master or slave mode.*
I2C (x2)	I^2C bus [14] *Compliant with the I2C bus specification, version 2. Supports master and slave modes.*
CAN (x2)	Controller Area Network *Bus interface controller compliant with ISO 118980-1, CAN 2.0A and CAN 2.0B standards.*
UART (x2)	Universal Asynchronous Receiver Transmitter *Low rate data modem interface for serial communication. Often used for Terminal connections to a host PC.*
GPIO	General Purpose Input/Output *There are 4 banks GPIO, each of 32 bits.*
SD (x2)	*For interfacing with SD card memory.*
USB (x2)	Universal Serial Bus *Compliant with USB 2.0, and can be used as a host, device, or flexibly ("on-the-go" or OTG mode, meaning that it can switch between host and device modes).*
GigE (x2)	Ethernet *Ethernet MAC peripheral, supporting 10Mbps, 100Mbps and 1Gbps modes.*

Figure: Interfaces

+ Programmable Logic

- The second principal part of the Zynq architecture is the programmable logic. This is based on the Artix-7 and Kintex-7 FPGA fabric
- The PL is predominantly composed of general purpose FPGA logic fabric, which is composed of slices and Configurable Logic Blocks (CLBs), and there are also Input/ Output Blocks (IOBs) for interfacing.

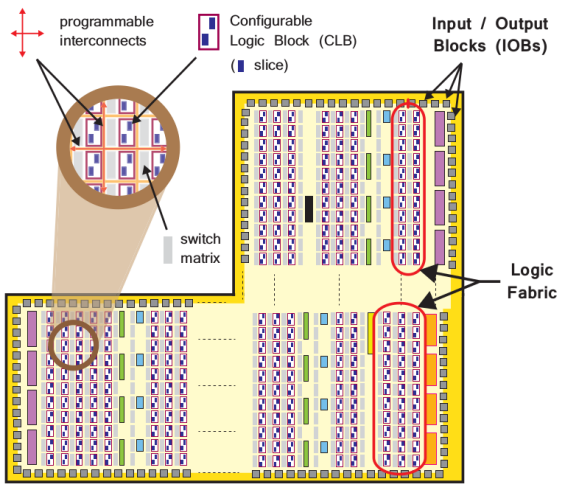


Figure: Programable Logic

Features of the PL

- Configurable Logic Block (CLB) — CLBs are small, regular groupings of logic elements that are laid out in a two-dimensional array on the PL, and connected to similar resources via programmable interconnects. Each CLB is positioned next to a switch matrix and contains two logic slices
- Slice — A sub-unit within the CLB, which contains resources for implementing combinatorial and sequential logic circuits. Zynq slices are composed of 4 Lookup Tables, 8 Flip-Flops, and other logic.

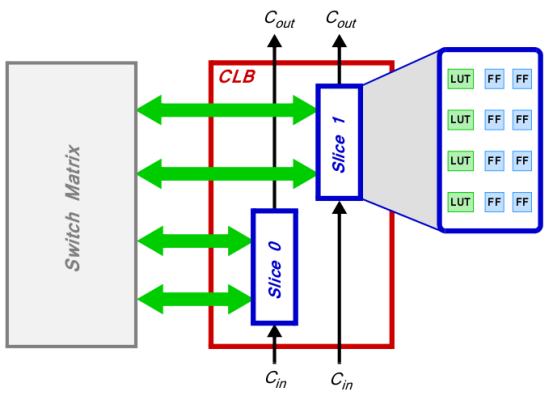
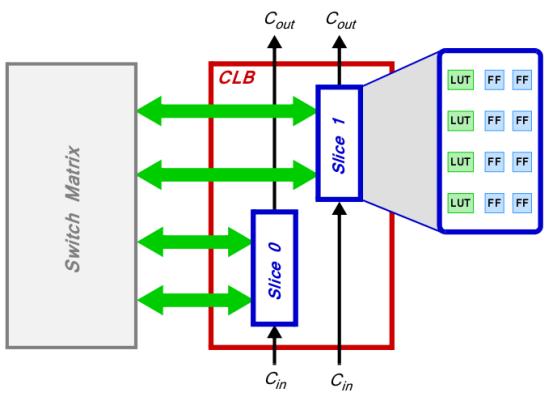


Figure: CLB Structure

Features of the PL

- Lookup Table (LUT) — A flexible resource capable of implementing
  - Logic function of up to six inputs
  - Small Read Only Memory (ROM)
  - Small Random Access Memory (RAM)
  - Shift register
- Flip-flop (FF) — A sequential circuit element implementing a 1-bit register, with reset functionality. One of the FFs can optionally be used to implement a latch.
- Switch Matrix — A switch matrix sits next to each CLB, and provides a flexible routing facility for making connections
  - Between elements within a CLB.
  - From one CLB to other resources on the PL.



Features of the PL

- Switch Matrix — A switch matrix sits next to each CLB, and provides a flexible routing facility for making connections
  - Between elements within a CLB.
  - From one CLB to other resources on the PL.
- Carry logic — Arithmetic circuits require intermediate signals to be propagated between adjacent slices, and this is achieved via carry logic. The carry logic comprises a chain of routes and multiplexers to link slices in a vertical column.
- Input / Output Blocks (IOBs) — IOBs are resources that provide interfacing between the PL logic resources, and the physical device 'pads' used to connect to external circuitry. Each IOB can handle a 1-bit input or output signal. IOBs are usually located around the perimeter of the device.

Special Resources

- In addition to the general fabric, there are two special purpose components: Block RAMs for dense memory requirements; and DSP48E1 slices for high-speed arithmetic.

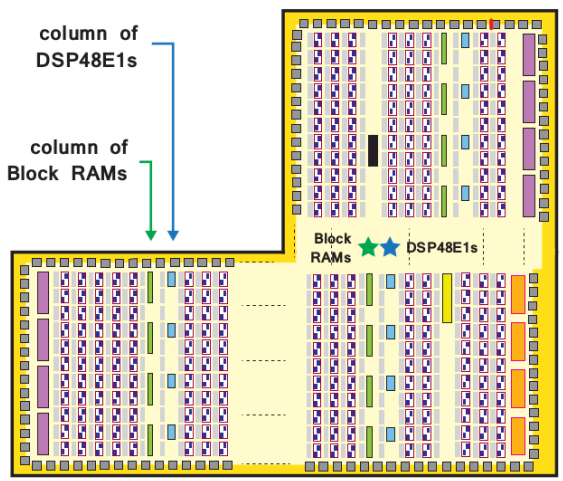


Figure: FPGA BRAM and DSP

Block RAM

- Each Block RAM can store up to 36Kb of information. The RAM can also be reshaped.
- Using a Block RAM means that a large amount of data can be stored in a small physical space on the device, within a dedicated and optimised memory element; the alternative is Distributed RAM, which is constructed from the LUTs within the logic fabric.
- Large Memories - BRAM, Small Memories - LUT (DRAM)
- Block RAMs can normally be clocked at the highest clock frequency supported by the device.

DSP Resources

- DSP48E1s are specialist slices for implementing high-speed arithmetic on signals with medium to long arithmetic wordlengths.
- They are dedicated silicon resources, and primarily comprise a pre-adder/subtractor, multiplier, and post-adder/subtractor with logic unit.
- Wide arithmetic - DSP blocks, Narrow arithmetic - LUT
- DSP48E1s can be clocked at the maximum clock frequency of the device

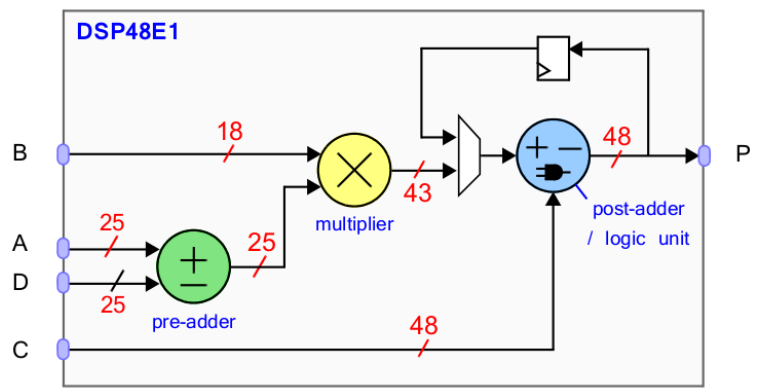


Figure: DSP architecture

General Purpose Input/Output

- The general purpose input / output facilities (IOBs) on the Zynq are collectively referred to as SelectIO Resources, and these are organised into banks of 50 IOBs each. Each IOB contains one pad, which provides the physical connection to the outside world for a single input or output signal.
- The I/O banks are categorised as High Performance (HP) or High Range (HR), and these support a variety of I/O standards and voltages.
- The HP interfaces are limited to voltages of 1.8V and are typically used for high-speed interfaces to memory and other chips.
- The HR interfaces permit voltages of up to 3.3V and cater for a wider variety of IO standards. Both single-ended and differential signalling are supported, requiring 1 IOB and 2 IOBs per connection, respectively.
- Each IOB also includes an IOSERDES resource for programmable conversion between parallel and serial data formats (serialisation and deserialisation)

Communications Interfaces

- The more highly specified Zynq devices include GTX Transceivers, high-speed commu- nications interface blocks which are embedded into the logic fabric.
- These are dedicated silicon blocks ("Hard IP" blocks), and they are capable of supporting a number of standard interfaces including PCI Express, Serial RapidIO, SCSI and SATA.
- GTX Transceivers are implemented as 'quads', i.e. groups of 4 individual channels, each of which comprises a dedicated Phase Locked Loop (PLL) for that channel, a transmitter, and a receiver.

Other Programmable Logic External Interfaces

- Analogue to Digital Conversion — The PL includes another hard IP component: the XADC block. This is a dedicated set of Analogue to Digital Converter (ADC) mixed signal hardware, which features two separate 12-bit ADCs both capable of sampling external analogue input signals at 1Msps.
- Clocks — The PL receives four separate clock inputs from the PS, and additionally has the facilities to generate and distribute its own clock signals independently of the PS.
- Programming and Debug — A set of JTAG ports are provided in the PL section to facil- itate configuration and debugging of the PL. JTAG configuration is often used during the development phase.

+ Processing System — Programmable Logic Interfaces

- AXI Inetrfaces and EMIO Interfaces
- The primary interface between the PS and PL is via a set of nine AXI interfaces, each of which is composed of multiple channels.
- AXI4-Full — For memory-mapped links, and providing the highest performance: an address is supplied followed by a data burst transfer of up to 256 data words.
- AXI4-Lite — A simplified link supporting only one data transfer per connection (no bursts). AXI4-Lite is also memory-mapped: in this case an address and single data word are transferred.
- AXI4-Stream — For high-speed streaming data, supporting burst transfers of unrestricted size. There is no address mechanism; this bus type is best suited to direct data flow between source and destination (non memory mapped).

Processing System — Programmable Logic Interfaces

- Interconnect — An interconnect is effectively a switch which manages and directs traffic between attached AXI interfaces. There are several interconnects within the PS, some which are directly interfaced to the PL, and others which are for internal use only. The connections between these interconnects are also formed using AXI interfaces.
- Interface — A point-to-point connection for passing data, addresses, and handshaking signals between master and slave clients within the system.

Interfaces between PS and PL

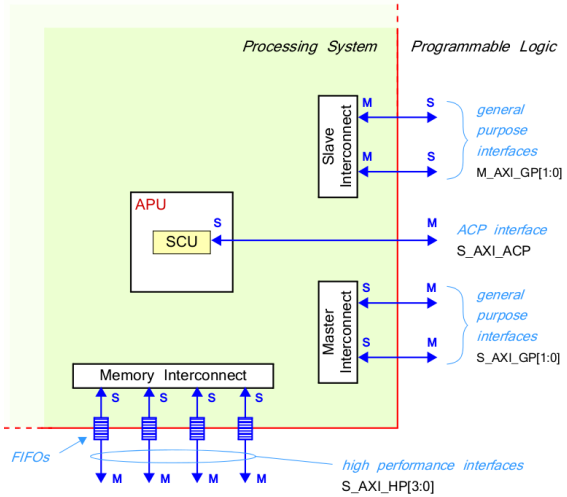


Figure: The structure of AXI connections

Interface Name	Interface Description	Master	Slave
M_AXI_GP0	General Purpose (AXI_GP)	PS	PL
M_AXI_GP1		PS	PL
S_AXI_GP0	General Purpose (AXI_GP)	PL	PS
S_AXI_GP1		PL	PS
S_AXI_ACP	Accelerator Coherency Port (ACP), cache coherent transaction	PL	PS
S_AXI_HP0	High Performance Ports (AXI_HP) with read/write FIFOs. (Note that AXI_HP interfaces are sometimes referred to as AXI Fifo Interfaces, or AFIs).	PL	PS
S_AXI_HP1		PL	PS
S_AXI_HP2		PL	PS
S_AXI_HP3		PL	PS

Figure: Interfaces between PS and PL

AXI Interfaces

- General Purpose AXI — A 32-bit data bus, which is suitable for low and medium rate communications between the PL and PS. The interface is direct and does not include buffering. There are four general purpose interfaces in total: the PS is the master of two, and the PL is the master of the other two.
- Accelerator Coherency Port — A single asynchronous connection between the PL and the SCU within the APU, with a bus width of 64 bits. This port is used to achieve coherency between the APU caches and elements within the PL. The PL is the master.
- High Performance Ports — The four high performance AXI interfaces include FIFO buffers to accommodate "bursty" read and write behaviour, and support high rate communications between the PL and memory elements in the PS. The data width is either 32 or 64 bits, and the PL is the master of all four interfaces.

EMIO Interfaces

- EMIO involves signal transfer between the two domains, and is achieved through a simple set of wire connections; consequently, not all MIO interfaces are supported in EMIO, and some of those which are supported have reduced capability.

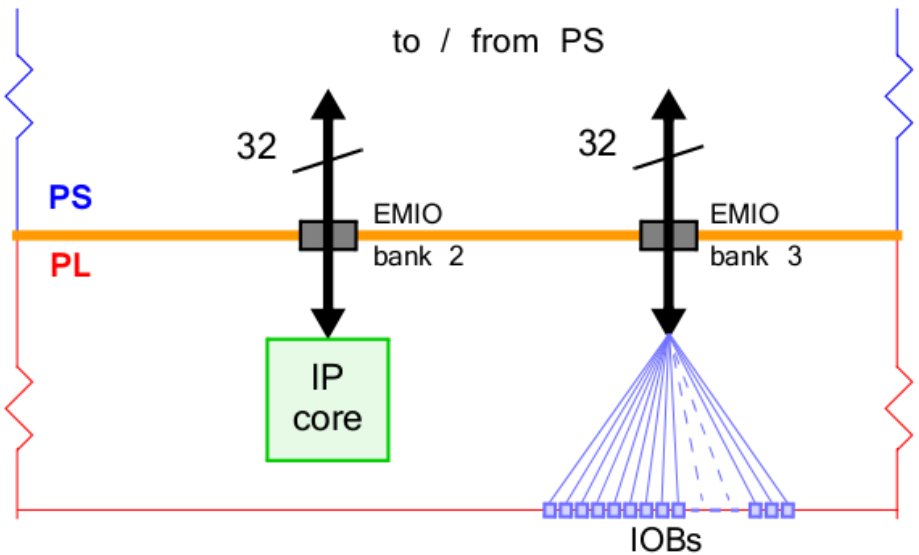


Figure: EMIO Interfaces

+ Zynq-7000 Family

	Z-7010	Z-7015	Z-7020	Z-7030	Z-7045	Z-7100
Processor	Dual core ARM Cortex-A9 with NEON and FPU extensions					
Max. processor clock frequency	866MHz			1GHz		
Programmable Logic	Artix-7			Kintex-7		
No. of FlipFlops	35,200	96,400	106,400	157,200	437,200	554,800
No. of 6-input LUTs	17,600	46,200	53,200	78,600	218,600	277,400
No. of 36Kb Block RAMs	60	95	140	265	545	755
No. of DSP48 slices (18x25 bit)	80	160	220	400	900	2020
No. of SelectIO Input/Output Blocks[a]	HR: 100 HP: 0	HR: 150 HP: 0	HR: 200 HP: 0	HR: 100 HP: 150	HR: 212 HP: 150	HR: 250 HP: 150
No. of PCI Express Blocks	-	4	-	4	8	8
No. of serial transceivers	-	4	-	4	8 or 16[b]	16
Serial transceivers maximum rate	-	6.25Gbps	-	6.6Gbps / 12.5Gbps [c]	6.6Gbps / 12.5Gbps [b]	10.3Gbps

Figure: Zynq-7000 Family