

**TTL
MSI**

CIRCUIT TYPES SN5442, SN5443, SN5444, SN7442, SN7443, SN7444 4-LINE-TO-10-LINE DECODERS (1-OF-10)

- BCD-to-Decimal
- Excess-3-to-Decimal
- Excess-3-Gray-to-Decimal

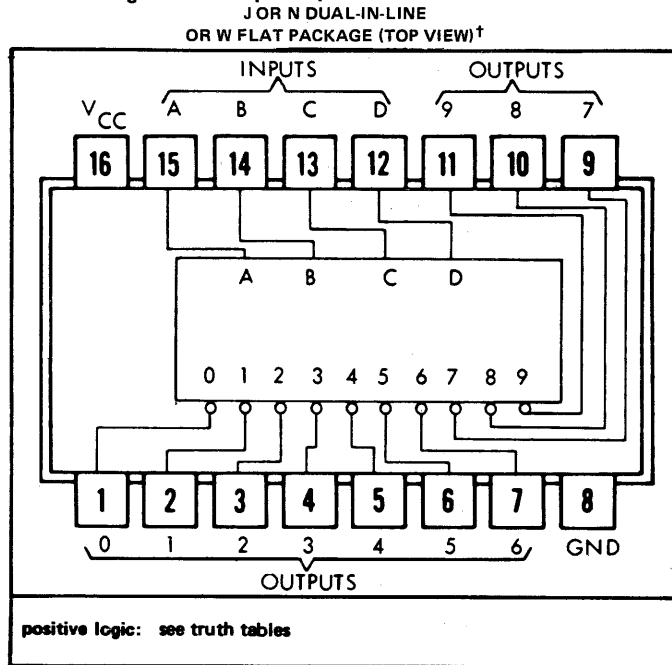
Also for applications as

- 4-Line-to-16-Line Decoders
- 3-Line to 8-Line Decoders
- featuring diode-clamped inputs

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The SN5442/SN7442 BCD-to-decimal, SN5443/SN7443 excess-3-to-decimal, and SN5444/SN7444 excess-3-gray-to-decimal decoders feature familiar transistor-transistor-logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt and power dissipation is typically 140 milliwatts. Full fan-out of 10 is available at all outputs.



[†]Pin assignments for these circuits are the same for all packages.

SN5442/SN7442

BCD
INPUT

SN5443/SN7443

EXCESS 3
INPUT

SN5444/SN7444

EXCESS 3 GRAY
INPUT

ALL TYPES
DECIMAL
OUTPUT

D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	0	1	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1
0	0	1	0	0	1	0	1	0	1	1	1	1	0	1	1	1	1	1	1	1	1
0	0	1	1	0	1	1	0	0	1	0	1	1	1	0	1	1	1	1	1	1	1
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0	1	1	0	0	1	0	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1
1	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
1	0	0	1	0	1	1	0	0	1	1	0	1	1	1	1	1	1	1	1	1	0
1	0	1	0	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	0	1	1	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

CIRCUIT TYPES SN5442, SN5443, SN5444, SN7442, SN7443, SN7444 4-LINE-TO-10-LINE DECODERS (1-OF-10)

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (See Note 1)	7 V
Input Voltage, V_{in} (See Note 1)	5.5 V
Operating Free-Air Temperature Range: SN5442, SN5443, SN5444 Circuits	−55°C to 125°C
SN7442, SN7443, SN7444 Circuits	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V _{CC} (See Note 1): SN5442, SN5443, SN5444 Circuits	4.5	5	5.5	V
SN7442, SN7443, SN7444 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output (N)			10	

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	1 and 2		2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	1 and 2				0.8	V
$V_{out(1)}$ Logical 1 output voltage	2	$V_{CC} = \text{MIN}, V_{in(1)} = 2 \text{ V}, V_{in(0)} = 0.8 \text{ V}, I_{load} = -400 \mu\text{A}$	2.4			V
$V_{out(0)}$ Logical 0 output voltage	1	$V_{CC} = \text{MIN}, V_{in(1)} = 2 \text{ V}, V_{in(0)} = 0.8 \text{ V}, I_{sink} = 16 \text{ mA}$			0.4	V
$I_{in(1)}$ Logical 1 level input current (each input)	3	$V_{CC} = \text{MAX}, V_{in} = 2.4 \text{ V}$ $V_{CC} = \text{MAX}, V_{in} = 5.5 \text{ V}$			40 1	μA mA
$I_{in(0)}$ Logical 0 level input current (each input)	4	$V_{CC} = \text{MAX}, V_{in} = 0.4 \text{ V}$			−1.6	mA
I_{OS} Short-circuit output current§	5	$V_{CC} = \text{MAX}$	−20 −18		−55 −55	mA mA
I_{CC} Supply current	4	$V_{CC} = \text{MAX}$		28 28	41 56	mA mA

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switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}, N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0} Propagation delay time to logical 0 level through two logic levels	6	$C_L = 15 \text{ pF}, R_L = 400 \Omega$	10	22	30	ns
t_{pd0} Propagation delay time to logical 0 level through three logic levels	6	$C_L = 15 \text{ pF}, R_L = 400 \Omega$		23	35	ns
t_{pd1} Propagation delay time to logical 1 level through two logic levels	6	$C_L = 15 \text{ pF}, R_L = 400 \Omega$	10	17	25	ns
t_{pd1} Propagation delay time to logical 1 level through three logic levels	6	$C_L = 15 \text{ pF}, R_L = 400 \Omega$		26	35	ns

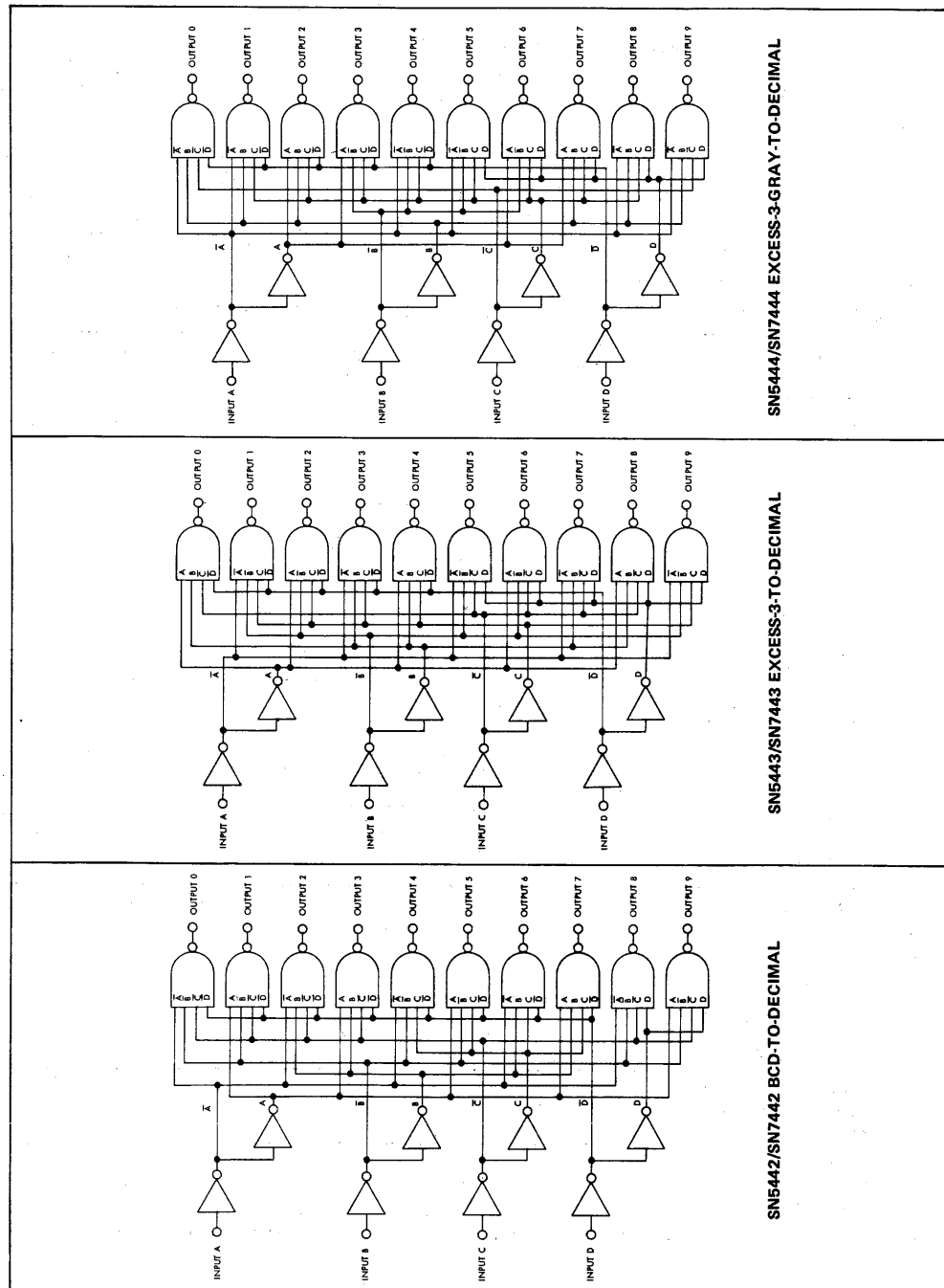
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

CIRCUIT TYPES SN5442, SN5443, SN5444, SN7442, SN7443, SN7444 **4-LINE-TO-10-LINE DECODERS (1-OF-10)**

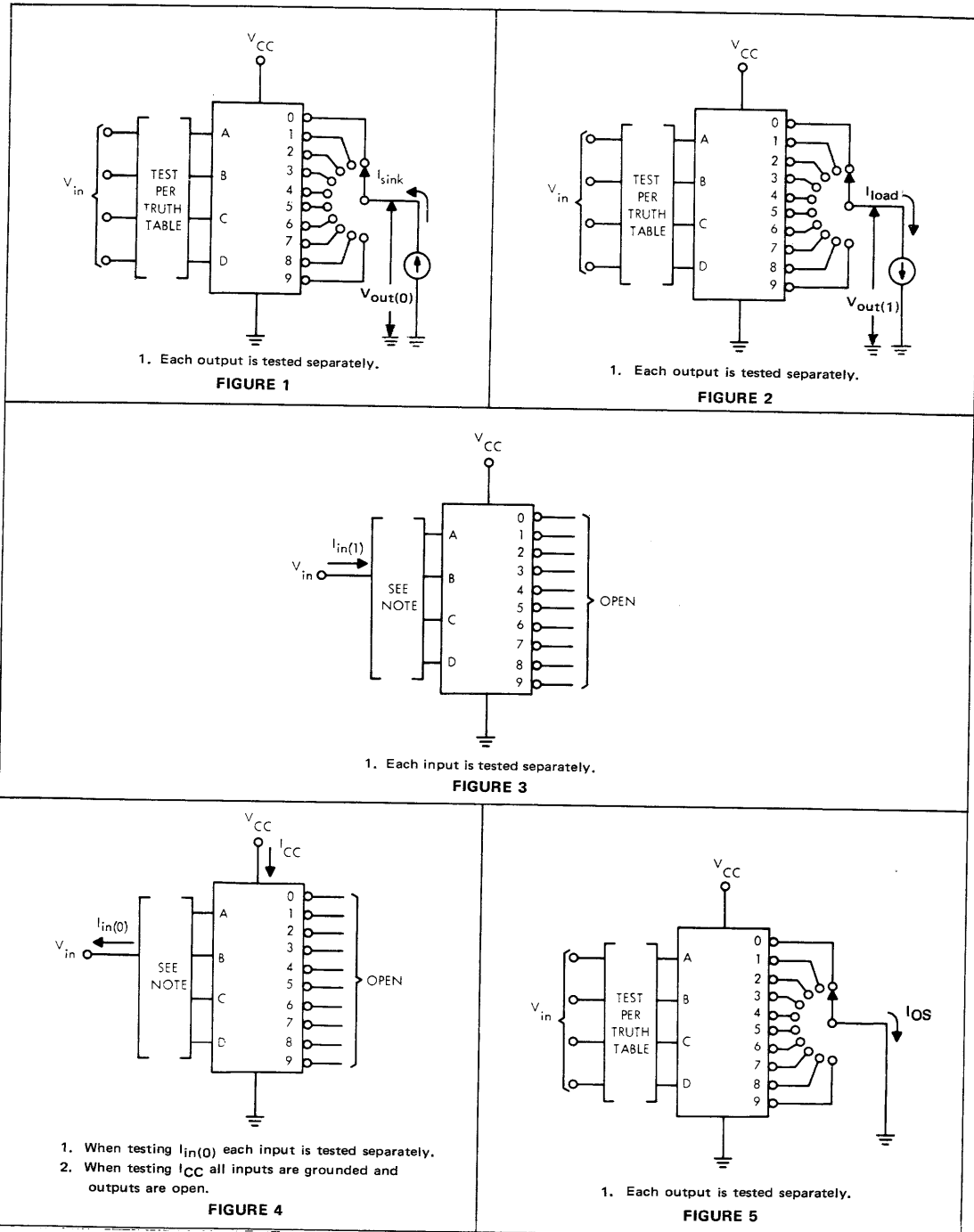
functional block diagrams



**CIRCUIT TYPES SN5442, SN5443, SN5444,
SN7442, SN7443, SN7444
4-LINE-TO-10-LINE DECODERS (1-OF-10)**

PARAMETER MEASUREMENT INFORMATION

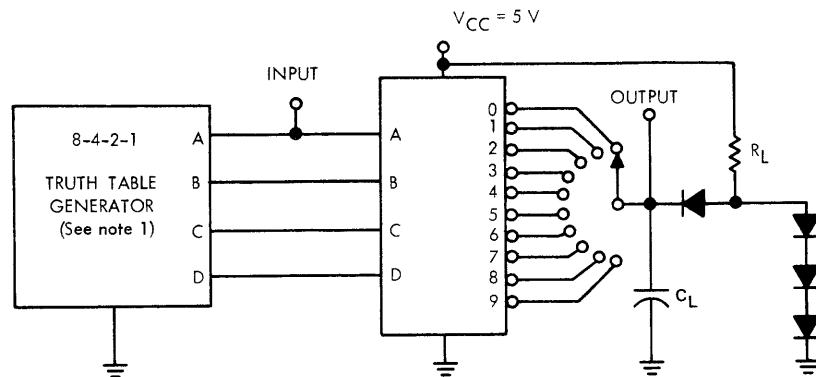
d-c test circuits[†]



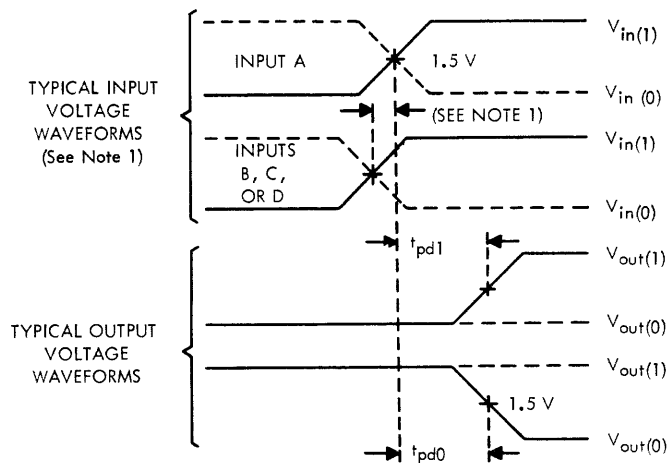
[†]Arrows indicate actual direction of current flow

**CIRCUIT TYPES SN5442, SN5443, SN5444,
SN7442, SN7443, SN7444
4-LINE-TO-10-LINE DECODERS (1-OF-10)**

switching characteristics



TEST CIRCUIT



- NOTES: 1. The truth table generator has the following characteristics:
 $V_{out(1)} \geq 2.4 \text{ V}$, $V_{out(0)} \leq 0.4 \text{ V}$, t_r and $t_f < 10 \text{ ns}$, and
 $\text{PRR} = 1 \text{ MHz}$. Input B, C, and D transitions occur simultaneously with or prior to input A transitions.
 2. C_L includes probe and jig capacitance.
 3. All diodes are 1N3064.

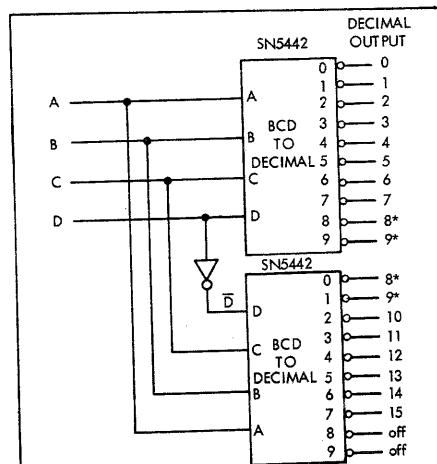
FIGURE 6—SWITCHING TIMES

CIRCUIT TYPES SN5442, SN5443, SN5444, SN7442, SN7443, SN7444 4-LINE-TO-10-LINE DECODERS (1-OF-10)

TYPICAL APPLICATIONS

decoding binary-to-decimal with SN5442/SN7442,

Figure A demonstrates a method for utilizing two SN5442/SN7442 decoders to perform 4-wire to 16-wire (1-of-16) decoding. Inputs A, B, and C of the two decoders are paralleled, D is applied to one decoder, and \bar{D} is applied to the other as shown in figure A. Decimal equivalents are available as indicated. Note that decimal 8 and 9 are available from both decoders.



*These decimal outputs are available from both decoders.

FIGURE A

decoding 3-wire binary-to-octal

This application demonstrates a method for decoding 3-wire binary-to-octal using the SN5442/SN7442. See figure B. The binary code ABC is applied to the A, B, and C inputs and the D input is used as a strobe. When the strobe is taken to a logical 0 the octal data may be taken from outputs 0 through 7. Note that decimal outputs 8 and 9 are not used. See BCD truth table.

This application demonstrates a method for decoding 3-wire binary-to-octal using the SN5444/SN7444. See figure C. The binary code ABC is applied to the A, B, and D inputs respectively and the C input is used as a strobe. When the strobe is taken to a logical 1 the octal data (as identified in figure C) may be taken from outputs 1 through 8. Note that outputs 0 and 9 are not used.

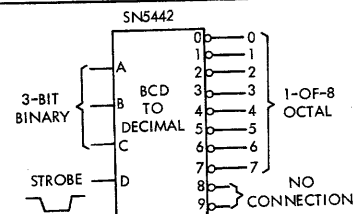


FIGURE B

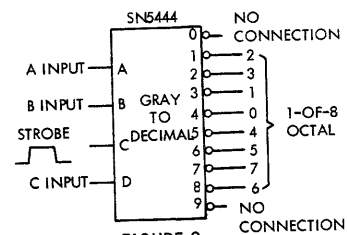


FIGURE C

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