RL78/G12

A/D Converter (Software Trigger and Sequential Conversion Modes)

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Introduction

This application note describes the procedures for performing A/D conversion on analog voltages using the RL78/G12's A/D converter (supporting software trigger and sequential conversion modes).

The sample program discussed in this application note performs data conversion on the A/D conversion results and places the converted values in the RL78/G12's internal RAM.

Target Device

RL78/G12

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specification

This application note provides examples of using the software trigger and sequential conversion modes of the A/D converter. The A/D converter is placed in select mode and the analog signal input from the P20/ANI0 pin is converted to digital values. Subsequently, the conversion result is subjected to data conversion (shifting the data to the right) and the result is stored in the RL78/G12's internal RAM.

Table 1.1 lists the peripheral function to be used and its usage and figure 1.1 shows the outline of the conversion operation of the A/D converter.

Table 1.1 Peripheral Function to be Used and its Usage

Peripheral Function	Usage
A/D converter	Converts the level of the analog signal input from the P20/ANI0 pin.

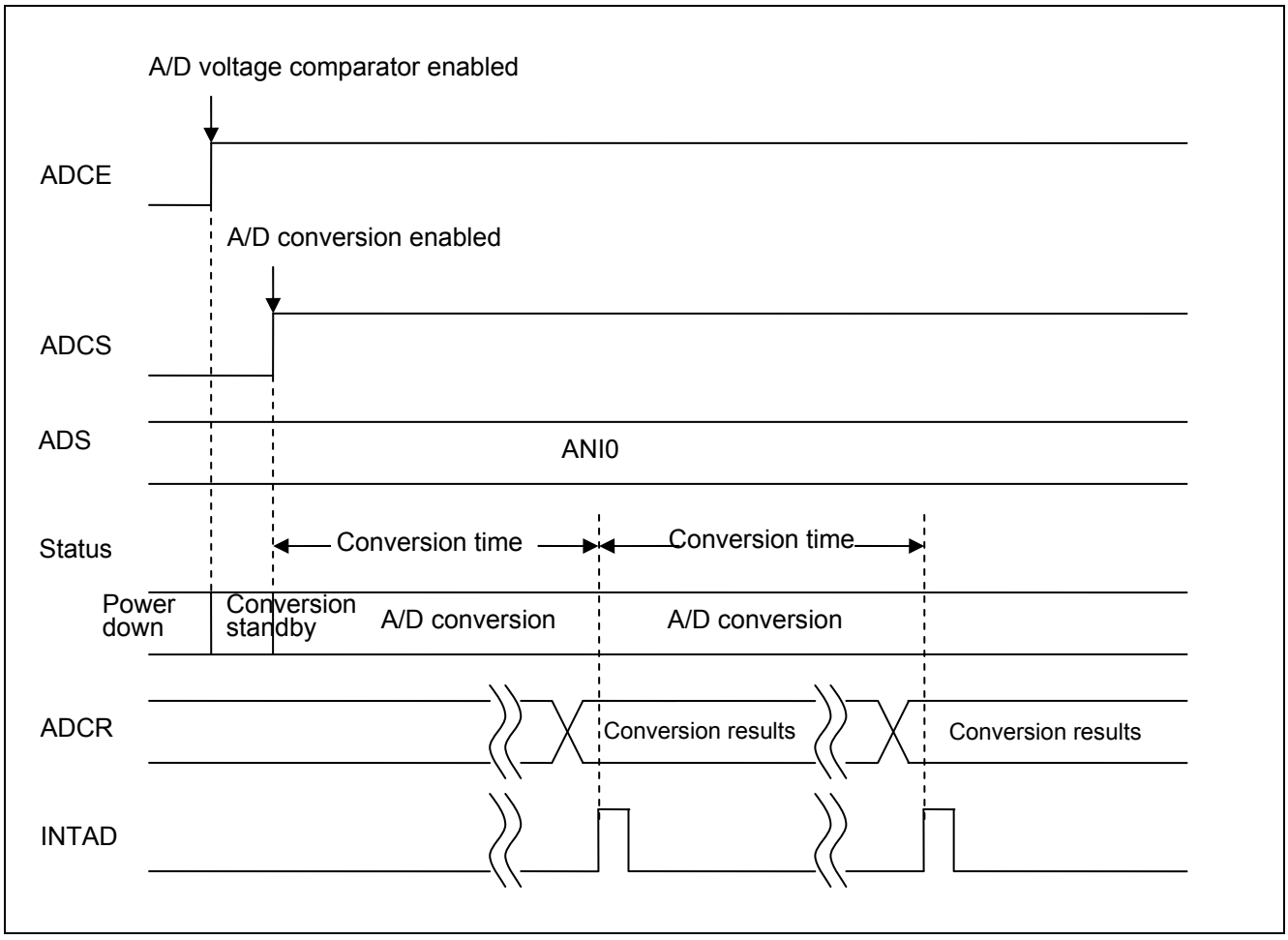


Figure 1.1 Outline of the A/D Converter Conversion Processing

2. Operation Evaluate Conditions

The sample code contained in this application note has been evaluated under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G12 (R5F1026A)
Operating frequency	High-speed on-chip oscillator (HOCO) clock: 24 MHz CPU/peripheral hardware clock: 24 MHz
Operating voltage	5.0 V (can run on a voltage range of 3.9 V to 5.5 V.) LVD operation (VLVI): Reset mode 3.75 V +/- 0.07 V
Integrated development environment	Cube Suite+ V1.01.01 from Renesas Electronics Corp.
Assembler	RA78K0R V1.50 from Renesas Electronics Corp.
Board used	RL78/G12 target board (QB-R5F1026A-TB)

3. Related Application Note

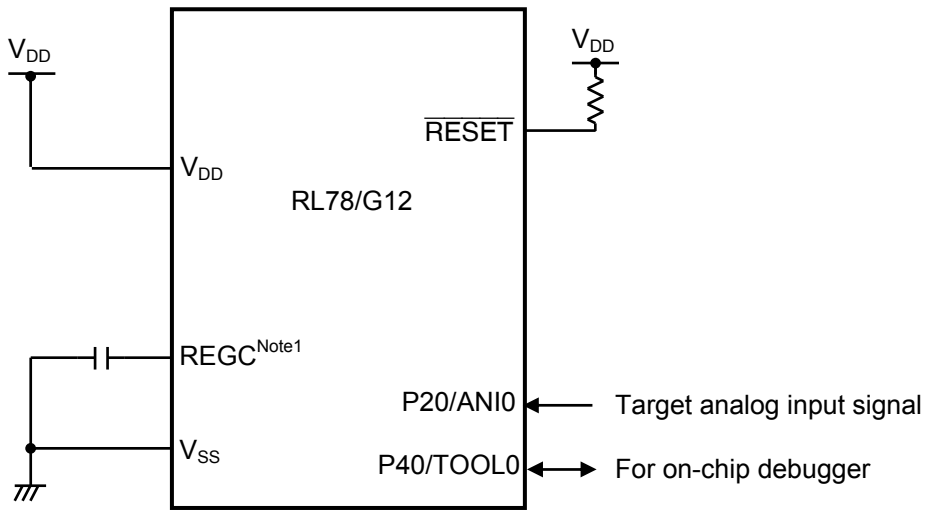
The application note that is related to this application note is listed below for reference.

RL78/G12 Initialization (R01AN1030E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.



Note 1. 30-pin products only.

Figure 4.1 Hardware Configuration

Notes 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-dedicated ports separately to V_{DD} or V_{SS} via a resistor).

2. V_{DD} must be held at not lower than the LVD detection voltage (V_{LVI}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the pin to be used and its function.

Table 4.1 Pin to be Used and its Function

Pin Name	I/O	Description
P20/ANI0	Input	A/D converter analog input port

5. Description of the Software

5.1 Operation Outline

This sample code performs A/D conversion on the analog voltage that is input to pin ANI0 using the software trigger and sequential conversion modes of the A/D converter. It awaits the end of A/D conversion in HALT mode. After A/D conversion is completed, the sample code shifts the result of A/D conversion 6 bits to the right and places the result in the internal RAM of the RL78/G12.

(1) Initialize the A/D converter.
<Setup conditions>
- Pin P20/ANI0 is used for the analog input.
- A/D conversion channel selection mode is set to select mode.
- A/D conversion operation mode is set to sequential conversion mode.
- A/D conversion is started using the software trigger.
- The A/D conversion end interrupt (INTAD) is used.

(2) The sample program sets the ADCS bit of the ADM0 register to 1 (A/D conversion start) to start A/D conversion and executes the HALT instruction and into the HALT mode and wait for an A/D conversion end interrupt.

(3) After completing the A/D conversion of the voltage input from pin ANI0, the A/D converter transfers the result of A/D conversion to the ADCR register and generates an A/D conversion end interrupt.

(4) On release from the HALT mode in response to the A/D conversion end interrupt, the sample program reads the result of A/D conversion from the ADCR register, shifts the result 6 bits to the right, and stores the shifted data in the internal RAM of the RL78/G12.

(5) The chip returns to the HALT mode and waits for a next A/D conversion end interrupt.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Setting Value	Description
000C0H	01101110B	Disables the watchdog timer. (Stops counting after the release of the reset state.)
000C1H	01010011B	LVD reset mode, 3.75 V +/- 0.07 V
000C2H	11100000B	HS mode, HOCO: 24 MHz
000C3H	10000101B	Enables the on-chip debugger.

5.3 List of Variables

Table 5.2 lists the variable that is used by this sample program.

Table 5.2 Variable

Type	Variable Name	Contents	Function Used
16-bit variable	RADCBUF	Area for storing the A/D conversion results	main

5.4 List of Functions (Subroutine)

Table 5.3 lists the functions (subroutine) that are used by this sample program.

Table 5.3 Functions (Subroutine)

Function Name	Outline
SINIADC	Initialize A/D converter.
SSTARTAD	Starts A/D conversion.

5.5 Function (Subroutine) Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] RESET_START

Synopsis	Initialize CPU at reset start.
Explanation	Sets the stack pointer and, after making initial hardware settings, calls the main processing routine.
Arguments	None
Return value	None
Remarks	None

[Function Name] SINIADC

Synopsis	Initialize A/D converter.
Explanation	Sets the A/D converter to sequential conversion mode enabled, 10-bit conversion.
Arguments	None
Return value	None
Remarks	None

[Function Name] SSTARTAD

Synopsis	Start A/D conversion.
Explanation	Enables the A/D conversion end interrupt and starts A/D conversion operation.
Arguments	None
Return value	None
Remarks	None

5.6 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

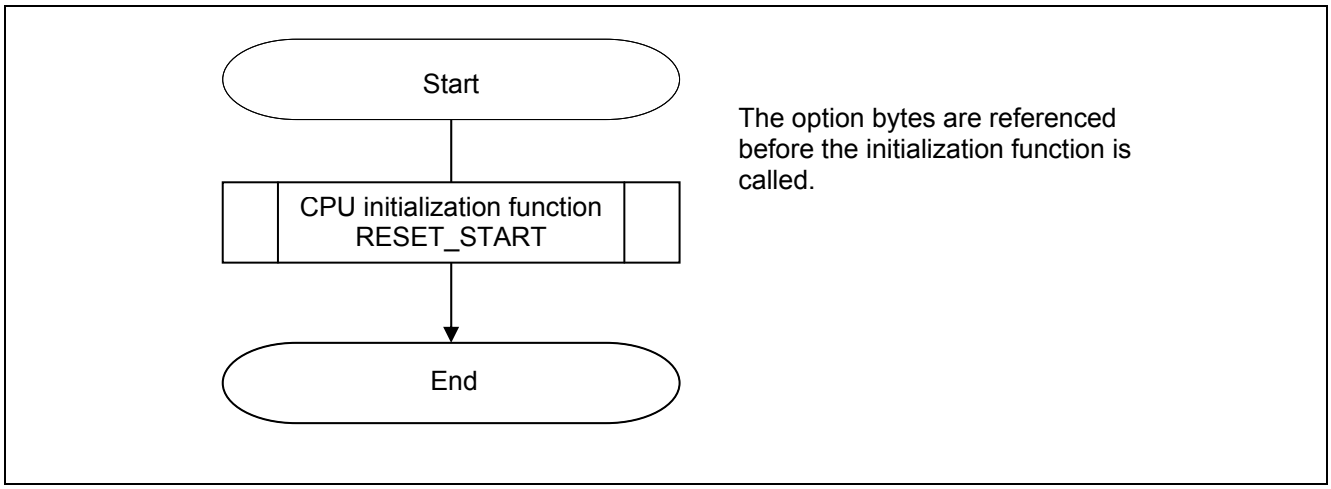


Figure 5.1 Overall Flow

5.6.1 CPU Initialization Function

Figure 5.2 shows a flowchart of the CPU initialization function.

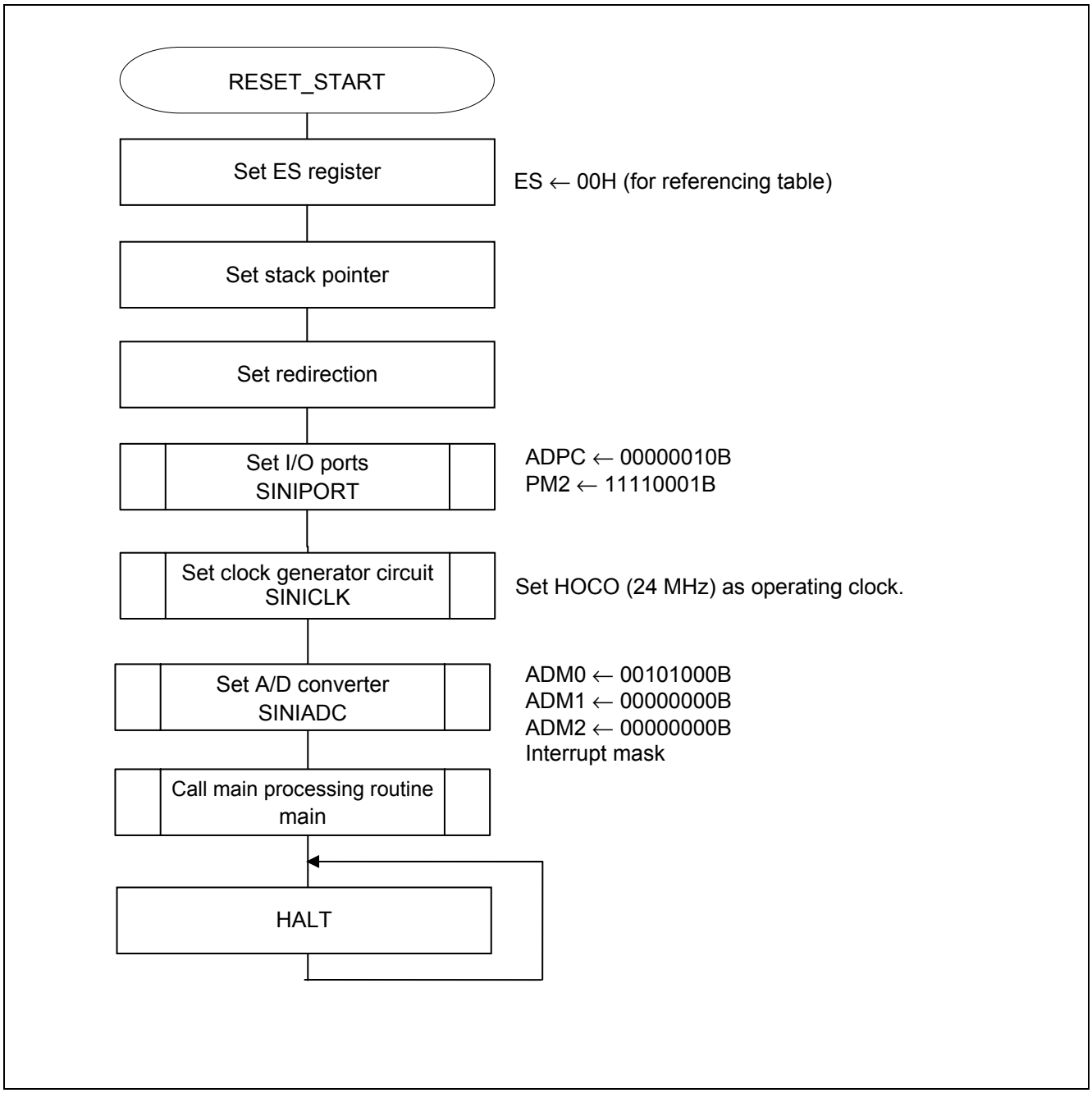


Figure 5.2 CPU Initialization

5.6.2 I/O Port Setup

Figure 5.3 shows the flowchart for I/O port setup.

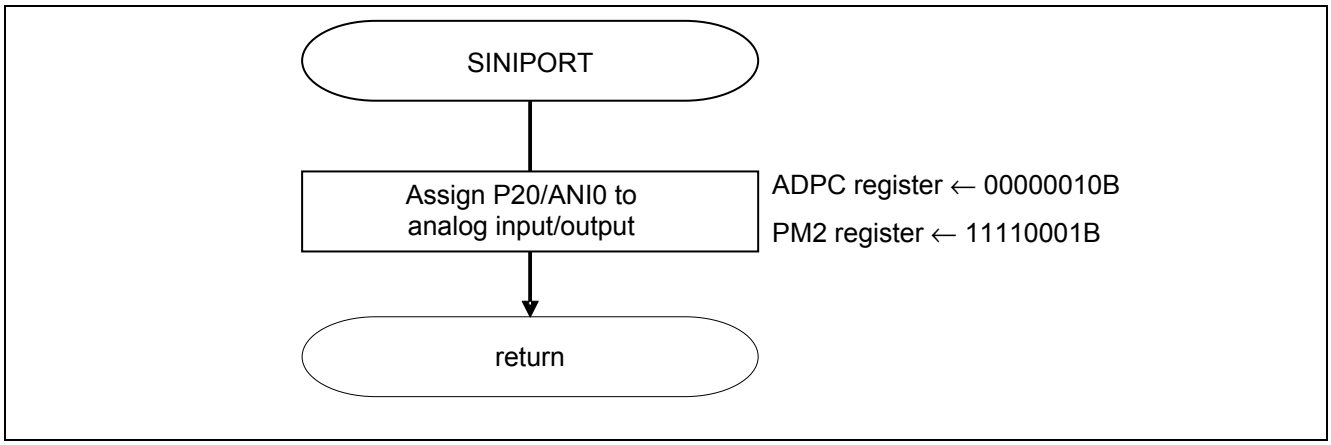


Figure 5.3 I/O Port Setup

Notes 1. Refer to the section entitled "Flowcharts" in RL78/G12 Initialization Application Note (R01AN1030E) for the configuration of the unused ports.

2. Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via separate resistors, independently.

Setting Up the Channel to be Used for A/D Conversion

- A/D port configuration register (ADPC)
  Switches between A/D converter analog input and digital I/O port.
- Port mode register 2 (PM2)
  Selects the I/O mode of each port.

Symbol: ADPC

7	6	5	4	3	2	1	0
0	0	0	0	ADPC3	ADPC2	ADPC1	ADPC0
0	0	0	0	0	0	1	0

Bits 3 to 0:

ADPC3	ADPC2	ADPC1	ADPC0	Available Analog Input
0	0	0	0	ANI0 to ANI14
			1	None
		1	0	ANI0
			1	ANI0 and ANI1
		0	0	ANI0 to ANI2
			1	ANI0 to ANI3
		1	0	ANI0 to ANI4
			1	ANI0 to ANI5
	1	0	0	ANI0 to ANI6
			1	ANI0 to ANI7
Other than above				Setting prohibited

Symbol: PM2

7	6	5	4	3	2	1	0
PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20
1	1	1	1	x	x	x	1

Bit 0:

PM20	PM20 I/O Mode Select
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Note: For details on the procedure for setting up the registers, refer to RL78/G12 User's Manual: Hardware.

5.6.3 Clock Generator Circuit Settings

Figure 5.4 shows a flowchart of the clock generator circuit settings.

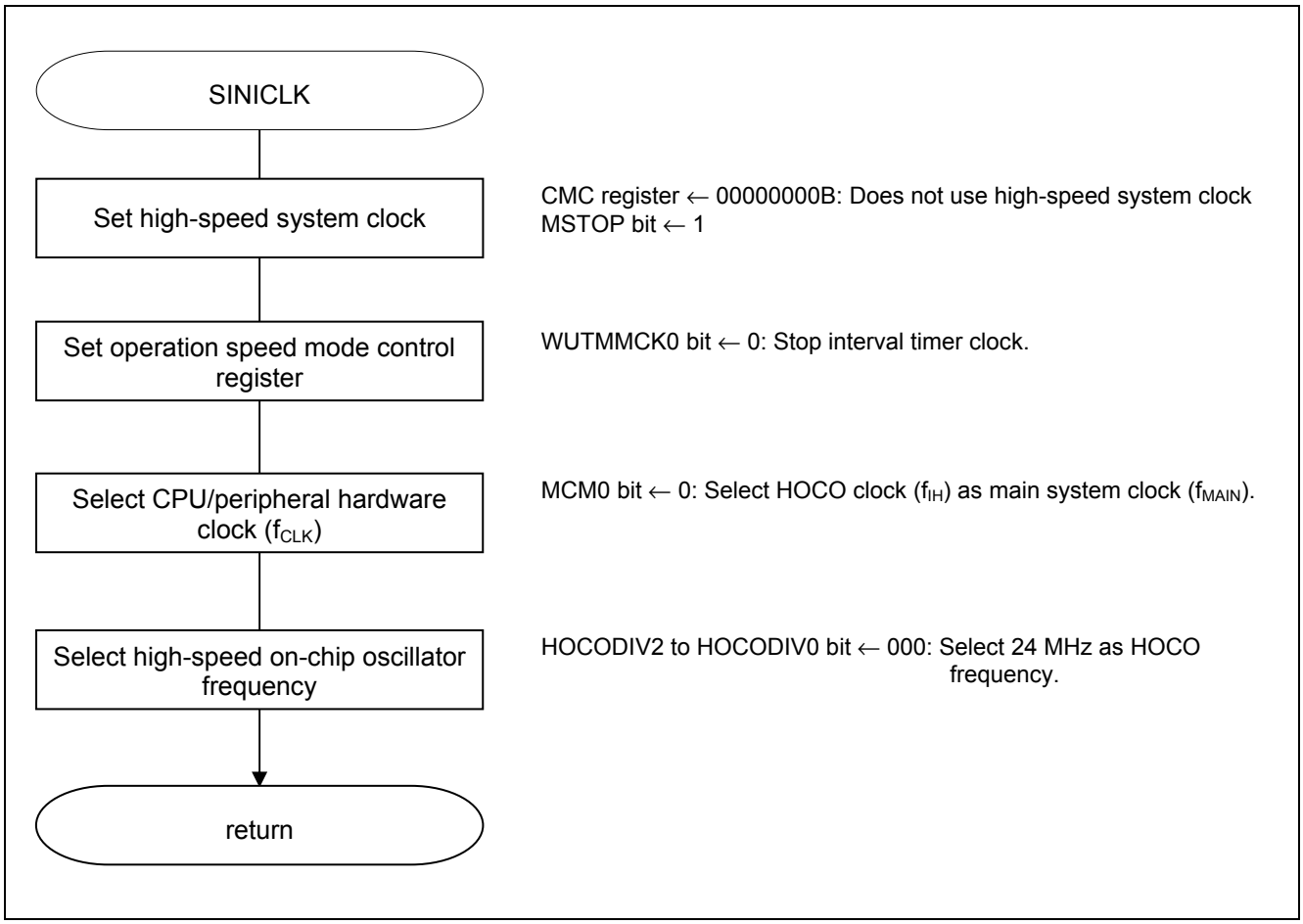


Figure 5.4 Clock Generator Circuit Settings

Note: For details on the procedure for clock generator circuit settings (SINICLK), refer to the section entitled "Flowcharts" in RL78/G12 Initialization Application Note (R01AN1030E).

5.6.4 Setting up the A/D Converter

Figure 5.5 shows the flowchart for setting up the A/D converter.

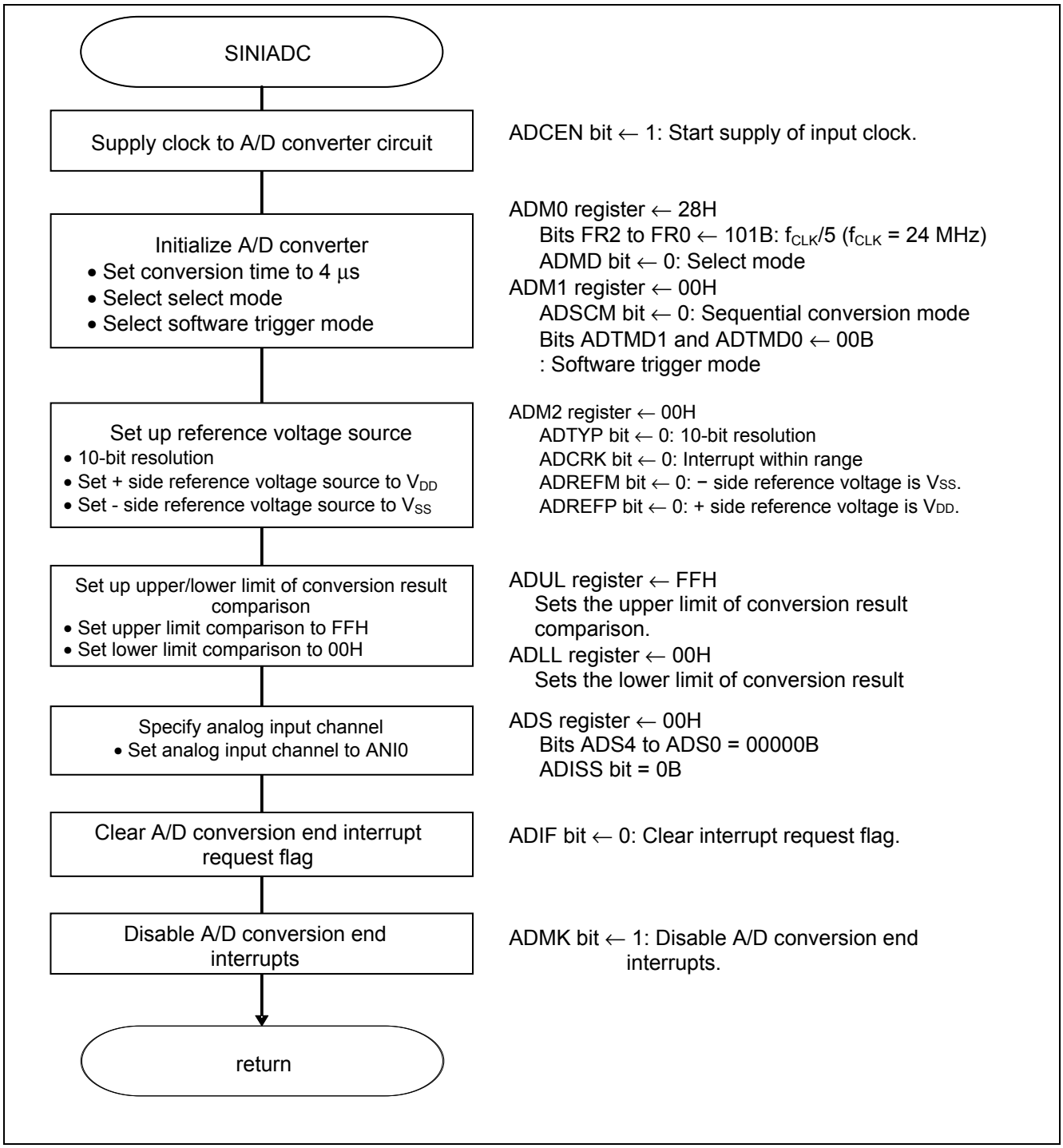


Figure 5.5 A/D Converter Setup Flowchart

Starting the Supply of Clock to the A/D Converter

- Peripheral enable register 0 (PER0)
  Starts the supply of the clock to the A/D converter.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN
x	0	1	x	x	x	0	x

Bit 5:

ADCEN	A/D converter input clock control Supply
0	Stops input clock supply.
1	Enables input clock supply.

Note: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Setting Up the A/D Conversion Time and Operation Mode

- A/D converter mode register 0 (ADM0)
  Controls the A/D conversion operation.
  Specifies the A/D conversion channel selection mode.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	0	1	0	1	0	0	x

Bit 6:

ADMD	A/D channel selection mode select
0	Select mode
1	Scan mode

Bits 5 to 1:

ADM0					Mode	Conversion Time Selection					Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16M Hz	f_{CLK} = 24 MHz	
0	0	0	0	0	Standard 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/64
		1							38 µs	25.33 µs	f_{CLK}/32
	1	0						38 µs	19 µs	12.67 µs	f_{CLK}/16
		1					38 µs	19 µs	9.5 µs	6.33 µs	f_{CLK}/8
1	0	0					28.5 µs	14.25 µs	7.125 µs	4.75 µs	f_{CLK}/6
		1					23.75 µs	11.875 µs	5.938 µs	3.96 µs	f_{CLK}/5
	1	0					19 µs	9.5 µs	4.75 µs	3.17 µs	f_{CLK}/4
		1				38 µs	9.5 µs	4.75 µs	2.375 µs	Setting prohibited	f_{CLK}/2
0	0	0	0	1	Standard 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/64
		1							34 µs	22.67 µs	f_{CLK}/32
	1	0						34 µs	17 µs	11.33 µs	f_{CLK}/16
		1					34 µs	17 µs	8.5 µs	5.67 µs	f_{CLK}/8
1	0	0					25.5 µs	12.75 µs	6.375 µs	4.25 µs	f_{CLK}/6
		1					21.25 µs	10.625 µs	5.3125 µs	3.54 µs	f_{CLK}/5
	1	0					17 µs	8.5 µs	4.25 µs	2.83 µs	f_{CLK}/4
		1				34 µs	8.5 µs	4.25 µs	2.125 µs	Setting prohibited	f_{CLK}/2
x	x	x	1	0	Low voltage 1	Setting prohibited					—
				1	Low voltage 2	Setting prohibited					—

Note: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Setting Up the A/D Conversion Trigger Mode

- A/D converter mode register 1 (ADM1)
  Selects the A/D conversion trigger mode.
  Selects the A/D conversion mode.

Symbol: ADM1

7	6	5	4	3	2	1	0
ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0
0	0	0	0	0	0	0	0

Bits 1 and 0:

ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	0	End of timer channel 1 count or capture end interrupt signal (INTTM01)
1	1	12 bits interval timer
Other than above		Setting prohibited

Bit 5:

ADSCM	Specification of the A/D Conversion Mode
0	Sequential conversion mode
1	One-shot conversion mode

Bits 7 and 6:

ADTMD1	ADTMD0	Selection of the Hardware Trigger Signal
0	—	Software trigger mode
1	0	Hardware trigger no-wait mode
	1	Hardware trigger wait mode

Note: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Setting Up the Reference Voltage

- A/D converter mode register 2 (ADM2)
  Sets up the reference voltage source.

Symbol: ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADCRK	AWC	0	ADTYP
0	0	0	0	0	0	0	0

Bit 0:

ADTYP	Selection of the A/D Conversion Resolution
0	10-bit resolution
1	8-bit resolution

Bit 2:

AWC	Specification of the Wakeup Function (SNOOZE mode)
0	Do not use the SNOOZE mode function.
1	Use the SNOOZE mode function.

Bit 3:

ADCRK	Checking the Upper Limit and Lower Limit Conversion Result Values
0	The interrupt signal (INTAD) is output when the ADLL register ≤ the ADCR register ≤ the ADUL register.
1	Interrupt signal (INTAD) is output when ADCR register < ADLL register and ADUL register < ADCR register.

Bit 5:

ADREFM	Selection of the – Side Reference Voltage Source of the A/D Converter
0	Supplied from V_{SS}.
1	Supplied from P21/AVREFM/ANI1.

Bits 7 and 6:

ADREFP1	ADREFP0	Selection of the + Side Reference Voltage Source of the A/D Converter
0	0	Supplied from V_{DD}.
	1	Supplied from P20/AVREFP/ANI0.
1	0	Supplied from internal reference voltage (1.44 V).
	1	Setting prohibited

Note: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Setting up the Conversion Result Comparison Upper Limit/Lower Limit

- Conversion result comparison upper limit setting register (ADUL)
- Conversion result comparison lower limit setting register (ADLL)

Symbol: ADUL

7	6	5	4	3	2	1	0
ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0
1	1	1	1	1	1	1	1

Symbol: ADLL

7	6	5	4	3	2	1	0
ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0
0	0	0	0	0	0	0	0

Specifying the Input Channel

- Analog input channel specification register (ADS)
  Specifies the input channel for the analog voltage to be subjected to A/D conversion.

Symbol: ADS

7	6	5	4	3	2	1	0
ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
0	0	0	0	0	0	0	0

Bits 7, 4 to 0:

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog Input Channel	Input Source[Note1]
0	0	0	0	0	0	ANI0	P20/ANI0 pin/AV_{REFP} pin
					1	ANI1	P21/ANI1 pin/AV_{REFM} pin
				1	0	ANI2	P22/ANI2 pin
					1	ANI3	P23/ANI3 pin
	1	0	0	0	0	ANI16	P10/ANI16 pin P01/ANI16 pin
					1	ANI17	P11/ANI17 pin P00/ANI17 pin
				1	0	ANI18	P12/ANI18 pin P147/ANI18 pin
					1	ANI19	P13/ANI19 pin P120/ANI19 pin
			1	0	0	ANI20	P14/ANI20 pin —
					1	ANI21	P42/ANI21 pin —
				1	0	ANI22	P41/ANI22 pin —
1	0	0	0	0	0	—	Temperature sensor output
					1	—	Internal reference voltage output (1.45 V)
Other than above						Setting prohibited	

Note 1. First line applies to 20- and 24-pin products; second line applies to 30-pin products.

Note: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Setting Up End of A/D Conversion Interrupts

- Interrupt request flag register (IF1L)
  Clears the interrupt request flag.
- Interrupt mask flag register (MK1L)
  Disables interrupts.

Symbol: IF1L

7	6	5	4	3	2	1	0
—	FLIF	MDIF	KRIF	TMKAIF	ADIF	TMIF03	TMIF02
x	x	x	x	x	0	x	x

Bit 2:

ADIF	Interrupt Request Flag
0	No interrupt request signal is generated.
1	Interrupt request is generated, interrupt request status

Symbol: MK1L

7	6	5	4	3	2	1	0
—	FLMK	MDMK	KRMK	TMKAMK	ADMK	TMMK03	TMMK02
x	x	x	x	x	1	x	x

Bit 2:

ADMK	Interrupt Processing Control
0	Enables interrupt processing.
1	Disables interrupt processing.

Note: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

5.6.5 Main Processing

Figure 5.6 shows the flowchart for the main processing routine.

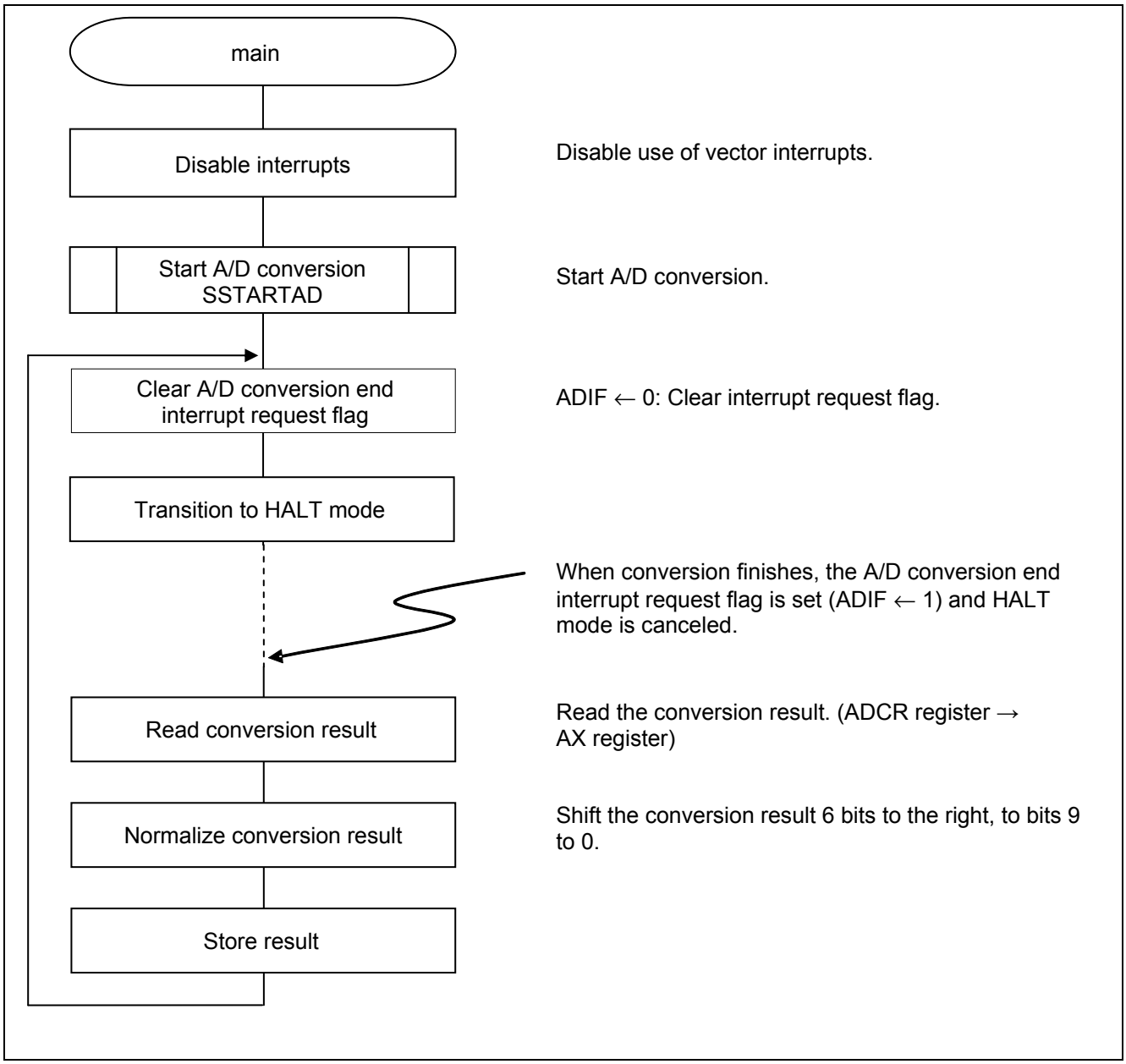


Figure 5.6 Main Processing

5.6.6 A/D Conversion Start Processing

Figure 5.7 shows a flowchart of the A/D conversion start processing.

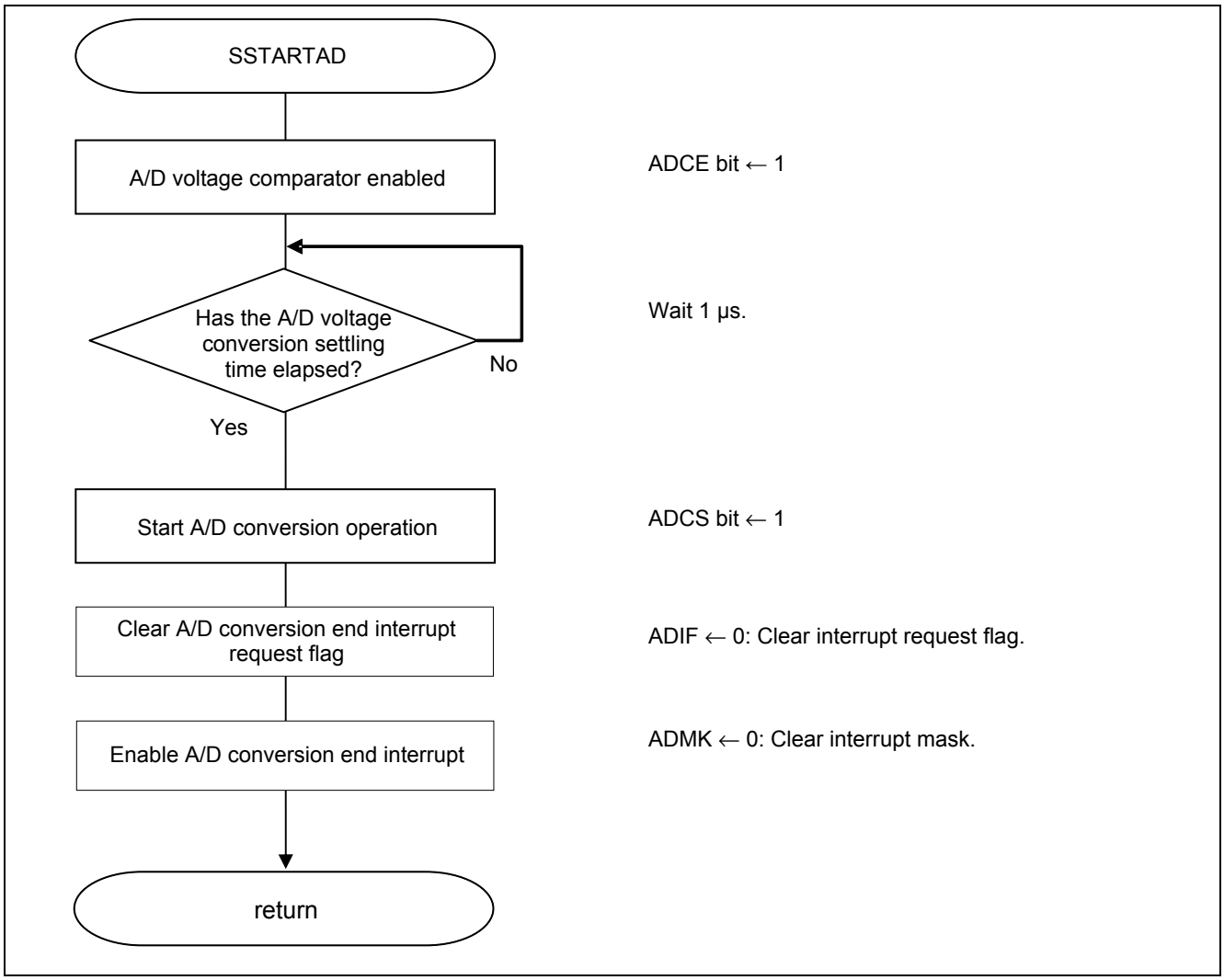


Figure 5.7 A/D Conversion Start Processing

Starting Conversion Operation

- A/D converter mode register 0 (ADM0)
  Controls the A/D conversion operation.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV2	ADCE
1	x	x	x	x	x	x	1

Bit 0:

ADCE	A/D Voltage Comparator Operation Control
0	Stops A/D voltage comparator operation.
1	Enables A/D voltage comparator operation.

Bit 7:

ADCS	A/D Conversion Operation Control
0	Stops conversion operation.
1	Enables conversion operation.

Note: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

- RL78/G12 User's Manual: Hardware (R01UH0200E)
- RL78 Family User's Manual: Software (R01US0015E)
  (The latest versions of the documents are available on the Renesas Electronics Website.)
- Technical Updates/Technical Brochures
  (The latest versions of the documents are available on the Renesas Electronics Website.)

Website and Support

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Revision Record	RL78/G12 A/D Converter (Software Trigger and Sequential Conversion Modes)

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 30, 2012	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

— The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

— The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

— The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

— When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

— The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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