EPSON
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S1D19600 Series
Technical Manual

SEIKO EPSON CORPORATION

Rev.1.1

NOTICE

Configuration of product number

•DEVICES

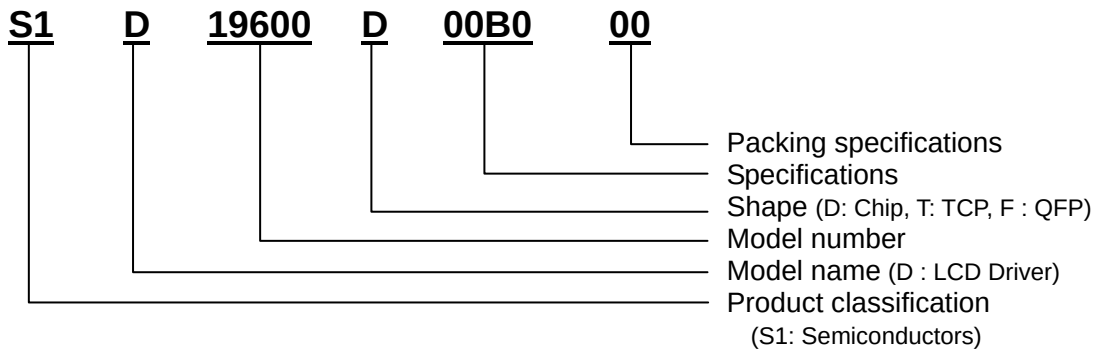


Table of Contents

1. DESCRIPTION

The S1D19600 series is a 1-chip driver for driving amorphous Si-TFT with built-in data RAM that contains 320 × 320 dots, supporting 16 gray scale display. It include built-in power supply circuit that all voltage level are generated for display, and it can directly connectable to MPU bus with 8bit parallel interface or 4 wire serial interface.

16, 4, and 2 gray scale are supported.

Built-in power supply circuit for LCD drive and built-in oscillator can realize display system with minimum external part.

2. FEATURES

LCD drive circuit
- Source output: 320outputs. Number of output can be selectable from 2 to 320.
  - Built-in buffer for all outputs
  - Drive load: from 10pF, 0.5KΩto 60pF, 35KΩ
- Gate output: 320outputs. Number of output can be selectable from 10 to 320.
  - 160outpus on both side of chip, and interlace driving is available.

MPU interface
- 8bit parallel (80 system MPU),
- 4-wire serial ($\overline{CS}$, SCL, SD, A0 signals)
- EEPROM interface *1
- Schmidt trigger input
- Transfer data error detection circuit.

Gray scale
- 16 gray scale (4bpp), 4 gray scale (2bpp) and 2gray scale (1bpp) are available.

Display data RAM
- RAM capacity 320 × 320 × 4 = 409,600 bits
  - When 1bpp mode: 4 frames are available.
  - When 2bpp mode: 2 frames are available.
  - When 4bpp mode and 160 lines or less: 2 frames are available.
  - Display data error detection circuit.

Convenient commands
- BLKFIL: Fill data to appointed rectangle area.
- BLIN: Blinking function

AC drive methods
- 1 line inversion, 2 line inversion, frame inversion and interlace.

Built-in circuits
- Internal logic power supply
- LCD drive power supply
- CR oscillating circuit.
- Multi-time PROM *2
  - 8bit x 2: for VCOM adjustment, 32bits: for user ID)

Operation voltages
- V_{DDI}-V_{SS} = 2.7 to 5.5V (Interface I/O power supply)
- V_{DD2}–V_{SS} = 2.7 to 5.5V (Power supply for internal power supply)
- Source voltage = Max 5.5V
- Gate voltage : VDDHG-VEE= Max 32V
- Common voltage : VCOMH-VCOML= Max 6.0V

Operation temperature range
- -40 to 110 °C

Package models available
- Au bump chip

Remark 1: Recommended EEPROM = ROHM (BR25H series) / Seiko Instruments (S-25C series). Capacity :1 to 4Kbit

Remark 2: The Multi-time PROM is for temporary memory such as VCOM adjustment data carrier from LCD module to final application. Prohibit to access (include read) the Multi time PROM after mounting final application.

3. BLOCK DIAGRAM

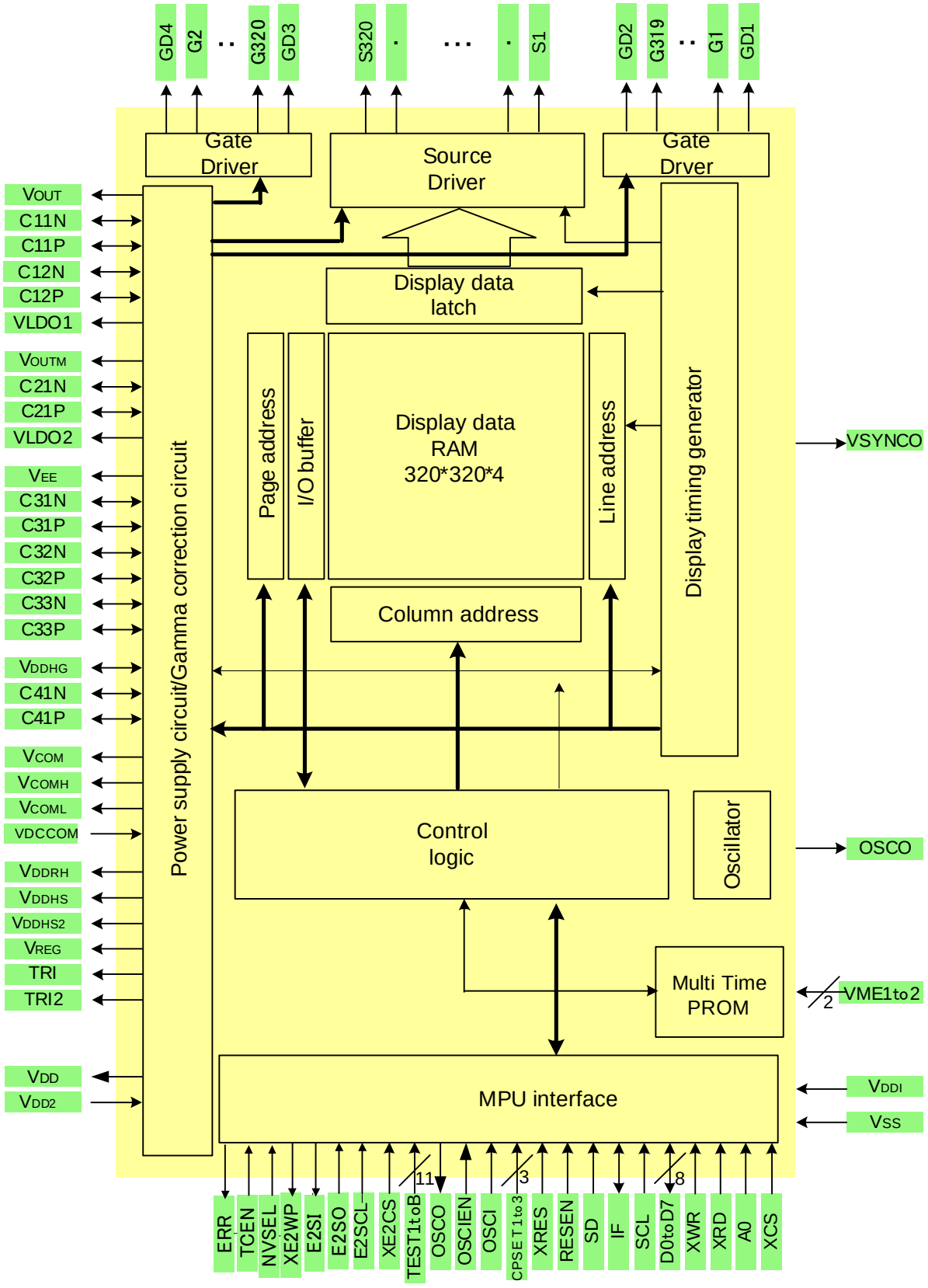


Fig.1 S1D19600 Series Block Diagram

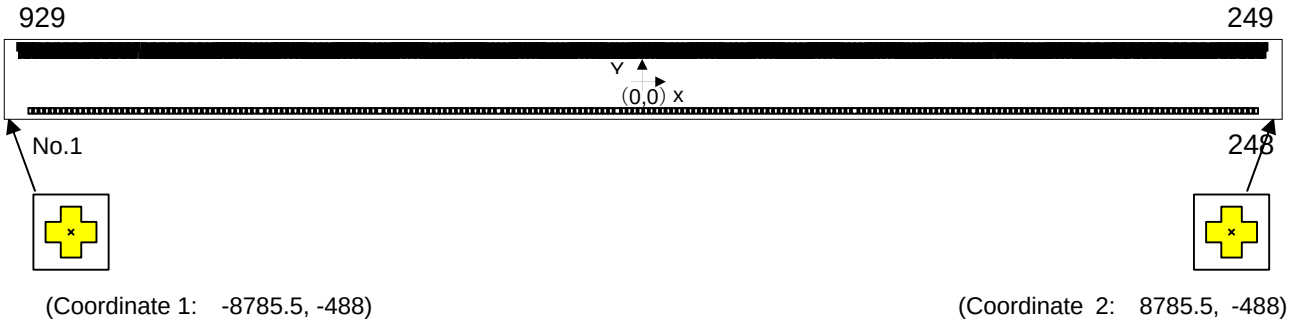
4. PIN ASSIGNMENT

4.1 S1D19600 Specifications of Chip

Table 1 Specifications of Chip

Parameter		Dimensions		Unit
		X	Y	
Chip size		17.865	1.200	mm
Chip thickness		300		μm
Bump pitch		Min.52		μm
Bump size	No. 1 to 248	44	70	μm
	No. 249 to 929	26	87	μm
Bump height		Typ.15		μm
Bump area total		2,304,262		μm^2

Note: These values are given for reference only.



(Coordinate 1: -8785.5, -488) (Coordinate 2: 8785.5, -488)

The alignment mark is put on two locations.

Fig.2 Bump Assignment Drawing (Top view from bump side)

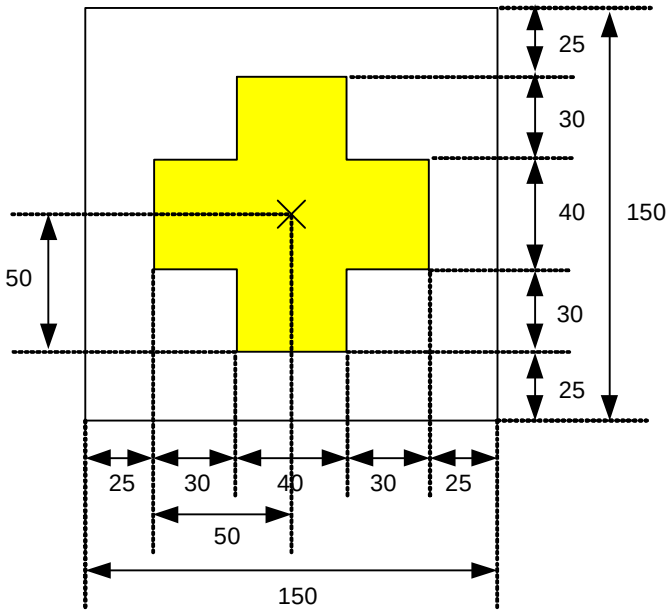


Fig.3 Alignment mark (Unit: um)

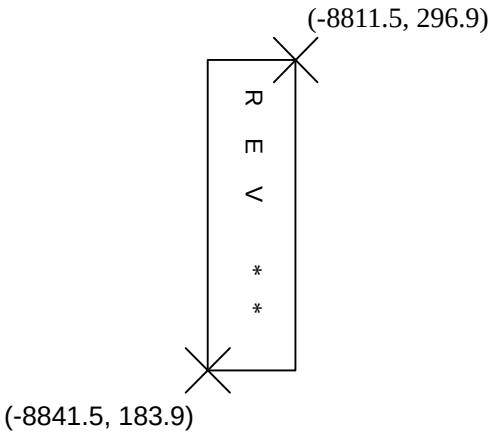
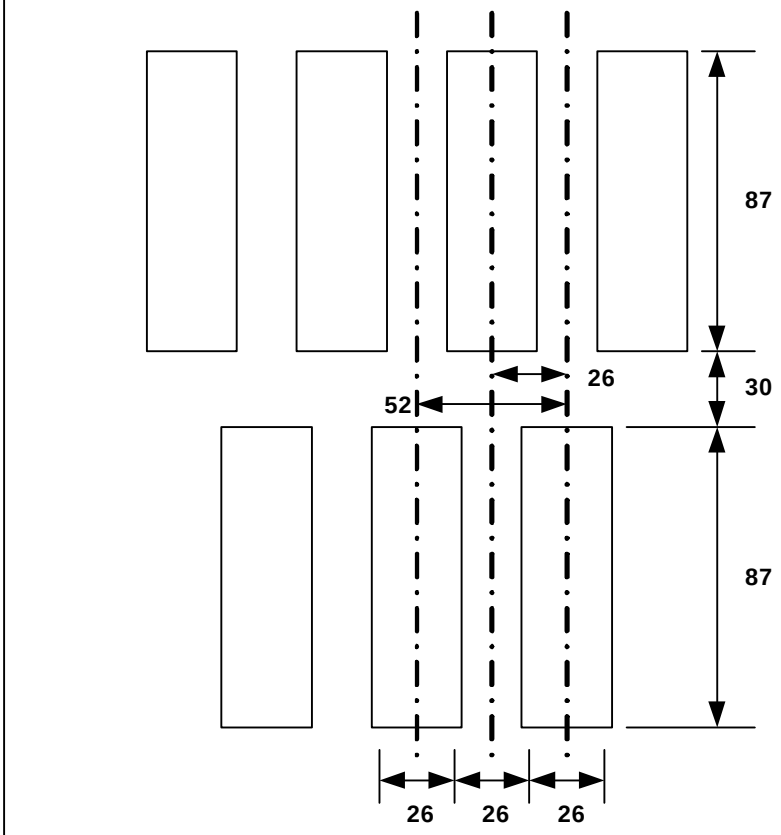


Fig.4 Revision mark

4. PIN ASSIGNMENT

S1 to S 320
G1 to G 320
GD 1 / 2 / 3 / 4
A - DDUMMY
Output side: DUMMY



I / O Pins

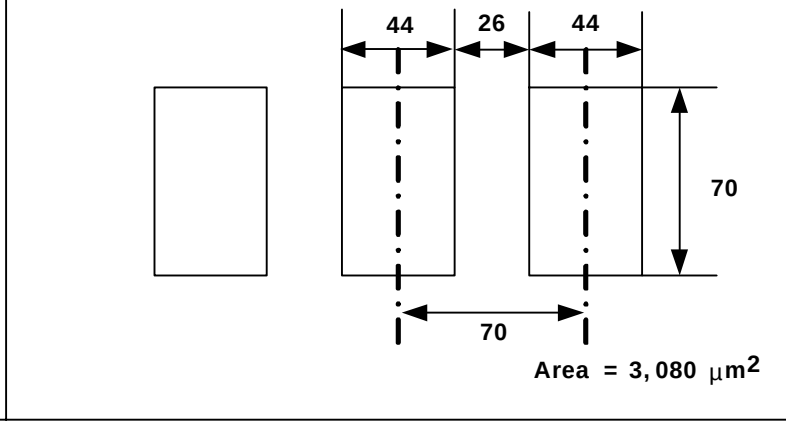


Fig.5 Bump size and layout (Unit: um)

4.2 Bump center coordinates

Table 2 Bump center coordinates

BUMP No.	Pin Name	X (μm)	Y (μm)
1	ADUMMY	-8645	-500
2	BDUMMY	-8575	-500
3	DUMMY	-8505	-500
4	VCOM	-8435	-500
5	VCOM	-8365	-500
6	VCOM	-8295	-500
7	DUMMY	-8225	-500
8	VCOMH	-8155	-500
9	VCOMH	-8085	-500
10	VCOMH	-8015	-500
11	DUMMY	-7945	-500
12	VCOML	-7875	-500
13	VCOML	-7805	-500
14	VCOML	-7735	-500
15	DUMMY	-7665	-500
16	VME1	-7595	-500
17	TEST5	-7525	-500
18	TEST4	-7455	-500
19	VME2	-7385	-500
20	VME2	-7315	-500
21	TRI2	-7245	-500
22	VSS	-7175	-500
23	VSS	-7105	-500
24	VSS	-7035	-500
25	VSS	-6965	-500
26	VDD2	-6895	-500
27	VDD2	-6825	-500
28	VDD2	-6755	-500
29	VDD2	-6685	-500
30	VDCCOM	-6615	-500
31	VDCCOM	-6545	-500
32	VDCCOM	-6475	-500
33	VDCCOM	-6405	-500
34	VLDO2	-6335	-500
35	VLDO2	-6265	-500
36	VLDO2	-6195	-500
37	VLDO2	-6125	-500
38	DUMMY	-6055	-500
39	C21P	-5985	-500
40	C21P	-5915	-500
41	C21P	-5845	-500
42	C21P	-5775	-500
43	C21P	-5705	-500
44	DUMMY	-5635	-500
45	C21N	-5565	-500
46	C21N	-5495	-500
47	C21N	-5425	-500
48	C21N	-5355	-500
49	C21N	-5285	-500
50	DUMMY	-5215	-500
51	VOUTM	-5145	-500
52	VOUTM	-5075	-500
53	VOUTM	-5005	-500
54	VOUTM	-4935	-500
55	VOUTM	-4865	-500
56	DUMMY	-4795	-500
57	VDD2	-4725	-500
58	VDD2	-4655	-500
59	VDD2	-4585	-500
60	VDD2	-4515	-500
61	VSS	-4445	-500
62	VSS	-4375	-500
63	VSS	-4305	-500
64	VSS	-4235	-500
65	DUMMY	-4165	-500
66	C33P	-4095	-500
67	C33P	-4025	-500
68	DUMMY	-3955	-500
69	C32P	-3885	-500
70	C32P	-3815	-500
71	DUMMY	-3745	-500
72	C31P	-3675	-500
73	C31P	-3605	-500
74	DUMMY	-3535	-500
75	C31N	-3465	-500
76	C31N	-3395	-500
77	DUMMY	-3325	-500
78	C32N	-3255	-500
79	C32N	-3185	-500
80	DUMMY	-3115	-500

4. PIN ASSIGNMENT

BUMP No.	Pin Name	X (µm)	Y (µm)
81	C33N	-3045	-500
82	C33N	-2975	-500
83	DUMMY	-2905	-500
84	VEE	-2835	-500
85	VEE	-2765	-500
86	DUMMY	-2695	-500
87	DUMMY	-2625	-500
88	VLDO1	-2555	-500
89	C12P	-2485	-500
90	C12P	-2415	-500
91	C12P	-2345	-500
92	C12P	-2275	-500
93	C12P	-2205	-500
94	C12N	-2135	-500
95	C12N	-2065	-500
96	C12N	-1995	-500
97	C12N	-1925	-500
98	C12N	-1855	-500
99	VSS	-1785	-500
100	VSS	-1715	-500
101	VSS	-1645	-500
102	VSS	-1575	-500
103	VSS	-1505	-500
104	VDD2	-1435	-500
105	VDD2	-1365	-500
106	VDD2	-1295	-500
107	VDD2	-1225	-500
108	VDD2	-1155	-500
109	VOUT	-1085	-500
110	VOUT	-1015	-500
111	VOUT	-945	-500
112	VOUT	-875	-500
113	VOUT	-805	-500
114	C11P	-735	-500
115	C11P	-665	-500
116	C11P	-595	-500
117	C11P	-525	-500
118	C11P	-455	-500
119	C11N	-385	-500
120	C11N	-315	-500

BUMP No.	Pin Name	X (µm)	Y (µm)
121	C11N	-245	-500
122	C11N	-175	-500
123	C11N	-105	-500
124	VDD2	-35	-500
125	VDD2	35	-500
126	VDD2	105	-500
127	VDD2	175	-500
128	VDD2	245	-500
129	VSS	315	-500
130	VSS	385	-500
131	VSS	455	-500
132	VSS	525	-500
133	VSS	595	-500
134	DUMMY	665	-500
135	C41N	735	-500
136	C41N	805	-500
137	DUMMY	875	-500
138	C41P	945	-500
139	C41P	1015	-500
140	DUMMY	1085	-500
141	VDDHG	1155	-500
142	VDDHG	1225	-500
143	DUMMY	1295	-500
144	DUMMY	1365	-500
145	VDD2	1435	-500
146	VDD2	1505	-500
147	VDD2	1575	-500
148	VSS	1645	-500
149	VSS	1715	-500
150	VSS	1785	-500
151	TRI	1855	-500
152	DUMMY	1925	-500
153	VDDRH	1995	-500
154	VDDHS	2065	-500
155	VDDHS	2135	-500
156	VDDHS2	2205	-500
157	VREG	2275	-500
158	VDDI	2345	-500
159	VDDI	2415	-500
160	VDDI	2485	-500

BUMP No.	Pin Name	X (µm)	Y (µm)
161	TESTB	2555	-500
162	TESTA	2625	-500
163	TEST9	2695	-500
164	TEST8	2765	-500
165	TEST7	2835	-500
166	TEST6	2905	-500
167	TEST3	2975	-500
168	TEST2	3045	-500
169	TEST1	3115	-500
170	ERR	3185	-500
171	DUMMY	3255	-500
172	TCEN	3325	-500
173	OSCIEN	3395	-500
174	OSCI	3465	-500
175	OSCO	3535	-500
176	DUMMY	3605	-500
177	CPSET3	3675	-500
178	CPSET2	3745	-500
179	CPSET1	3815	-500
180	IF	3885	-500
181	DUMMY	3955	-500
182	VSYNCO	4025	-500
183	DUMMY	4095	-500
184	$\overline{WR}$	4165	-500
185	$\overline{RD}$	4235	-500
186	VSS	4305	-500
187	VSS	4375	-500
188	VSS	4445	-500
189	VDDI	4515	-500
190	VDDI	4585	-500
191	VDDI	4655	-500
192	VDD2	4725	-500
193	VDD2	4795	-500
194	VDD2	4865	-500
195	DUMMY	4935	-500
196	D0	5005	-500
197	DUMMY	5075	-500
198	D1	5145	-500
199	DUMMY	5215	-500
200	D2	5285	-500

BUMP No.	Pin Name	X (µm)	Y (µm)
201	DUMMY	5355	-500
202	D3	5425	-500
203	DUMMY	5495	-500
204	D4	5565	-500
205	DUMMY	5635	-500
206	D5	5705	-500
207	DUMMY	5775	-500
208	D6	5845	-500
209	DUMMY	5915	-500
210	D7	5985	-500
211	DUMMY	6055	-500
212	$\overline{CS}$	6125	-500
213	A0	6195	-500
214	DUMMY	6265	-500
215	SD	6335	-500
216	DUMMY	6405	-500
217	SCL	6475	-500
218	DUMMY	6545	-500
219	XE2WP	6615	-500
220	DUMMY	6685	-500
221	E2SO	6755	-500
222	DUMMY	6825	-500
223	E2SI	6895	-500
224	E2SCL	6965	-500
225	DUMMY	7035	-500
226	XE2CS	7105	-500
227	DUMMY	7175	-500
228	NVSEL	7245	-500
229	RESEN	7315	-500
230	$\overline{RES}$	7385	-500
231	VDD	7455	-500
232	VDD	7525	-500
233	VSS	7595	-500
234	VSS	7665	-500
235	VSS	7735	-500
236	VDDI	7805	-500
237	VDDI	7875	-500
238	VDDI	7945	-500
239	VDD2	8015	-500
240	VDD2	8085	-500

4. PIN ASSIGNMENT

BUMP No.	Pin Name	X (µm)	Y (µm)
241	VDD2	8155	-500
242	DUMMY	8225	-500
243	VCOM	8295	-500
244	VCOM	8365	-500
245	VCOM	8435	-500
246	DUMMY	8505	-500
247	CDUMMY	8575	-500
248	DDUMMY	8645	-500
249	DDUMMY	8840	500
250	CDUMMY	8814	383
251	DUMMY	8788	500
252	DUMMY	8762	383
253	GD1	8736	500
254	G1	8710	383
255	G3	8684	500
256	G5	8658	383
		.	
		.	
		.	
411	G315	4628	500
412	G317	4602	383
413	G319	4576	500
414	GD2	4550	383
415	DUMMY	4524	500
416	DUMMY	4498	383
		.	
		.	
		.	
423	DUMMY	4316	500
424	DUMMY	4290	383
425	S1	4264	500
426	S2	4238	383
427	S3	4212	500
		.	
		.	
		.	
455	S31	3484	500
456	S32	3458	383
457	DUMMY	3432	500
458	S33	3406	383
459	S34	3380	500
460	S35	3354	383

BUMP No.	Pin Name	X (µm)	Y (µm)
		.	
		.	
		.	
488	S63	2626	383
489	S64	2600	500
490	DUMMY	2574	383
491	S65	2548	500
492	S66	2522	383
		.	
		.	
		.	
521	S95	1768	500
522	S96	1742	383
523	DUMMY	1716	500
524	S97	1690	383
525	S98	1664	500
		.	
		.	
		.	
554	S127	910	383
555	S128	884	500
556	DUMMY	858	383
557	S129	832	500
558	S130	806	383
		.	
		.	
		.	
587	S159	52	500
588	S160	26	383
589	DUMMY	0	500
590	S161	-26	383
591	S162	-52	500
		.	
		.	
		.	
620	S191	-806	383
621	S192	-832	500
622	DUMMY	-858	383
623	S193	-884	500
624	S194	-910	383
		.	
		.	

BUMP No.	Pin Name	X (μm)	Y (μm)
		・	
653	S223	-1664	500
654	S224	-1690	383
655	DUMMY	-1716	500
656	S225	-1742	383
657	S226	-1768	500
		・ ・ ・	
686	S255	-2522	383
687	S256	-2548	500
688	DUMMY	-2574	383
689	S257	-2600	500
690	S258	-2626	383
		・ ・ ・	
719	S287	-3380	500
720	S288	-3406	383
721	DUMMY	-3432	500
722	S289	-3458	383
723	S290	-3484	500
		・ ・ ・	
751	S318	-4212	500
752	S319	-4238	383
753	S320	-4264	500
754	DUMMY	-4290	383
755	DUMMY	-4316	500
		・ ・ ・	
762	DUMMY	-4498	383
763	DUMMY	-4524	500
764	GD3	-4550	383
765	G320	-4576	500
766	G318	-4602	383
767	G316	-4628	500
		・ ・ ・	

BUMP No.	Pin Name	X (μm)	Y (μm)
922	G6	-8658	383
923	G4	-8684	500
924	G2	-8710	383
925	GD4	-8736	500
926	DUMMY	-8762	383
927	DUMMY	-8788	500
928	BDUMMY	-8814	383
929	ADUMMY	-8840	500

G_{2n-1} Pin (n=1 to 160)
X: 8710 − 26 x (n−1)
Y: When n is odd: 383
When n is even: 500

G_{2n} Pin (n=1 to 160)
X: −8710 + 26 x (n−1)
Y: When n is odd: 383
When n is even: 500

S_n Pin (n = 1 to 32)
X: 4264 − 26 x (n−1)
Y: Wnen n is odd: 500
When n is even: 383

S_n Pin (n = 33 to 64)
X: 4264 − 26 x n
Y: When n is odd: 383
When n is even: 500

S_n Pin (n = 65 to 96)
X: 4264 − 26 x (n+1)
Y: When n is odd: 500
When n is even: 383

S_n Pin (n = 97 to 128)
X: 4264 − 26 x (n+2)
Y: When n is odd: 383
When n is even: 500

S_n Pin (n = 129 to 160)
X: 4264 − 26 x (n+3)
Y: When n is odd: 500
When n is even: 383

S_n Pin (n = 161 to 192)
X: 4264 − 26 x (n+4)
Y: When n is odd: 383
When n is even: 500

S_n Pin (n = 193 to 224)
X: 4264 − 26 x (n+5)
Y: When n is odd: 500
When n is even: 383

S_n Pin (n = 225 to 256)
X: 4264 − 26 x (n+6)
Y: When n is odd: 383
When n is even: 500

S_n Pin (n = 257 to 288)
X: 4264 − 26 x (n+7)
Y: When n is odd: 500
When n is even: 383

S_n Pin (n = 289 to 320)
X: 4264 − 26 x (n+8)
Y: When n is odd: 383
When n is even: 500

5. PIN DESCRIPTION

5.1 External Power Pins

Table 3 External Power Pins

Pin Name	I/O	Connected To	Description	Number of pins
V_{DD2}	Power supply I	External power	Power pins for built-in power supply circuit . Used as the reference power supply for the 1st and 2nd booster. Supply external power.	27
V_{DDI}	Power supply I	External power	Power pins for MPU interface circuit. Supply external power.	9
V_{SS}	Power supply I	External power	They are ground pins. The 0V pin connected to the system ground.	27

5.2 Built-in Power Pins

Table 4 Built-in Power Pins

Pin Name	I/O	Connected To	Description	Number of Pins
V_{DD}	O	Capacitor	Power pins for internal logic, RAM and Multi-time-PROM.	2
V_{REG}	O	Capacitor	Reference voltage for built-in power supply.	1
V_{DDHS}	O	Capacitor	Voltage for generating source driver drive voltage.	2
V_{DDHS2}	O	Capacitor	Voltage for generating source driver drive voltage. 1/2 V_{DDHS} is output	1
V_{DDRH}	O	Open	Reference voltage for generating V_0 for γ correction. Normally, VSS is output.	1
V_{LDO1}	I/O	Open	Voltage for 1st booster. Set it to open.	1
V_{LDO2}	I/O	Capacitor/ VDCCOM/ Open/	Voltage for 2nd booster and V_{COML} generator. Connect it to Capacitor if it connects to VDCCOM. Refer to 6.6.2 External power circuit connection.	4

5.3 1st Booster Pins

Table 5 the 1st Booster Pins

Pin Name	I/O	Connected To	Description	Number of Pins
C11P	I/O	Capacitor/ Open	Flying capacitor for generating VOUT output Connecting pins on the positive side. Leave open if 1st booster is not used.	5
C11N	I/O	Capacitor/ Open	Flying capacitor for generating VOUT output Connecting pins on the negative side. Leave open if 1st booster is not used.	5
C12P	I/O	Capacitor/ Open	Flying capacitor for generating VOUT output Connecting pins on the positive side. Leave open if 1st booster is not used.	5
C12N	I/O	Capacitor/ Open	Flying capacitor for generating VOUT output Connecting pins on the negative side. Leave open if 1st booster is not used.	5
VOUT	I/O	Capacitor/ External power / SBD	The 1st booster voltage. Outputs double of VLDO1. when built-in power supply. Connecting schottky barrier diode Between VOUT-VDD2. See section 6.7 connection diagram of external parts.	5

5.4 2nd Booster Pins

Table 6 The 2nd Booster Pins

Pin Name	I/O	Connected To	Description	Number of Pins
C21P	I/O	Capacitor	Flying capacitor for generating VOUTM output Connecting pins on the positive side	5
C21N	I/O	Capacitor	Flying capacitor for generating VOUTM output Connecting pins on the negative side	5
VOUTM	O	Capacitor/ VSS	2nd boosting output voltage. Voltage for generating VCOML Output voltage is –VLDO2. When VCOML=VSS, Connect this pin to VSS. Refer to section 7.3.28 PWRCTL.	5

5.5 3rd Booster Pins

Table 7 The 3rd Booster Pins

Pin Name	I/O	Connected To	Description	Number of Pins
C31P	I/O	Capacitor	Flying capacitor for generating V_{EE} output Connecting pins on the positive side	2
C31N	I/O	Capacitor	Flying capacitor for generating V_{EE} output Connecting pins on the negative side	2
C32P	I/O	Capacitor/ Open	Flying capacitor for generating V_{EE} output Connecting pins on the positive side. Leave open if x1 boosting is used.	2
C32N	I/O	Capacitor/ V_{EE}	Flying capacitor for generating V_{EE} output Connecting pins on the negative side. Leave open if x1 boosting is used.	2
C33P	I/O	Capacitor/ Open	Flying capacitor for generating V_{EE} output Connecting pins on the positive side. Leave open if x1/x2 boosting is used.	2
C33N	I/O	Capacitor/ V_{EE}	Flying capacitor for generating V_{EE} output Connecting pins on the negative side. Leave open if x1/x2 boosting is used.	2
V_{EE}	O	Capacitor/ SBD	3^{rd} boosting output voltage. Gate off voltage. It is substrate voltage of this IC. Connecting schottky barrier diode Between V_{EE}-V_{SS}. See section 6.7 connection diagram of external parts.	2

5.6 4th Booster Pins

Table 8 The 4th Booster Pins

Pin Name	I/O	Connected To	Description	Number of Pins
C41P	I/O	Capacitor	Flying capacitor connecting pins on the positive side for generating V_{DDHG} output	2
C41N	I/O	Capacitor	Flying capacitor connecting pins on the negative side for generating V_{DDHG} output	2
V_{DDHG}	O	Capacitor	4^{th} boosting output voltage. V_{DDHG} output pin. Gate on voltage	2

5.7 V_{COM} Generation Pins

Table 9 V_{COM} Generation Pins

Pin Name	I/O	Connected To	Description	Number of Pins
V_{COMH}	O	Capacitor	Voltage output pin on the side of high voltage level of the V_{COM} signal. It is possible to adjust V_{COMH} voltage, by EVSET1 command and external EEPROM.	3
V_{COML}	O	Capacitor	Voltage output pin on the side of low voltage level of the V_{COM} signal. $V_{COML}=V_{COMH} – VCA \times 2$ Outputs voltage by the above equation. VCA is the value of the built-in electronic control used for determining the amplitude of V_{COM}.	3
VDCCOM	I	V_{DD2}/ V_{LDO2}	It is for V_{COML} generating. Select connecting pin to refer to section 6.6.2 external power supply connection. When VCOML=VSS, connect this pin to VDD2.	4

5.8 Multi time PROM Pins

Table 10 Multi time PROM Pins

Pin Name	I/O	Connected To	Description	Number of Pins
VME1	Power supply	External power supply/ Open	Erase power supply for Multi time PROM. Opened under normal conditions.	1
VME2	Power supply	External power supply/ Open	Program power supply for Multi time PROM. Opened under normal conditions.	2

5.9 Control Pins

Table 11 Control Pins

Pin Name	I/O	Connected To	Description	Number of Pins
$\overline{CS}$	I	MPU	Chip Select pin. When $\overline{CS}$ = LOW, the pin is active and data or command input is enabled.	1
A0	I	MPU/	Data/command identification pin A0= HIGH : The display data or command parameters are entered in the Data Bus pins. A0= LOW : The commands are entered in the Data Bus pins.	1
$\overline{RD}$	I	MPU/ V_{SS}/ V_{DDI}	Read pin. While this signal is kept LOW, the data bus is output enabled at the $\overline{RD}$ signal pin. When the serial interface is selected, fix V_{DDI} or V_{SS} for the level.	1
$\overline{WR}$	I	MPU/ V_{SS}/ V_{DDI}	Write pin. Used for connecting MPU's $\overline{WR}$ signal. A signal on the data bus is latched at the rising edge of the $\overline{WR}$ signal. When the serial interface is selected, fix V_{DDI} or V_{SS} for the level.	1
D0 to D7	I/O	MPU/ LCDC/ Open	Data bus pin. 8-bit bi-directional data bus. When the parallel MPU interface is selected and the Chip Select is in the non-active state, operations of all pins stop, disabling both input and output. When serial interface is selected, it can possible to leave open.	8

HIGH = V_{DDI} level, LOW = V_{SS} level

Pin Name	I/O	Connected To	Description	Number of Pins
SCL	I	MPU/ V_{SS}/ V_{DDI}	Serial clock pin. Serial clock input pins used when the serial interface is selected. When not choosing the serial interface, this pin must be connected to VDD or VSS.	1
SD	I/O	MPU/ Open/ V_{SS}/ V_{DDI}	Serial data input/output pin. Serial data input/output pin used when the serial interface is selected. When not choosing a serial interface, it is possible to make it to open.	1
IF	I	V_{SS}/ V_{DDI}	MPU interface switching pin. Fix to HIGH or LOW. Don't change it during operation. HIGH: Serial interface LOW: Parallel interface	1
$\overline{RES}$	I	MPU	Reset pin. This pin is effective when RESEN pin is HIGH. Initialization is execlted when this pin is set to LOW. SWRESET command must be required after initialization by XRES pin.	1
RESEN	I	MPU / V_{SS}/ V_{DDI}	Distinction pin of the Reset pin signal. HIGH: XRES pin signal is effective. LOW: XRES pin signal is not effective. Set HIGH when power-on, and change to LOW after releasing XRES.	1
CPSET1, CPSET2, CPSET3	I	V_{SS}/ V_{DDI}	Select pins of VLDO1, VLDO2, VDCCOM, V_{OUT} Refer to section 6.6.2. External power supply pins.	3
NVSEL	I	V_{SS}/ V_{DDI}	EEPROM select pin. HIGH: Enable External EEPROM LOW: Disable external EEPROM	1
TCEN	I	MPU/ V_{SS}	Enable pin for TEST command. HIGH: Enable Test command. LOW: Disable Test command.(Normally usage)	1
OSCI	I	V_{SS}/V_{DDI}/ External clock	External clock input. It is enable when OSCIEN pin is HIGH. Connect to V_{DDI} or V_{SS} when built-in oscillator is used.	1
OSCIEN	I	V_{SS}/ V_{DDI}	Select pin of booster oscillator or external clock input. HIGH: Built-in oscillator is stopped. External clock from OSCI pin is used. LOW: Built-in oscillator is used.	1
OSCO	O	OPEN	Clock output pin. It is output by P36 = "1" of DISSET1 command.	1
VSYNCO	O	MPU/ LCDC/ Open	Vertical synchronization output pins. Outputs the vertical synchronization signal.	1
ERR	O	MPU/ LCDC/ Open	Error status monitor pin. HIGH : Error detected LOW : Normal operation	1

HIGH = V_{DDI} level, LOW = V_{SS} level

5.10 EEPROM control Pin

Table 12 EEPROM control Pin

Pin Name	I/O	Connected To	Description	Number of Pins
XE2CS	O	EEPROM/ Open	Chip select output pin for EEPROM. Input and output of Data/command is possible. It is enable when XE2CS = LOW. Leave open if it is not used.	1
E2SCL	O	EEPROM/ Open	Serial clock output pin for EEPROM. Leave open if it is not used.	1
E2SI	I	EEPROM/ V_{SS}/V_{DDI}	Serial data input pin for EEPROM. Connect to V_{DDI} or V_{SS} if it is not used.	1
E2SO	O	EEPROM/ Open	Serial data output pin for EEPROM. Leave open if it is not used.	1
XE2WP	O	EEPROM/ Open	Write protect output pin for EEPROM. Leave open if it is not used.	1

HIGH = V_{DDI} level, LOW = V_{SS} level

5.11 LCD Output Pins

Table 13 LCD Output Pins

Pin Name	I/O	Connected To	Description	Number of Pins
S1 to S320	O	LCD/ Open	Source line drive output pins. Converts digital display data into analog form (D/A conversion) and outputs it. Unused pin should be kept to open. Unused pin output Hi-Z (set by DISAR command)	320
G1 to 320	O	LCD/ Open	Gate line drive output pins. Outputs gate line selection level: V_{DDHG} and non-selection level: V_{EE}. Unused pin should be kept to open. Unused pin output VEE (set by DISAR command)	320
GD1 to 4	O	LCD/ Open	Dummy gate line drive output pins. Continuously outputs V_{EE} voltage level. Unused pin should be kept to open.	4
V_{COM}	O	LCD	V_{COM} signal output pin. Used as the common electrode signal for the TFT panel.	6

5.12 Test Pins

Table 14 Test Pins

Pin Name	I/O	Connected To	Description	Number of Pins
TEST1	I	Vss	Test pin. Customer doesn't use. Fix to Vss.	1
TEST2	I	Vss	Test pin. Customer doesn't use. Fix to Vss.	1
TEST3	I	Vss	Test pin. Customer doesn't use. Fix to Vss.	1
TEST4	Power	Open	Test pin. Customer doesn't use. Leave it open.	1
TEST5	O	Open	Test pin. Customer doesn't use. Leave it open.	1
TEST6	I	Vss	Test pin. Customer doesn't use. Fix to Vss.	1
TEST7	I	Vss	Test pin. Customer doesn't use. Fix to Vss.	1
TEST8	I	Vss	Test pin. Customer doesn't use. Fix to Vss.	1
TEST9	I	Vss	Test pin. Customer doesn't use. Fix to Vss.	1
TESTA	I	Vss	Test pin. Customer doesn't use. Fix to Vss.	1
TESTB	I	Vss	Test pin. Customer doesn't use. Fix to Vss.	1
TRI	O	Open	Test pin. Customer doesn't use. Leave it open.	1
TRI2	O	Open	Test pin. Customer doesn't use. Leave it open.	1

5.13 Dummy Pins

Table 15 Dummy Output Pins

Pin Name	I/O	Connected To	Description	Number of Pins
DUMMY	—	Open	Dummy pin Do not input the voltage to the DUMMY pin.	78
ADUMMY	—	Open	There are two pins that are connected by aluminum winding. When it is used, connect it within VOUT to Vss.	2
BDUMMY	—	Open	There are two pins that are connected by aluminum winding. When it is used, connect it within VOUT to Vss.	2
CDUMMY	—	Open	There are two pins that are connected by aluminum winding. When it is used, connect it within VOUT to Vss.	2
DDUMMY	—	Open	There are two pins that are connected by aluminum winding. When it is used, connect it within VOUT to Vss.	2

6. FUNCTIONAL DESCRIPTION

6.1 MPU Interface

This IC is provided with 8-bit MPU interface and 8-bit/4wire serial interface for command and display data transfer from the MPU.

Data / Command is recognized by A0 pin.

When too much parameters are input, the S1D19600 accept defined parameters and over parameters are ignored.

Prohibited to change the MPU interface during operation.

6.1.1 MPU Interface Selection

The MPU interface is selected by IF pin.

Table 16 MPU Interface Selection

IF	Interface	CS	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0	SD	SCL
LOW	8-bit parallel	A	A	A	A	A	Hi-Z	Fix
HIGH	Serial	A	A	Fix	Fix	Hi-Z	A	A

A: Avaitable for interface pins.
Fix: Fix to HIGH or LOW.
Hi-Z: High impetance state. Leave Open or Fix to HIGH or Fix to LOW.

6.1.2 Parallel MPU Interface

When data is transferred, the S1D19600 is generated a internal pulse each access, and the data handle by a kind of pipe line operation. Therefore system clock is not required from MPU, and realize low power consumption.

No need wait cycle if the cycle time (AC timing) is satisfied.

For example, when MPU write a data to the display data RAM, the data is kept by write bus holder once, and the data is written to the display data RAM by internal write signal until next data write cycle.

When MPU read the display data, from display data RAM, it is read by 1st data read cycle (dummy cycle), and data is kept by read bus holder and it is read to MPU bus in next data read cycle. Therefore one dummy read is required after RDRAM command.

Fig.6, Fig.7 and Fig.8 are examples of MPU interface. Intermediate level of data in them means Hi-Z state.

Table 17 MPU Interface Identification

A0	$\overline{RD}$	$\overline{WR}$	Function
LOW	HIGH	LOW	Command write
HIGH	LOW	HIGH	RAM data read, parameter read
HIGH	HIGH	LOW	RAM data write, command parameter write
Other setting is invalid			

◇ Write operation

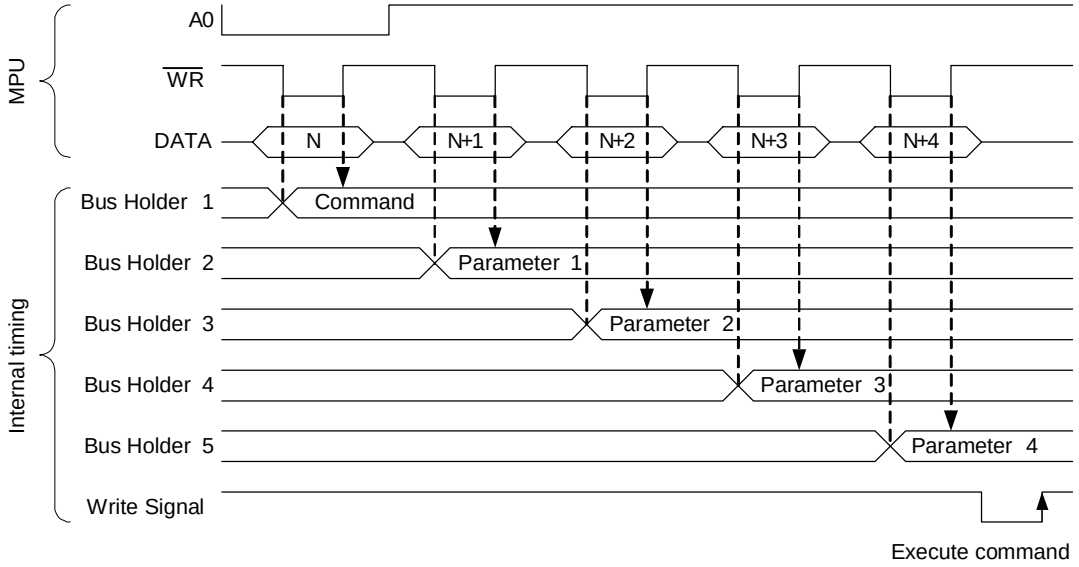


Fig.6 Parallel interface write operation (in case of 5Bytes command)

◇ Read opetation

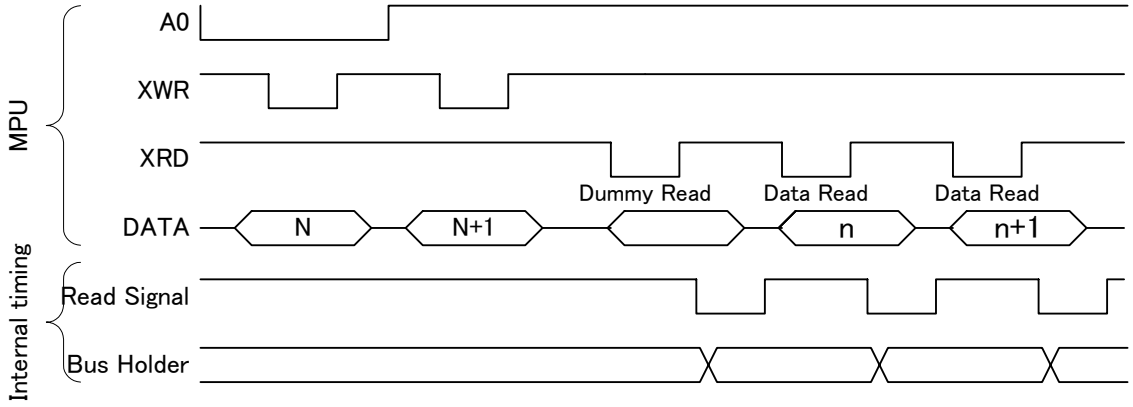


Fig.7 parallel interface read operation (RAM data read)

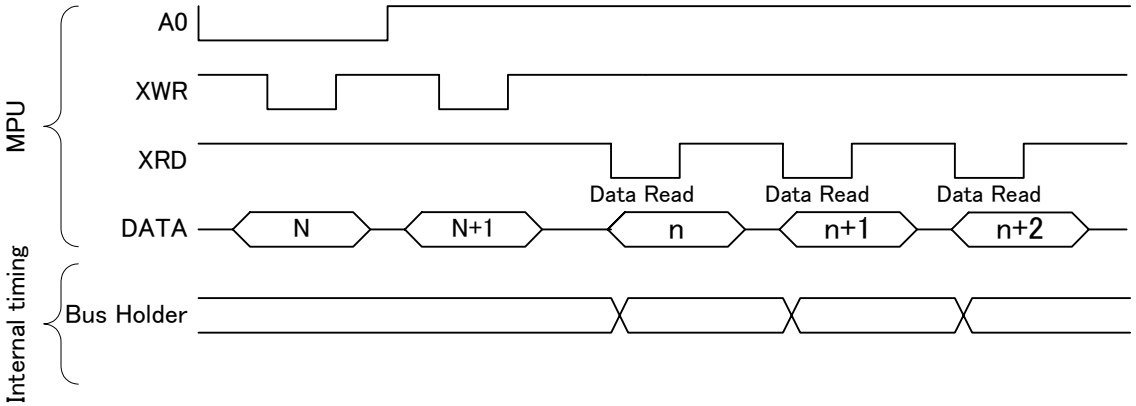


Fig. 8 Parallel interface read operation (Parameter read)

6.1.3 Serial Interface

The serial interface supports 8-bit mode. The 8-bit mode consists of 4-wires: chip select ($\overline{CS}$), serial clock (SCL), and serial data I/O (SD) and indicator of command/parameter (A0). When the serial interface is selected, data can be input/output by clocks while the chip is active ($\overline{CS}$=LOW). Data is transferred in the unit of 8 bits. At input, data is read in order from MSB at the clock rising edge.

To prevent malfunction due to noise, it is recommended to set the $\overline{CS}$ signal to HIGH every 8 bits. (The serial counter is reset at the falling edge of the $\overline{CS}$ signal.)

Table 18 8-bit Serial Interface

Data type	Serial interface bit position								
	A0	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	Command							
Parameter	1	Parameter							

A0: Data/command identification bit

Processing starts when D0 is input by the serial transfer clock. Writing to or reading from the display data RAM is possible. When too much parameters are input, the S1D19600 accept defined parameters and over parameters are ignored.

The interface examples are given as Fig.9, Fig10 and Fig.11. (The intermediate level of SD in the following diagram must be kept HIGH or LOW except during reading period.)

◇ When writing

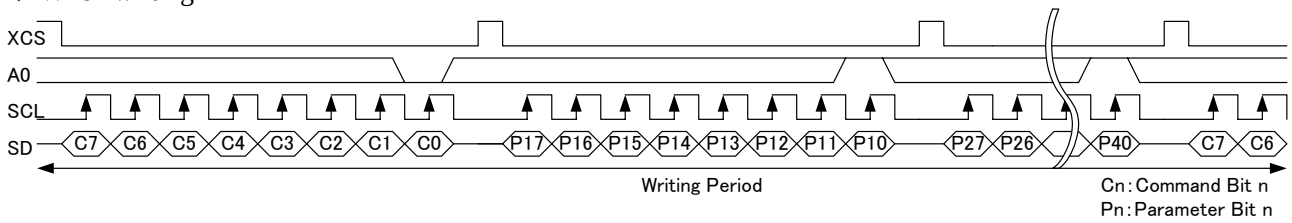


Fig 9 Serial interface write operation (example of 5Byte command input)

$\overline{CS}$ must be kept at LOW level during 8-bit serial data (1 packet) transfer. When $\overline{CS}$ sets to LOW, SCL should be in the state of LOW. If $\overline{CS}$ is set HIGH during 1-packet transfer, the packet in the process of transfer is cancelled. Setting LOW for $\overline{CS}$ again brings the state of accepting retransfer of the packet.

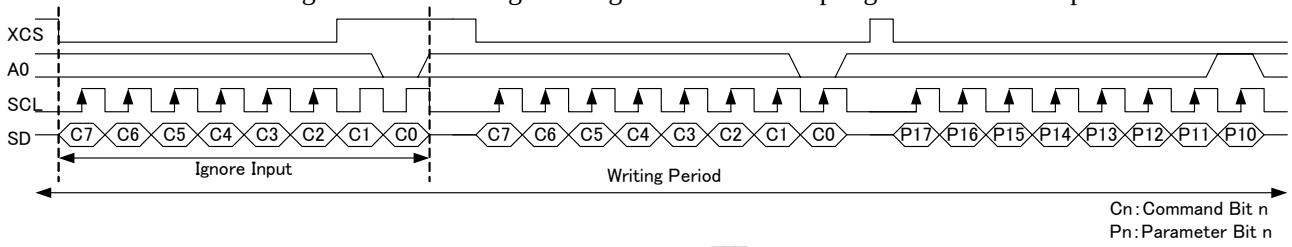


Fig 10 Serial interface write operation (example when $\overline{CS}$ is high during 1 packet transferring.)

◇ When reading

When data is read using each read command, the operation is as following. $\overline{CS}$ must be low between parameter of read command and read data output. $\overline{CS}$ must be HIGH after final bit of read data is transferred. When $\overline{CS}$ is set to high during the read data transferring, read state is cancelled. When $\overline{CS}$ is set to LOW, command can be acceptable again.

Only in case by RAM data read, 1st packet of output data is dummy data.

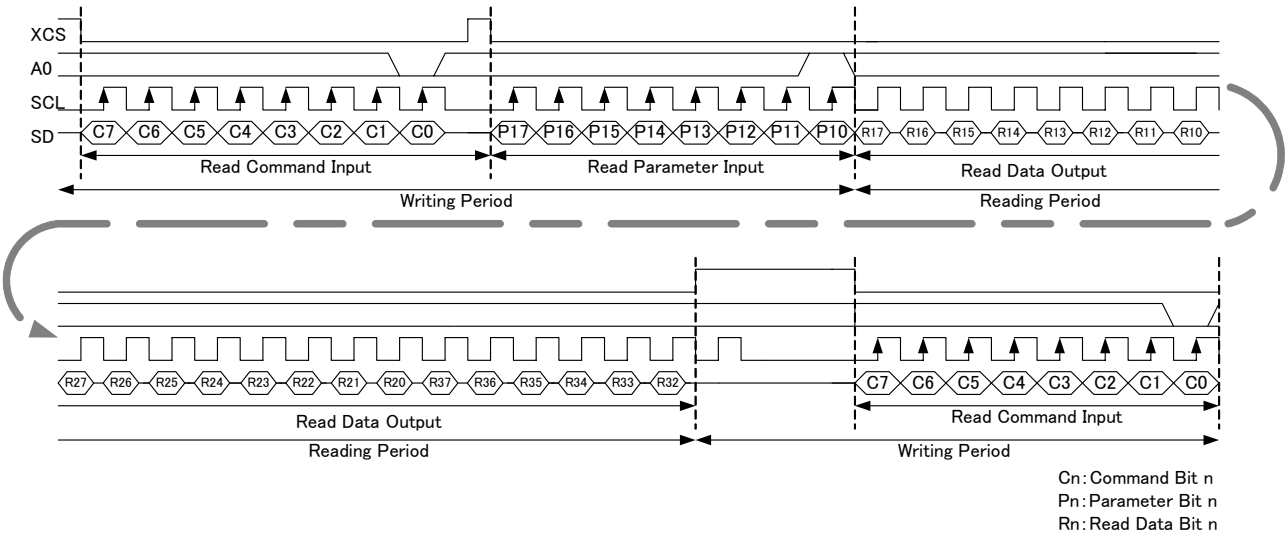


Fig 11 Serial interface read operation

6.1.4 Internal Data Bus Expansion of Display Data

Display data read or written in the parallel MPU interface is expanded to 8-bit internal data bus and gray-scale data as shown in the table below.

Display data is stored to display data RAM by BPPSEL command.

4bpp mode: 8bit data to 1source * 2line
2bpp mode: 8bit data to 1source * 4line
1bpp mode: 8bit data to 1source * 8line

Sequence of transfer from external data bus to internal data bus (4bpp mode)

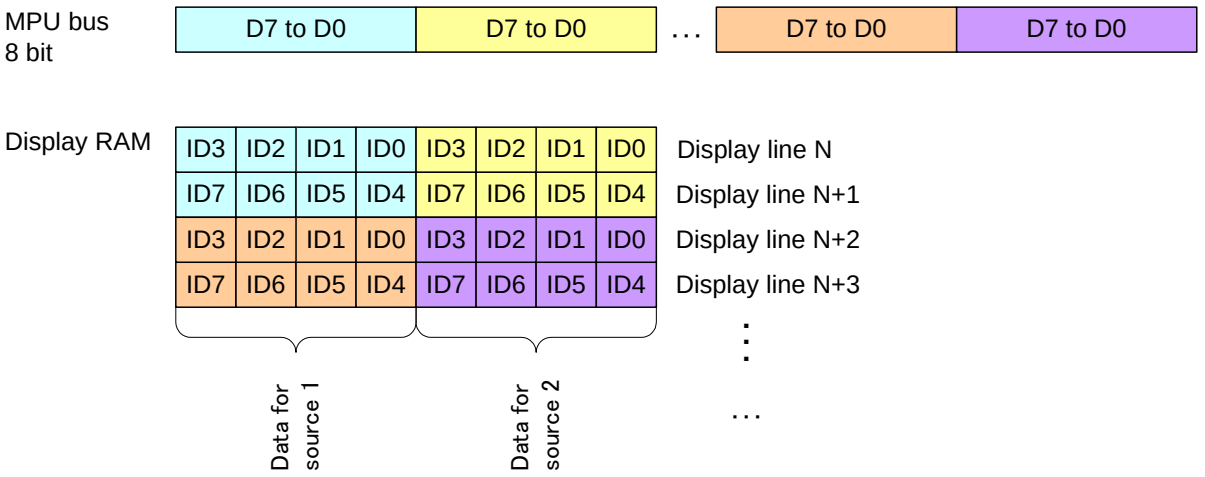


Fig.12 Expansion from external bus to internal bus (4bpp mode)

Sequence of transfer from external data bus to internal data bus (2bpp mode)

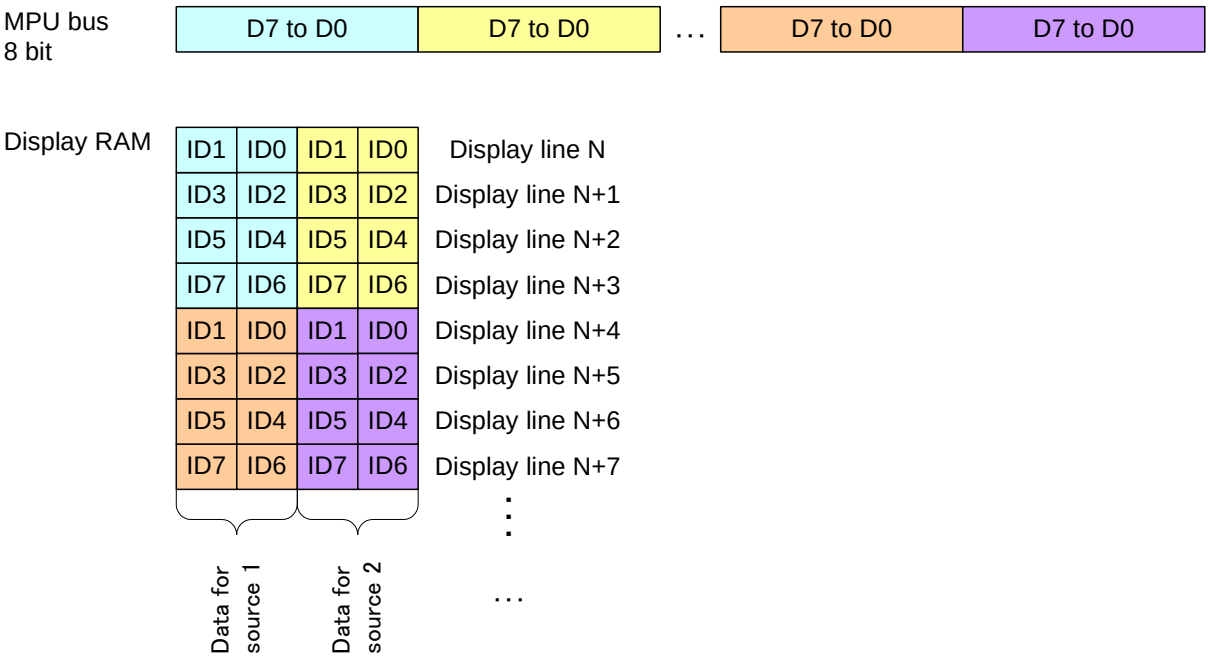


Fig.13 Expansion from external bus to internal bus (2bpp mode)

Sequence of transfer from external data bus to internal data bus (1bpp mode)

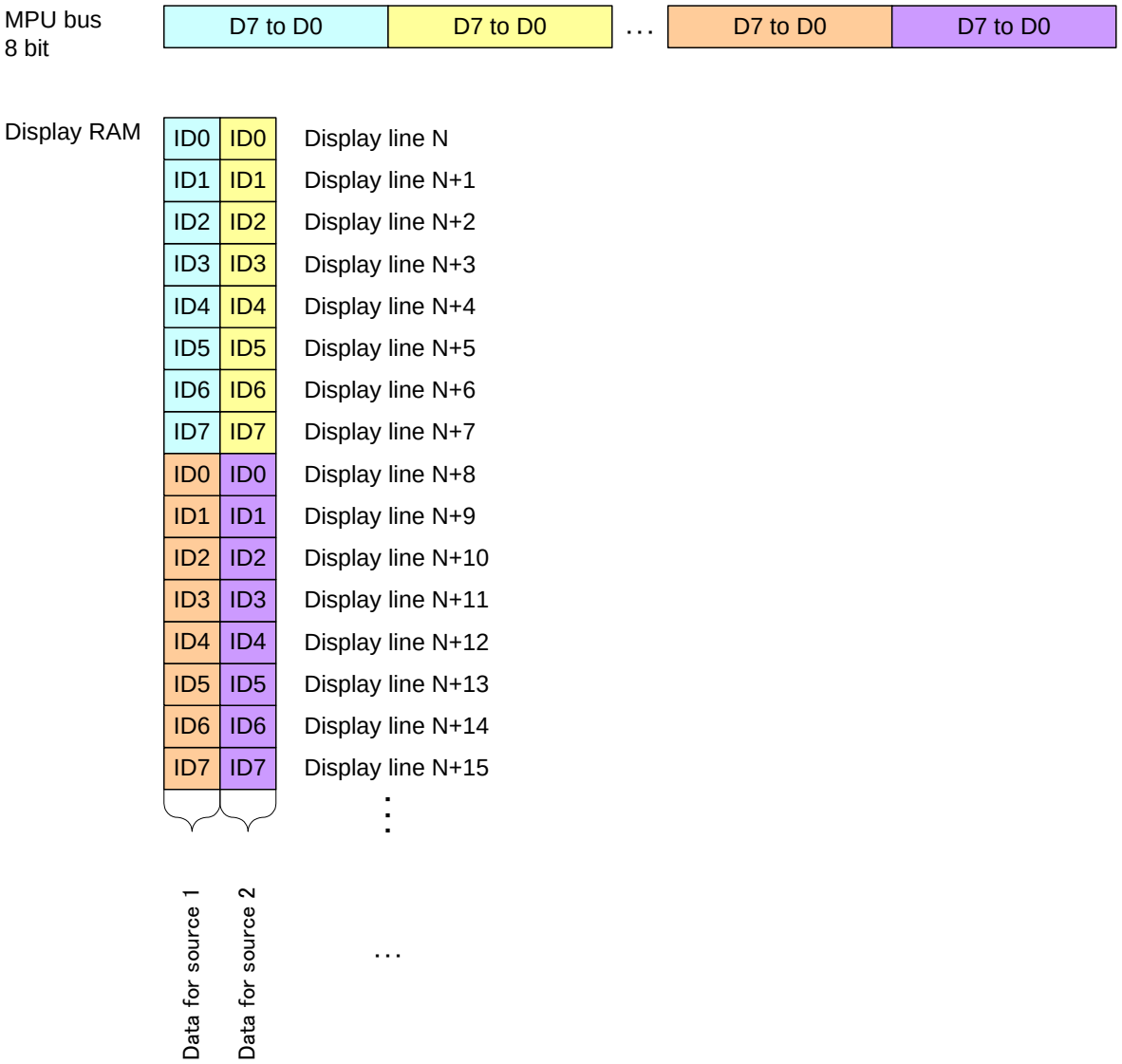


Fig.14 Expansion from external bus to internal bus (1bpp mode)

6.2 Display Data RAM

6.2.1 Display Data RAM

RAM that stores dot data for display and mapping is shown as Table 19.
An 8 bit internal data (ID0 to ID7) is provided to 2 pixels(4bit/pixel * 1source line * 2 display lines).
Maximum display size is 320 * 320 pixel and corresponded display RAM is 409,600 (320 * 320 * 4) bits.
1 pixel data (4bit) is corresponded to gray scales as below.

(0000): Gray scale 0 (black)
:
(1110):
(1111): Gray scale 15 (white)

Table 19 Display Data Memory Map (4bpp mode)

Page address												Display
Normal	**Invert**	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**		**S318**	**S319**	**S320**	**line**
0	159	ID0 to ID7	ID0 to ID7	ID0 to ID7	ID0 to ID7	ID0 to ID7	ID0 to ID7		ID0 to ID7	ID0 to ID7	ID0 to ID7	1
1	158											3
.	.	.	.	.	.	.	.	.	.	.	.	.
158	1	ID0 to ID7	ID0 to ID7	ID0 to ID7	ID0 to ID7	ID0 to ID7	ID0 to ID7		ID0 to ID7	ID0 to ID7	ID0 to ID7	319
159	0											320
Column	Normal	0	1	2	3	4	5		317	318	319	
Address	Invert	319	318	317	316	315	314		2	1	0	

The MPU interfaces access the display RAM in the unit of “1pixel x 2 display line” (when 4bpp mode). Source output is sent by 1 horizontal period independent from MPU interface.

Normal or reverse setup of page and column addresses are specified with MADCTL command.

Relationship between page address, frame address and display line is shown as Table 21.
It is changed as BPPSEL command (4bpp, 2bpp, 1bpp) and DISAR command.
Access to the Display data RAM is executed by column address and page address unit. When 4bpp mode, the accessing is executed by 2 display line unit. When 2bpp mode, the accessing is executed by 4 display line unit. When 1bpp mode, the accessing is executed by 8 display line unit. When number of display lines is not dividable by above unit, data with dummy data must be transferred. Interframe access is not available.
When data is written to display data RAM by WRRAM command, the transfer data can be maskable only to start page address and end page address. (Refer to 7.3.12 MDCTL command)
This function is invalid for writing by BLKFIL command.

Table 20 BPPSEL and number of frame RAM

BPP(BPPSEL)	4bpp		2bpp	1bpp
Display line	Over 160 lines	160 lines or less	Any	Any
Number of frame RAM	1	2	2	4

Table 21 Relationship between page address , frame address and display line

<table>
<tr><th rowspan="2">Display line</th><th colspan="2">4bpp mode (over 160 lines)</th><th colspan="2">4bpp mode (160 lines or less)</th><th colspan="2">2bpp mode</th><th colspan="2">1bpp mode</th></tr>
<tr><th>Page address</th><th>Frame address</th><th>Page address</th><th>Frame address</th><th>Page address</th><th>Frame address</th><th>Page address</th><th>Frame address</th></tr>
<tr><td>1</td><td rowspan="2">0</td><td rowspan="10">0</td><td>0</td><td rowspan="10">0 / 1</td><td rowspan="2">0</td><td rowspan="10">0 / 1</td><td rowspan="8">0</td><td rowspan="10">0 / 1 / 2 / 3</td></tr>
<tr><td>2</td></tr>
<tr><td>3</td><td rowspan="2">1</td><td>1</td></tr>
<tr><td>4</td></tr>
<tr><td>5</td><td rowspan="2">2</td><td rowspan="2">2</td><td rowspan="2">1</td></tr>
<tr><td>6</td></tr>
<tr><td>7</td><td rowspan="2">3</td><td rowspan="2">3</td></tr>
<tr><td>8</td></tr>
<tr><td>9</td><td rowspan="2">4</td><td rowspan="2">4</td><td>2</td><td>1</td></tr>
<tr><td>10</td></tr>
<tr><td colspan="9">⋮</td></tr>
<tr><td>311</td><td rowspan="2">155</td><td rowspan="10">0</td><td rowspan="2">75</td><td rowspan="10">0 / 1</td><td>77</td><td rowspan="10">0 / 1</td><td>38</td><td rowspan="10">0 / 1 / 2 / 3</td></tr>
<tr><td>312</td><td rowspan="8">39</td></tr>
<tr><td>313</td><td rowspan="2">156</td><td rowspan="2">76</td><td rowspan="3">78</td></tr>
<tr><td>314</td></tr>
<tr><td>315</td><td rowspan="2">157</td><td rowspan="2">77</td></tr>
<tr><td>316</td></tr>
<tr><td>317</td><td rowspan="2">158</td><td rowspan="2">78</td><td rowspan="3">79</td></tr>
<tr><td>318</td></tr>
<tr><td>319</td><td rowspan="2">159</td><td rowspan="2">79</td></tr>
<tr><td>320</td></tr>
</table>

*: Normal/Invert of Page address/Column address are set by MADCTL command.

6.2.2 Page Address Circuit/Column Address Circuit

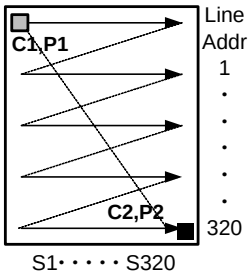
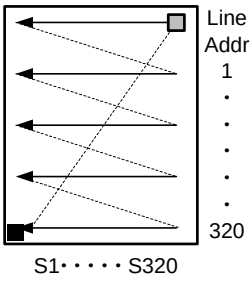
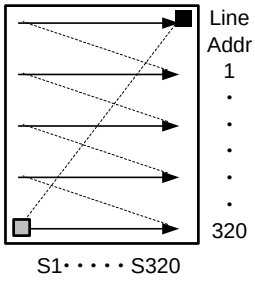
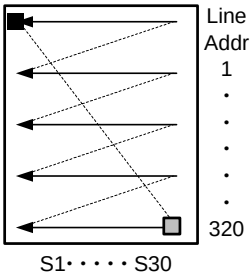
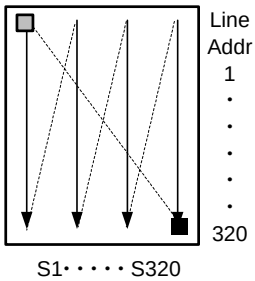
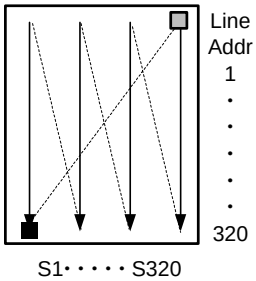
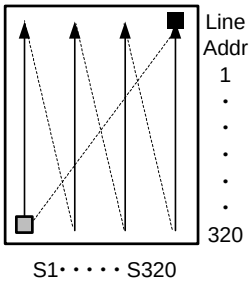
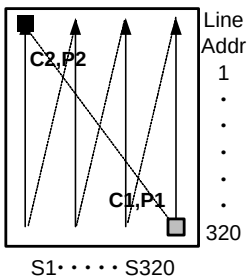
An access area of the RAM is defined by a rectangle having the vertex identified by the start address and end address. Assume that the start address has column address C1 and page address P1, and that the end address has column address C2 and page address P2. The display data is written in address (C1, P1) and subsequent addresses, and if the scan direction is in the column direction, the column address is incremented by +1 automatically by write pulse and read pulse. After the data has been written in column address C2, the page address is incremented by +1 and the column address is returned to C1.

When display RAM is accessed by MPU interface, column address and page address are set to start address are set automatically by WRRAM or RDRAM command.

Column address has relationship to number of display column by DISAR, and when number of display lines is under 320, position is adjusted automatically. Therefore the column address is set within number of display column.

The address direction of a column or a page address and the address scan direction can be inverted by MADCTL command.

Table 22 Page /Column Display Sequence

Address transition **Display start position C1,P1** ■ **Display end position C2,P2** ■	**Page address normal**		**Page address reverse**	
	Column address normal	**Column address reverse**	**Column address normal**	**Column address reverse**
P12=0 Scan direction right and left				
P12=1 Scan direction up and down				

6.2.3 Partial Display

2 partial area can be set by PTLSET1 command.
Source outputs the following:

- Display area: Normal source output corresponded to Display data RAM.
- Non display area: When display refresh is used, minimum voltage against VCOM (V0 or V15) is output.
  When display refresh is not used, voltages set by P3 of PTLSET3 command is output.

It is possible to set the booster clock frequency of non-refreshing and non -display area by P4 of PWRCTL command.

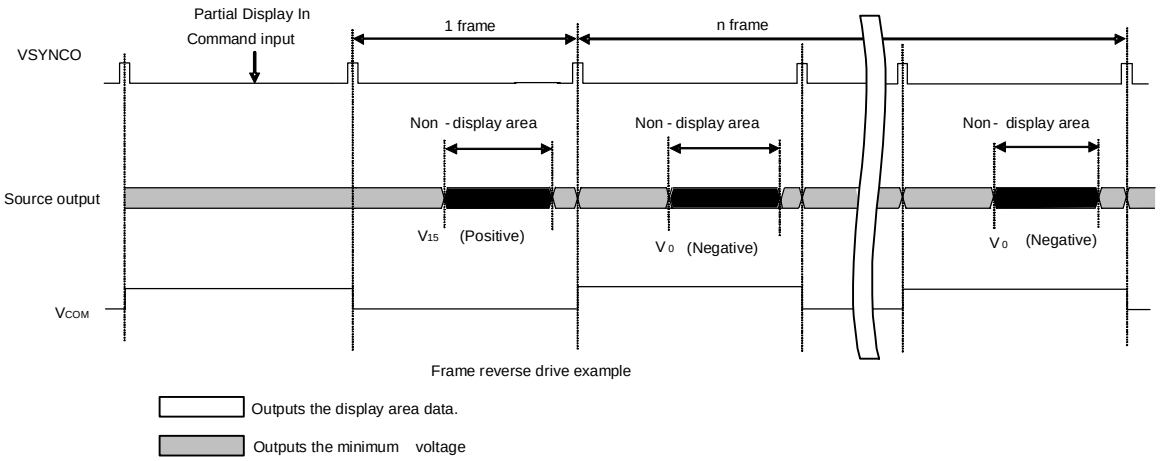


Fig.15 Partial Display example (refresh rate 1/1, frame inversion)

The driving method of front poaching period(FP) and back poaching period(BP) during partial display are as follows. The front poaching becomes being the same as that of a non-displaying area. The back poaching becomes being the same as that of display area.

6.2.4 AC Operation Drive

With this IC, the following AC operation modes can be used.

(1) 1-line inverted drive: Inverts an AC signal with each 1-line display.
(2) 2-line inverted drive: Inverts an AC signal with each 2-line display.
(3) Frame reverse driving: Reverses the AC operation signals once for each frame.
(4) Interlace drive: Reverses the AC operation signals three times for each frame with 3-line interlace drive.

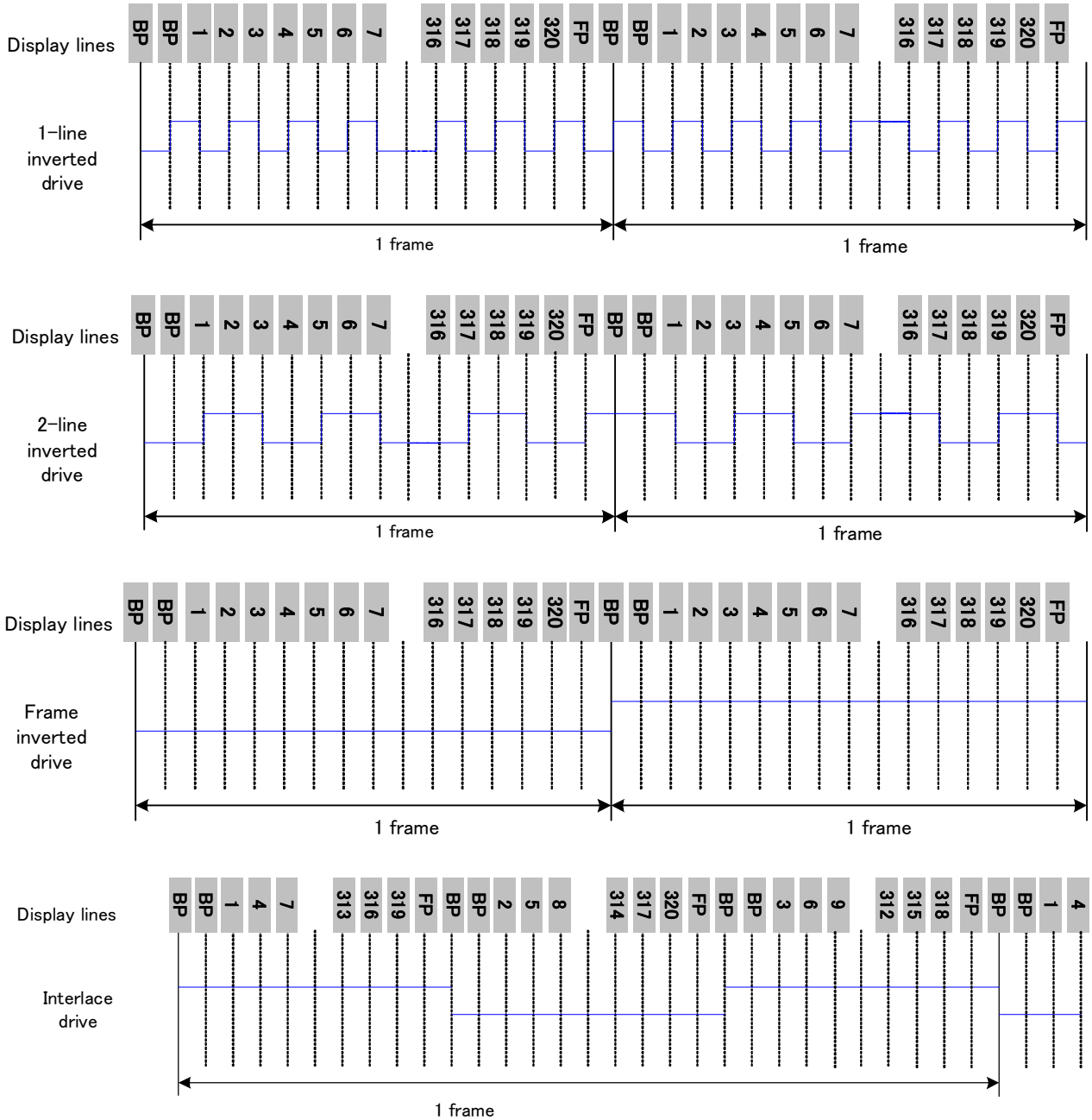


Fig.16 AC Operation Drive

6.3 Oscillation Circuit

This is a fully built-in CR-type oscillator to generate display clocks. The oscillation starts when reset is released after power-ON.

6.4 Setting Gate Line Scan Mode

It can be selected two-side interlace driving or two-side up and down driving.

The drive mode is specified with the GATESET command. There is a gate line of a maximum of 320 lines. And the gate line of 160 lines is in right and left. When using it by less than 320 lines, it assigns equally from both side (G1 and G2, outer gate pins are used) or both side(G320 and G319, inner gate pins are used). Odd line number can be set. Unused gate lines output VEE.

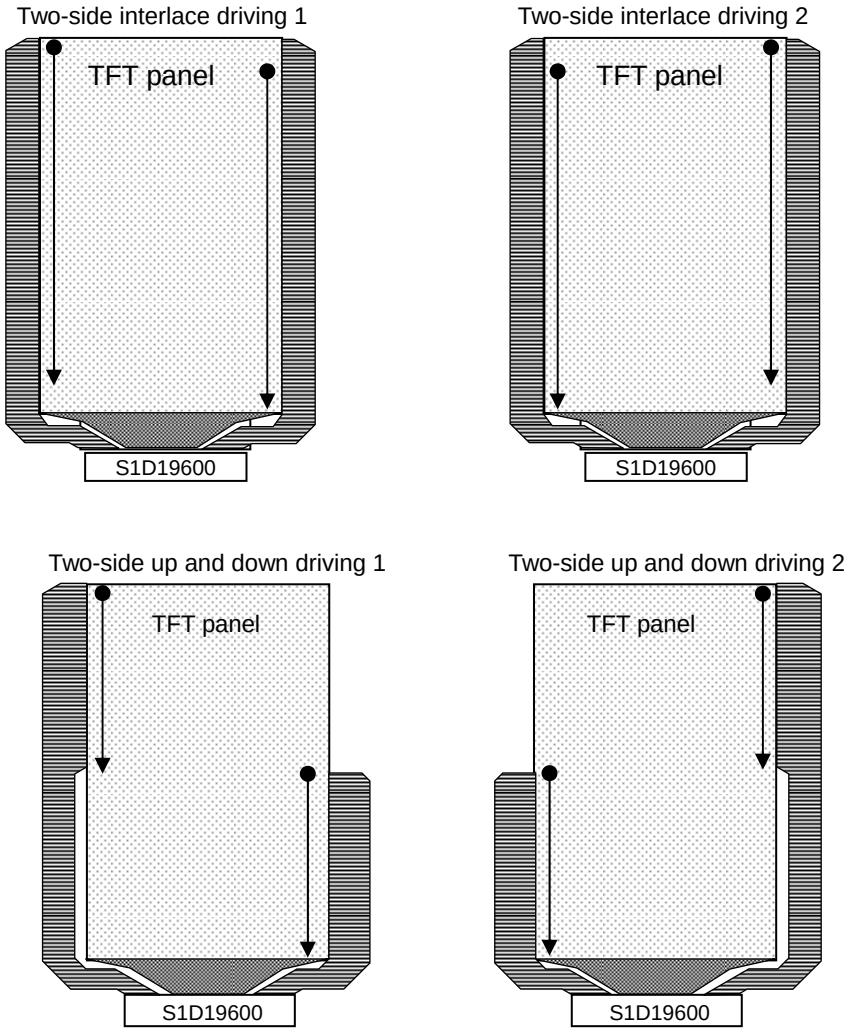
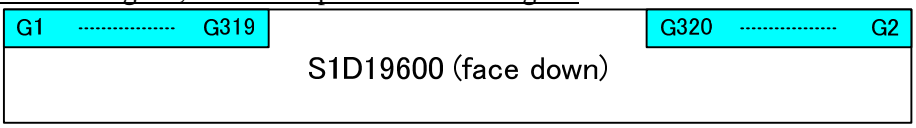


Fig.17 Gate line scan mode

- Example of 320 display line (Both Outer gate lines used and Inner gate lines used are common)

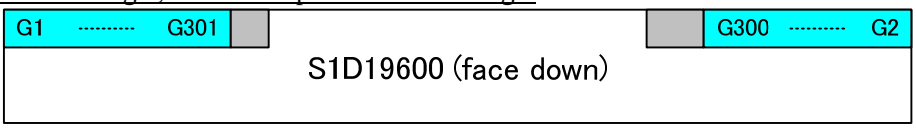
Two-side interlace driving 1/2, Two-side up and down driving 1/2



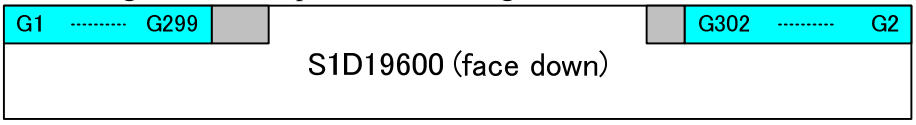
Scan mode		Scan order
Two-side interlace driving 1	Normal	G1 → G2 → G3 → G4 → ・・・ → G319 → G320
	Reverse	G320 → G319 → G318 → G317 → ・・・ → G2 → G1
Two-side interlace driving 2	Normal	G2 → G1 → G4 → G3 → ・・・ → G320 → G319
	Reverse	G319 → G320 → G317 → G318 → ・・・ → G1 → G2
Two-side up and down driving 1	Normal	G1 → G3 → ・・・ → G317 → G319 → G2→ G4→ ・・・ → G318 → G320
	Reverse	G320→ G318→ ・・・ → G4 → G2 → G319 → G317 → ・・・ → G3 → G1
Two-side up and down driving 2	Normal	G2 → G4 → ・・・ → G318 → G320 → G1 → G3 → ・・・ → G317 → G319
	Reverse	G319 → G317 → ・・・ → G3 → G1 → G320 → G318 → ・・・ → G4 → G2

- Example of 301 display line (Outer gate lines used)

Two-side interlace driving 1, Two-side up and down driving 1



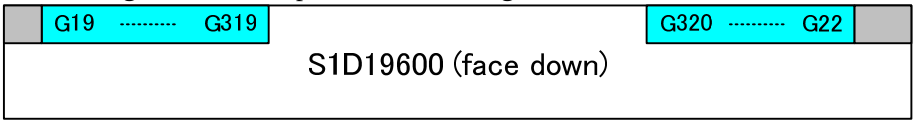
Two-side interlace driving 2, Two-side up and down driving 2



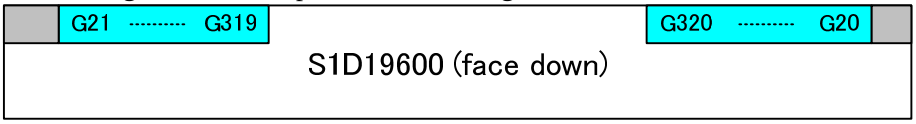
Scan mode		Scan order
Two-side interlace driving 1	Normal	G1 → G2 → G3 → G4 → ・・・ → G300 → G301
	Reverse	G301 → G300 →G299 → G298 → ・・・ → G2 → G1
Two-side interlace driving 2	Normal	G2 → G1 → G4 → G3 → ・・・ → G299 → G302
	Reverse	G302 → G299 → G300 → G297 → ・・・ → G1 → G2
Two-side up and down driving 1	Normal	G1 → G3 → ・・・ → G299 → G301 → G2 → G4 → ・・・ → G298 → G300
	Reverse	G300 → G298 → ・・・ → G4 → G2 → G301 → G299 → ・・・ → G3 → G1
Two-side up and down driving 2	Normal	G2 → G4 → ・・・ → G300 → G302 → G1 → G3 → ・・・ → G297 → G299
	Reverse	G299 → G297 → ・・・ → G3 → G1 → G302 → G300 → ・・・ → G4 → G2

- Example of 301 display line (Inner gate lines used)

Two-side interlace driving 1, Two-side up and down driving 1



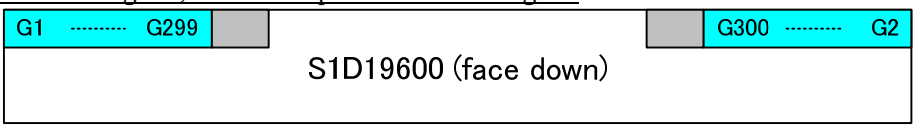
Two-side interlace driving 2, Two-side up and down driving 2



Scan mode		Scan order
Two-side interlace driving 1	Normal	G19 → G22 → G21 → G24 → ・・・ → G320 → G319
	Reverse	G319 → G320 →G317 → G318 → ・・・ → G22 → G19
Two-side interlace driving 2	Normal	G20 → G21 → G22 → G23 → ・・・ → G319 → G320
	Reverse	G320 → G319 → G318 → G317 → ・・・ → G21 → G20
Two-side up and down driving 1	Normal	G19 → G21 → ・・・ → G317 → G319 → G22 → G24 → ・・・ → G318 → G320
	Reverse	G320 → G318 → ・・・ → G24 → G22 → G319 → G317 → ・・・ → G21 → G19
Two-side up and down driving 2	Normal	G20 → G22 → ・・・ → G318 → G320 → G21 → G23 → ・・・ → G317 → G319
	Reverse	G319 → G317 → ・・・ → G23 → G21 → G320 → G318 → ・・・ → G22 → G20

- Example of 300 display line (Outer gate lines used)

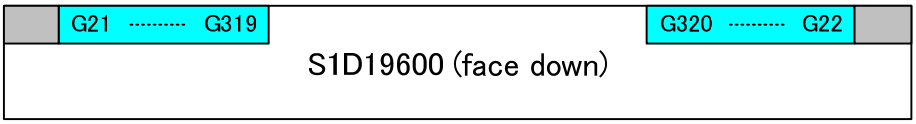
Two-side interlace driving 1/2, Two-side up and down driving 1/2



Scan mode		Scan order
Two-side interlace driving 1	Normal	G1 → G2 → G3 → G4 → ・・・ → G299 → G300
	Reverse	G300 → G299 →G298 → G297 → ・・・ → G2 → G1
Two-side interlace driving 2	Normal	G2 → G1 → G4 → G3 → ・・・ → G300 → G299
	Reverse	G299 → G300 → G297 → G298 → ・・・ → G1 → G2
Two-side up and down driving 1	Normal	G1 → G3 → ・・・ → G297 → G299 → G2 → G4 → ・・・ → G298 → G300
	Reverse	G300 → G298 → ・・・ → G4 → G2 → G299 → G297 → ・・・ → G3 → G1
Two-side up and down driving 2	Normal	G2 → G4 → ・・・ → G298 → G300 → G1 → G3 → ・・・ → G297 → G299
	Reverse	G299 → G297 → ・・・ → G3 → G1 → G300 → G298 → ・・・ → G4 → G2

- Example of 300 display line (Inner gate lines used)

Two-side interlace driving 1/2, Two-side up and down driving 1/2



Scan mode		Scan order
Two-side interlace driving 1	Normal	G21 → G22 → G23 → G24 → ・・・ → G319 → G320
	Reverse	G320 → G319 → G318 → G317 → ・・・ → G22 → G21
Two-side interlace driving 2	Normal	G22 → G21 → G24 → G23 → ・・・ → G320 → G319
	Reverse	G319 → G320 → G317 → G318 → ・・・ → G21 → G22
Two-side up and down driving 1	Normal	G21 → G23 → ・・・ → G317 → G319 → G22 → G24 → ・・・ → G318 → G320
	Reverse	G320 → G318 → ・・・ → G24 → G22 → G319 → G317 → ・・・ → G23 → G21
Two-side up and down driving 2	Normal	G22 → G24 → ・・・ → G318 → G320 → G21 → G23 → ・・・ → G317 → G319
	Reverse	G319 → G317 → ・・・ → G23 → G21 → G320 → G318 → ・・・ → G24 → G22

6.5 Overview of built-in power supply

The S1D19600 can generate all the voltages to driver LCD as below.

Regulated voltage	: V_{REG}
Power	: VLDO1, VLDO2, V_{OUT}, V_{OUTM},
Voltages for source	: VDDHS, VDDHS2, VDDRH
Voltages for gate	: V_{ONREG}, V_{OFREG}, V_{DDHG}, V_{EE}
Voltages for common electrode	: V_{COMH}, V_{COML}, VCA

The S1D19600 has electric volume function, therefore it is possible to adjust each voltages. Electric volume can be controlled by EVSET1,2 (electric volume set) command. And built-in regulator circuit provide stabilized voltages for LCD due to separate to external system voltages.

1st / 2nd/ 3rd/ 4th/ boosters are built-in.

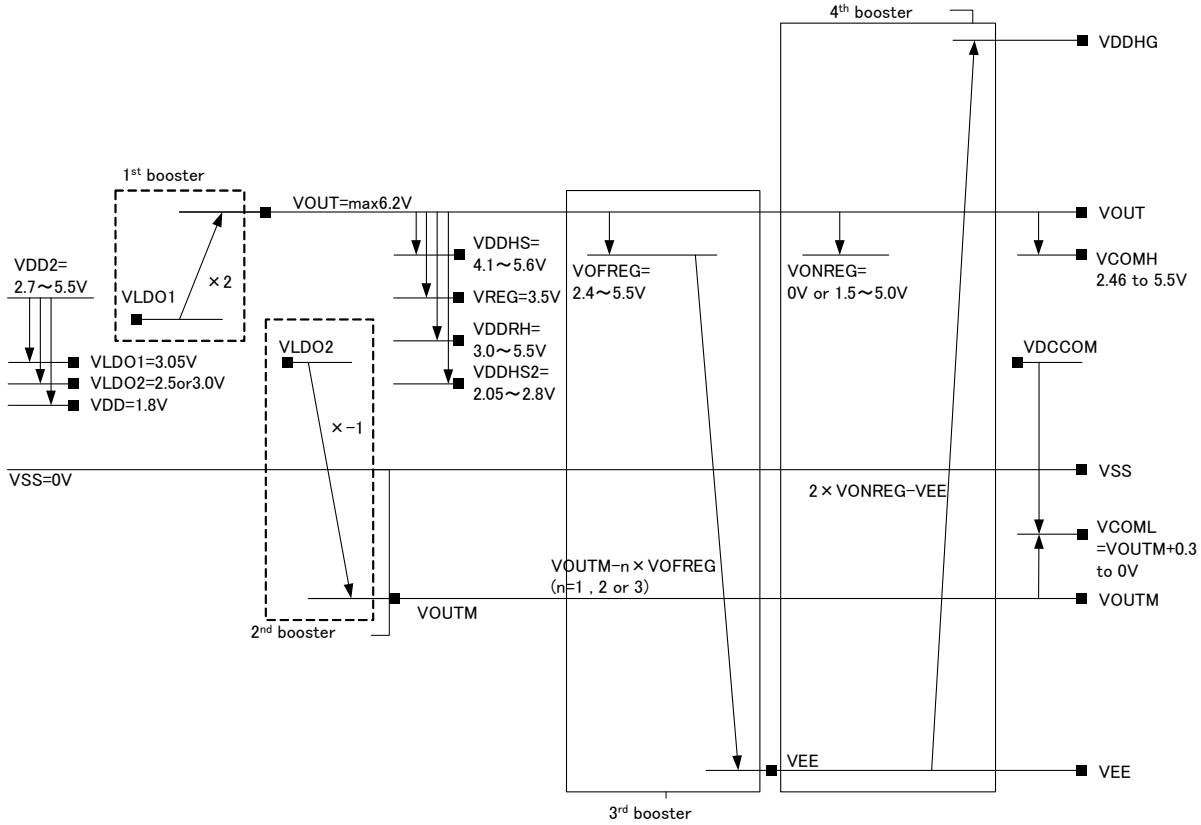


Fig.18 Relationship between voltages

6.6 Power Supply for LCD and Main Specifications for Power Supply

Table 23 Power Supply for LCD and Main Specifications for Power Supply

No.	Parameter		value
1	Number of source lines for TFT panel		320
2	Number of gate lines for TFT panel		320
3	Structure of TFT panel holding capacity		Cst structure
4	Output for LCD driving	S1-S320	V_0 to V_{15}(analog gray scale)
		G1-G320	Gate ON voltage: V_{DDHG} Gate OFF voltage: V_{EE}
		V_{COM}	Common HIGH voltage V_{COMH} Adjustment with the electronic control or external EEPROM. Common LOW voltage V_{COML} Automatic setting with V_{COMH} - VCA × 2 Common amplitude: VCA × 2 Adjustment with electronic control
5	External power supply	V_{DDI}	IO power supply
		V_{DD2}	Reference power supply for booster circuit, for generate V_{DD}, V_{LDO1} and V_{LDO2}.
		V_{OUT} (1^{st} booster input)	Voltage for source and V_{COM} voltages (V_{DD2} is enough higher than LCD voltage)
		V_{DCCOM}	Voltage for V_{COM} generating
6	Bulit-in power supply	V_{DD}	RAM and logic power supply.
		V_{LDO1}	Voltage for V_{OUT} generating
		V_{LDO2}	Voltage for V_{OUTM} generating
		V_{OUT} (1^{st} booster output)	Power supply for source and V_{COM} generation V_{LDO1} × 2
		V_{REG}	Reference voltage
		V_{DDHS2}	Voltage for source driver
		V_{DDHS}	Voltage for source driver
		V_{DDRH}	Maximum gray scale voltage
		V_{COMH}	V_{COM} HIGH voltage
		V_{OUTM} (2nd booster output)	Voltage for V_{COML} generation. V_{LDO2} × -1
		V_{COML}	V_{COM} LOW voltage
		V_{EE} (3rd booster output)	Gate OFF voltage
		V_{DDHG} (4th booster output)	Gate ON voltage

6.6.1 Basic Configuration Diagram of Built-in Power Supply

The S1D19600 contains a power supply circuit for liquid crystal drive. Select the external circuit configuration appropriate for your specifications by referring to the recommended basic circuits provided for stable use of built-in power circuit.

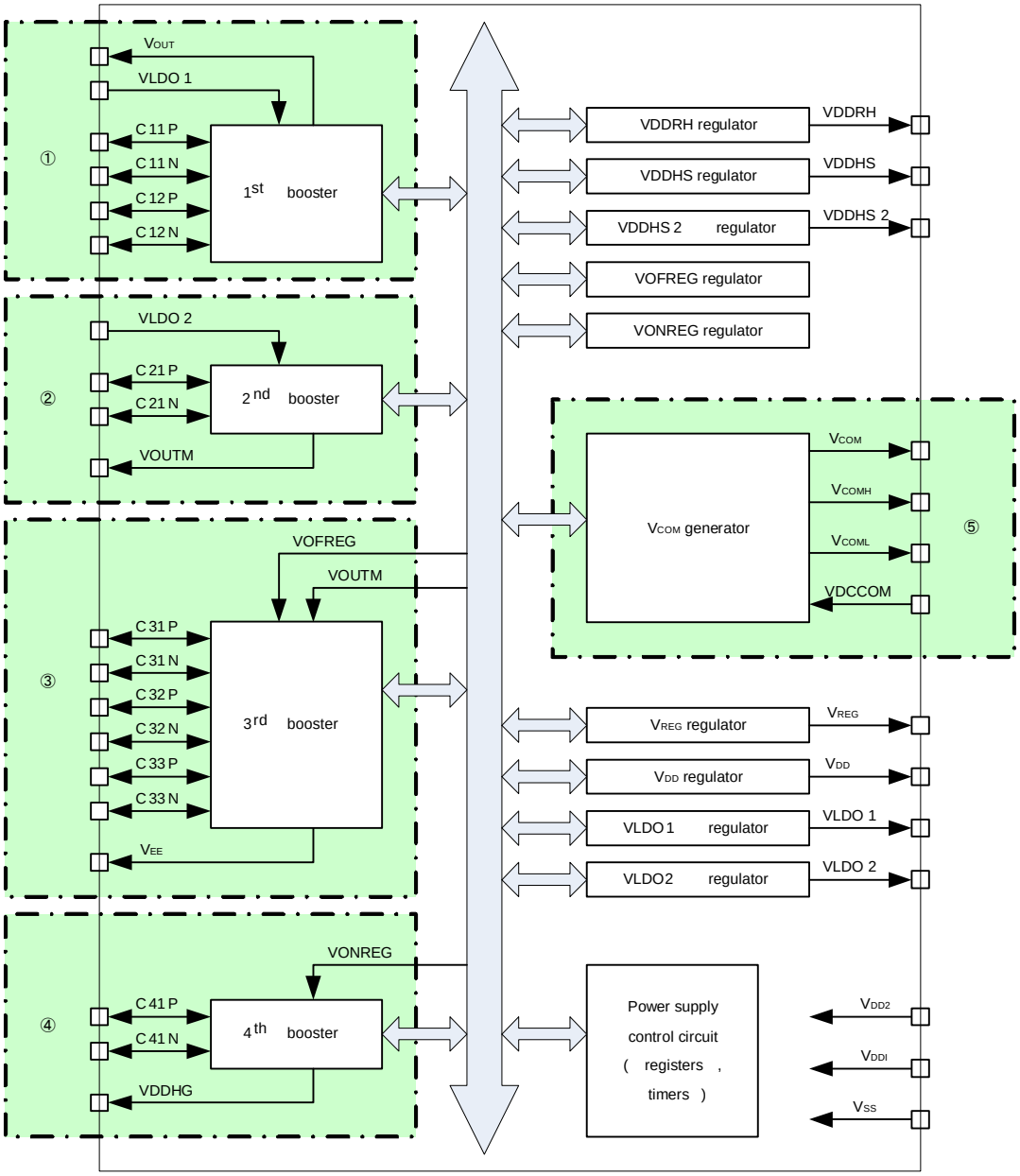


Fig.19 Basic Configuration Diagram of Built-in Power Circuits

6.6.2 External power supply connection

The external power supply (*1) for 1st and 2nd booster circuit has some combination by V_{DDI} and V_{DD2} voltages. This combination can be changed by CPSET1/2/3 pins.

CPSET1 pin changes output voltage of V_{LDO2}. (H: V_{LDO2} = 2.5V, L: V_{LDO2} = 3.0V)

When CPSET1 = LOW, a stabilized capacitance between V_{LDO2} and V_{SS} is required.

CPSET2 pin changes VOUT external input or built-in V_{OUT}. (H: V_{OUT} external input, L: built-in V_{OUT})

$V_{OUT} - 0.4V \geq V_{DDRH}$ (maximum source output voltage) must be satisfied.

V_{OUT} external input can reduce external capacitance, however please be careful to source output voltage range.

CPSET3 pin must be LOW.

*1 V_{LDO2}, V_{DCCOM}, C11P, C11N, C12P, C12N, V_{OUT} pins.

Table 24 connection by CPSET1/2/3

CPSET3	CPSET2	CPSET1	Connect to						State
			V_{DDI}	V_{DD2}	V_{LDO2}	V_{DCCOM}	C11P,C11N, C12P,C12N	V_{OUT}	
L	L	L	2.7 to 5.5V input	2.7 to 5.5V input	CAP	VLDO2	CAP	CAP	Built-in VOUT VLDO2 = 3.0 V
L	L	H	2.7 to 5.5V input	2.7 to 3.6V input	OPEN	VDD2	CAP	CAP	Built-in VOUT VLDO2 = 2.5 V
L	H	L	2.7 to 5.5V input	4.5 to 5.5V input	CAP	VLDO2	OPEN	VDD2 *1	VOUT external input VLDO2 = 3.0 V
L	H	H	2.7 to 3.6V input	4.5 to 5.5V input	OPEN	VDDI	OPEN	VDD2 *1	VOUT external input VLDO2 = 2.5 V

*1: External power supply is possible within 5.5 to 6.2 V range.

Followings are examples each for external supply voltages;

■ Case: External VDDI = VDD2 = 3.0±0.3V or VDDI = VDD2 = 3.3±0.3V

Example 1-2 has a merit that no need capacitance to VLDO2, however VOUTM voltage is higher than the voltage of example 1-1. Choose by VCOML voltage.

Table 25 Examples in case of VDD2=3.0±0.3V or VDD2=3.3±0.3V

	CPSET3	CPSET2	CPSET1	Connect to				State
				VLDO2	VDCCOM	C11P,C11N, C12P,C12N	VOUT	
Example 1-1	L	L	L	CAP	VLDO2	CAP	CAP	Built-in VOUT VLDO2 = 3.0 V
Example 1-2	L	L	H	OPEN	VDD2	CAP	CAP	Built-in VOUT VLDO2 = 2.5 V

Table 26 usable range of V_{OUT} and V_{OUTM}

	V_{OUT}		V_{OUTM}
	2.7≤VDD2≤3.05	3.05≤VDD2≤3.3	
Example 1-1	V_{DD2} x 2 – a	6.1V – a	−3.0V+b
Example 1-2	V_{DD2} x 2 – a	6.1V – a	−2.5V+b

a: Voltage drop by V_{OUT} system power consumption

b: Voltage up by V_{OUTM} system power consumption

■ Case : External voltage $V_{DDI}=V_{DD2}=5.0\pm0.5V$

$V_{OUT} - 0.4V \geq V_{DDRH}$ (maximum source output voltage) must be satisfied. VOUT external input can reduce external capacitance, however please be careful to source output voltage range.

Table 27 Example of $V_{DDI}=V_{DD2}=5.0\pm0.5V$

	CPSET3	CPSET2	CPSET1	Connect to				State
				VLDO2	VDCCOM	C11P,C11N, C12P,C12N	VOUT	
Example 2-1	L	L	L	CAP	VLDO2	CAP	CAP	Built-in VOUT VLDO2 = 3.0 V
Example 2-2	L	H	L	CAP	VLDO2	OPEN	VDD2	VOUT external input VLDO2 = 3.0 V

Table 28 usable range of V_{OUT} and V_{OUTM}

	V_{OUT}	V_{OUTM}
Example 2-1	6.1 V – a	−3.0V + b
Example 2-2	VDD2 – a	−3.0V + b

a: Voltage drop by V_{OUT} system power consumption
b: Voltage up by V_{OUTM} system power consumption

■ Case : External voltage $V_{DDI}=3.0\pm0.3V$, $V_{DD2}=5.0\pm0.5V$ or $V_{DDI}=3.3\pm0.3V$, $V_{DD2}=5.0\pm0.5V$

Table 29 Example of $V_{DDI}=3.0\pm0.3V$, $V_{DD2}=5.0\pm0.5V$ or $V_{DDI}=3.3\pm0.3V$, $V_{DD2}=5.0\pm0.5V$

	CPSET3	CPSET2	CPSET1	Connect to				State
				VLDO2	VDCCOM	C11P,C11N, C12P,C12N	VOUT	
Example 3-1	L	H	H	OPEN	VDDI	OPEN	VDD2	VOUT external input VLDO2 = 2.5 V

Table 30 usable range of V_{OUT} and V_{OUTM}

	V_{OUT}	V_{OUTM}
Example 3-1	VDD2 – a	−2.5V + b

a: Voltage drop by V_{OUT} system power consumption
b: Voltage up by V_{OUTM} system power consumption

6.6.3 The 1st Booster Circuit

The 1st booster circuit, comprised of a charge pump type DC/DC converter. The booster converts the input voltage (V_{LDO1}) to the power supply for the LCD power supply circuit for driving (V_{OUT}) by doubling the voltage.

When V_{DD2} is enough higher than LCD voltage, the 1st booster can be stopped by $V_{OUT}=V_{DD2}$ or VDDI. And it is possible to supply other voltage than VDD2 and VDDI to VOUT. (Refer to 6.6.2 external power supply connection.) In this case, external CAP and schottky barrier diode can be deleted.

$$V_{OUT} = 2 \times V_{LDO1} \text{ [V]}$$

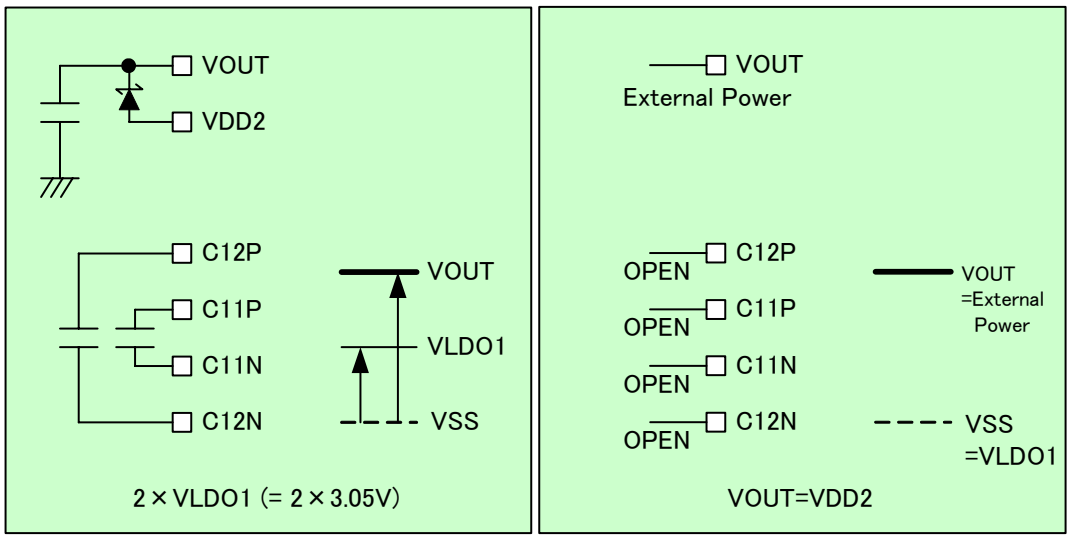


Fig.20 The 1st Booster Circuit (Connection Example)

6.6.4 The 2nd Booster Circuit

The 2nd booster circuit, comprised of a charge pump type DC/DC converter. The booster converts the input power voltage (V_{LDO2}) to the power voltage (V_{OUTM}) for the V_{COM} circuit by multiplying the voltage by -1 time with reference to V_{SS}.

$$V_{OUTM} = -1 \times V_{LDO2} \text{ [V]}$$

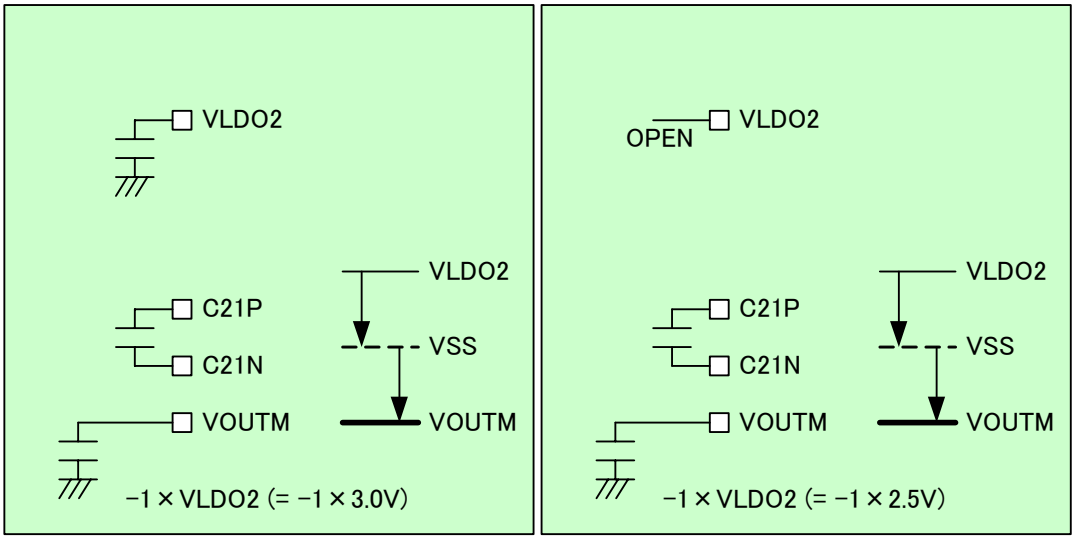


Fig.21 The 2nd Booster Circuit (Connection Example)

6.6.5 The 3rd Booster Circuit

The 3rd booster circuit, comprised of a charge pump type DC/DC converter. The booster converts the input power voltage (V_{OFREG}) to gate driver negative power voltage (V_{EE}) by multiplying the voltage by –n times with reference to V_{OUTM}.

$$V_{EE} = V_{OUTM} – n \times V_{OFREG} \text{ [V]} \quad (n = 1, 2 \text{ or } 3)$$

The 3rd booster circuit can be changed by following connections from Fig.19

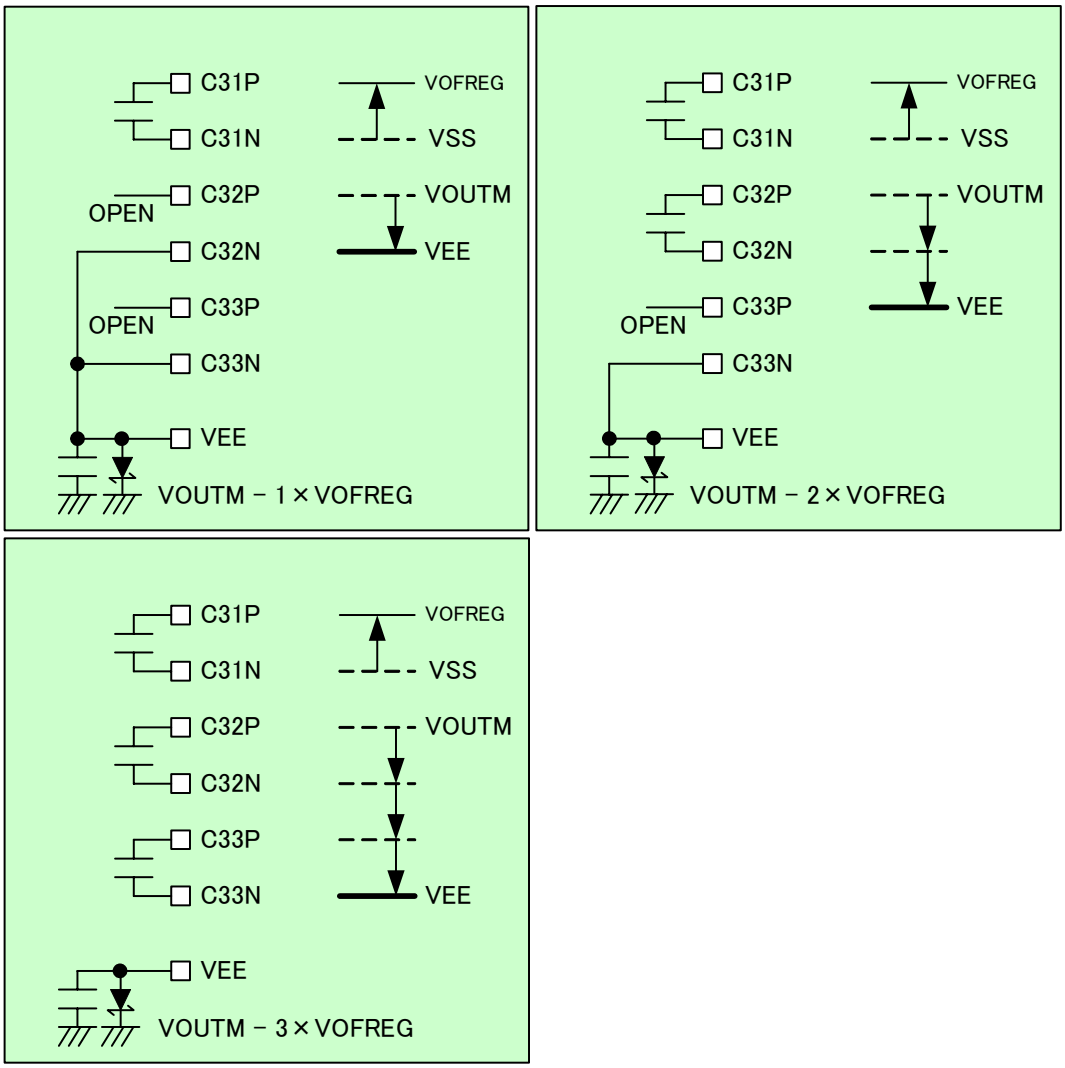


Fig.22 The 3rd Booster Circuit (Connection Example)

6.6.6 The 4th Booster Circuit

The 4th booster circuit, comprised of a charge pump type DC/DC converter, is a reverse booster circuit. The 4th booster circuit inverts input voltage (V_{ONREG}-V_{EE}) based on V_{ONREG}.

$$V_{DDHG} = 2 \times V_{ONREG} - V_{EE} \text{ [V]}$$

The 4th booster circuit can be changed by following connections from Fig.19

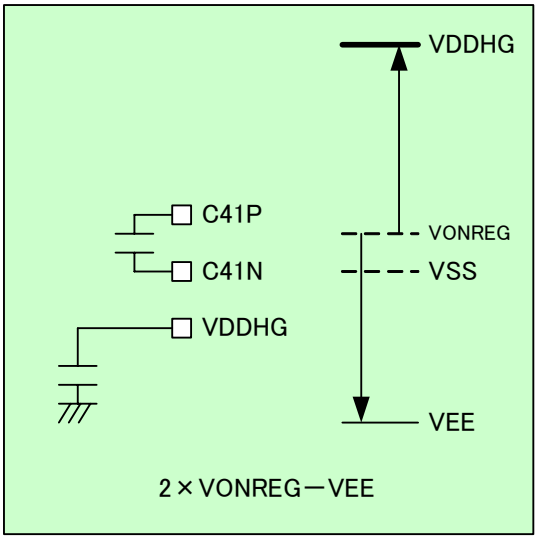


Fig.23 The 4th Booster Circuit Connection Example

6.6.7 VCOM Generation Circuit

The VCOM generation circuit generates the voltage of VCOMH and VCOML needed for generating VCOM output voltage.

VCOMH voltage can be adjusted by EVSET1 command and offset data which is set by VCMDAT commad.

2 setings of offset data can be set. And they are changeable. Offset data can be set either by P2 and P3 of the VCMDAT command or by a data in EEPROM. More detail of EEPROM setting, refer to section 6.11 EEPROM interface.

- Adjustment by EVSET1(No offset)

  Set each parameters as below.

VCMDAT	P13 = 0
EVSET1	P27 to P20 = VCOMH output voltage (Refer to Table 40 Electric volume value)

- Adjustment by EVSET1(With offset)

  Set each parameters as below.

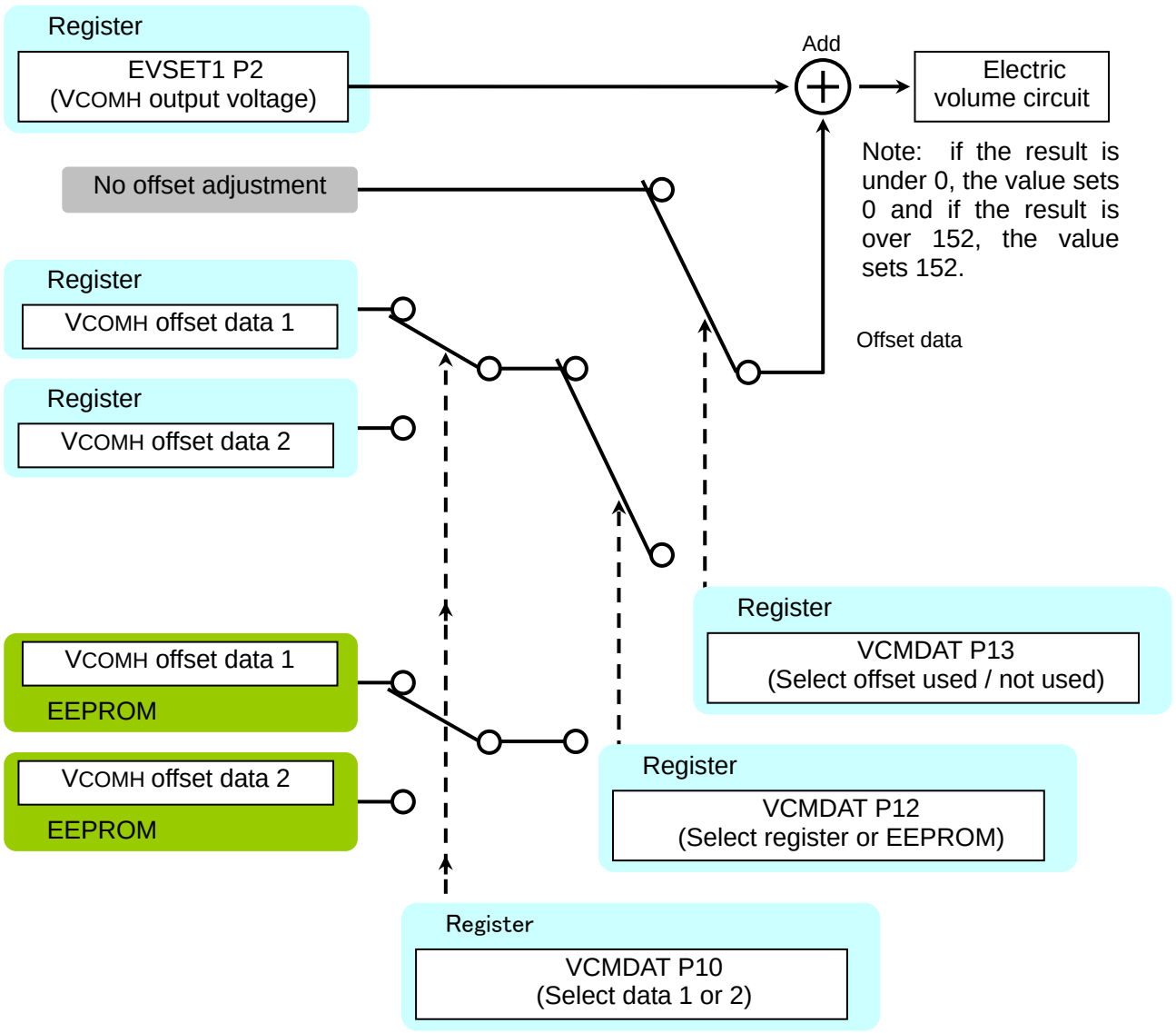
VCMDAT	P13 = 1 (Offset reference place is set by P12 to P10.)
EVSET1	P27 to P20 = VCOMH output voltage (Refer to Table 40 Electric volume value)

VCOMH output voltage offset adjustment circuit is as Fig.24.

VCOML output voltage is as below. (VCOMH voltage is independent from VCOMH adjustment method).

VCOML: $V_{COML} = V_{COMH} - VCA \times 2$ [V]

VCOM output voltage offset circuit.



In case of EEPROM connected, when NVSEL = H, VCMDAT P12 is valid.

Fig.24 VCOMH output voltage offset adjustment circuit.

6.7 Connection Diagram of External Parts

Example of external circuit.
Conditions :
1st booster is used, 3rd booster is -2x
VDD2=3.3 V, VOFREG=4.5 V , VONREG=3.0 V. Below are each voltages with no load.

VOUT	=	2 * VLDO1	=	6.1	[V]
VOUTM	=	-1 * VLDO2	=	- 3.0	[V]
VEE	=	VOUTM – 2 * VOFREG	=	- 12.0	[V]
VDDHG	=	2 *VONREG - VEE	=	18.0	[V]

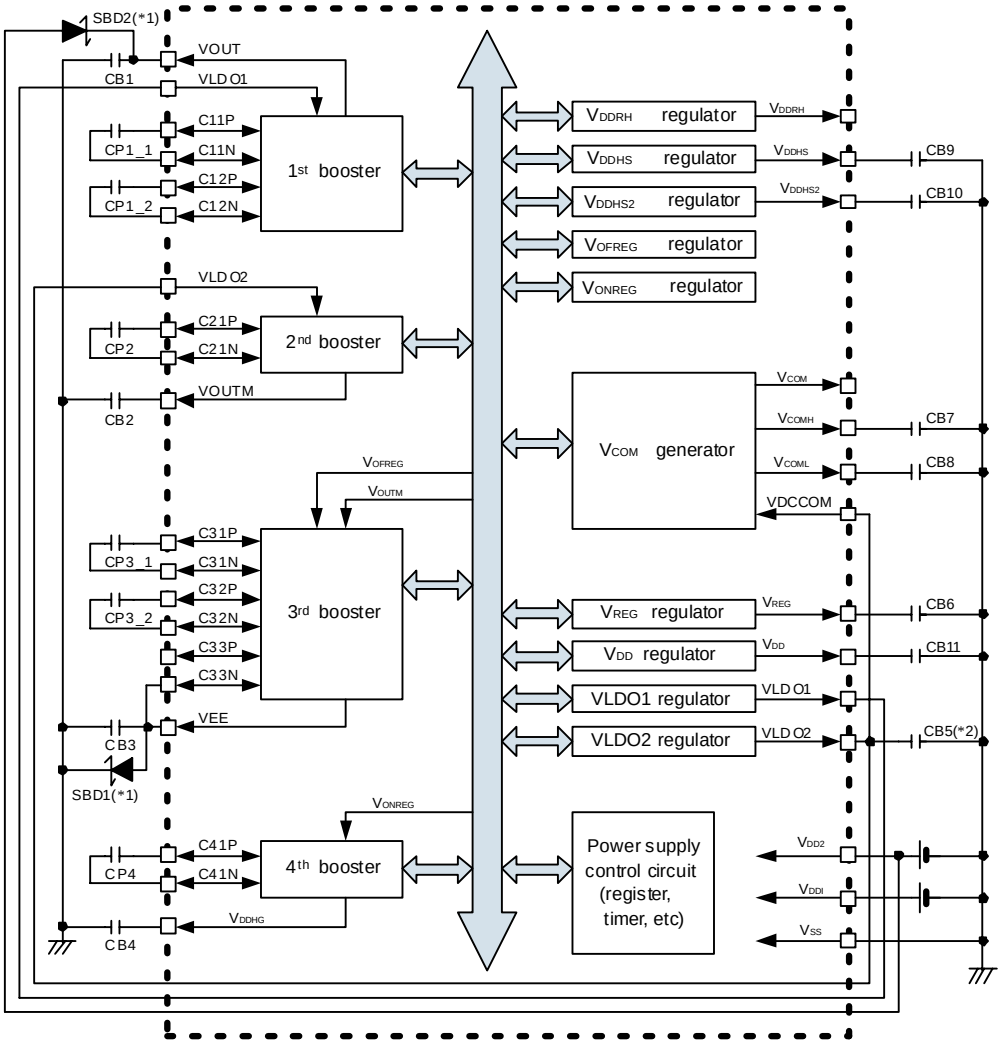


Fig.25 Example of external circuit

*1 Schottky barrier diode is required (approx. VF=0.4V/20mA VR>30V)
When VOUT is supplied externally, no need SBD2

*2 In case of CPSET1=HIGH, it is not required.

Table 31 recommended values

Circuit	Capacitance	Value [µF]	Logical equation between both sides of Capacitance	Logical equation maximum value between both sides of Capacitance
1st booster	CP1_1	2.2	V_{DD2}-V_{SS}	V_{DD2}
	CP1_2	2.2	V_{DD2}-V_{SS}	V_{DD2}
	CB1	2.2	V_{OUT}-V_{SS}	V_{DD2} × 2
2nd booster	CP2	2.2	V_{DD2}-V_{SS}	V_{DD2}
	CB2	2.2	V_{SS}-V_{OUTM}	V_{DD2}
	CB5	2.2	VLDO2	VLDO2
3rd booster	CP3_1	1.0	V_{OFREG}-V_{OUTM}	8.6V
	CP3_2	1.0	(2 × V_{OFREG})-V_{OUTM}	14.1V
	CP3_3 *1	1.0	(3 × V_{OFREG})-V_{OUTM}	15V
	CB3	1.0	V_{EE}-V_{SS}	15V
4th booster	CP4	1.0	V_{ONREG} - V_{EE}	15V
	CB4	1.0	V_{DDHG}-V_{SS}	19V
V_{COM} generator	CB6	1.0 to 2.2	V_{REG}	V_{REG}
	CB7	2.2 to 10.0	V_{COMH}	V_{COMH}
	CB8	2.2 to 10.0	V_{COML}	V_{COML}
Voltage regulator	CB9	2.2	V_{DDHS}	V_{DDHS}
	CB10	1.0	V_{DDHS2}	V_{DDHS2}
Power supply	CB11	2.2	V_{DD}	V_{DD}

*1) It is required in case of 3rd booster used as -3 multipe. This CAP is connected between C33P and C33N.

Above maximum voltage is settable maximum voltage when V_{REG} = 3.5V and built-in electric volume is used. It doesn't include V_{REG} deviation.

Capacitance values are recommendation. Please decide capacitance value to evaluate display quality and to confirm stability of LCD driving voltages.

Concerning kind of capacitors, R-characteristics or X7R-characteristics are recommended. When the S1D19600 is used under 85 °C, B-characteristics is recommended. It is recommend to use input voltage between capacitor's pin and pin within 70% of Maximum rated voltage range of the capacitor

Table 32 Recommended schottky barrier diode

Specification	Diode name	Connected pins
VF < 0.4V/20mA, VR >= 30V (at 25°C)	SBD1	Between GND and V_{EE}
	SBD2*1	Between V_{OUT} and V_{DD2}

*1: SBD2 is not required when Vout is connected to external power supply.

Table 33 Recommended wiring resistance in COG case

Kind of pins	Pin name	Resistance
Power supply	V_{DDI}, V_{DD2}, V_{SS}	Under 10 Ω
Multi Time PROM power supply	VME2	Under 20 Ω
	VME1	Under 100 Ω
Boosters	1st , 2nd booster pins VLDO1, VLDO2, VDCCOM	Under 10 Ω
	3rd , 4th booster pins	Under 30 Ω
Regulators	V_{DD}, V_{COML} , V_{COMH} V_{DDHS}	Under 10 Ω
	V_{DDHS2}, V_{REG}	Under 30 Ω
Logic	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0, D0 to D7, SCL, SD etc	Under 100 Ω

Above value is recommendation, and even if it is not satisfied, it maybe operated.

However, wiring resistance of booster pins affects power efficiency, therefore lower resistance as well as possible is recommended

Resistance at VDDHS, VCOMH, VCOML affect display quality. Therefore lower resistance as well as possible is recommended

VREG pin is a base voltage, therefore it is recommended to shield both side by V_{SS} to protect from interference of other signal.

There are VCOM pins at both side of the LSI. Main pins are No.4 to 6 and sub pins are No. 243 to 245. It is recommended to connect both side VCOM pins, however if you choose to use one side, Main pins must be connected. And Resistance at VCOM pins affects display quality. Therefore lower resistance as well as possible is recommended

6.8 Gray scale generating circuit

This circuit generate 64 levels x 2(Positive / Negative) voltages for AC driving. Grayscale voltages can be set to optimize display characteristics.

When 4bpp mode is used, the gray scale setting is done by GAMSET4P1 to 4 / GAMSET4N1 to 4 commands.

When 2bpp mode is used, the gray scale setting is done by GAMSET2P / GAMSET2N command.

When 1bpp mode is used, the gray scale setting is done by GAMSET1 command

- Gray scale voltages

The each voltages are determined as following equation (Table 34) by above commands.

The voltages must be set as following

$V_0 > V_1 > \ldots > V_{14} > V_{15}$

Table 34 Grayscale voltage equation

Command parameters **P*5 to P*0**	**Equation of voltages**	Command parameters **P*5 to P*0**	**Equation of voltages**
0 0 0 0 0 0	V_{DDRH}	1 0 0 0 0 0	$V_{DDRH} \times 31 / 63$
0 0 0 0 0 1	$V_{DDRH} \times 62 / 63$	1 0 0 0 0 1	$V_{DDRH} \times 30 / 63$
0 0 0 0 1 0	$V_{DDRH} \times 61 / 63$	1 0 0 0 1 0	$V_{DDRH} \times 29 / 63$
0 0 0 0 1 1	$V_{DDRH} \times 60 / 63$	1 0 0 0 1 1	$V_{DDRH} \times 28 / 63$
0 0 0 1 0 0	$V_{DDRH} \times 59 / 63$	1 0 0 1 0 0	$V_{DDRH} \times 27 / 63$
0 0 0 1 0 1	$V_{DDRH} \times 58 / 63$	1 0 0 1 0 1	$V_{DDRH} \times 26 / 63$
0 0 0 1 1 0	$V_{DDRH} \times 57 / 63$	1 0 0 1 1 0	$V_{DDRH} \times 25 / 63$
0 0 0 1 1 1	$V_{DDRH} \times 56 / 63$	1 0 0 1 1 1	$V_{DDRH} \times 24 / 63$
0 0 1 0 0 0	$V_{DDRH} \times 55 / 63$	1 0 1 0 0 0	$V_{DDRH} \times 23 / 63$
0 0 1 0 0 1	$V_{DDRH} \times 54 / 63$	1 0 1 0 0 1	$V_{DDRH} \times 22 / 63$
0 0 1 0 1 0	$V_{DDRH} \times 53 / 63$	1 0 1 0 1 0	$V_{DDRH} \times 21 / 63$
0 0 1 0 1 1	$V_{DDRH} \times 52 / 63$	1 0 1 0 1 1	$V_{DDRH} \times 20 / 63$
0 0 1 1 0 0	$V_{DDRH} \times 51 / 63$	1 0 1 1 0 0	$V_{DDRH} \times 19 / 63$
0 0 1 1 0 1	$V_{DDRH} \times 50 / 63$	1 0 1 1 0 1	$V_{DDRH} \times 18 / 63$
0 0 1 1 1 0	$V_{DDRH} \times 49 / 63$	1 0 1 1 1 0	$V_{DDRH} \times 17 / 63$
0 0 1 1 1 1	$V_{DDRH} \times 48 / 63$	1 0 1 1 1 1	$V_{DDRH} \times 16 / 63$
0 1 0 0 0 0	$V_{DDRH} \times 47 / 63$	1 1 0 0 0 0	$V_{DDRH} \times 15 / 63$
0 1 0 0 0 1	$V_{DDRH} \times 46 / 63$	1 1 0 0 0 1	$V_{DDRH} \times 14 / 63$
0 1 0 0 1 0	$V_{DDRH} \times 45 / 63$	1 1 0 0 1 0	$V_{DDRH} \times 13 / 63$
0 1 0 0 1 1	$V_{DDRH} \times 44 / 63$	1 1 0 0 1 1	$V_{DDRH} \times 12 / 63$
0 1 0 1 0 0	$V_{DDRH} \times 43 / 63$	1 1 0 1 0 0	$V_{DDRH} \times 11 / 63$
0 1 0 1 0 1	$V_{DDRH} \times 42 / 63$	1 1 0 1 0 1	$V_{DDRH} \times 10 / 63$
0 1 0 1 1 0	$V_{DDRH} \times 41 / 63$	1 1 0 1 1 0	$V_{DDRH} \times 9 / 63$
0 1 0 1 1 1	$V_{DDRH} \times 40 / 63$	1 1 0 1 1 1	$V_{DDRH} \times 8 / 63$
0 1 1 0 0 0	$V_{DDRH} \times 39 / 63$	1 1 1 0 0 0	$V_{DDRH} \times 7 / 63$
0 1 1 0 0 1	$V_{DDRH} \times 38 / 63$	1 1 1 0 0 1	$V_{DDRH} \times 6 / 63$
0 1 1 0 1 0	$V_{DDRH} \times 37 / 63$	1 1 1 0 1 0	$V_{DDRH} \times 5 / 63$
0 1 1 0 1 1	$V_{DDRH} \times 36 / 63$	1 1 1 0 1 1	$V_{DDRH} \times 4 / 63$
0 1 1 1 0 0	$V_{DDRH} \times 35 / 63$	1 1 1 1 0 0	$V_{DDRH} \times 3 / 63$
0 1 1 1 0 1	$V_{DDRH} \times 34 / 63$	1 1 1 1 0 1	$V_{DDRH} \times 2 / 63$
0 1 1 1 1 0	$V_{DDRH} \times 33 / 63$	1 1 1 1 1 0	$V_{DDRH} \times 1 / 63$
0 1 1 1 1 1	$V_{DDRH} \times 32 / 63$	1 1 1 1 1 1	V_{SS}

6.9 Resetting

When the power is turned on, resetting by the $\overline{RES}$ pin and SWRESET command are necessary. The $\overline{RES}$ pin must be LOW and RESEN must be HIGH when power is turned on. And the $\overline{RES}$ pin must be kept LOW 1ms or more, and after that, change XRES to HIGH and after that, input SWRESET command. Each input pin must be normally controlled after reset. In case of reset except power-ON, the LOW pulse width of XRES must be 20μs or more.

For the default value of the command and parameter after reset, refer to 7.2 default values of command parameter.

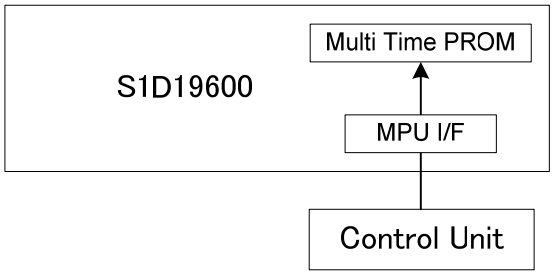
To set RESEN to Low after releasing RESET disables XRES pin in order to reduce exrenal noise malfunction. When RESEN is not used, set RESEN to HIGH. (Refer to 8.2)

6.10 Multi Time PROM Circuit

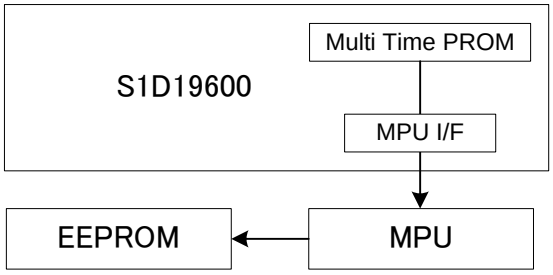
6.10.1 Overview

The S1D19600 has a 48bit Multi- Time-PROM which can be rewritable up to 5times.
8 + 8bits for adjustment V_{COMH} offset, and 32bits for user ID.
The Multi Time PROM is temporary memory. The usage is data carrier such as that unique data of LCD module is stored to the Multi Time PROM of the S1D19600, and the data is stored to external non volatile memory on final application. After that, the access of Multi Time PROM is prohibited.
Following is procedure of handring over the data;

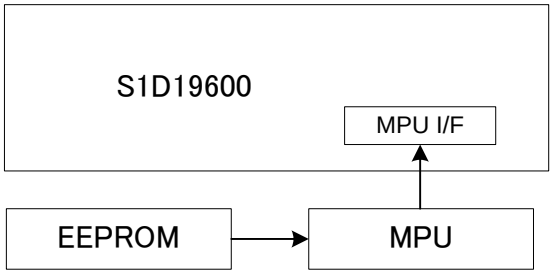
1) Decide VCOM offset data (refer to 6.6.7 VCOM generation circuit) and write the data to the Multi- Time PROM.



2) Read the Multi Time PROM data to MPU by RDVCMDAT command, and write the data to external EEPROM.



3) After installing the S1D19600 to final application, read the data from external EEPROM and write the data to the S1D19600.



6.10.2 Multi Time PROM read

VCOMH offset data in Multi Time PROM can be read by RDVCMDAT command.
And User ID data can be read by RDUID command.

6.10.3 Multi Time PROM erase

Before writing to Multi Time PROM, it is required to erase data in the Multi Time PROM.
The Multi Time PROM erase can be done each 2 blocks independently. Each 2 blocks are following;

- VCOMH offset data 16bit (8bit x 2 sets) + user ID 16bit
- Other user ID 16bit

The erase operation is shown on figure 26.

Note) High voltage which is input to VME1 is input directly to internal memory cells, therefore input it with attention to overshoot and undershoot.

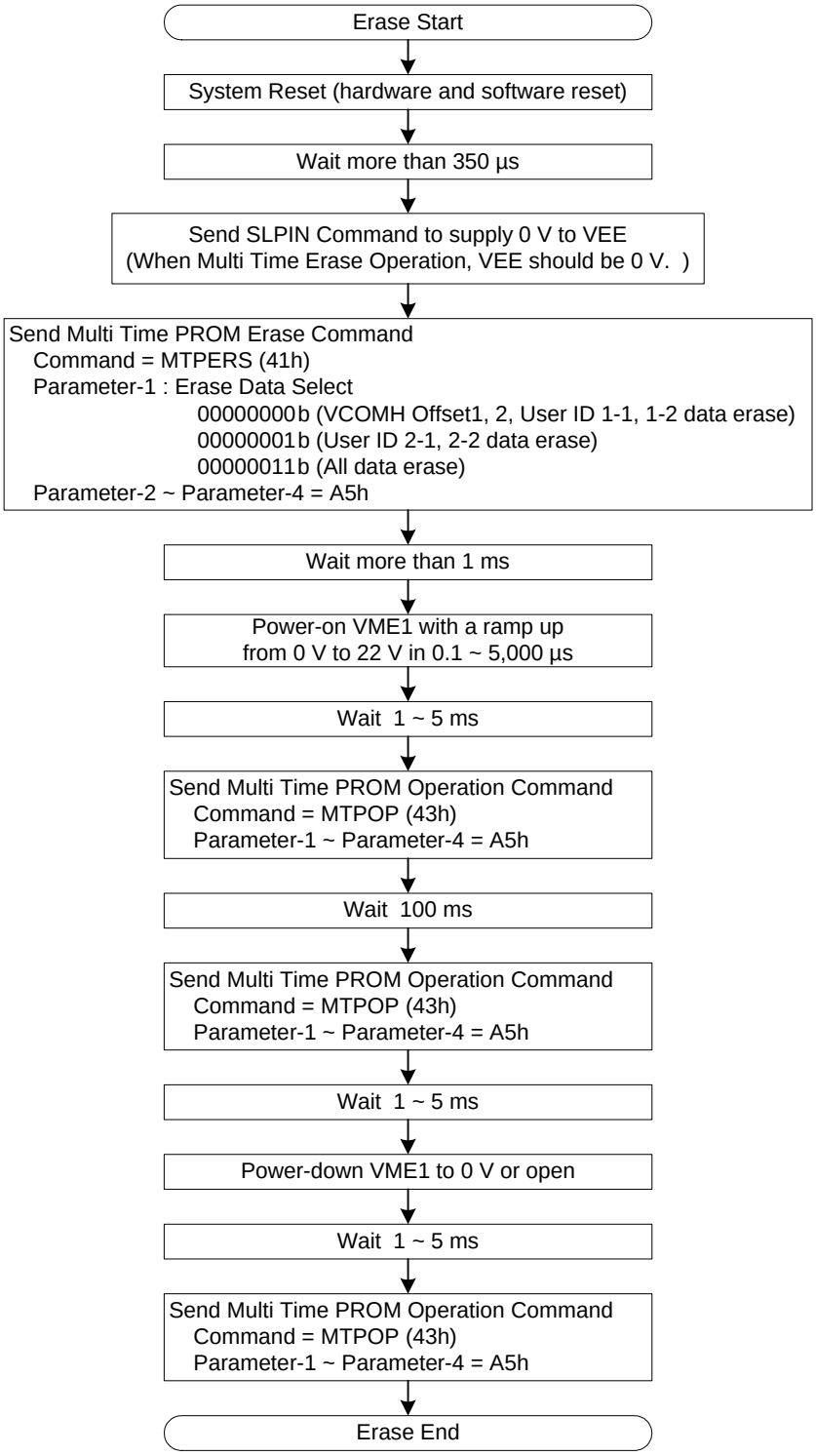


Fig. 26 Multi Time PROM erase sequence

6.10.4 Multi Time PROM programming

Multi time PROM programming sequence is shown as fig. 27.
Before programming, the programming area must be erased. Prohibit to programming without erasing.

Note)
1. High voltage which is input to VME2 is input directly to internal memory cells, therefore input it with attention to overshoot and undershoot.
2. Programming (writing) must be execute after erasing.
3. Data after erasing is “0”. Writing operation is changing from “0” to “1”. Writing from “1” to “0” is not available. Prohibit to over-write “1” to “1”.

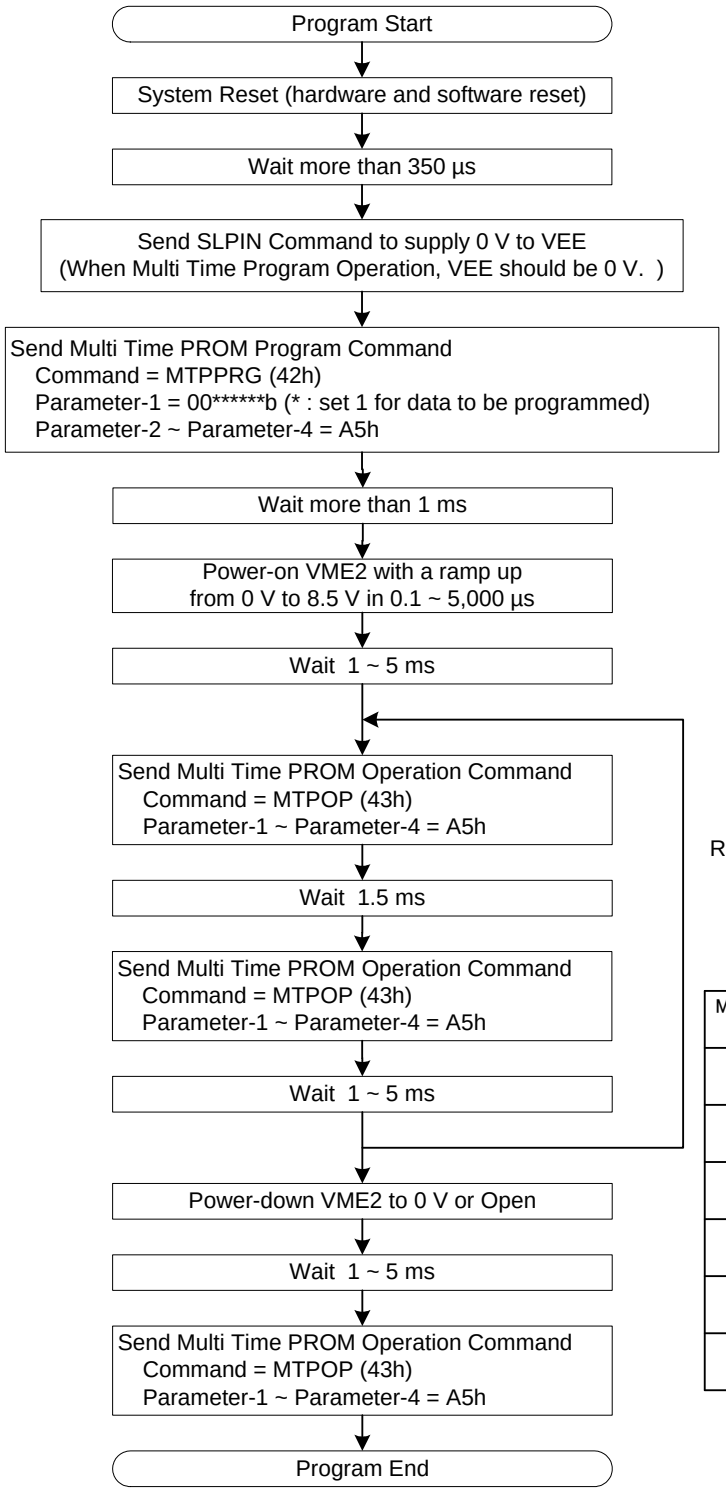


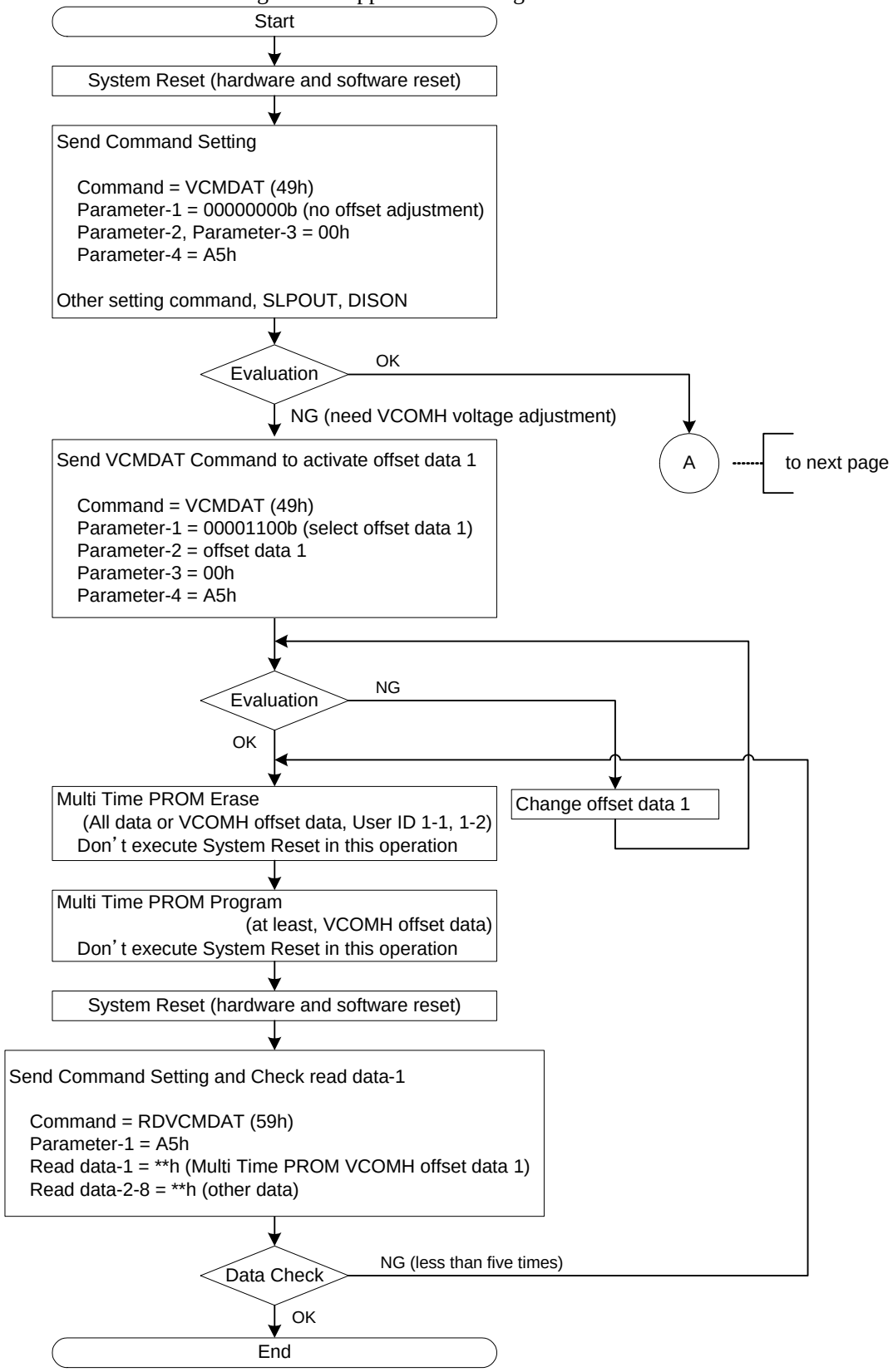
Table of Repeat Coefficient

MTPPRG Px	Contents	Repeat Coefficient
P15	VCOMH Offset-1	4
P14	VCOMH Offset-2	4
P13	User ID 1-1	2
P12	User ID 1-2	2
P11	User ID 2-1	2
P10	User ID 2-2	2

fig 27 Multi Time PROM programming sequence

6.10.5 VCOMH offset data adjustment sequence

VCOMH offset data adjustiment sequence whichi is written to Multi Time PROM is shown fig. 28.
Data of the Multi Time PROM at shipping is “0”.
The Data retention after assembling in final application is not guaranteed.



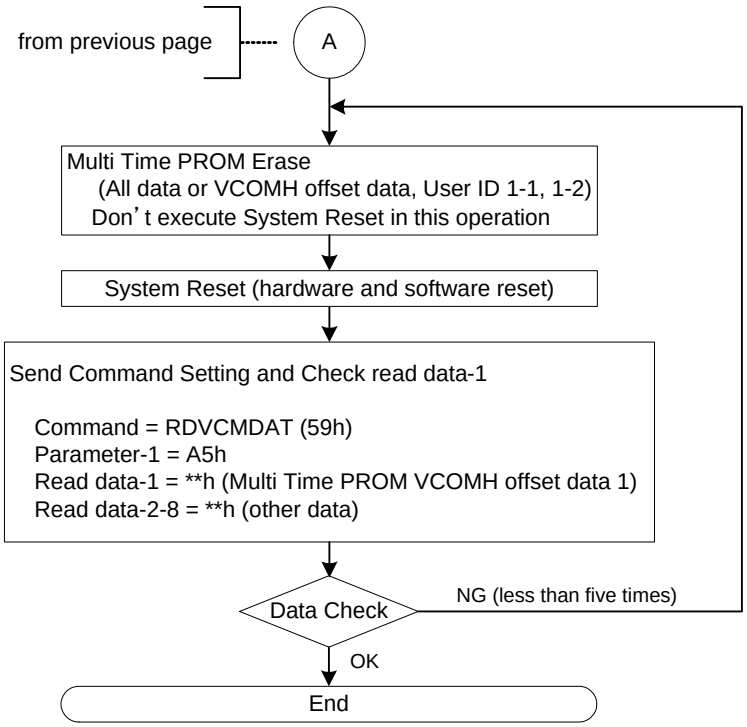


Fig.28 VCOMH offset data adjustment sequence

6.11 EEPROM Interface

6.11.1 Overview of EEPROM interface

The S1D19600 can communicate external 1k/2k/4kbit EEPROM by EEPROM data bus. Volume of register setting is under 1Kbit, therefore 2kbit or 4kbit EEPROM is used, 2set or 4set of settings can be stored.

Writing methods to EEPROM are following 3;

1) thru S1D19600 writing
2) MPU direct writing
3) Automatic writing

Reading methods from EEPROM are following 2;

1) Boot reading: Automatic register setting after resetting
2) Refresh reading: Automatic periodical setting read. Read start address can be set.

When refresh reading, read start address can be programmable.

This function is controlled by NVSEL pin.

NVSEL pin = LOW	NVSEL pin = HIGH
Disable EEPROM interface	Enable EEPROM interface

6.11.2 Connections to EEPROM

There are 3 ways to connect to EEPROM for each above writeing methods as followings;

1) Thru S1D19600 writing

When writing, D4 to D0 pins of the S1D19600 are connected to control pins of EEPROM (XE2WP, E2SO, E2SI, E2SCL, XE2CS) internally. Therefore EEPROM accessing can possible by D4 to D0 pins thru S1D19600. The connnection is as following:

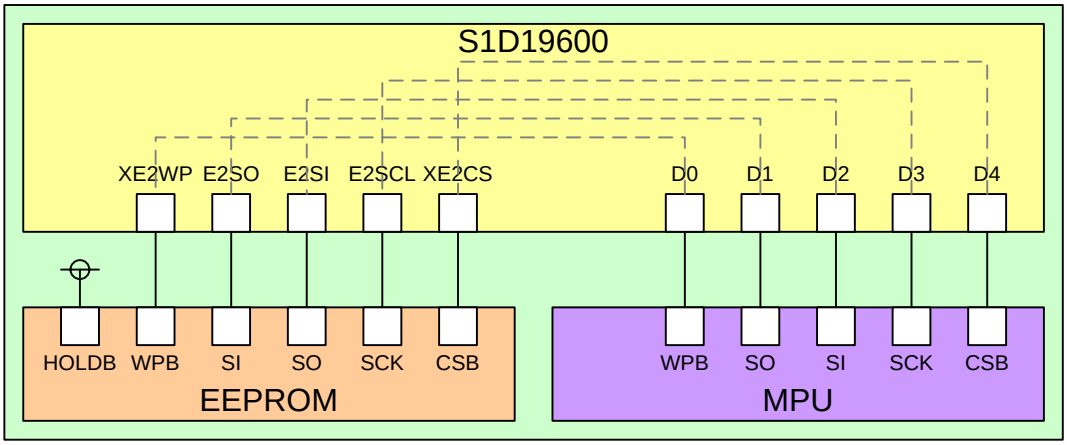


Fig 29 thru S1D19600 writing

2) MPU direct writing

When writing, EEPROM control pins of the S1D19600 is changed to Hi-Z state. Therefore MPU can access EEPROM directly.

The connnection is as following.

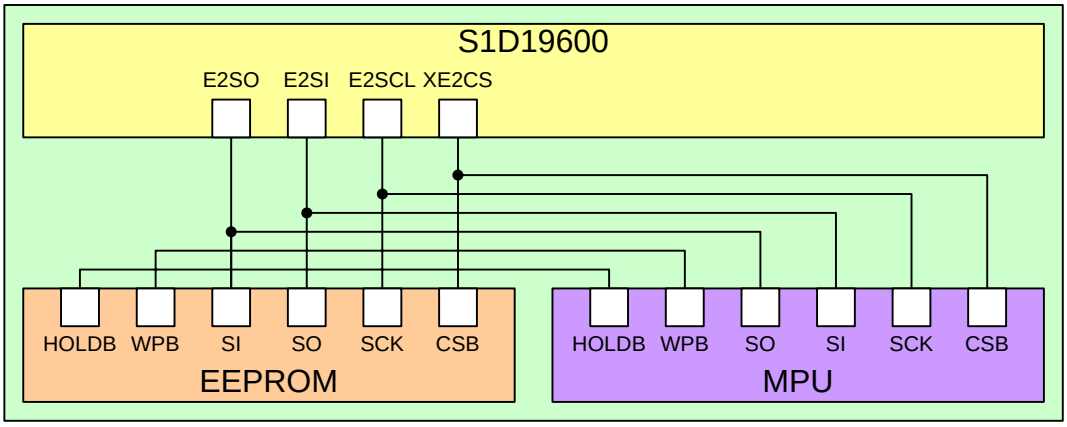


Fig 30 MPU direct writing

3) Automatic writing

When writing, register values in the S1D19600 are written automatically. Therefore EEPROM is connected to only EEPROM control pins of the S1D19600.

The connnection is as following.

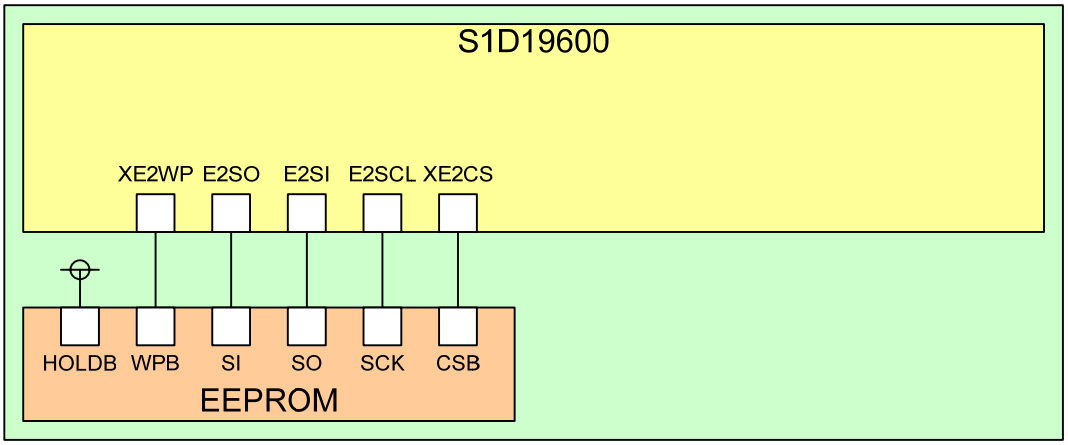


Fig 31 Automatic write writing

6.11.3 EEPROM writng timing chart

Timing charts for each writing method are following;

- Thru S1D19600 writing

When Thru S1D19600 writing is selected by EPRMIN command, D4 to D0 pins are connected to EEPROM control pins (XE2WP, E2SO, E2SI, E2SCL, XE2CS) thru S1D19600 inside. During EEPROM accessing, $\overline{CS}$ must be kept to LOW. And when $\overline{CS}$ is changed to HIGH, the writing sequence is finished. (inside connection is released). The timing chart is shown as fig. 32.

When Thru S1D19600 writing is selected, Only D2 pin is changed from input to output. It is required 150us maximum to change D2 direction.

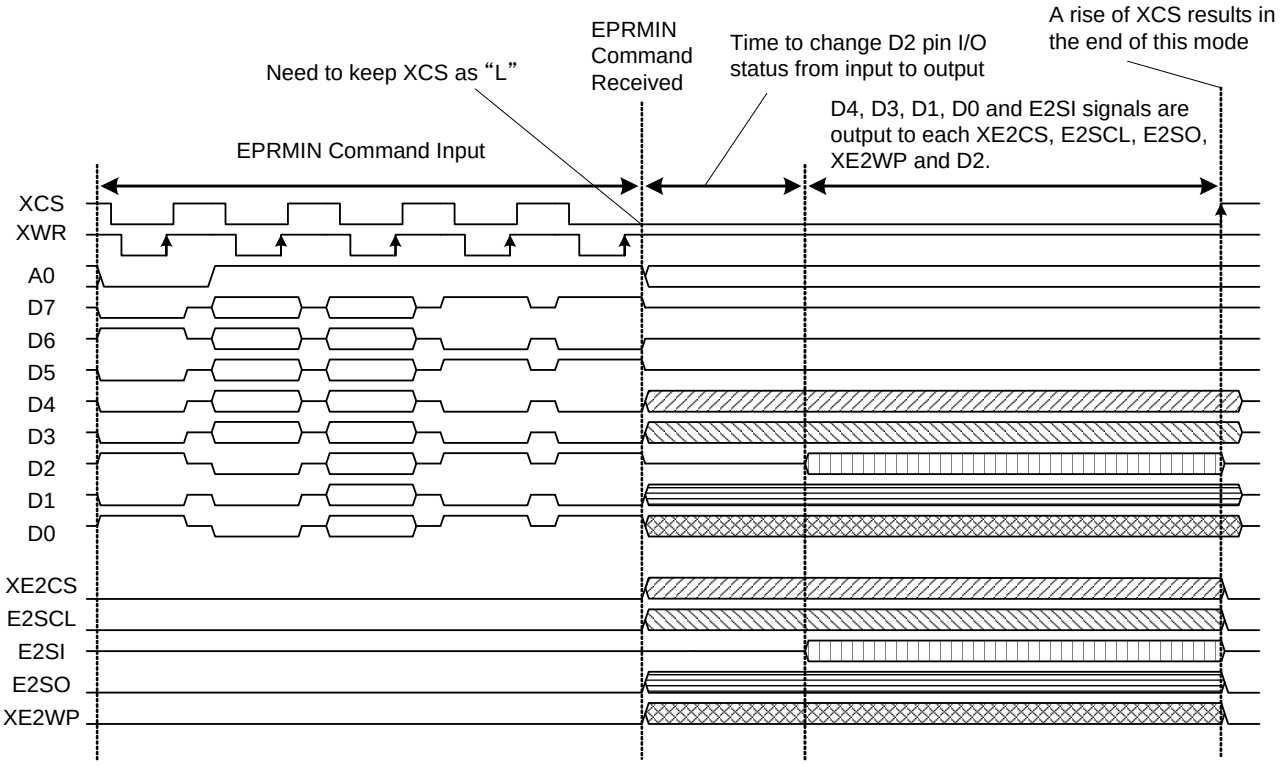


Fig 32 Timing chart using Thru S1D19600 writing

EEPROM output pins are normally Hi-Z. Therefore E2SI pin of the S1D19600 is floating.

In this time, the S1D19600 analyze D4, D3 and D1 pin input and send “Read Status Register “ or “Read “ command to EEPROM, and output input signal of E2SI to D2 pin in order to reduce the leak current. During other term (output pins of EEPROM is Hi-Z), D2 pin output VSS. Detail isas fig. 33.

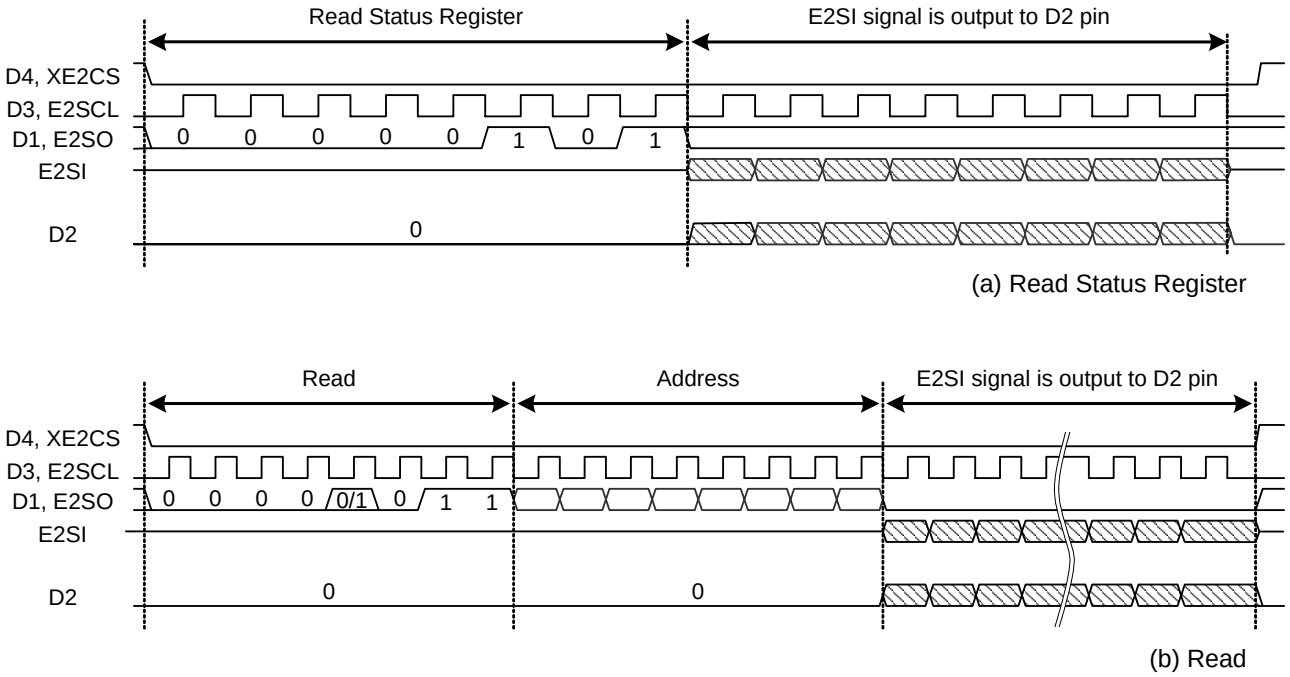


fig. 33 E2SI input term and D2 pin output when Thru S1D19600 writing is used.

- MPU direct writing

When the MPU direct writing is selected by EPRMIN command, the EEPROM control output pins of the S1D19600 (XE2CS, E2SCL, E2SO, XE2WP) are Hi-Z. During this term, MPU can access to EEPROM directly. The timing chart is as fig. 34.
During this term, E2SI pin is not input and not output therefore no leak current is not generated even if Hi-Z state.

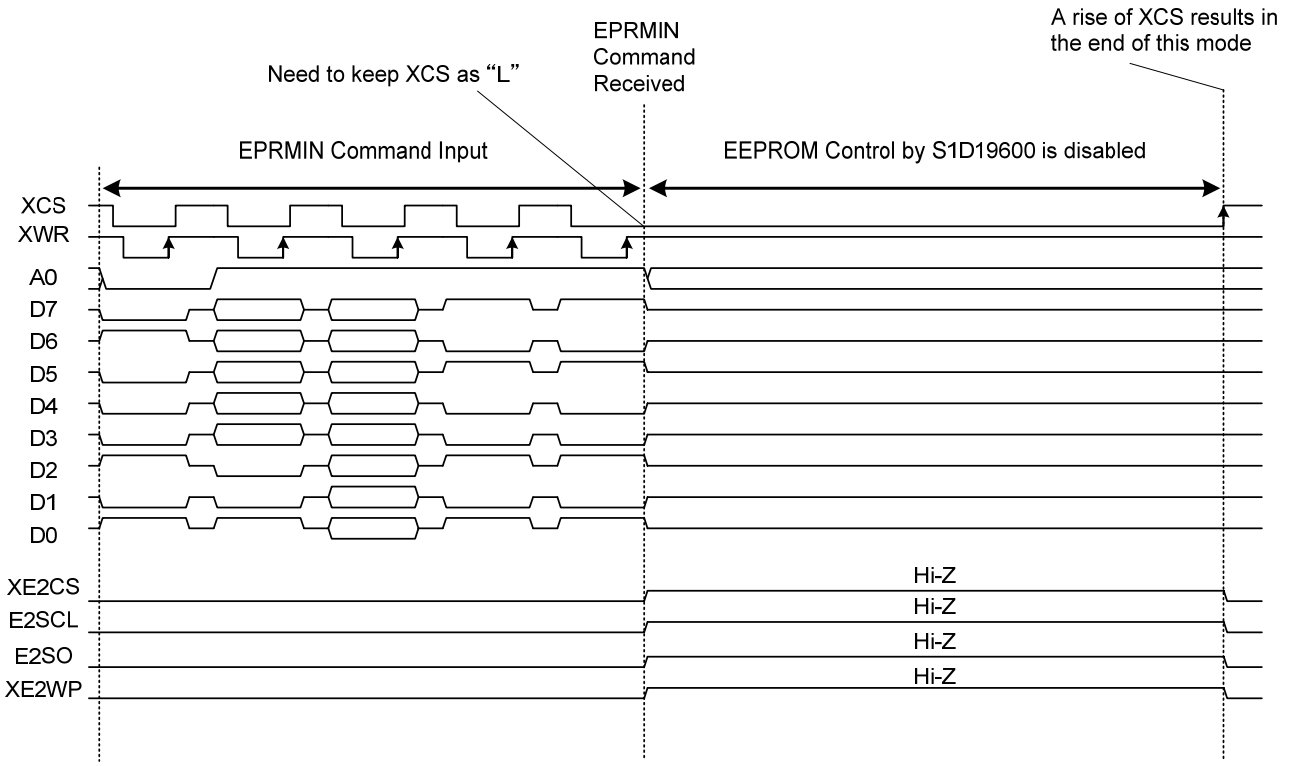


Fig.34 Timing chart of MPU direct writing

- Automatic Writing

Data of registers in the S1D19600 is written to EEPROM. No need to write from MPU to EEPROM. The writing sequens is shown as fig. 35.

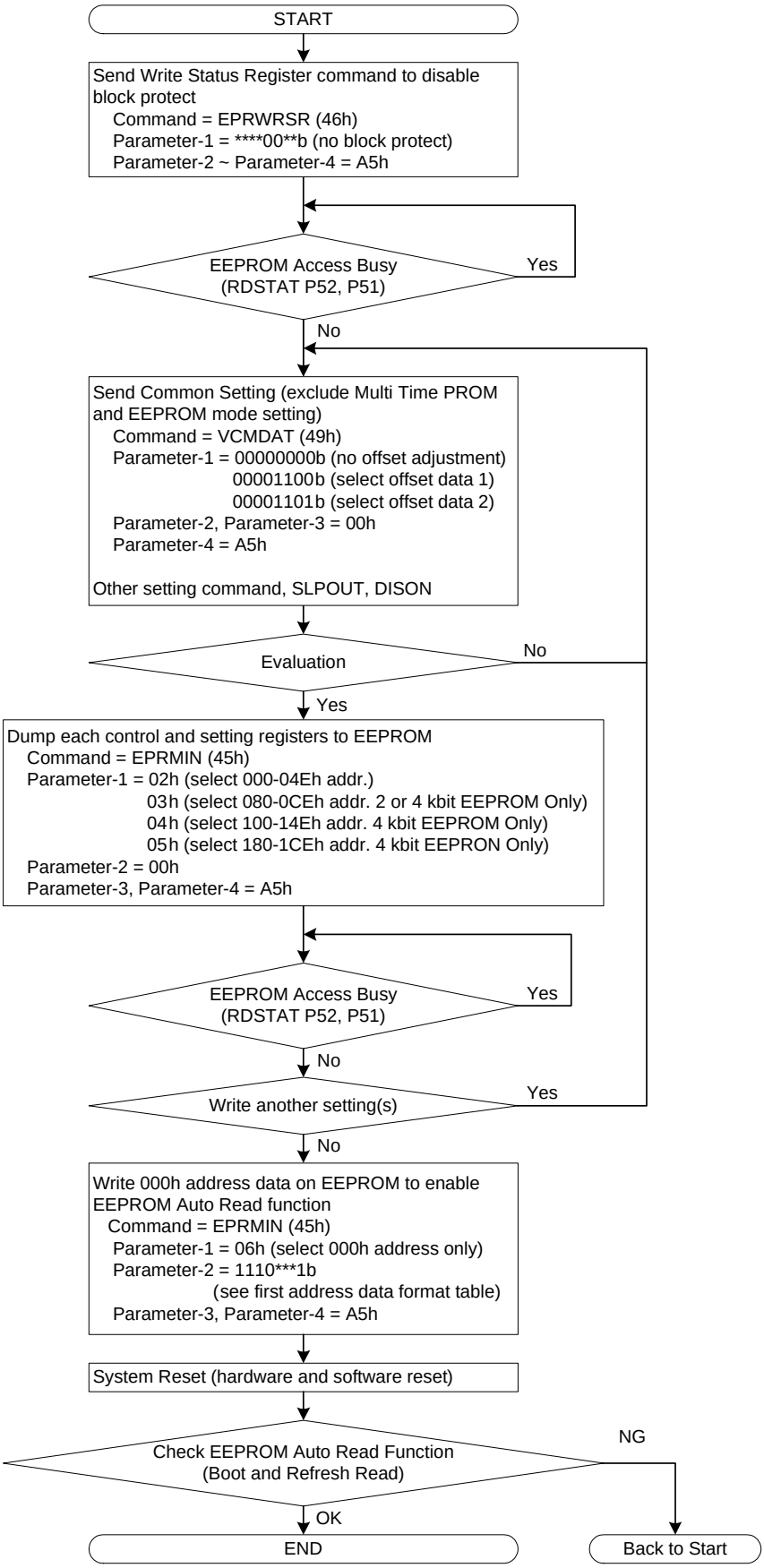


Fig. 35 Automatic writing sequence

6.11.4 EEPROM automatic read

The S1D19600 has 2 automatic register value reading functions as below.
1) Boot reading
Register values are read automatically after reset release.
(Refer to Fig 36)

2) Refresh reading
Register values are read periodically
(Refer to Fig 37)

When the EEPROM interface is enable, any command what are set from EEPROM can not change register values. Register values are shown in table 36 EEPROM address map.

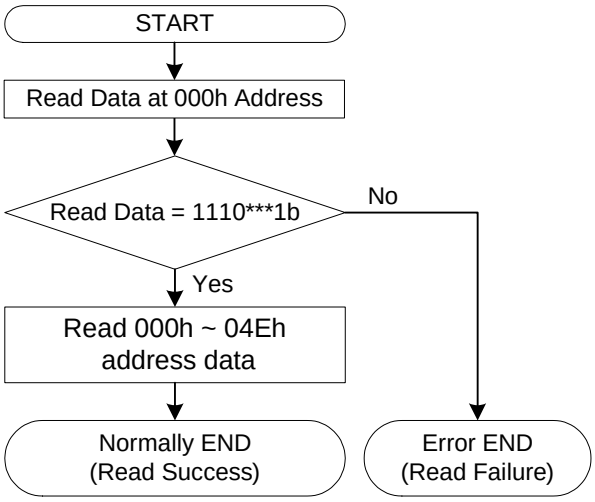


Fig 36 Sequence of EEPROM boot reading

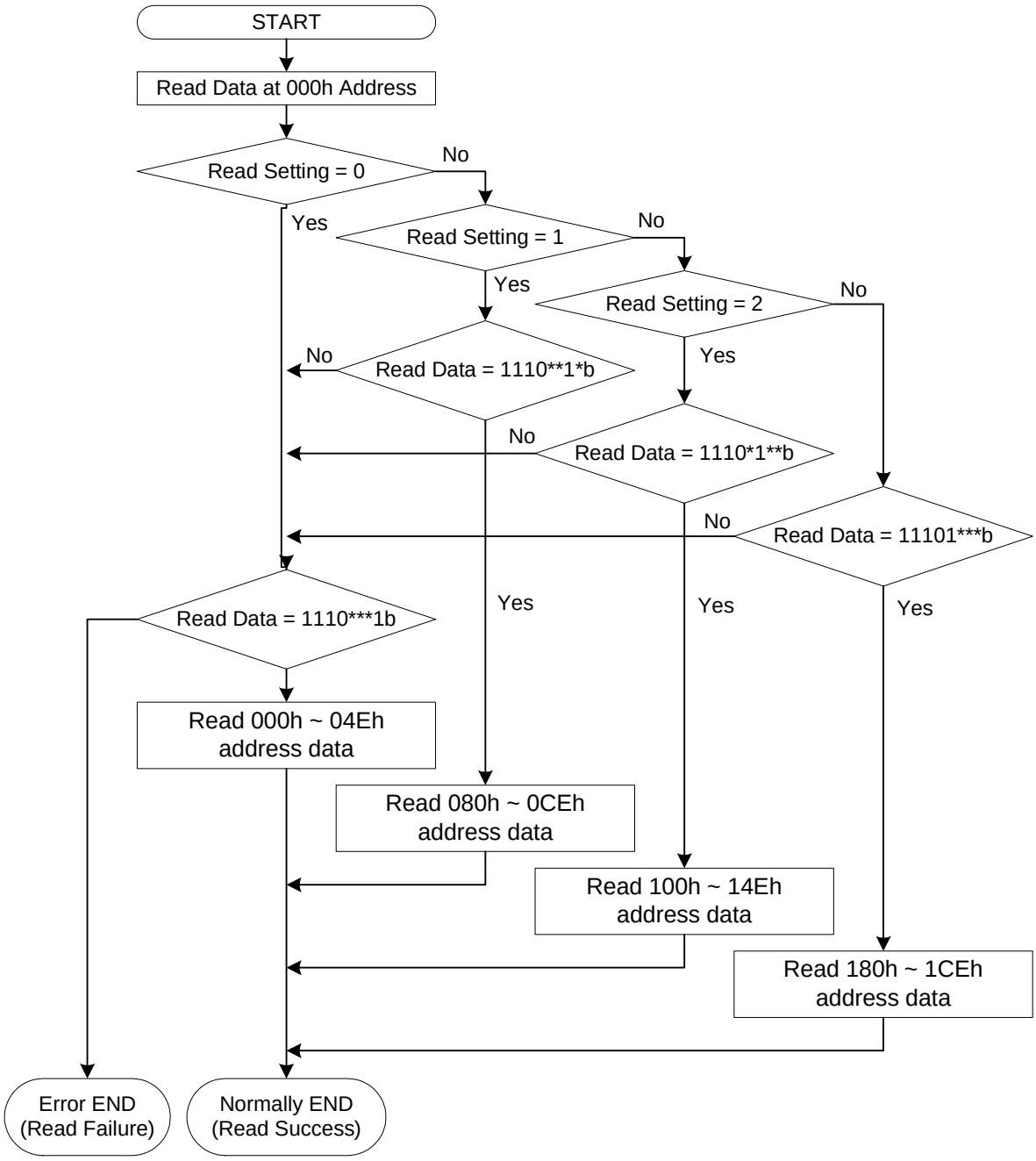


Fig 37 Sequence of EEPROM Refresh Reading

6.11.5 EEPROM data format

The S1D19600 uses following address area as table 35. And each area of address map is shown in table 36. Each register values are shown in Section 7.

Table 35 EEPROM used address area

EEPROM Address		1 kbit	2 kbit	4 kbit
000h	Boot-load Address Setting			
001h 04Eh	Boot-load, Refresh-load Setting 1			
04Fh 07Fh	Reserved			
080h	No-use (*1)			
081h 0CEh	Refresh-load Setting 2			
0CFh 0FFh	Reserved			
100h	No-use (*1)			
101h 14Eh	Refresh-load Setting 3			
14Fh 17Fh	Reserved			
180h	No-use (*1)			
181h 1CEh	Refresh-load Setting 4			
1CFh 1FFh	Reserved			

*1: When automatic writing mode is used, 00h is written.

Table 36 EEPROM address map

EEPROM address (HEX)				Command parameter	Contents
000	080	100	180	EEPROM read address setting (EEPROM address 000h only)	
001	081	101	181	VCMDAT P2, RDVCMDAT R3	VCOMH offset data 1
002	082	102	182	VCMDAT P3, RDVCMDAT R4	VCOMH offset data 2
003	083	103	183	UIDSET P1, RDUID R5	UID 1-1 Data
004	084	104	184	UIDSET P2, RDUID R6	UID 1-2 Data
005	085	105	185	UIDSET P3, RDUID R7	UID 2-1 Data
006	086	106	186	UIDSET P4, RDUID R8	UID 2-2 Data
007	087	107	187	DISAR P1	# of display lines (MSB)
008	088	108	188	DISAR P2	# of display lines (LSB)
009	089	109	189	DISAR P3	# of display columns (MSB)
00A	08A	10A	18A	DISAR P4	# of display columns (LSB)
00B	08B	10B	18B	DISSET1 P1	# of 1H clock
00C	08C	10C	18C	DISSET1 P2	# of back porch line
00D	08D	10D	18D	DISSET1 P3	LCD type, OSCO output, # of front porch line (MSB)
00E	08E	10E	18E	DISSET1 P4	# of front porch line (LSB)
00F	08F	10F	18F	DISSET2 P1	Source output ON timing
010	090	110	190	DISSET2 P2	Source output OFF timing
011	091	111	191	DISSET2 P3	Gate output ON timing
012	092	112	192	DISSET2 P4	Gate output OFF timing
013	093	113	193	GATESET P1	Gate driver scan mode
014	094	114	194	ACSET P1	AC mode
015	095	115	195	GAMSET4P1 P1	V0 voltage set (4bpp mode, Positive)
016	096	116	196	GAMSET4P1 P2	V1 voltage set (4bpp mode, Positive)
017	097	117	197	GAMSET4P1 P3	V2 voltage set (4bpp mode, Positive)
018	098	118	198	GAMSET4P1 P4	V3 voltage set (4bpp mode, Positive)
019	099	119	199	GAMSET4P2 P1	V4 voltage set (4bpp mode, Positive)
01A	09A	11A	19A	GAMSET4P2 P2	V5 voltage set (4bpp mode, Positive)
01B	09B	11B	19B	GAMSET4P2 P3	V6 voltage set (4bpp mode, Positive)
01C	09C	11C	19C	GAMSET4P2 P4	V7 voltage set (4bpp mode, Positive)
01D	09D	11D	19D	GAMSET4P3 P1	V8 voltage set (4bpp mode, Positive)
01E	09E	11E	19E	GAMSET4P3 P2	V9 voltage set (4bpp mode, Positive)
01F	09F	11F	19F	GAMSET4P3 P3	V10 voltage set (4bpp mode, Positive)
020	0A0	120	1A0	GAMSET4P3 P4	V11 voltage set (4bpp mode, Positive)
021	0A1	121	1A1	GAMSET4P4 P1	V12 voltage set (4bpp mode, Positive)
022	0A2	122	1A2	GAMSET4P4 P2	V13 voltage set (4bpp mode, Positive)
023	0A3	123	1A3	GAMSET4P4 P3	V14 voltage set (4bpp mode, Positive)
024	0A4	124	1A4	GAMSET4P4 P4	V15 voltage set (4bpp mode, Positive)
025	0A5	125	1A5	GAMSET4N1 P1	V0 voltage set (4bpp mode, Negative)
026	0A6	126	1A6	GAMSET4N1 P2	V1 voltage set (4bpp mode, Negative)
027	0A7	127	1A7	GAMSET4N1 P3	V2 voltage set (4bpp mode, Negative)
028	0A8	128	1A8	GAMSET4N1 P4	V3 voltage set (4bpp mode, Negative)
029	0A9	129	1A9	GAMSET4N2 P1	V4 voltage set (4bpp mode, Negative)
02A	0AA	12A	1AA	GAMSET4N2 P2	V5 voltage set (4bpp mode, Negative)
02B	0AB	12B	1AB	GAMSET4N2 P3	V6 voltage set (4bpp mode, Negative)
02C	0AC	12C	1AC	GAMSET4N2 P4	V7 voltage set (4bpp mode, Negative)
02D	0AD	12D	1AD	GAMSET4N3 P1	V8 voltage set (4bpp mode, Negative)
02E	0AE	12E	1AE	GAMSET4N3 P2	V9 voltage set (4bpp mode, Negative)
02F	0AF	12F	1AF	GAMSET4N3 P3	V10 voltage set (4bpp mode, Negative)

Continue…

EEPROM address (HEX)				Command parameter	Contents
030	0B0	130	1B0	GAMSET4N3 P4	V11 voltage set (4bpp mode, Negative)
031	0B1	131	1B1	GAMSET4N4 P1	V12 voltage set (4bpp mode, Negative)
032	0B2	132	1B2	GAMSET4N4 P2	V13 voltage set (4bpp mode, Negative)
033	0B3	133	1B3	GAMSET4N4 P3	V14 voltage set (4bpp mode, Negative)
034	0B4	134	1B4	GAMSET4N4 P4	V15 voltage set (4bpp mode, Negative)
035	0B5	135	1B5	GAMSET2P P1	V0 voltage set (2bpp mode, Positive)
036	0B6	136	1B6	GAMSET2P P2	V1 voltage set (2bpp mode, Positive)
037	0B7	137	1B7	GAMSET2P P3	V2 voltage set (2bpp mode, Positive)
038	0B8	138	1B8	GAMSET2P P4	V3 voltage set (2bpp mode, Positive)
039	0B9	139	1B9	GAMSET2N P1	V0 voltage set (2bpp mode, Negative)
03A	0BA	13A	1BA	GAMSET2N P2	V1 voltage set (2bpp mode, Negative)
03B	0BB	13B	1BB	GAMSET2N P3	V2 voltage set (2bpp mode, Negative)
03C	0BC	13C	1BC	GAMSET2N P4	V3 voltage set (2bpp mode, Negative)
03D	0BD	13D	1BD	GAMSET1 P1	V0 voltage set (1bpp mode, Positive)
03E	0BE	13E	1BE	GAMSET1 P2	V1 voltage set (1bpp mode, Positive)
03F	0BF	13F	1BF	GAMSET1 P3	V0 voltage set (1bpp mode, Negative)
040	0C0	140	1C0	GAMSET1 P4	V1 voltage set (1bpp mode, Negative)
041	0C1	141	1C1	EVSET1 P1	VDDHS output voltage setting
042	0C2	142	1C2	EVSET1 P2	VCOMH output voltage setting
043	0C3	143	1C3	EVSET1 P3	VCA output voltage setting
044	0C4	144	1C4	EVSET1 P4	VDDRH output voltage setting
045	0C5	145	1C5	EVSET2 P1	VOFREG output voltage setting
046	0C6	146	1C6	EVSET2 P2	VONREG output voltage setting
047	0C7	147	1C7	PWRCTL P1	Boost control, VCOML control
048	0C8	148	1C8	PWRCTL P2	Source amp setting, Display wait
049	0C9	149	1C9	PWRCTL P3	# of boost clock (Normal display)
04A	0CA	14A	1CA	PWRCTL P4	# of boost clock (Partial display)
04B	0CB	14B	1CB	PTLSET3 P1	Refresh rate of non display area (Partial display)
04C	0CC	14C	1CC	PTLSET3 P2	Boost clock return time (Partial display)
04D	0CD	14D	1CD	PTLSET3 P3	Driving way of non display area (Partial display)
04E	0CE	14E	1CE	REFCYC P1	EEPROM Refresh cycle

A data that EEPROM address is valid/invalid is stored at EEPROM address 000h.

To enable EEPROM automatic read function, the data at address 000h must be set 1110***1b (*: don't care) If any other value is set, the automatic read stops.

Table 37 Address data specification of EEPROM 000h

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
000h	When bit 7 to 4 = 1110b, EEPROM is valid. When the bit 7 to 4 is the other value, EEPROM is invalid and automatic read stops.。				180 to 1CEh 1=valid 0=invalid	101 to 14Eh 1=valid 0=invalid	081 to 0CEh 1=valid 0=invalid	001 to 04Eh 1=valid 0=invalid

7. COMMANDS

Data bus is controlled by $\overline{CS}$, A0, $\overline{RD}$ and $\overline{WR}$ in parallel mode. Command interpreting and execution are done by not external signal but internal clock.

Data is recognized as a command when A0 = LOW, and as a command parameter or data when A0 = HIGH.

Every command and command parameter are defined as 8bit, D7 to D0 is correspond the 8bit in parallel mode.

In serial interface, A0 state when 8th bit data is latched is recognized.

All commands are 5 Byte length or 2 Byte length, and non usage parameter must filled by A5h and must be finished. 4 Byte parameter is required for 5Byte command, and a Byte parameter is required for 2Byte command.

In parallel interface, during input parameter, if A0 set to LOW and access $\overline{WR}$, other command can be input. In serial interface, during input parameter if $\overline{CS}$ set to HIGH, other command can be input. It is prohibited to input over number of command parameter.

Commands that be executed synchronized by frame are executed at first front porch or during front porch after all parameters are input.

RAMWR and RAMRD commands are finished by A0=LOW and input next command.

Read operation is done by $\overline{RD}$ pin set to LOW, and write operation is done by $\overline{WR}$ pin set to LOW.

Don't input command which is not on the command list.

It is recommend to rewrite command and frame RAM periodically, due to recover display when some external noise is input .

7. COMMANDS

7.1 command list

Table 38 Command List

No.	Command name	Code (Hex)	Length (Byte)	Execute Timing *1	Function
1	SWRESET	5E	2	Immediate	Software reset
2	DISAR	91	5	Immediate	Display Area setting(number of line / column)
3	DISSET1	92	5	Immediate	Display setting1 (number of 1H period/clock, lines of BP/FP, LCD type)
4	DISSET2	93	5	Immediate	Display setting2 (set source timing/ gate timing)
5	DINVIN	16	2	Frame	Display Inverted mode IN
6	DINVOUT	15	2	Frame	Display Inverted mode OUT
7	MADCTL	21	5	Immediate	Memory address control(set column / page address direction / auto increment direction
8	CASET	23	5	Immediate	Column address setting
9	PASET	22	5	Immediate	Page address setting
10	STFRAME	24	5	Frame	Display start frame address setting
11	BPPSEL	25	5	Frame	Bpp mode setting(4bpp / 2bpp / 1bpp)
12	MDCTL	26	5	Immediate	Memory data control (write data bit mask)
12	GATESET	A2	5	Frame	Gate scan mode setting(Interlace / up and down drive)
13	ACSET	A1	5	Frame	AC drive method setting
14	GAMSET4P1	81	5	Immediate	Gamma curve setting positive(V_0-V_3) in 4bpp mode
15	GAMSET4P2	82	5	Immediate	Gamma curve setting positive(V_4-V_7) in 4bpp mode
16	GAMSET4P3	83	5	Immediate	Gamma curve setting positive(V_8-V_{11}) in 4bpp mode
17	GAMSET4P4	84	5	Immediate	Gamma curve setting positive(V_{12}-V_{15}) in 4bpp mode
18	GAMSET4N1	89	5	Immediate	Gamma curve setting negative(V_0-V_3) in 4bpp mode
19	GAMSET4N2	8A	5	Immediate	Gamma curve setting negative(V_4-V_7) in 4bpp mode
20	GAMSET4N3	8B	5	Immediate	Gamma curve setting negative(V_8-V_{11}) in 4bpp mode
21	GAMSET4N4	8C	5	Immediate	Gamma curve setting negative(V_{12}-V_{15}) in 4bpp mode
23	GAMSET2P	85	5	Immediate	Gamma curve setting positive(V_0-V_3) in 2bpp mode
24	GAMSET2N	8D	5	Immediate	Gamma curve setting negative(V_0-V_3) in 2bpp mode
25	GAMSET1	86	5	Immediate	Gamma curve setting positive/negative(V_0-V_1) in 1bpp mode
26	EVSET1	71	5	Immediate	Electric volume setting1
27	EVSET2	72	5	Immediate	Electric volume setting2
28	PWRCTL	61	5	Immediate	Power circuit control(Booster , source amplifier)
29	SLPIN	14	2	Immediate	Sleep In
30	SLPOUT	13	2	Immediate	Sleep Out
31	DISON	12	2	Frame	Display ON
32	DISOFF	11	2	Frame	Display OFF
33	WRRAM	3A	2	Immediate	Write to display RAM
34	RDRAM	39	2	Immediate	Read from display RAM
35	PTLSET1	29	5	Frame	Partial display setting 1(1st partial area start / end line setting)
36	PTLSET2	2A	5	Frame	Partial display setting 2(2nd partial area start / end line setting)

No.	Command name	Code (Hex)	Length (Byte)	Execute Timing *1	Function
37	PTLSET3	AB	5	Frame	Partial display setting 3(refresh rate of non-display area, booster clock return time)
38	PTLIN	19	2	Frame	Partial display IN
39	PTLOUT	1A	2	Frame	Partial display OUT
40	BLSET	2B	5	Frame	Setting of blinking
41	BLIN	1B	2	Frame	Blinking display IN
42	BLOUT	1C	2	Frame	Blinking display OUT
43	BLKFIL	31	5	Immediate	Block fill, (fill data to block area)
44	VCMDAT	49	5	Immediate	V_{COMH} offset data setting
45	UIDSET	4A	5	Immediate	User ID data setting
46	MTPERS	41	5	Immediate	Multi Time PROM erase setting
47	MTPPRG	42	2	Immediate	Multi Time PROM programming setting
48	MTPOP	43	4	Immediate	Multi Time PROM erase/programming operation
49	EPRMIN	45	4	Immediate	EEPROM control mode IN
50	EPRWRSR	46	4	Immediate	Write EEPROM status register
51	RDVCMDAT	59	10	Immediate	Read VCOM offset data
52	RDUID	55	14	Immediate	Read User ID
53	REFCYC	B1	5	Frame	Refresh cycle setting
54	EPRRDADR	4B	5	Immediate	EEPROM address setting in refresh read
55	RDERR	51	4	Immediate	Read error status
56	RDSTAT	52	8	Immediate	Read status
57	RDREV	53	5	Immediate	Read revision
58	RDCRC	54	4	Immediate	Read CRC
59	NOP	00	1	-	Non operation

*1 Commands that be executed synchronized by frame are executed at first front porch or during front porch after all parameters are input.

7.2 Initial Values of parameters

Table 39 Parameter Initial Value List

No.	Command	Parameter	Code (Bin)								Hex	Decimal	Initial state
			D7	D6	D5	D4	D3	D2	D1	D0			
1	SWRESET	P1	*	*	*	*	*	*	*	*	—	—	
2	DISAR	P1	*	*	*	*	*	*	*	1	01	319	320 lines display
		P2	0	0	1	1	1	1	1	1	3F		
		P3	*	*	*	*	*	*	*	1	01	319	320 columns display
		P4	0	0	1	1	1	1	1	1	3F		
3	DISSET1	P1	0	0	1	1	0	0	1	0	32	50	1H=51 clocks
		P2	0	0	0	0	0	0	1	0	02	2	Number of back porch; 3
		P3	0	0	*	*	0	0	0	0	00	1	LCD: Normally white OSCO output: Vss Number of front porch: 2
		P4	0	0	0	0	0	0	0	1	01		
4	DISSET2	P1	0	0	0	0	1	0	1	0	0A	10	Source output ON: 11th clock
		P2	0	0	1	0	1	0	0	0	28	40	Source output OFF: 41st clock
		P3	0	0	0	0	1	1	0	0	0C	12	Gate output ON; 13th clock
		P4	0	0	1	0	0	1	1	0	26	38	Gate output OFF: 39th clock
5	DINVIN	P1	*	*	*	*	*	*	*	*	-	-	
6	DINVOUT	P1	*	*	*	*	*	*	*	*	-	-	Default value
7	MADCTL	P1	*	*	*	*	*	0	0	0	00	—	Column/Pageaddress: Normal Column increment direction
		P2	*	*	*	*	*	*	*	*	—	—	
		P3	*	*	*	*	*	*	*	*	—	—	
		P4	*	*	*	*	*	*	*	*	—	—	
8	CASET	P1	*	*	*	*	*	*	*	0	00	0	Column start address: 0
		P2	0	0	0	0	0	0	0	0	00		
		P3	*	*	*	*	*	*	*	1	01	319	Column end address: 319
		P4	0	0	1	1	1	1	1	1	3F		
9	PASET	P1	0	0	0	0	0	0	0	0	00	0	Page start address: 0
		P2	1	0	0	1	1	1	1	1	9F	159	Page end address: 159
		P3	*	*	*	*	*	*	0	0	00	0	Frame start address: 0
		P4	*	*	*	*	*	*	*	*	—	—	
10	STFRAME	P1	*	*	*	*	*	*	0	0	00	0	Start frame address: 0
		P2	*	*	*	*	*	*	*	*	—	—	
		P3	*	*	*	*	*	*	*	*	—	—	
		P4	*	*	*	*	*	*	*	*	—	—	
11	BPPSEL	P1	*	*	*	*	*	*	1	0	02	—	Number of grayscale: 4bpp
		P2	*	*	*	*	*	*	*	*	—	—	
		P3	*	*	*	*	*	*	*	*	—	—	
		P4	*	*	*	*	*	*	*	*	—	—	
12	MDCTL	P1	*	*	*	*	*	*	0	0	00	0	No bit operation
		P2	0	0	0	0	0	0	0	0	00	0	Mask data at start page address
		P3	0	0	0	0	0	0	0	0	00	0	Mask data at end page address
		P4	*	*	*	*	*	*	*	*	—	—	

No.	Command	Parameter	Code (Bin)								Hex	Decimal	Initial state
			D7	D6	D5	D4	D3	D2	D1	D0			
13	GATESET	P1	0	*	*	0	*	*	0	0	00	—	Interlace driving, Normal scan direction
		P2	*	*	*	*	*	*	*	*	—	—	
		P3	*	*	*	*	*	*	*	*	—	—	
		P4	*	*	*	*	*	*	*	*	—	—	
14	ACSET	P1	*	*	0	0	*	*	0	0	00	—	1 line inversion driving
		P2	*	*	*	*	*	*	*	*	—	—	
		P3	*	*	*	*	*	*	*	*	—	—	
		P4	*	*	*	*	*	*	*	*	—	—	
15	GAMSET4P1	P1	*	*	0	0	0	0	0	0	00	—	V_0 (Positive polarity)
		P2	*	*	0	0	0	1	0	0	04	—	V_1 (Positive polarity)
		P3	*	*	0	0	1	0	0	0	08	—	V_2 (Positive polarity)
		P4	*	*	0	0	1	1	0	0	0C	—	V_3 (Positive polarity)
16	GAMSET4P2	P1	*	*	0	1	0	0	0	0	10	—	V_4 (Positive polarity)
		P2	*	*	0	1	0	1	0	0	14	—	V_5 (Positive polarity)
		P3	*	*	0	1	1	0	0	0	18	—	V_6 (Positive polarity)
		P4	*	*	0	1	1	1	0	0	1C	—	V_7 (Positive polarity)
17	GAMSET4P3	P1	*	*	1	0	0	0	1	1	23	—	V_8 (Positive polarity)
		P2	*	*	1	0	0	1	1	1	27	—	V_9 (Positive polarity)
		P3	*	*	1	0	1	0	1	1	2B	—	V_{10} (Positive polarity)
		P4	*	*	1	0	1	1	1	1	2F	—	V_{11} (Positive polarity)
18	GAMSET4P4	P1	*	*	1	1	0	0	1	1	33	—	V_{12} (Positive polarity)
		P2	*	*	1	1	0	1	1	1	37	—	V_{13} (Positive polarity)
		P3	*	*	1	1	1	0	1	1	3B	—	V_{14} (Positive polarity)
		P4	*	*	1	1	1	1	1	1	3F	—	V_{15} (Positive polarity)
19	GAMSET4N1	P1	*	*	0	0	0	0	0	0	00	—	V_0 (Negative polarity)
		P2	*	*	0	0	0	1	0	0	04	—	V_1 (Negative polarity)
		P3	*	*	0	0	1	0	0	0	08	—	V_2 (Negative polarity)
		P4	*	*	0	0	1	1	0	0	0C	—	V_3 (Negative polarity)
20	GAMSET4N2	P1	*	*	0	1	0	0	0	0	10	—	V_4 (Negative polarity)
		P2	*	*	0	1	0	1	0	0	14	—	V_5 (Negative polarity)
		P3	*	*	0	1	1	0	0	0	18	—	V_6 (Negative polarity)
		P4	*	*	0	1	1	1	0	0	1C	—	V_7 (Negative polarity)
21	GAMSET4N3	P1	*	*	1	0	0	0	1	1	23	—	V_8 (Negative polarity)
		P2	*	*	1	0	0	1	1	1	27	—	V_9 (Negative polarity)
		P3	*	*	1	0	1	0	1	1	2B	—	V_{10} (Negative polarity)
		P4	*	*	1	0	1	1	1	1	2F	—	V_{11} (Negative polarity)
22	GAMSET4N4	P1	*	*	1	1	0	0	1	1	33	—	V_{12} (Negative polarity)
		P2	*	*	1	1	0	1	1	1	37	—	V_{13} (Negative polarity)
		P3	*	*	1	1	1	0	1	1	3B	—	V_{14} (Negative polarity)
		P4	*	*	1	1	1	1	1	1	3F	—	V_{15} (Negative polarity)
23	GAMSET2P	P1	*	*	0	0	0	0	0	0	00	—	V_0 (Positive polarity)
		P2	*	*	0	1	0	1	0	1	15	—	V_1 (Positive polarity)
		P3	*	*	1	0	1	0	1	0	2A	—	V_2 (Positive polarity)
		P4	*	*	1	1	1	1	1	1	3F	—	V_3 (Positive polarity)

No.	Command	Parameter	Code (Bin)								Hex	Decimal	Initial state
			D7	D6	D5	D4	D3	D2	D1	D0			
24	GAMSET2N	P1	*	*	0	0	0	0	0	0	00	—	V_0 (Negative polarity)
		P2	*	*	0	1	0	1	0	1	15	—	V_1 (Negative polarity)
		P3	*	*	1	0	1	0	1	0	2A	—	V_2 (Negative polarity)
		P4	*	*	1	1	1	1	1	1	3F	—	V_3 (Negative polarity)
25	GAMSET1	P1	*	*	0	0	0	0	0	0	00	—	V_0 (Positive polarity)
		P2	*	*	1	1	1	1	1	1	3F	—	V_1 (Positive polarity)
		P3	*	*	0	0	0	0	0	0	00	—	V_0 (Negative polarity)
		P4	*	*	1	1	1	1	1	1	3F	—	V_1 (Negative polarity)
26	EVSET1	P1	*	*	*	*	1	1	1	1	0F	—	V_{DDHS}
		P2	0	1	0	0	1	1	0	1	4D	—	V_{COMH}
		P3	*	*	*	1	0	1	0	0	14	—	VCA
		P4	*	*	*	1	0	1	0	0	14	—	V_{DDRH}
27	EVSET2	P1	*	*	*	1	0	1	0	1	15	—	V_{OFREG}
		P2	*	*	0	0	0	1	1	0	06	—	V_{ONREG}
		P3	*	*	*	*	*	*	*	*	*	—	
		P4	*	*	*	*	*	*	*	*	*	—	
28	PWRCTL	P1	0	1	*	0	0	0	0	0	40	—	Boosters: OFF VCOML reg: OFF 3rd booster: x(-2)
		P2	0	0	0	0	*	0	0	1	01	—	Setting 1, wait 5 frames
		P3	*	0	0	0	*	0	0	0	00	—	In normal display: 1st to 4th Frequency of1H x1
		P4	*	0	0	0	*	0	0	0	00	—	In partial display: 1st to 4th Frequency of1H x1
29	SLPIN	P1	*	*	*	*	*	*	*	*	—	—	Default
30	SLPOUT	P1	*	*	*	*	*	*	*	*	—	—	
31	DISON	P1	*	*	*	*	*	*	*	*	—	—	
32	DISOFF	P1	*	*	*	*	*	*	*	*	—	—	Default
33	WRRAM	P1	*	*	*	*	*	*	*	*	—	—	
34	RDRAM	P1	*	*	*	*	*	*	*	*	—	—	
35	PTLSET1	P1	*	*	*	*	*	*	*	0	00	0	Area 1 start line (MSB)
		P2	0	0	0	0	0	0	0	0	00	0	Area 1 start line (LSB)
		P3	*	*	*	*	*	*	*	0	00	0	Area 1 end line (MSB)
		P4	0	0	0	0	0	0	0	0	00	0	Area 1 end line (LSB)
36	PTLSET2	P1	*	*	*	*	*	*	*	0	00	0	Area 2 start line (MSB)
		P2	0	0	0	0	0	0	0	0	00	0	Area 2 start line (LSB)
		P3	*	*	*	*	*	*	*	0	00	0	Area 2 end line (MSB)
		P4	0	0	0	0	0	0	0	0	00	0	Area 2 end line (LSB)
37	PTLSET3	P1	*	0	0	0	0	0	0	0	00	0	Non display refresh rate 1
		P2	*	*	*	*	*	0	0	0	00	0	Booster clock frequency return time
		P3	*	*	*	*	*	*	0	0	00	0	Driving method in non display area
		P4	*	*	*	*	*	*	*	*	*	—	
38	PTLIN	P1	*	*	*	*	*	*	*	*	—	—	
39	PTLOUT	P1	*	*	*	*	*	*	*	*	—	—	Default

No.	Command	Parameter	Code (Bin)								Hex	Decimal	Initial state
			D7	D6	D5	D4	D3	D2	D1	D0			
40	BLSET	P1	0	0	0	1	1	1	0	1	1D	29	
		P2	*	*	*	*	0	0	0	1	01	—	1st frame: frame address 0 2nd frame: frame address 1
		P3	*	*	*	*	*	*	*	*	—	—	
		P4	*	*	*	*	*	*	*	*	—	—	
41	BLIN	P1	*	*	*	*	*	*	*	*			
42	BLOUT	P1	*	*	*	*	*	*	*	*	—	—	Default
43	BLKFIL	P1	*	*	*	*	0	0	0	0	00	0	Data: 0
		P2	*	*	*	*	*	*	*	*	—	—	
		P3	*	*	*	*	*	*	*	*	—	—	
		P4	*	*	*	*	*	*	*	*	—	—	
44	VCMDAT	P1	*	*	*	*	0	0	0	0	00	—	No offset
		P2	0	0	0	0	0	0	0	0	00	0	VCOMH adjust value 1: +/-0
		P3	0	0	0	0	0	0	0	0	00	0	VCOMH adjust value 2: +/-0
		P4	*	*	*	*	*	*	*	*	—	—	
45	UIDSET	P1	0	0	0	0	0	0	0	0	00	0	User ID1-1 0
		P2	0	0	0	0	0	0	0	0	00	0	User ID1-2 0
		P3	0	0	0	0	0	0	0	0	00	0	User ID2-1 0
		P4	0	0	0	0	0	0	0	0	00	0	User ID2-2 0
46	MTPERS	P1	*	*	*	*	*	*	0	0	00	—	Multi-time-PROM: erase VCOM offset 1,2: UserID 1-1, 1,2
		P2	*	*	*	*	*	*	*	*	—	—	
		P3	*	*	*	*	*	*	*	*	—	—	
		P4	*	*	*	*	*	*	*	*	—	—	
47	MTPPRG	P1	*	*	*	0	0	0	0	0	00	0	No choice
		P2	*	*	*	*	*	*	*	*	—	—	
		P3	*	*	*	*	*	*	*	*	—	—	
		P4	*	*	*	*	*	*	*	*	—	—	
48	MTPOP	P1	*	*	*	*	*	*	*	*	—	—	
		P2	*	*	*	*	*	*	*	*	—	—	
		P3	*	*	*	*	*	*	*	*	—	—	
		P4	*	*	*	*	*	*	*	*	—	—	
49	EPRMIN	P1	*	*	*	*	*	0	0	0	00	0	Thru S1D19600 mode
		P2	0	0	0	0	0	0	0	0	00	0	Start address write data
		P3	*	*	*	*	*	*	*	*	—	—	
		P4	*	*	*	*	*	*	*	*	—	—	
50	EPRWRSR	P1	0	0	0	0	0	0	0	0	00	0	Status register write data
		P2	*	*	*	*	*	*	*	*	—	—	
		P3	*	*	*	*	*	*	*	*	—	—	
		P4	*	*	*	*	*	*	*	*	—	—	

No.	Command	Parameter	Code (Bin)								Hex	Decimal	Initial state
51	RDVCMDAT	P1	*	*	*	*	*	*	*	*	—	—	
52	RDUID	P1	*	*	*	*	*	*	*	*	—	—	
53	REFCYC	P1	*	*	*	*	*	*	0	0	00	—	Refresh each 16 frames
		P2	*	*	*	*	*	*	*	*	—	—	
		P3	*	*	*	*	*	*	*	*	—	—	
		P4	*	*	*	*	*	*	*	*	—	—	
54	EPRRDADR	P1	*	*	*	*	*	*	0	0	00	—	EEPROM read area: 000 to 04Eh
		P2	*	*	*	*	*	*	*	*	—	—	
		P3	*	*	*	*	*	*	*	*	—	—	
		P4	*	*	*	*	*	*	*	*	—	—	
55	RDERR	P1	*	*	*	*	*	*	*	*	—	—	
56	RDSTAT	P1	*	*	*	*	*	*	*	*	—	—	
57	RDREV	P1	*	*	*	*	*	*	*	*	—	—	
58	RDCRC	P1	*	*	*	*	*	*	*	*	—	—	
59	NOP	P1	*	*	*	*	*	*	*	*	—	—	

7.3 Command description

7.3.1 SWRESET (Software Reset: 5E h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	0	1	1	1	1	0	5E	Command SWRESET
1	0	1	0	0	1	0	1	A5	Parameter 1 (P1) Dummy

This command make a reset as same as hardware reset. However, It is required Hardware reset at power-on reset. It is always required to input this command after hardware reset.

7.3.2 DISAR (Display Area: 91h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	0	1	0	0	0	1	91	Command DISAR
0	0	0	0	0	0	0	P10	—	Parameter 1(P1) number of display lines (MSB)
P27	P26	P25	P24	P23	P22	P21	P20	—	Parameter 2(P2) number of display lines (LSB)
0	0	0	0	0	0	0	P30	—	Parameter 3(P3) number of display columns (MSB)
P47	P46	P45	P44	P43	P42	P41	P40	—	Parameter 3(P3) number of display columns (LSB)

Set display area (number of display lines, number of display columns)

Parameter 1:
Parameter 2: set “number of display dots of Y direction” - 1
When number of display lines is decreased, porch term should be adjusted by DISET1 command to satisfy “1H =< 150us)
Number of display lines must be 10 to 320 (P1, P2 = 9 to 319). Setting of gate line scan mode should be refer to section 6.4.
When 4bpp mode is selected and the number of display lines is 160 or less, 2 frames of display data RAM are available. According to display data RAM, refer to 6.2.1.
Parameter 3:
Parameter 4: set “number of display dots of X direction” – 1
Number of display columns must be 2 to 320 (P3, P4 = 1 to 319). When it set under 320, disable source output as following. RAM column address is automatically changed same time.

P1	P2	Number of display line	Disabled source output
1	0011_1111	320	Non
1	0011_1110	319	S320
1	0011_1101	318	S1, S320
1	0011_1100	317	S1, S319, S320
1	0011_1011	316	S1, S2, S319, S320
:	:	:	:
0	0000_0100	5	S1-S157, S163-S320
0	0000_0011	4	S1-S158, S163-S320
0	0000_0010	3	S1-S158, S162-S320
0	0000_0001	2	S1-S159, S162-S320
Prohibit to set other number			

7.3.3 DISSET1 (Display Set 1: 92h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	0	1	0	0	1	0	92	Command DISSET1
P17	P16	P15	P14	P13	P12	P11	P10	—	Parameter 1 (P1) number of clocks in 1H
P27	P26	P25	P24	P23	P22	P21	P20	—	Parameter 2 (P2) number of back porch
P37	P36	0	0	P33	P32	P31	P30	—	Parameter 3 (P3) LCD type setting, OSCO output setting, number of front porch (MSB)
P47	P46	P45	P44	P43	P42	P41	P40	—	Parameter 4 (P4) number of front porch (LSB)

Set display conditions.

Parameter 1: set “number of clocks in 1H” - 1.
Take care to relationship between DISSET2/3 command and this command when this parameter is set. The number of clocks in 1H must be longer than timings set by DISSET2/3 command.
When this value is decreased during display, DISSET1 command must be set first. This value must be set 150 or less. When number of display lines is small and 1H period is large, number of front porch must be increased in order to the number of clocks in 1H is set 150 or less.

Ex) Frame frequency fFR = 60 Hz, Number of display lines = 320 lines, back porch = 3lines, front porch = 2lines, Clock cycle = 1us,
1 / 60 / (320 + 2 + 3) ≒ 51 us (1H)
Setting value = 51 – 1 = 50

Parameter 2: set “number of back porch” – 1.
P27 to 20: set number of back porch from 1 to 256.
To change number of lines is recommended to do before sleep out. When it is changed during display, VCOM polarity may be not changed in continuous 2 frames, and the display may jumble for a moment.
(VCOM polarity continuity is occurred when it is changed from odo number to even number , or from even number to odo number.
No occurring when it is changed from odo number to odo number or from even number to ever number)

Parameter 3 (P37 to 36):
P36: Select OSCO pin function
0: VSS output
1: Clock output
P37: Select LCD type
0: Normally white
1: Normally black

Parameter 3 (P33 to 30):
Parameter 4: set “number of front porch lines” -1.
Set “number of front porch lines” from 1 to 4096.
When frame frequency is decreased like to use partial display, it is recommend to increase the number in order to decrease frame frequency. It makes possible to reduce power consumption.

7.3.4 DISSET2 (Display Set 2: 93h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	0	1	0	0	1	1	93	Command DISSET2
P17	P16	P15	P14	P13	P12	P11	P10	—	Parameter 1 (P1) Source output ON timing
P27	P26	P25	P24	P23	P22	P21	P20	—	Parameter 2 (P2) Source output OFF timing
P37	P36	P35	P34	P33	P32	P31	P30	—	Parameter 3 (P3) Gate output ON timing
P47	P46	P45	P44	P43	P42	P41	P40	—	Parameter 4 (P4) Gate output OFF timing

Set source ON/OFF timing gate output ON/OFF timing.
Optimized output timing is set by setting the display timing clock.
P1 of DISSET1 command set timing within "number of 1H select period clock" -1.
Changing point of VCOM is start point (1st clock).

Parameter 1: Set source ON timing by "number of clock from starting" - 1.

Parameter 2: Set source OFF timing (Hi-Z) by "number of clock from starting" - 1.

Parameter 1 and 2 must be set as following condition.
1 < "Source ON timing" < "Source OFF timing" < "number of 1H clocks" – 1.
And Source output Hi-Z period must be set 20us or more.
(refer to fig.38)

Parameter 3: set gate ON (V_{DDHG}) timing by "number of clock from starting" - 1.

Parameter 4: set gate OFF (V_{EE}) timing by "number of clock from starting" - 1.

Parameter 3 and 4 must be set as following condition.

Source ON Timing	<	Gate ON Timing	<	Gate OFF Timing	<	Source OFF Timing

Example) When "number of 1H clock" is 51 clocks.

Source ON timing	DISSET2	P1 = 10
Source OFF timing	DISSET2	P2 = 40
Gate ON timing	DISSET2	P3 = 12
Gate OFF timing	DISSET2	P4 = 38

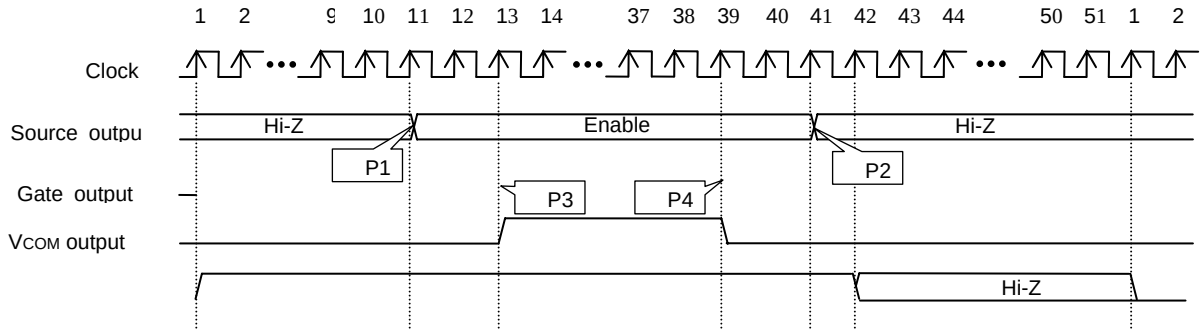


Fig.38 Display timing chart

7.3.5 DINVIN (Display invert IN: 16h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	0	1	0	1	1	0	16	Command DINVIN
1	0	1	0	0	1	0	1	A5	Parameter 1 (P1) Dummy

This command inverts Display without re-writing display RAM. It is enable next frame after receiving the command.

7.3.6 DINVOUT (Display invert OUT: 15h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	0	1	0	1	0	1	15	Command DINVOUT
1	0	1	0	0	1	0	1	A5	Parameter 1 (P1) Dummy

This command quits from display inverting state. It is enable next frame after receiving the command.

7.3.7 MADCTL (Memory Address Control: 21h)

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
0	0	1	0	0	0	0	1	21	Command MADCTL
0	0	0	0	0	P12	P11	P10	—	Parameter 1 (P1) Display data RAM control
1	0	1	0	0	1	0	1	A5	Parameter 2 (P2) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 3 (P3) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 4 (P4) Dummy

Set about Display data RAM.
To access display RAM, it is required 1ms or more wait after input this command.

Parameter 1:
P10: Display data RAM column address NORMAL / REVERSE
0: Normal (S1: address 0, S320: address 319)
1: Reverse (S1: address 319, S320: address 0)
P11: Display data RAM page address NORMAL / REVERSE
0: Normal
1: Reverse
P12: Select address increment direction when MPU writes or read to display data RAM)
0: Increment column address direction.
1: Increment page address direction.

7.3.8 CASET (Column Address Set: 23h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	1	0	0	0	1	1	23	Command CASET
0	0	0	0	0	0	0	P10	—	Parameter 1 (P1) Start address (MSB)
P27	P26	P25	P24	P23	P22	P21	P20	—	Parameter 2 (P2) Start address (LSB)
0	0	0	0	0	0	0	P30	—	Parameter 3 (P3) End address (MSB)
P47	P46	P45	P44	P43	P42	P41	P40	—	Parameter 4 (P4) End address (LSB)

Set column start address and column end address of display data RAM.
They must be “Start address < End address”

Parameter 1, Parameter 2: Set column start address.
Parameter 3, Parameter 4: Set column end address.

P10 P30	P27 P47	P26 P46	P25 P45	P24 P44	P23 P43	P22 P42	P21 P41	P20 P40	Column address
0	0	0	0	0	0	0	0	0	00h
0	0	0	0	0	0	0	0	1	01h
0	0	0	0	0	0	0	1	0	02h
:	:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	1	0	13Eh
1	0	0	1	1	1	1	1	1	13Fh

7.3.9 PASET (Page Address Set: 22h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	1	0	0	0	1	0	22	Command PASET
P17	P16	P15	P14	P13	P12	P11	P10	—	Parameter 1(P1) start address
P27	P26	P25	P24	P23	P22	P21	P20	—	Parameter 2(P2) end address
0	0	0	0	0	0	P31	P30	—	Parameter 3(P3) frame address
1	0	1	0	0	1	0	1	A5	Parameter 4(P4) dummy

Set page start address, page end address and frame address.
Relationship between page address and display line address is changed by 7.3.11 BPPSEL command.
They must be “Start address < end address”.

Parameter 1: set page start address
Parameter 2: set page end address
Address range by PASET command is depend on setting of 7.3.11 BPPSEL command.

P17 P27	P16 P26	P15 P25	P14 P24	P13 P23	P12 P22	P11 P21	P10 P20	Page Address	Display line 4bit	2bit	1bit
0	0	0	0	0	0	0	0	00h	1	1	1
0	0	0	0	0	0	0	1	01h	3	5	9
0	0	0	0	0	0	1	0	02h	5	9	17
:	:	:	:	:	:	:	:	:	:	:	:
0	0	1	0	0	1	0	1	25h	75	149	297
0	0	1	0	0	1	1	0	26h	77	153	305
0	0	1	0	0	1	1	1	27h	79	157	313
:	:	:	:	:	:	:	:	:	:	:	
0	1	0	0	1	1	0	1	4Dh	235	309	
0	1	0	0	1	1	1	0	4Eh	237	313	
0	1	0	0	1	1	1	1	4Fh	239	317	
:	:	:	:	:	:	:	:	:	:		
1	0	0	1	1	1	0	1	9Dh	315		
1	0	0	1	1	1	1	0	9Eh	317		
1	0	0	1	1	1	1	1	9Fh	319		

Parameter 3: set frame address
Frame address range by PASET command is depend on setting of 7.3.11 BPPSEL command (refer to Table 21 Display line page address frame address relation)

P31	P30	Frame address
0	0	0
0	1	1
1	0	2
1	1	3

7.3.10 STFRAME (Start Frame Address: 24h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	1	0	0	1	0	0	24	Command STFRAME
0	0	0	0	0	0	P11	P10	—	Parameter 1 (P1) Frame address
1	0	1	0	0	1	0	1	A5	Parameter 2 (P2) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 3 (P3) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 4 (P4) Dummy

Set display start address of the display data RAM

Parameter 1: set frame address
Frame address range by PASET command is depend on setting of 7.3.11 BPPSEL command.
(refer to Table 21 Display line, page address and frame address relationship)

P11	P10	Frame address
0	0	0
0	1	1
1	0	2
1	1	3

7.3.11 BPPSEL (Bpp Sel: 25h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	1	0	0	1	0	1	25	Command BPPSEL
0	0	0	0	0	0	P11	P10	—	Parameter 1 (P1) Data format
1	0	1	0	0	1	0	1	A5	Parameter 2(P2) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 3(P3) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 4(P4) Dummy

Set data format (bit per pixel) as following table.
It is enable in next frame after receiving the command.
Possible to change 4bpp / 2bpp / 1bpp.
It must be input during display off state, and display data must be written after changing

Parameter 1:
P11 to 10: Data format

P11	P10	Data format
0	0	1 bpp (2 grayscale)
0	1	2 bpp (4 grayscale)
1	*	4 bpp (16 grayscale)

7.3.12 MDCTL (Memory Data Control: 26h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	1	0	0	1	1	0	26	Command MDCTL
0	0	0	0	0	0	P11	P10	–	Parameter 1 (P1) Data mask option
P27	P26	P25	P24	P23	P22	P21	P20	–	Parameter 2 (P2) Mask at start page address
P37	P36	P35	P34	P33	P32	P31	P30	–	Parameter 3 (P3) Mask at end page address
1	0	1	0	0	1	0	1	A5	Parameter 4 (P4) Dummy

When Display data is written to display data RAM by WRRAM command, data which is sent from MPU is masked by this command. This mask function is applied to start page address and end page address only.

This setting does not affect to writing by BLKFIL command.

Parameter 1:

P11 to P10: Select mask (bit operation) option as following.

P11	P10	Bit operation
0	0	No operation
0	1	AND
1	0	OR
1	1	No operation

Parameter 2:

P27 to P20: Mask data of Start page address.

Parameter 3:

P37 to P30: Mask data of End page address.

Example) P1=01h, P2=FCh, P3=3Fh

Display data transferred by MPU for start page address

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	1	1

&

Mask data (parameter 2)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	0	0

↓

Display data written in start page address of display data RAM

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0

Display data transferred by MPU for end page address

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	0	0	0	0

&

Mask data (parameter 3)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	1

↓

Display data written in end page address of display data RAM

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	0	0

7.3.13 GATESET (Gate Set: C3h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	1	0	0	0	1	0	A2	Command GATESET
P17	0	0	P14	0	0	P11	P10	—	Parameter 1 (P1) Scan mode
1	0	1	0	0	1	0	1	A5	Parameter 2 (P2) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 3 (P3) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 4 (P4) Dummy

Set line scan mode of gate driver. Refer to section 6.4 to set in detail.
This command must be input before SLPOUT command.

Parameter 1: set gate line scan mode.
P11 to P10: Scan mode

P11	P10	Gate line scan mode
0	0	Interlace drive 1
0	1	Interlace drive 2
1	0	Up and down drive 1
1	1	Up and down drive 2

P14: Scan direction
0: Normal scan direction
1: Reverse scan direction

P17: Valid gate pin position
0: inside Number of display lines from G1, G2 pin side is valid
1: outside Number of display lines from G320, G319 pin side is valid.
(Example) in case of “Number of display lines” = 300
P17=0: G1 to G300 are valid
P17=1: G21 to G320 are valid.

7.3.14 ACSET (AC Set: C1h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	1	0	0	0	0	1	A1	Command ACSET
0	0	P15	P14	0	0	P11	P10	—	Parameter 1 (P1) AC driver mode
1	0	1	0	0	1	0	1	A5	Parameter 2 (P2) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 3 (P3) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 4 (P4) Dummy

Set AC drive mode. It is enable in next frame after receiving the command.

Parameter 1: set AC drive mode.
P11 to P10: set AC drive mode in display ON
P15 to P14: set AC drive mode in display OFF

P11/P15	P10/P14	AC drive mode
0	0	1 line inversion drive
0	1	2 line inversion drive
1	0	frame inversion drive
1	1	Interlace drive

7.3.15 GAMSET4P1 (Gamma Set 4bpp Positive 1: 81h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	0	0	0	0	0	1	81	Command GAMSET4P1
0	0	P15	P14	P13	P12	P11	P10	—	Parameter 1 (P1) V_0 voltage setting (Positive polarity)
0	0	P25	P24	P23	P22	P21	P20	—	Parameter 2 (P2) V_1 voltage setting (Positive polarity)
0	0	P35	P34	P33	P32	P31	P30	—	Parameter 3 (P3) V_2 voltage setting (Positive polarity)
0	0	P45	P44	P43	P42	P41	P40	—	Parameter 4 (P4) V_3 voltage setting (Positive polarity)

Set LCD gamma voltage setting of positive polarity in 4bpp mode. This command must be input before SLPOUT. In detail refer to 6.8 grayscale voltage generating circuit.

7.3.16 GAMSET4P2 (Gamma Set 4bpp Positive 1: 82h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	0	0	0	0	1	0	82	Command GAMSET4P2
0	0	P15	P14	P13	P12	P11	P10	—	Parameter 1 (P1) V_4 voltage setting (Positive polarity)
0	0	P25	P24	P23	P22	P21	P20	—	Parameter 2 (P2) V_5 voltage setting (Positive polarity)
0	0	P35	P34	P33	P32	P31	P30	—	Parameter 3 (P3) V_6 voltage setting (Positive polarity)
0	0	P45	P44	P43	P42	P41	P40	—	Parameter 4 (P4) V_7 voltage setting (Positive polarity)

Set LCD gamma voltage setting of positive polarity in 4bpp mode. This command must be input before SLPOUT. In detail refer to 6.8 grayscale voltage generating circuit.

7.3.17 GAMSET4P3 (Gamma Set 4bpp Positive 1: 83h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	0	0	0	0	1	1	83	Command GAMSET4P3
0	0	P15	P14	P13	P12	P11	P10	—	Parameter 1 (P1) V_8 voltage setting (Positive polarity)
0	0	P25	P24	P23	P22	P21	P20	—	Parameter 2 (P2) V_9 voltage setting (Positive polarity)
0	0	P35	P34	P33	P32	P31	P30	—	Parameter 3 (P3) V_{10} voltage setting (Positive polarity)
0	0	P45	P44	P43	P42	P41	P40	—	Parameter 4 (P4) V_{11} voltage setting (Positive polarity)

Set LCD gamma voltage setting of positive polarity in 4bpp mode. This command must be input before SLPOUT. In detail refer to 6.8 grayscale voltage generating circuit.

7.3.18 GAMSET4P4 (Gamma Set 4bpp Positive 1: 84h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	0	0	0	1	0	0	84	Command GAMSET4P4
0	0	P15	P14	P13	P12	P11	P10	—	Parameter 1 (P1) V_{12} voltage setting (Positive polarity)
0	0	P25	P24	P23	P22	P21	P20	—	Parameter 2 (P2) V_{13} voltage setting (Positive polarity)
0	0	P35	P34	P33	P32	P31	P30	—	Parameter 3 (P3) V_{14} voltage setting (Positive polarity)
0	0	P45	P44	P43	P42	P41	P40	—	Parameter 4 (P4) V_{15} voltage setting (Positive polarity)

Set LCD gamma voltage setting of positive polarity in 4bpp mode. This command must be input before SLPOUT.

In detail refer to 6.8 grayscale voltage generating circuit.

7.3.19 GAMSET4N1 (Gamma Set 4bpp Negative 1: 89h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	0	0	1	0	0	1	89	Command GAMSET4N1
0	0	P15	P14	P13	P12	P11	P10	—	Parameter 1(P1)V_0 voltage setting (Negative polarity)
0	0	P25	P24	P23	P22	P21	P20	—	Parameter 2(P2)V_1 voltage setting (Negative polarity)
0	0	P35	P34	P33	P32	P31	P30	—	Parameter 3(P3)V_2 voltage setting (Negative polarity)
0	0	P45	P44	P43	P42	P41	P40	—	Parameter 4(P4)V_3 voltage setting (Negative polarity)

Set LCD gamma voltage setting of negative polarity in 4bpp mode. This command must be input before SLPOUT. In detail refer to 6.8 grayscale voltage generating circuit.

7.3.20 GAMSET4N2 (Gamma Set 4bpp Negative 2: 8Ah)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	0	0	1	0	1	0	8A	Command GAMSET4N2
0	0	P15	P14	P13	P12	P11	P10	—	Parameter 1(P1)V_4 voltage setting (Negative polarity)
0	0	P25	P24	P23	P22	P21	P20	—	Parameter 2(P2)V_5 voltage setting (Negative polarity)
0	0	P35	P34	P33	P32	P31	P30	—	Parameter 3(P3)V_6 voltage setting (Negative polarity)
0	0	P45	P44	P43	P42	P41	P40	—	Parameter 4(P4)V_7 voltage setting (Negative polarity)

Set LCD gamma voltage setting of negative polarity in 4bpp mode. This command must be input before SLPOUT. In detail refer to 6.8 grayscale voltage generating circuit.

7.3.21 GAMSET4N3 (Gamma Set 4bpp Negative 2: 8Bh)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	0	0	1	0	1	1	8B	Command GAMSET4N3
0	0	P15	P14	P13	P12	P11	P10	—	Parameter 1(P1)V_8 voltage setting (Negative polarity)
0	0	P25	P24	P23	P22	P21	P20	—	Parameter 2(P2)V_9 voltage setting (Negative polarity)
0	0	P35	P34	P33	P32	P31	P30	—	Parameter 3(P3)V_{10} voltage setting (Negative polarity)
0	0	P45	P44	P43	P42	P41	P40	—	Parameter 4(P4)V_{11} voltage setting (Negative polarity)

Set LCD gamma voltage setting of negative polarity in 4bpp mode. This command must be input before SLPOUT. In detail refer to 6.8 grayscale voltage generating circuit.

7.3.22 GAMSET4N4 (Gamma Set 4bpp Negative 2: 8Ch)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	0	0	1	1	0	0	8C	Command GAMSET4N4
0	0	P15	P14	P13	P12	P11	P10	—	Parameter 1(P1)V_{12} voltage setting (Negative polarity)
0	0	P25	P24	P23	P22	P21	P20	—	Parameter 2(P2)V_{13} voltage setting (Negative polarity)
0	0	P35	P34	P33	P32	P31	P30	—	Parameter 3(P3)V_{14} voltage setting (Negative polarity)
0	0	P45	P44	P43	P42	P41	P40	—	Parameter 4(P4)V_{15} voltage setting (Negative polarity)

Set LCD gamma voltage setting of negative polarity in 4bpp mode. This command must be input before SLPOUT. In detail refer to 6.8 grayscale voltage generating circuit.

7.3.23 GAMSET2P (Gamma Set 2bpp Positive: 85h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	0	0	0	1	0	1	85	Command GAMSET2P
0	0	P15	P14	P13	P12	P11	P10	—	Parameter 1(P1)V_0 voltage setting (Positive polarity)
0	0	P25	P24	P23	P22	P21	P20	—	Parameter 2(P2)V_1 voltage setting (Positive polarity)
0	0	P35	P34	P33	P32	P31	P30	—	Parameter 3(P3)V_2 voltage setting (Positive polarity)
0	0	P45	P44	P43	P42	P41	P40	—	Parameter 4(P4)V_3 voltage setting (Positive polarity)

Set LCD gamma voltage setting of negative polarity in 2bpp mode. This command must be input before SLPOUT. In detail refer to 6.8 grayscale voltage generating circuit.

7.3.24 GAMSET2N (Gamma Set 2bpp Negative: 8Dh)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	0	0	1	1	0	1	8D	Command GAMSET2N
0	0	P15	P14	P13	P12	P11	P10	—	Parameter 1(P1)V_0 voltage setting (Negative polarity)
0	0	P25	P24	P23	P22	P21	P20	—	Parameter 2(P2)V_1 voltage setting (Negative polarity)
0	0	P35	P34	P33	P32	P31	P30	—	Parameter 3(P3)V_2 voltage setting (Negative polarity)
0	0	P45	P44	P43	P42	P41	P40	—	Parameter 4(P4)V_3 voltage setting (Negative polarity)

Set LCD gamma voltage setting of negative polarity in 2bpp mode. This command must be input before SLPOUT. In detail refer to 6.8 grayscale voltage generating circuit.

7.3.25 GAMSET1 (Gamma Set 1bpp: 86h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	0	0	0	1	1	0	86	Command GAMSET1
0	0	P15	P14	P13	P12	P11	P10	—	Parameter 1(P1)V_0 voltage setting (positive polarity)
0	0	P25	P24	P23	P22	P21	P20	—	Parameter 2(P2)V_1 voltage setting (positive polarity)
0	0	P35	P34	P33	P32	P31	P30	—	Parameter 3(P3)V_0 voltage setting (Negative polarity)
0	0	P45	P44	P43	P42	P41	P40	—	Parameter 4(P4)V_1 voltage setting (Negative polarity)

Set LCD gamma voltage setting of negative polarity in 1bpp mode. This command must be input before SLPOUT. In detail refer to 6.8 grayscale voltage generating circuit.

7.3.26 EVSET1 (Electronic Volume Set 1: 71h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	1	1	0	0	0	1	71	Command EVSET1
0	0	0	0	P13	P12	P11	P10	—	Parameter 1(P1)V_{DDHS}
P27	P26	P25	P24	P23	P22	P21	P20	—	Parameter 2(P2)V_{COMH}
0	0	0	P34	P33	P32	P31	P30	—	Parameter 3(P3)VCA
0	0	0	P44	P43	P42	P41	P40	—	Parameter 4(P4)V_{DDRH}

Set each output voltages of built-in voltage regulators.
Refer to Table 40 Electric volume value for setting voltages.

Parameter 1 to Parameter 4: Set each output voltages of built-in voltage regulators.

7.3.27 EVSET2 (Electronic Volume Set 2: 72h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	1	1	0	0	1	0	72	Command EVSET2
0	0	0	P14	P13	P12	P11	P10	—	Parameter 1(P1)V_{OFREG}
0	0	P25	P24	P23	P22	P21	P20	—	Parameter 2(P2)V_{ONREG}
1	0	1	0	0	1	0	1	A5	Parameter 3(P3) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 4(P4) Dummy

Set each output voltages of built-in voltage regulators.
Refer to Table 40 Electric volume value for setting voltages.

Parameter 1 to Parameter 2: Set each output voltages of built-in voltage regulators.

Table 40 Electric volume value

Unit: V

EVR	VDDHS
0 (00h)	4.10
1 (01h)	4.20
2 (02h)	4.30
3 (03h)	4.40
4 (04h)	4.50
5 (05h)	4.60
6 (06h)	4.70
7 (07h)	4.80
8 (08h)	4.90
9 (09h)	5.00
10 (0Ah)	5.10
11 (0Bh)	5.20
12 (0Ch)	5.30
13 (0Dh)	5.40
14 (0Eh)	5.50
15 (0Fh)	5.60

EVR	VOFREG	VDDRH	VCA
0 (00h)	2.40	3.00	1.50
1 (01h)	2.50	3.10	1.55
2 (02h)	2.60	3.20	1.60
3 (03h)	2.70	3.30	1.65
4 (04h)	2.80	3.40	1.70
5 (05h)	2.90	3.50	1.75
6 (06h)	3.00	3.60	1.80
7 (07h)	3.10	3.70	1.85
8 (08h)	3.20	3.80	1.90
9 (09h)	3.30	3.90	1.95
10 (0Ah)	3.40	4.00	2.00
11 (0Bh)	3.50	4.10	2.05
12 (0Ch)	3.60	4.20	2.10
13 (0Dh)	3.70	4.30	2.15
14 (0Eh)	3.80	4.40	2.20
15 (0Fh)	3.90	4.50	2.25
16 (10h)	4.00	4.60	2.30
17 (11h)	4.10	4.70	2.35
18 (12h)	4.20	4.80	2.40
19 (13h)	4.30	4.90	2.45
20 (14h)	4.40	5.00	2.50
21 (15h)	4.50	5.10	2.55
22 (16h)	4.60	5.20	2.60
23 (17h)	4.70	5.30	2.65
24 (18h)	4.80	5.40	2.70
25 (19h)	4.90	5.50	2.75
26 (1Ah)	5.00	−(5.50)	2.80
27 (1Bh)	5.10	−(5.50)	2.85
28 (1Ch)	5.20	−(5.50)	2.90
29 (1Dh)	5.30	−(5.50)	2.95
30 (1Eh)	5.40	−(5.50)	3.00
31 (1Fh)	5.50	−(5.50)	−(3.00)

EVR	VONREG	EVR	VONREG
0 (00h)	0	32 (20h)	4.60
1 (01h)	1.50	33 (21h)	4.70
2 (02h)	1.60	34 (22h)	4.80
3 (03h)	1.70	35 (23h)	4.90
4 (04h)	1.80	36 (24h)	5.00
5 (05h)	1.90	37 (25h)	−(5.00)
6 (06h)	2.00	38 (26h)	−(5.00)
7 (07h)	2.10	39 (27h)	−(5.00)
8 (08h)	2.20	40 (28h)	−(5.00)
9 (09h)	2.30	41 (29h)	−(5.00)
10 (0Ah)	2.40	42 (2Ah)	−(5.00)
11 (0Bh)	2.50	43 (2Bh)	−(5.00)
12 (0Ch)	2.60	44 (2Ch)	−(5.00)
13 (0Dh)	2.70	45 (2Dh)	−(5.00)
14 (0Eh)	2.80	46 (2Eh)	−(5.00)
15 (0Fh)	2.90	47 (2Fh)	−(5.00)
16 (10h)	3.00	48 (30h)	−(5.00)
17 (11h)	3.10	49 (31h)	−(5.00)
18 (12h)	3.20	50 (32h)	−(5.00)
19 (13h)	3.30	51 (33h)	−(5.00)
20 (14h)	3.40	52 (34h)	−(5.00)
21 (15h)	3.50	53 (35h)	−(5.00)
22 (16h)	3.60	54 (36h)	−(5.00)
23 (17h)	3.70	55 (37h)	−(5.00)
24 (18h)	3.80	56 (38h)	−(5.00)
25 (19h)	3.90	57 (39h)	−(5.00)
26 (1Ah)	4.00	58 (3Ah)	−(5.00)
27 (1Bh)	4.10	59 (3Bh)	−(5.00)
28 (1Ch)	4.20	60 (3Ch)	−(5.00)
29 (1Dh)	4.30	61 (3Dh)	−(5.00)
30 (1Eh)	4.40	62 (3Eh)	−(5.00)
31 (1Fh)	4.50	63 (3Fh)	−(5.00)

Unit: V

EVR	VCOMH	EVR	VCOMH	EVR	VCOMH	EVR	VCOMH	EVR	VCOMH
0 (00h)	2.46	32 (20h)	3.10	64 (40h)	3.74	96 (60h)	4.38	128 (80h)	5.02
1 (01h)	2.48	33 (21h)	3.12	65 (41h)	3.76	97 (61h)	4.40	129 (81h)	5.04
2 (02h)	2.50	34 (22h)	3.14	66 (42h)	3.78	98 (62h)	4.42	130 (82h)	5.06
3 (03h)	2.52	35 (23h)	3.16	67 (43h)	3.80	99 (63h)	4.44	131 (83h)	5.08
4 (04h)	2.54	36 (24h)	3.18	68 (44h)	3.82	100 (64h)	4.46	132 (84h)	5.10
5 (05h)	2.56	37 (25h)	3.20	69 (45h)	3.84	101 (65h)	4.48	133 (85h)	5.12
6 (06h)	2.58	38 (26h)	3.22	70 (46h)	3.86	102 (66h)	4.50	134 (86h)	5.14
7 (07h)	2.60	39 (27h)	3.24	71 (47h)	3.88	103 (67h)	4.52	135 (87h)	5.16
8 (08h)	2.62	40 (28h)	3.26	72 (48h)	3.90	104 (68h)	4.54	136 (88h)	5.18
9 (09h)	2.64	41 (29h)	3.28	73 (49h)	3.92	105 (69h)	4.56	137 (89h)	5.20
10 (0Ah)	2.66	42 (2Ah)	3.30	74 (4Ah)	3.94	106 (6Ah)	4.58	138 (8Ah)	5.22
11 (0Bh)	2.68	43 (2Bh)	3.32	75 (4Bh)	3.96	107 (6Bh)	4.60	139 (8Bh)	5.24
12 (0Ch)	2.70	44 (2Ch)	3.34	76 (4Ch)	3.98	108 (6Ch)	4.62	140 (8Ch)	5.26
13 (0Dh)	2.72	45 (2Dh)	3.36	77 (4Dh)	4.00	109 (6Dh)	4.64	141 (8Dh)	5.28
14 (0Eh)	2.74	46 (2Eh)	3.38	78 (4Eh)	4.02	110 (6Eh)	4.66	142 (8Eh)	5.30
15 (0Fh)	2.76	47 (2Fh)	3.40	79 (4Fh)	4.04	111 (6Fh)	4.68	143 (8Fh)	5.32
16 (10h)	2.78	48 (30h)	3.42	80 (50h)	4.06	112 (70h)	4.70	144 (90h)	5.34
17 (11h)	2.80	49 (31h)	3.44	81 (51h)	4.08	113 (71h)	4.72	145 (91h)	5.36
18 (12h)	2.82	50 (32h)	3.46	82 (52h)	4.10	114 (72h)	4.74	146 (92h)	5.38
19 (13h)	2.84	51 (33h)	3.48	83 (53h)	4.12	115 (73h)	4.76	147 (93h)	5.40
20 (14h)	2.86	52 (34h)	3.50	84 (54h)	4.14	116 (74h)	4.78	148 (94h)	5.42
21 (15h)	2.88	53 (35h)	3.52	85 (55h)	4.16	117 (75h)	4.80	149 (95h)	5.44
22 (16h)	2.90	54 (36h)	3.54	86 (56h)	4.18	118 (76h)	4.82	150 (96h)	5.46
23 (17h)	2.92	55 (37h)	3.56	87 (57h)	4.20	119 (77h)	4.84	151 (97h)	5.48
24 (18h)	2.94	56 (38h)	3.58	88 (58h)	4.22	120 (78h)	4.86	152 (98h)	5.50
25 (19h)	2.96	57 (39h)	3.60	89 (59h)	4.24	121 (79h)	4.88	153 (99h)	−(5.50)
26 (1Ah)	2.98	58 (3Ah)	3.62	90 (5Ah)	4.26	122 (7Ah)	4.90	155 (9Ah)	−(5.50)
27 (1Bh)	3.00	59 (3Bh)	3.64	91 (5Bh)	4.28	123 (7Bh)	4.92	156 (9Bh)	−(5.50)
28 (1Ch)	3.02	60 (3Ch)	3.66	92 (5Ch)	4.30	124 (7Ch)	4.94	:	:
29 (1Dh)	3.04	61 (3Dh)	3.68	93 (5Dh)	4.32	125 (7Dh)	4.96	253 (FDh)	−(5.50)
30 (1Eh)	3.06	62 (3Eh)	3.70	94 (5Eh)	4.34	126 (7Eh)	4.98	254 (FEh)	−(5.50)
31 (1Fh)	3.08	63 (3Fh)	3.72	95 (5Fh)	4.36	127 (7Fh)	5.00	255 (FFh)	−(5.50)

Above values are calculated values. They are not guaranteed. Actual values are calculated based and output by voltage regulators therefore actual values include deviation of VREG and voltage regulators.

VCOMH output voltage setting by P27 to P20 of the EVSET1 command is possible to adjust offset voltage by VCMDAT command.

7.3.28 PWRCTL (Power Control: 61h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	1	0	0	0	0	1	61	Command PWRCTL
P17	P16	P15	P14	P13	P12	P11	P10	—	Parameter 1(P1) Booster circuit control, VCOMH and VCOML control
P27	P26	P25	P24	P23	P22	P21	P20	—	Parameter 2(P2) Source amp. Setting, Display wait and VCOMH regulator drivability setting.
0	P36	P35	P34	0	P32	P31	P30	—	Parameter 3(P3) Booster clock frequency setting in normal display
0	P46	P45	P44	0	P42	P41	P40	—	Parameter 4(P4) Booster clock frequency setting in partial display

Booster circuit control, source amp setting and booster clock frequency settings. This command must be input before SLPOUT command.

Parameter 1: Booster circuit setting VCOMH and VCOML voltage regulator setting.

P13 to P10: On/Off control of booster circuits. When external voltage is input to VOUT pin, 1st booster circuit must be OFF (P10=0). P11 to P13 must be "1".

0: Booster circuit OFF
1: Booster circuit ON
P10: 1st booster
P11: 2nd booster
P12: 3rd booster
P13: 4th booster

P14: VCOML regulator circuit ON/OFF is controlled. When VCOML=0V setting is used, set this parameter to 0, and the VCOML regulator is OFF (VCOML=VSS). In this time, 2nd booster circuit (include VLDO2 regulator) is off, even if P11=1. In this case, VCA of the EVSET1 command is ignored. And connect VDCCOM pin to VDD2 and VOUTM pin to VSS.

When VCOML is not set to 0V, set this parameter to 1.

0: VCOML regulator circuit OFF (VDCCOM=VDD2, VOUTM=VSS are required)
1: VCOML regulator circuit ON

P15: Regulator type of VCOML and VCOMH. It must be "0".

0: AB class regulator
1: B class regulator

P17 to P16: Step-up rate of the 3rd booster setting.

P17	P16	Step-up rate
0	0	*(-1)
0	1	*(-2)
1	0	*(-3)
1	1	Prohibit *(-2)

Parameter 2: Source amplifier setting

P22 to P20: Select source amplifier setting in order to adjust source line load. Refer to following graph with checking display quality. P20 to 22 must be set just only one.

P22	P21	P20	Source amp setting
0	0	1	Setting 1
0	1	0	Setting 2
1	0	0	Setting 3
Prohibit to set other number			

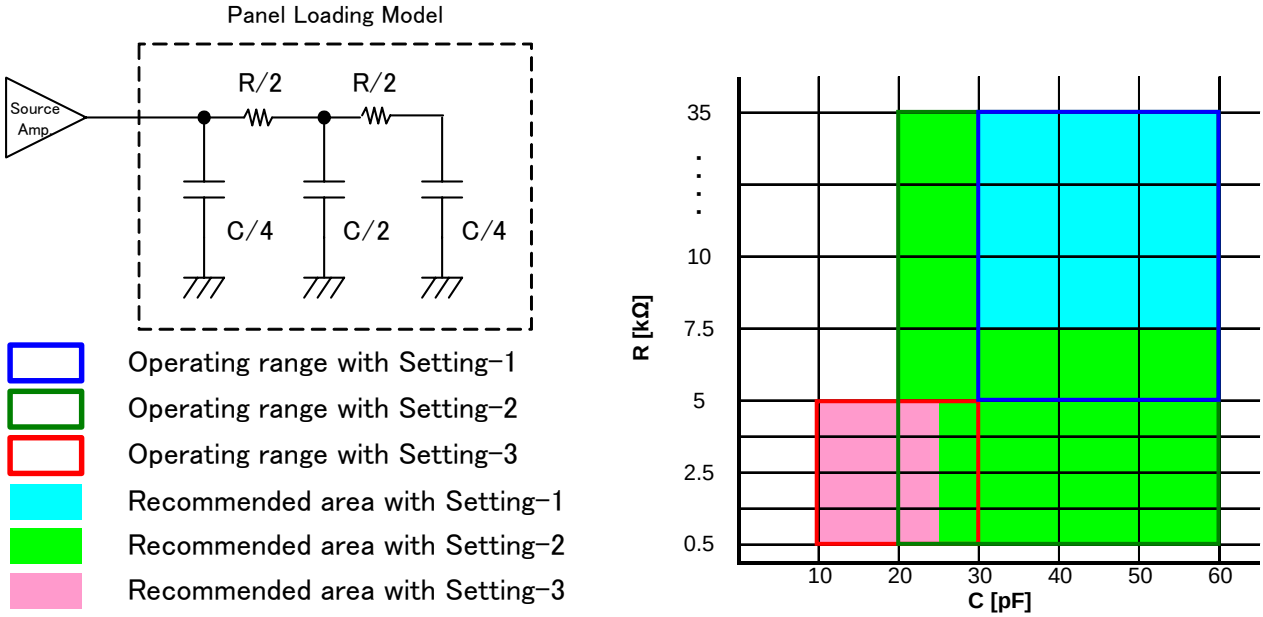


Table 39 Source amplifier settings vs Panel load

P23: Setting of VCOMH regulator (AB class) drivability. It is valid when AB class is selected in P15. Normally, it should be set to "0". Only when it is required to rise VCOMH fast, set to "1". In this case power consumption is up.
0: Normal
1: Drivability up

P27 to P24: Wait time setting by number of frames from sleepout to display ON.

P27	P26	P25	P24	Wait time
0	0	0	0	5 frames
0	0	0	1	6 frames
0	0	1	0	7 frames
0	0	1	1	8 frames
0	1	0	0	9 frames
0	1	0	1	10 frames
0	1	1	0	11 frames
0	1	1	1	12 frames
1	0	0	0	13 frames
1	0	0	1	14 frames
1	0	1	0	15 frames
1	0	1	1	16 frames
1	1	0	0	17 frames
1	1	0	1	18 frames
1	1	1	0	19 frames
1	1	1	1	20 frames

Parameter 3: Booster clock setting at display area when normal display.
After SLPOUT, once the booster clock becomes Frecuency of 1H, and setting of this parameter becomes valid after display possible state
P32 to P30: 1st and 2nd booster clock frequency settings
P36 to P34: 3rd and 4th booster clock frequency settings
Decide it with evaluation display

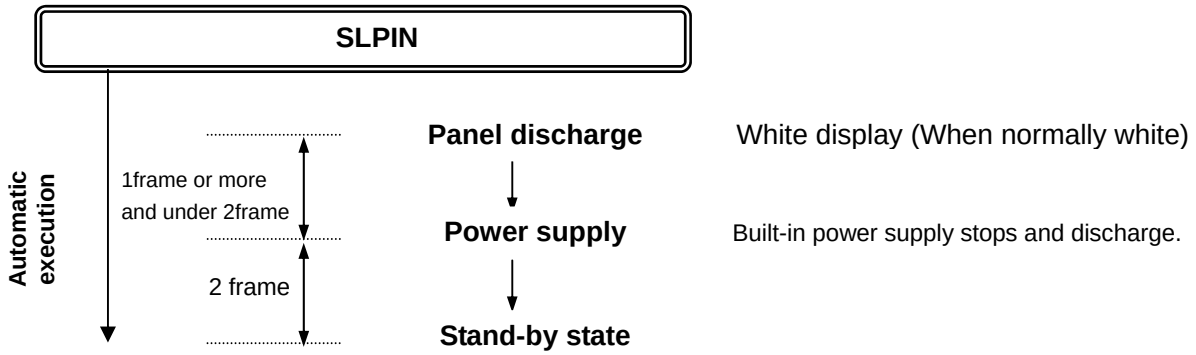
Parameter 4: Booster clock setting at non-display area of partial display period when non-refresh term and front porch period.
P42 to P40: 1st and 2nd booster clock frequency settings
P46 to P44: 3rd and 4th booster clock frequency settings
Decide it with evaluation display

P*2/P*6	P*1/P*5	P*0/P*4	Frequency
0	*	*	Frequency of 1H * 1
1	0	0	Frequency of 1H * 4
1	0	1	Frequency of 1H * 2
1	1	0	Frequency of 1H / 2
1	1	1	Frequency of 1H / 4

7.3.29 SLPIN (Sleep In: 14h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	0	1	0	1	0	0	14	Command SLPIN
1	0	1	0	0	1	0	1	A5	Parameter 1(P1) Dummy

Discharge panel and discharge built-in power supply, after that, go to stand-by state. This command is executed immediately after command input.



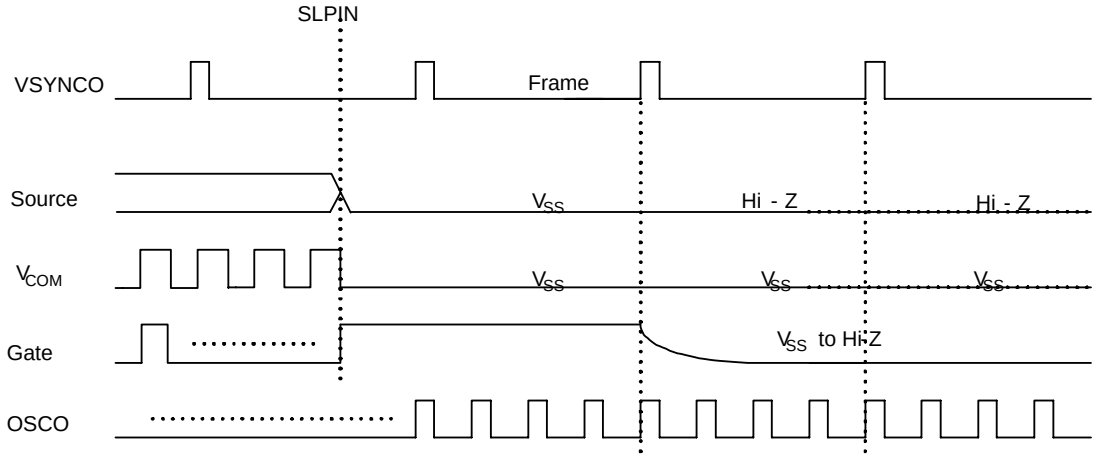
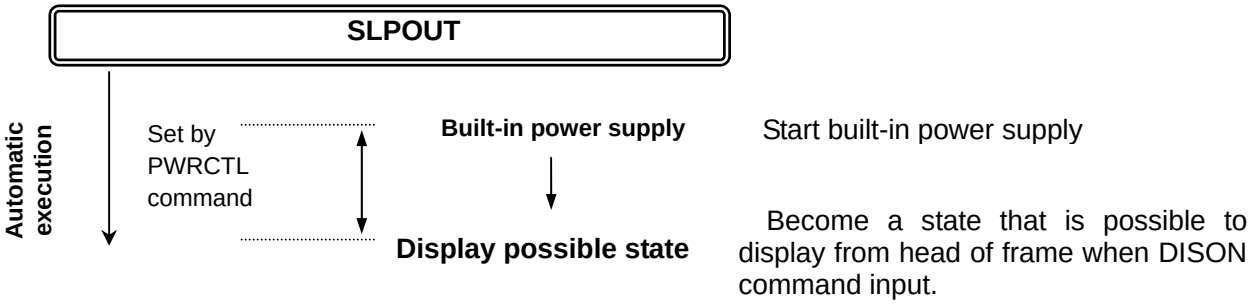


Fig 40 Sleep in timing chart

7.3.30 SLPOUT (Sleep Out: 13h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	0	1	0	0	1	1	13	Command SLPOUT
1	0	1	0	0	1	0	1	A5	Parameter 1(P1) Dummy

Wake up built-in power supply sequentially.
When DISON command is input after built-in power supply, display is started from head of frame.
When DISON command is input before built-in power supply, display is waited until waking up built-in power supply, and after that, display is started from head of frame.



Display when DISON command is input.
Display after waking up built-in power supply when DISON command is input. When DISON command is not input, “display possible state” is continued.

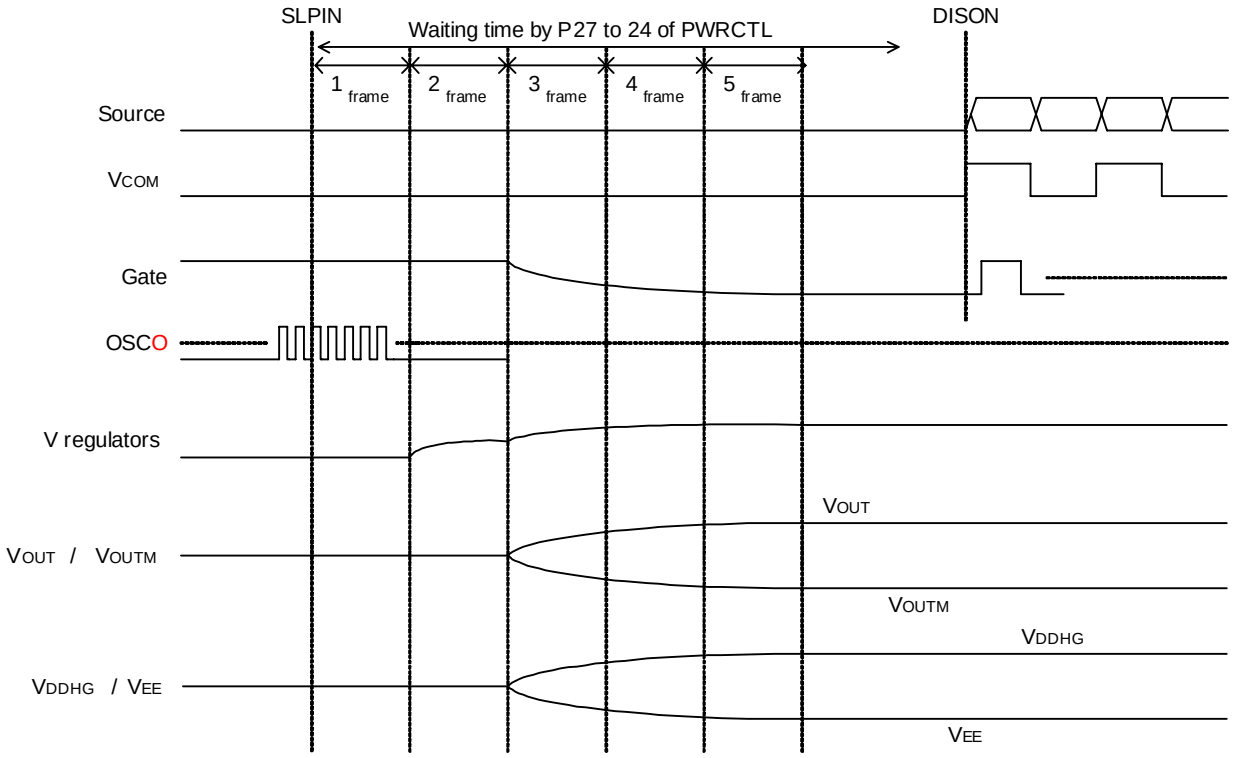


Fig 41 Sleep out timing chart

7.3.31 DISON (Display On: 12h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	0	1	0	0	1	0	12	Command DISON
1	0	1	0	0	1	0	1	A5	Parameter 1(P1) Dummy

Start to display. SLPOUT command must be input before this command. After SLPOUT command, DISON command is waited until "display possible state" and this command is executed after wait time set by PWRCTL command.

7.3.32 DISOFF (Display Off: 11h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	0	1	0	0	0	1	11	Command DISOFF
1	0	1	0	0	1	0	1	A5	Parameter 1(P1) Dummy

Display OFF. Following (Fig. 42) display off sequence is executed after the command input.

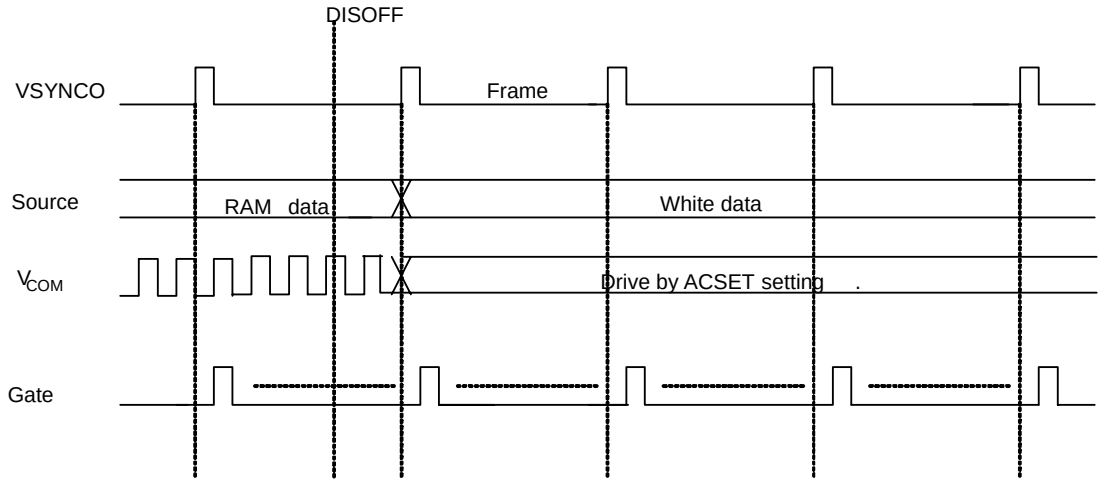


Fig 42 DISOFF timing chart

White display state (in case of normally white) is kept after next frame that input DISOFF command. If DISON command is input in this state, display starts from next frame. Source output voltage during white display state is fixed to V_0 and V_{15}. AC drive mode is that set by P14 to 15 of 7.3.14 ACSET command at this white display state.

7.3.33 WRRAM (Write RAM: 3A h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	1	1	1	0	1	0	3A	Command WRRAM
1	0	1	0	0	1	0	1	A5	Parameter 1(P1) dummy
*	*	*	*	*	*	*	*	*	Write data to Display RAM

After this WRRAM command, data is input at display area which is set by CASET and PASET command. RAM address is incremented automatically by $\overline{WR}$ signal.

Column address, page address and frame address are set to start addresses by WRRAM command input. There is no limit to input data, and it is continued to be written until next command input. When the address arrives to end address, it is return to start address.

During BLKFIL command, data writing by WRRAM command is cancelled.

7.3.34 RDRAM (Read Ram: 39h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	1	1	1	0	0	1	39	Command RDRAM
1	0	1	0	0	1	0	1	A5	Parameter 1(P1) Dummy
*	*	*	*	*	*	*	*	*	Dummy read data
*	*	*	*	*	*	*	*	*	Read data from Display RAM

After this RDRAM command, data is read at display area which is set by CASET and PASET command. RAM address is incremented automatically by $\overline{RD}$ signal.

Column address, page address and frame address are set to start addresses by RDRAM command input. There is no limit to read data, and it is continued to be read until next command input. When the address arrives to end address, it is return to start address.

During BLKFIL command, data reading by RDRAM command is cancelled.

7.3.35 PTLSET1 (Partial Set 1: 29h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	1	0	1	0	0	1	29	Command PTLSET1
0	0	0	0	0	0	0	P10	—	Parameter 1(P1) 1st partial display start line (MSB)
P27	P26	P25	P24	P23	P22	P21	P20	—	Parameter 2(P2) 1st partial display start line (LSB)
0	0	0	0	0	0	0	P30	—	Parameter 3(P3) 1st partial display end line (MSB)
P47	P46	P45	P44	P43	P42	P41	P40	—	Parameter 4(P4) 1st partial display end line (LSB)

It is used to display partially (line divided) in order to reduce power consumption.

2 display areas are settable. It is used with PTLSET2 and PTLSET3 command.

2 partial display areas are set within display lines set P1 and P2 of DISAR command. When 2nd area is not used, the start line and end line of the 2nd area must be set 511.

Panel		Setting
1st line	→	0
2nd line	→	1
3rd line	→	2
4th line	→	3
. . .		. . .
319th line	→	318
320th line	→	319

Parameter 1
Parameter 2: 1st partial display start line is set by above table.
Example) Set 1st partial display start line: 0
Set 4th partial display start line: 3

Parameter 3
Parameter 4: 1st partial display end line is set by above table. Following condition must be satisfied.
1st partial display start line < 1st partial display end line.

Example) Set 15th partial display start line: 14

Note: When interlace is set, 1st partial display end line and 2nd partial display end line must not be set to 0, 1 and 2.

7.3.36 PTLSET2 (Partial Set 2: 2A h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	1	0	1	0	1	0	2A	Command PTLSET2
0	0	0	0	0	0	0	P10	—	Parameter 1(P1) 2nd partial display start line (MSB)
P27	P26	P25	P24	P23	P22	P21	P20	—	Parameter 2(P2) 2nd partial display start line (LSB)
0	0	0	0	0	0	0	P30	—	Parameter 3(P3) 2nd partial display end line (MSB)
P47	P46	P45	P44	P43	P42	P41	P40	—	Parameter 4(P4) 2nd partial display end line (LSB)

It is used to display partially (line divided) in order to reduce power consumption.
2 display areas are settable. It is used with PTLSET1 and PTLSET3 command.
Refer to PTLSET1 command how to use PTLSET2.

Parameter 1
Parameter 2: 2nd partial display start line is set

Example) Set 300th partial display start line: 299

Parameter 3
Parameter 4: 2nd partial display end line is set. Following condition must be satisfied.

2nd partial display start line < 2nd partial display end line.

Example) Set 320th partial display end line: 319

Note: When interlace is set, 1st partial display end line and 2nd partial display end line must not be set to 0, 1 and 2.

7.3.37 PTLSET3 (Partial Set 3: AB h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	1	0	1	0	1	1	AB	Command PTLSET3
0	P16	P15	P14	P13	P12	P11	P10	—	Parameter 1(P1) Refresh rate of non-display area
0	0	0	0	0	P22	P21	P20	—	Parameter 2(P2) Return time of booster clock frequency.
0	0	0	0	0	0	P31	P30	—	Parameter 3(P3) AC drive setting during non-display area.
1	0	1	0	0	1	0	1	A5	Parameter 4(P4) Dummy

It is used to display partially (line devided) in order to reduce power consumption.
2 display areas are settable. It is used with PTLSET1 and PTLSET2 command.

Parameter 1: set refresh rate of non-display area.
P16 to 10: set refresh frame frequency of partial non-display area to 1/N of frame frequency of display area. Source and VCOM voltages during not refresh are set by P3.

0000000 : 1
0000001 : 1 / 3
0000010 : 1 / 5
0000011 : 1 / 7
• •
1111110 : 1 / 253
1111111 : 1 / 255

Parameter 2: set return time of booster clock frequency.
P22 to P20: set return time of booster clock frequency to normal mode setting by number of 1H period before.

000 : 0 H
001 : 1 H
010 : 2 H
• •
111 : 7 H

Parameter 3: set drive method during non-display area.
P31 to P30: set source and VCOM output at non-refresh non-display area.

P31	P30	Source output	VCOM
0	0	Hi-Z	Hi-Z
0	1	Vss	Vss
1	*	Hi-Z	Normal driving

7.3.38 PTLIN (Partial In: 19h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	0	1	1	0	0	1	19	Command PTLIN
1	0	1	0	0	1	0	1	A5	Parameter 1(P1) Dummy

It is used to display partially (line devided) in order to reduce power consumption.
Shift to partial display mode based on setting PTLSET1, 2 and 3.
It is enable at next frame after this command input.

7.3.39 PTLOUT (Partial Out: 1A h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	0	1	1	0	1	0	1A	Command PTLOUT
1	0	1	0	0	1	0	1	A5	Parameter 1(P1) Dummy

Exit from partial display state. It is enable at next frame after this command input.

7.3.40 BLSET (Blinking Set：2Bh)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	1	0	1	0	1	1	2B	Command BLSET
P17	P16	P15	P14	P13	P12	P11	P10	—	Parameter 1(P1) blinking cycle
0	0	0	0	P23	P22	P21	P20	—	Parameter 2(P2) frame address selection at 1bpp mode.
1	0	1	0	0	1	0	1	A5	Parameter 3(P3) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 4(P4) Dummy

This command is used to blink display to exchange frame RAMs.

The blinking is fixed between 1st and 2nd frame addresses in 4bpp mode (160 lines or less are used) or 2bpp mode, and blinking is set by parameter 2 in 1bpp mode. It is enable in next frame of the command input.

Parameter 1: set blinking period.

P17 to P10: set blinking period by frame unit.

0000_0000 : 2 frame
0000_0001 : 2 frame
0000_0010 : 4 frame
0000_0011 : 4 frame
0000_0100 : 6 frame
0000_0101 : 6 frame
• •
1111_1010 : 252 frame
1111_1011 : 252 frame
1111_1100 : 254 frame
1111_1101 : 254 frame
1111_1110 : 256 frame
1111_1111 : 256 frame

Parameter 2: Select frame addresses.

P23 to P20: Select blinking frame addresses. If invalid frame address is selected, it is return to initial value in 4bpp and 2bpp mode.

P23, P22: 1st frame (start frame)
P21, P20: 2nd frame
00 : frame address 0
01 : frame address 1
10 : frame address 2
11 : frame address 3

7.3.41 BLIN (Blinking In: 1Bh)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	0	1	1	0	1	1	1B	Command BLIN
1	0	1	0	0	1	0	1	A5	Parameter 1(P1) Dummy

This command is used for blinking display by changing frame address. The blinking state is set by BLSET command. It is enable in next frame of the command input.

During executing this command, RAM writing is invalid. However when1bpp mode with 4frames, other frames that is used by this command are valid to write RAM.

7.3.42 BLOUT (Blinking Out: 1C h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	0	1	1	1	0	0	1C	Command BLOUT
1	0	1	0	0	1	0	1	A5	Parameter 1(P1) Dummy

Exit blinking display state. Frame address after exit is address set by 7.3.10 STFRAME command. It is enable at frame changing of blinking cycle after the command.

When WRRAM or RDRAM command is input after BLOUT, 2 NOP commands must be required before WRRAM or RDRAM.

7.3.43 BLKFIL(Block Fill: 31h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	1	1	0	0	0	1	31	Command BLKFIL
0	0	0	0	P13	P12	P11	P10	—	Parameter 1(P1) Data
1	0	1	0	0	1	0	1	A5	Parameter 2(P2) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 3(P3) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 4(P4) Dummy

Write set data to display data RAM area which set by CASET and PASET command.

60ms wait time is required after BLKFIL command input. R23 of RDSTAT command is available to confirm display data RAM writing by BLKFIL command or not. During this term, prohibit DISAR, CASET, PASET, BPPSEL, WRRAM and RDRAM commands.

When WRRAM or RDRAM command is input after BLKFIL, two NOP commands are required before WRRAM, RDRAM.

Parameter 1:

P13 to P10: set data to write display data RAM.
Data is different by data format by BPPSEL.

Setting				Data to write pointed rectangle area		
P13	P12	P11	P10	4bit	2bit	1bit
0	0	0	0	0000	00	0
0	0	0	1	0001	01	1
0	0	1	0	0010	10	(0)
0	0	1	1	0011	11	(1)
0	1	0	0	0100	(00)	(0)
0	1	0	1	0101	(01)	(1)
0	1	1	0	0110	(10)	(0)
0	1	1	1	0111	(11)	(1)
1	0	0	0	1000	(00)	(0)
1	0	0	1	1001	(01)	(1)
1	0	1	0	1010	(10)	(0)
1	0	1	1	1011	(11)	(1)
1	1	0	0	1100	(00)	(0)
1	1	0	1	1101	(01)	(1)
1	1	1	0	1110	(10)	(0)
1	1	1	1	1111	(11)	(1)

7.3.44 VCMDAT (V_{COMH} Offset Data: 49h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	0	0	1	0	0	1	49	Command VCMDAT
0	0	0	0	P13	P12	P11	P10	—	Parameter 1(P1) Select V_{COMH} offset data from.
P27	P26	P25	P24	P23	P22	P21	P20	—	Parameter 2(P2) V_{COMH} offset data 1
P37	P36	P35	P34	P33	P32	P31	P30	—	Parameter 3(P3) V_{COMH} offset data 2
1	0	1	0	0	1	0	1	A5	Parameter 4(P4) Dummy

Set V_{COMH} offset data is imported from by P1. P2 and P3 are set V_{COMH} offset data to Multi Time PROM or EEPROM (Refer to Table 41). Refer to 6.6.7 to offset adjustment of V_{COMH} output voltage.

Parameter 1:

P13 to P10: Set V_{COMH} offset data is imported from.

P13	P12	P11	P10	VCOMH offset data is imported from
0	*	*	*	No offset adjustment
1	0	1	0	External EEPROM VCOMH offset data 1
1	0	1	1	External EEPROM VCOMH offset data 2
1	1	*	0	This command (V_{COMH} offset data 1)
1	1	*	1	This command (V_{COMH} offset data 2)
1	0	0	*	Prohibited

Note: When external EEPROM is refered, set NVSEL=HIGH.

Parameter 2: Set V_{COMH} offset data 1 to write Multi Time PROM or EEPROM.

Parameter 3: Set V_{COMH} offset data 2 to write Multi Time PROM or EEPROM.

Table 38 VCOMH offset data format (Complement of 2)

Offset	Parameter 2, 3 value
-127	1000_0001
-126	1000_0010
•••	•••
-1	1111_1111
0	0000_0000
+1	0000_0001
•••	•••
+126	0111_1110
+127	0111_1111

7.3.45 UIDSET (User ID Set: 4Ah)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	0	0	1	0	1	0	4A	Command UIDSET
P17	P16	P15	P14	P13	P12	P11	P10	—	Parameter 1(P1)Multi Time PROM/EEPROM write ID1-1 data
P27	P26	P25	P24	P23	P22	P21	P20	—	Parameter 2(P2)Multi Time PROM/EEPROM write ID1-2 data
P37	P36	P35	P34	P33	P32	P31	P30	—	Parameter 3(P3)Multi Time PROM/EEPROM write ID2-1 data
P47	P46	P45	P44	P43	P42	P41	P40	—	Parameter 4(P4)Multi Time PROM/EEPROM write ID2-2 data

Set user ID data to write Multi Time PROM

Parameter 1:

P17 to P10: User ID1-1 data to write Multi Time PROM or EEPROM

Parameter 2:

P27 to P20: User ID1-2 data to write Multi Time PROM or EEPROM

Parameter 3:

P37 to P30: User ID2-1 data to write Multi Time PROM or EEPROM

Parameter 4:

P47 to P40: User ID2-2 data to write Multi Time PROM or EEPROM

7.3.46 MTPERS (Multi Time PROM Erase: 41h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	0	0	0	0	0	1	41	Command MTPERS
0	0	0	0	0	0	P11	P10	—	Parameter 1(P1)Multi Time PROM erase area
1	0	1	0	0	1	0	1	A5	Parameter 2(P2) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 3(P3) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 4(P4) Dummy

This command erases built-in Multi time PROM.

This command is required internal clock, therefore when OSCIEN=HIGH, external clock must be input to OSCI pin before executing this command. This command is prohibited during 350us from release reset (hardware reset + SWRESET or only SWRESET) and during sleep out.

MTPERS and MTPPGR are also prohibited during Multi time PROM erase sequence.

Parameter 1:

P11 to P10: set erase area of the Multi time PROM. When all area is erased, P11 must be set 1.

P11	P10	Multi Time PROM Erase
0	0	VCOMH offset value 1 VCOMH offset value 2 User D1-1 User ID1-2
0	1	User ID2-1 User ID2-2
1	*	VCOMH offset value 1 VCOMH offset value 2 User ID1-1 User ID1-2 User ID2-1 User ID2-2

7.3.47 MTPPRG (Multi Time PROM Program; 42h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	0	0	0	0	1	0	42	Command MTPPGR
0	0	P15	P14	P13	P12	P11	P10	—	Parameter 1(P1)Multi Time PROM program data select
1	0	1	0	0	1	0	1	A5	Parameter 2(P2) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 3(P3) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 4(P4) Dummy

VCOMH offset data 1, 2 by VCMDAT and user ID data by UIDSET are programmed to Multi time PROM.

Programming data can be selected by Parameter 1, however the programming area must be erased.

This command is required internal clock, therefore when OSCIEN=HIGH, external clock must be input to OSCI pin before executing this command. This command is prohibited during 350us from release reset (hardware reset + SWRESET or only SWRESET) and during sleep out.

MTPERS and MTPPGR are also prohibited during Multi time PROM programming sequence.

Parameter 1:

P15 to P10: Programming data selection.

Parameter	Multi Time PROM programming data
P15	VCOMH offset value 1
P14	VCOMH offset value 2
P13	User ID1-1
P12	User ID1-2
P11	User ID2-1
P10	User ID2-2

7.3.48 MTPOP (Multi Time PROM Operation: 43h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	0	0	0	0	1	1	43	Command MTPOP
1	0	1	0	0	1	0	1	A5	Parameter 1(P1) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 2(P2) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 3(P3) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 4(P4) Dummy

This command is for Multi time PROM control.

This command is required internal clock, therefore when OSCIEN=HIGH, external clock must be input to OSCI pin before executing this command. This command is prohibited during 350us from release reset(hardware reset + SWRESET or SWRESET) and during sleep out. Refer to fig 26 and fig 27 in section 6. 10.

7.3.49 EPRMIN (EEPROM Mode IN: 45h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	0	0	0	1	0	1	45	Command EPRMIN
0	0	0	0	0	P12	P11	P10	–	Parameter 1(P1) EEPROM writing method select
P27	P26	P25	P24	P23	P22	P21	P20	–	Parameter 2(P2) EEPROM start address write date
1	0	1	0	0	1	0	1	A5	Parameter 3(P3) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 4(P4) Dummy

EEPROM writing method selection. Refer to 6.11.3 EEPROM writng timing chart.

This command is valid only when NVSEL=HIGH.

This command must be executed during Sleep in period which is after 350us after release reset(hardware reset + SWRESET or SWRESET) and during sleep out.

This command is invalid when NVSEL=LOW or during sleep out.

During writing EEPROM, no command can be input except RDSTAT and NOP.

EPRMIN command can operate only during EEPROM write protect bits = 00b.

During writing EEPROM by EPRMIN command, other command can be prohibited except RDSTAT and NOP.

If other command is input, XE2WP pin becomes LOW, and writing to EEPROM is disabled or contents of EEPROM may break.

Parameter 1:

P12 to P10: Programming data selection.

P12	P11	P10	EEPROM mode select	EEPROM capacity		
				1k	2k	4k
0	0	0	Writing thru S1D19600 *1 *2	Y	Y	Y
0	0	1	MPU direct writing *1	Y	Y	Y
0	1	0	S1D19600 auto writing (000 to 04Eh)	Y	Y	Y
0	1	1	S1D19600 auto writing (080 to 0CEh) *3	N	Y	Y
1	0	0	S1D19600 auto writing (100 to 14Eh) *3	N	N	Y
1	0	1	S1D19600 auto writing (180 to 1CEh) *3	N	N	Y
1	1	0	S1D19600 auto writing (Write P2 to 000h)	Y	Y	Y
1	1	1	invalid	-	-	-

*1: EEPROM address setting must be set by MPU side. , therefore Input signals from MPU are transferred to EEPROM directly or indirectly. If an address setting does not correspond to actual EEPROM, a data in unwilling address maybe destroyed.

*2: It is operable after 150us from command input. At this moment D2 pin change from Hi-Z to output, therefore take care bus contention.

*3: Choose setting correspond to actual EEPROM. If an address setting does not correspond to actual EEPROM, a data in unwilling address maybe destroyed.

Parameter 2: EEPROM start address write data.

P27 to P20: Set data to write to address 000h. Refer to table 37 “EEPROM start address data” about start address specification.

7.3.50 EPRWRSR (EEPROM Write Status Register: 46h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	0	0	0	1	1	0	46	Command EPRWRSR
P17	P16	P15	P14	P13	P12	P11	P10	P17	Parameter 1(P1) EEPROM status register write data
1	0	1	0	0	1	0	1	A5	Parameter 2(P2) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 3(P3) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 4(P4) Dummy

This command write P1 to status register of EEPROM.

It is valid only when NVSEL=HIGH.

This command must be executed during Sleep in period which is after 350us after release reset (hardware reset + SWRESET or SWRESET) and during sleep out.

This command is invalid when NVSEL=LOW or during sleep out.

During writing EEPROM, no command can be input except RDSTAT and NOP.

During writing EEPROM by EPRMIN command, other command can be prohibited except RDSTAT and NOP.

If other command is input, XE2WP pin becomes LOW, and writing to EEPROM is disabled or contents of EEPROM may break.

7.3.51 RDVCMDAT (Read VCOM Data: 59h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	0	1	1	0	0	1	59	Command RDVCMDAT
1	0	1	0	0	1	0	1	A5	Parameter 1(P1) Dummy
R17	R16	R15	R14	R13	R12	R11	R10	–	Read data 1 (R1) VCOMH offset value 1 (Multi Time PROM)
R27	R26	R25	R24	R23	R22	R21	R20	–	Read data 2(R2) VCOMH offset value 2 (Multi Time PROM)
R37	R36	R35	R34	R33	R32	R31	R30	–	Read data 3 (R3) VCOMH offset value 1 (EEPROM)
R47	R46	R45	R44	R43	R42	R41	R40	–	Read data 4 (R4) VCOMH offset value 2 (EEPROM)
R57	R56	R55	R54	R53	R52	R51	R50	–	Read data 5 (R5) VCOMH offset value 1 (VCMDAT register)
R67	R66	R65	R64	R63	R62	R61	R60	–	Read data 6 (R6) VCOMH offset value 2 (VCMDAT register)
R77	R76	R75	R74	R73	R72	R71	R70	–	Read data 7 (R7) VCOMH Electric volume
0	0	0	0	R83	R82	R81	R80	–	Read data 7 (R7) VCOMH offset data reference point

This command reads following VCOMH values.
If this command is input before writing Multi time PROM and EEPROM, each registers return 00h.
And if this command is input before inputting VCMDAT command, VCMDAT register return 00h.
This command must be executed after 5ms from release reset.

Read data 1: Read VCOMH offset value 1 in built-in Multi time PROM.
Read data 2: Read VCOMH offset value 2 in built-in Multi time PROM.
Read data 3: Read VCOMH offset value 1 in external EEPROM.
Read data 4: Read VCOMH offset value 2 in external EEPROM.
Read data 5: Read VCOMH offset value 1 written by parameter 2 of VCMDAT command.
Read data 6: Read VCOMH offset value 2 written by parameter 3 of VCMDAT command.
Read data 7: Read value added VCOMH electric volume value by EVSET1 command and offset value by VCMDAT command.
Read data 8: VCOMH electric volume offset data reference point.

R83	R82	R81	R80	VCOMH offset data reference point.
0	*	*	*	No offset
1	0	1	0	External EEPROM offset data 1 *1
1	0	1	1	External EEPROM offset data 2 *1
1	1	*	0	VCOMH offset data 1 of VCMDAT
1	1	*	1	VCOMH offset data2 of VCMDAT
Other values				Abnormal reference point

*: 0 or 1

7.3.52 RDUID (Read User ID: 55h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	0	1	0	1	0	1	55	Command RDUID
1	0	1	0	0	1	0	1	A5	Parameter 1 (P1) dummy
R17	R16	R15	R14	R13	R12	R11	R10	–	Read data 1 (R1) User ID1-1 (Multi Time PROM)
R27	R26	R25	R24	R23	R22	R21	R20	–	Read data 2 (R2) User ID1-2 (Multi Time PROM)
R37	R36	R35	R34	R33	R32	R31	R30	–	Read data 3 (R3) User ID2-1 (Multi Time PROM)
R47	R46	R45	R44	R43	R42	R41	R40	–	Read data 4 (R4) User ID2-2 (Multi Time PROM)
R57	R56	R55	R54	R53	R52	R51	R50	–	Read data 5 (R5) User ID1-1 (EEPROM)
R67	R66	R65	R64	R63	R62	R61	R60	–	Read data 6 (R6) User ID1-2 (EEPROM)
R77	R76	R75	R74	R73	R72	R71	R70	–	Read data 7 (R7) User ID2-1 (EEPROM)
R87	R86	R85	R84	R83	R82	R81	R80	–	Read data 8 (R8) User ID2-2 (EEPROM)
R97	R96	R95	R94	R93	R92	R91	R90	–	Read data 9 (R9) User ID1-1 (UIDSET register)
RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	–	Read data A (RA) User ID1-2 (UIDSET register)
RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	–	Read data B (RB) User ID2-1 (UIDSET register)
RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	–	Read data C (RC) User ID2-2 (UIDSET register)

This command read following user IDs.

When the command is input before reading Multi-time PROM and EEPROM, these IDs is read as 00h. When RDUID command is input before UIDSET command, UIDSET register is read as 00h. This command must be executed after 5ms from release reset.

Read data 1: Read User ID1-1 in built-in Multi time PROM.
Read data 2: Read User ID1-2 in built-in Multi time PROM.
Read data 3: Read User ID2-1 in built-in Multi time PROM.
Read data 4: Read User ID2-2 in built-in Multi time PROM.
Read data 5: Read User ID1-1 in external EEPROM.
Read data 6: Read User ID1-2 in external EEPROM.
Read data 7: Read User ID2-1 in external EEPROM。
Read data 8: Read User ID2-2 in external EEPROM.
Read data 9: Read User ID1-1 written by parameter 1 of UIDSET command.
Read data A: Read User ID1-2 written by parameter 2 of UIDSET command.
Read data B: Read User ID2-1 written by parameter 3 of UIDSET command.
Read data C: Read User ID2-2 written by parameter 4 of UIDSET command.

7.3.53 REFCYC (Refresh Cycle: B1h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	0	1	1	0	0	0	1	B1	Command REFCYC
0	0	0	0	0	0	P11	P10	—	Parameter 1(P1) Refresh cycle
1	0	1	0	0	1	0	1	A5	Parameter 2(P2) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 3(P3) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 4(P4) Dummy

Set refresh cycle to re-write from external EEPROM. When NVSEL=HIGH, this command is valid.

Parameter 1:

P11 to P10: Refresh cycle

P11	P10	Refresh cycle
0	0	16 frame
0	1	32 frame
1	0	48 frame
1	1	64 frame

7.3.54 EPRRDADR (EEPROM Read Address: 4Bh)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	0	0	1	0	1	1	4B	Command EPRRDADR
0	0	0	0	0	0	P11	P10	—	Parameter 1(P1) EEPROM read area
1	0	1	0	0	1	0	1	A5	Parameter 2(P2) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 3(P3) Dummy
1	0	1	0	0	1	0	1	A5	Parameter 4(P4) Dummy

P11 to P10: set EEPROM refresh read address. The boot read address is set to “000 to 04Eh” after reset. However refresh read address is set by this parameter. This command refer to data of start address, and when these area is active, read normally, and when these areas are inactive, read address of 000 to 04Eh. Additionally, when 000 to 04Eh area is also inactive, even if NVSEL=HIGH, EEPROM automated read function is inactive and CPU must set commands.

P11	P10	EEPROM read area
0	0	000 to 04Eh
0	1	080 to 0CEh
1	0	100 to 14Eh
1	1	180 to 1CEh

7.3.55 RDERR (Read Error Status: 51h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	0	1	0	0	0	1	51	Command RDERR
1	0	1	0	0	1	0	1	A5	Parameter 1(P1) Dummy
0	0	0	R14	R13	R12	R11	R10	—	Status 1(R1)
R27	R26	R25	R24	R23	R22	R21	R20	—	Status 2 (R2)

Read error factor when ERR pin outputs HIGH.

Status 1(R1):

R10: 0 Display data RAM normal
1 Display data RAM abnormal

R11: 0 DISAR or DISSET1 or DISSET2 command is normal
1 DISAR or DISSET1 or DISSET2 command is abnormal

R12: 0 logic state machine Normal
1 logic state machine Abnormal

R13: 0 Power circuit Normal
1 Power circuit Abnormal (Always 0 during Sleep in or Power off sequence)

R14: 0 Display data RAM address setting Normal
1 Display data RAM address setting Abnormal (If write start address of CASET, PASET is out of RAM effective range or over write end address, WRRAM and BLKFIL commands are invalid. In that case, RDRAM command returns 00h.

When R10=1, re-write Display RAM
When R11=1, re-write DISAR, DISSET1, DISSET2
When R12=1, set all commands after reset.
When R13=1, it is indicated that internal power supply circuits does not operate correctly.
When R14=1, re-write PASET and CASET commands.

Status 2 (R2):

Number of frames which occur display data RAM abnormal. The value is reset after RDERR command, and when the sum reach to 255, the value stops at 255.

7.3.56 RDSTAT (Read Status: 52h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	0	1	0	0	1	0	52	Command RDSTAT
1	0	1	0	0	1	0	1	A5	Parameter 1(P1) Dummy
R17	R16	R15	0	R13	R12	R11	R10	–	Status 1 (R1) Display
0	R26	R25	R24	R23	R22	R21	R20	–	Status 2 (R2) RAM
R37	R36	R35	R34	R33	R32	R31	R30	–	Status 3 (R3) RAM (Start page mask register)
R47	R46	R45	R44	R43	R42	R41	R40	–	Status 4 (R4) RAM (End page mask register)
0	0	0	0	0	R52	R51	R50	–	Status 5 (R5) EEPROM
0	P66	R65	R64	0	R62	R61	R60	–	Status 6 (R6) EEPROM

Read internal status.

Status1(R1):
- R10: 0 DISON
  1 DISOF
- R11: 0 SLPIN
  1 SLPOUT (Include power on sequence and not include power off sequence.)
- R12: 0 PTLOUT
  1 PTLIN
- R13: 0 DINVOUT (Release display invert function)
  1 DINVIN (Display invert)
- R17-R15: Display data format setting

R17	R16	R15	Data format
0	0	1	4bpp (bit / pixel)
0	1	0	2bpp (bit/pixel)
1	0	0	1bpp (bit/pixel)

Status 2 (R2) :
- R20: 0 Page address normal
  1 Page address reverse
- R21: 0 Column address normal
  1 Column address reverse
- R22: 0 Scan direction: Column
  1 Scan direction: Page
- R23: 0 BLKFIL command not executed
  1 BLKFIL command executed (WRRAM, RDRAM commands are cancelled)
- R24: 0 BLOUT state (not blinking)
  1 BLIN state (Blinking. If frame address of PASET is matched to indicated frame address of blinking frameaddress 1 or 2, WRRAM command input is cancelled.)
- R26 to R25; Bit peration of tart page and end page

R26	R25	Bit operation
0	1	AND
1	0	OR
Others		No bit operation

Status 3 (R3): Mask data of writing start page.

Status 4 (R4): Mask data of writing end page.

Status 5 (R5):
- R50: 0 EEPROM reading stop
  1 EEPROM reading (EEPROM Read in progress)

R51: 0 EEPROM writing stop
1 EEPROM writing (EEPROM Write in progress)
R52: 0 EEPROM access stopping
1 EEPROM accessing (EEPROM sequence in progress)

Status 6 (R6):

R62 to R60: EEPROM access area

R62	R61	R60	EEPROM automatic read status
0	0	0	Non access
0	0	1	EEPROM address 001 to 04Eh area
0	1	0	EEPROM address 081 to 0CEh area
0	1	1	EEPROM address 101 to 14Eh area
1	0	0	EEPROM address 181 to 1CEh area
1	0	1	EEPROM status register

R66 to R64: EEPROM access end code

R66	R65	R64	End code
0	0	0	EEPROM access not yet, or during access
0	0	1	Read Success
0	1	0	Write Success
1	0	0	Read Error
1	0	1	Write Error
1	1	1	EEPROM I/F operation abnormal
Others			invalid

7.3.57 RDREV (Read Revision: 53h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	0	1	0	0	1	1	53	Command RDREV
1	0	1	0	0	1	0	1	A5	Parameter 1(P1) Dummy
R17	R16	R15	R14	R13	R12	R11	R10	—	Read data 1(R1) IC revision
0	0	R25	R24	R23	R22	R21	R20	—	Read data 2(R2) Lot number (MSB)
R37	R36	R35	R34	R33	R32	R31	R30	—	Read data 3(R3) Lot number (LSB)

Read revision and Lot number

Read data 1(R1): Read revision of this IC.

Read data 2(R2):
Read data 3(R3): Read Lot number of this IC.

7.3.58 RDCRC (Read CRC: 54h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	1	0	1	0	1	0	0	54	Command RDCRC
1	0	1	0	0	1	0	1	A5	Parameter 1(P1) Dummy
R17	R16	R15	R14	R13	R12	R11	R10	—	Read data 1(R1) CRC value (MSB)
R27	R26	R25	R24	R23	R22	R21	R20	—	Read data 2(R2) CRC value (LSB)

This command reads CRC calculation result of all input data (include command, parameter, NOP, invalid code). This command is input after transferring input data, then CRC calculation result can be read. It is included this command code and parameter. To compare the result and expected value on MPU side, it is possible to confirm the data transfer was right or not. The CRC value is initialized by reset (Hardware reset and software reset). And The CRC value initialized after executed this command and restart CRC calculation. The initial value is FFFFh.

Status 1 (R1): CRC MSB 8 bit
Status 2 (R2): CRC LSB 8 bit

CRC calculation
Polynomial: $X^{16} + X^{12} + X^5 + 1$
Parity length: 16 bits

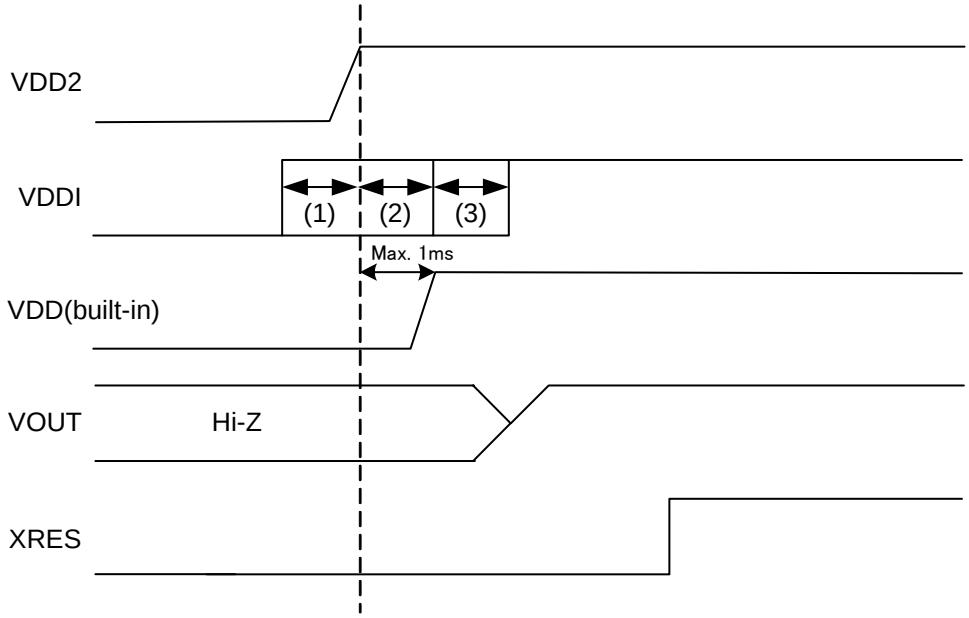
7.3.59 NOP (Non Operation: 00h)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
0	0	0	0	0	0	0	0	00	Command NOP

Non-operation. This command does not affect any operation.

8. Instruction Setup Example

8.1 Power ON sequence

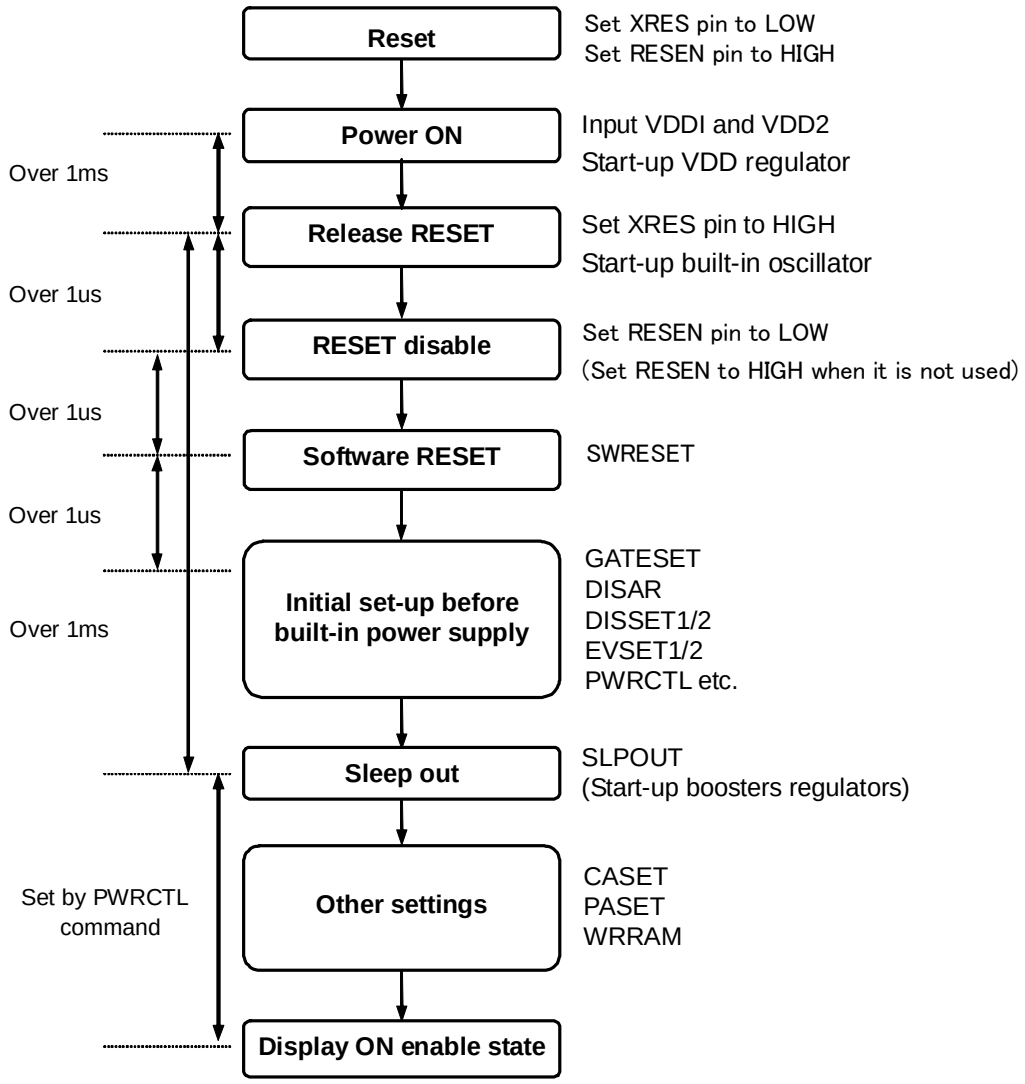


VDDI can be turned on in any time of (1) or (2) or (3).

When external VOUT is input, Vout must be Hi-Z before VDD2 and VDDI are ON, and Vout must be input after 1ms or over after VDD2 and VDDI are ON.

In this time keep VOUT >= VDD2.

8.2 Initial setting to Display ON:

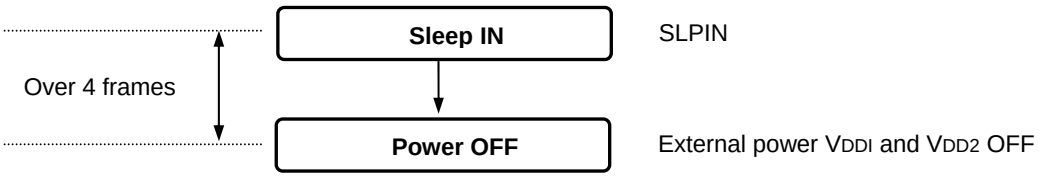


Display is possible any time after the “Display ON enable state”.

If DISON command is input before “Display ON enable state”, the S1D19600 wait to display automatically until “Display ON enable state”

(Refer to SLPOUT command)

8.3 Power off sequence:



In case of restart, execute reset of Power off sequence.

(refer to 7.3.29 SLPIN command about panel discharging and power discharging)

9. ABSOLUTE MAXIMUM RATINGS

Table 42 Absolute Maximum Ratings

V_{SS} = 0V

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{DDI}	-0.3 to +5.8	V
Supply voltage (2)	V_{DD2}	-0.3 to +6.1	
Supply voltage (3)	V_{DD}	-0.3 to +2.5	
Supply voltage (4)	V_{REG}	-0.3 to +3.9	
Supply voltage (5)	VLDO1	-0.3 to +3.4	
Supply voltage (6)	VLDO2	-0.3 to +3.3	
Supply voltage (7)	V_{DDHS}	-0.3 to +6.2	
Supply voltage (8)	V_{DDHS2}	-0.3 to +3.1	
Supply voltage (9)	V_{DDRH}	-0.3 to +6.1	
Supply voltage (10)	V_{OFREG}	-0.3 to +6.1	
Supply voltage (11)	V_{ONREG}	-0.3 to +5.5	
Supply voltage (12)	V_{COMH}	-0.3 to +6.1	
Supply voltage (13)	V_{COML}	-3.5 to +0.6	
Supply voltage (14)	VDCCOM	-0.3 to +4.0	
Supply voltage (15)	V_{OUT}	-0.3 to +7.0	
Supply voltage (16)	V_{OUTM}	-3.5 to +0.3	
Supply voltage (17)	V_{EE}	-17.0 to +0.3	
Supply voltage (18)	V_{DDHG}	-0.3 to 21.0	
Logic input voltage	VLIN	-0.3 to V_{DDI} + 0.3	
Logic output voltage	VLOUT	-0.3 to V_{DDI} + 0.3	
Storage temperature	Tstr	-55 to 125	°C

Notes:

1. Unless otherwise noted, all voltages are specified based on V_{SS}=0V.
2. Substrate voltage is V_{EE}.
3. If the IC exceeds its absolute maximum ratings, it may be damaged. Also, if the IC is operated with the absolute maximum ratings for a long time, its reliability may drop.
4. The absolute maximum rating of the voltage difference between V_{DDHG} to V_{EE} is 34V.
5. The absolute maximum rating of the voltage difference between V_{DCCOM} to V_{OUTM} is 7V.
6. The absolute maximum rating of the voltage difference between V_{OUT} to V_{COML} is 9V.
7. The absolute maximum rating of the voltage difference between V_{COMH} to V_{OUTM} is 9V.

Table 43 operationg temperature

Item	Symbol	Rating	Unit
Operating temperature (1)	ToPN1	-40 to 110	°C
Operating temperature (2)	ToPN2	10 to 40	

Note 1. Operating temperature (1) is normal operating temperature of this IC. It includes Multi-Time-PROM read operation.

Note 2. Operating temperature (2) is programming and erasing operating temperature of the Multi Time PROM.

10. DC CHARACTERISTICS

Table 44 DC Characteristics

V_{SS} = 0 V, V_{DDI} = 2.7 to 5.5 V, V_{DD2} = 2.7 to 5.5 V, T_a = -40 to 110°C

Parameter	Symbol	Condition	Rating			Unit	Applicable pin
			Min.	Typ.	Max.		
Operating voltage(1)	V_{DDI}	External supply	2.7	—	5.5	V	V_{DDI}
Operating voltage(2)	V_{DD2}	External supply	2.7	—	5.5	V	V_{DD2}
Operating voltage (3)	V_{DD}	Built-in power supply	—	1.8	—	V	V_{DD}
Operating voltage (4)	V_{REG}	Built-in power supply	—	3.5	—	V	V_{REG}
Operating voltage (5)	VLDO1	Built-in power supply	—	3.05	—	V	VLDO1
Operating voltage (6)	VLDO2	Built-in power supply	—	2.5 3.0	—	V	VLDO2
Operating voltage (7)	V_{DDHS}	Built-in power supply	4.1	—	5.6	V	V_{DDHS}
Operating voltage (8)	V_{DDHS2}	Built-in power supply	2.05	—	2.8	V	V_{DDHS2}
Operating voltage (9)	V_{DDRH}	Built-in power supply	3.0	—	5.5	V	V_{DDRH}
Operating voltage (10)	V_{OFREG}	Built-in power supply	2.4	—	5.5	V	V_{OFREG}
Operating voltage (11)	V_{ONREG}	Built-in power supply	1.5	—	5.0	V	V_{ONREG}
Operating voltage (12)	V_{COMH}	Built-in power supply	2.46	—	5.5	V	V_{COMH}
Operating voltage (13)	V_{COML}	Built-in power supply	V_{OUTM}+0.3V	—	0.0	V	V_{COML}
Operating voltage (14)	VDCCOM	Built-in power supply	—	3.0	—	V	V_{DCCOM}
		External power supply	2.7	—	3.6		
Operating voltage (15)	V_{OUT}	Built-in power supply / External power supply	4.5	—	6.2	V	V_{OUT}
Operating voltage (16)	V_{OUTM}	Built-in power supply	-3.1	—	0.0	V	V_{OUTM}
Operating voltage (17)	V_{EE}	Built-in power supply	-15.0	—	-5.0	V	V_{EE}
Operating voltage (18)	V_{DDHG}	Built-in power supply	8.0	—	19.0	V	V_{DDHG}
LOW level input voltage	V_{IL}	—	V_{SS}	—	0.2 × V_{DDI}	V	Logic system input pins
HIGH level input voltage	V_{IH}		0.8 × V_{DDI}	—	V_{DDI}		
Hysteresis voltage	V_{IS1}	V_{DDI}=3.3V	0.4	—			*7
	V_{IS2}	V_{DDI}=5.0V	0.5	—			
Input leakage	I_{LI1}	V_{IN} = V_{DDI} or V_{SS}	-1.0	—	1.0	µA	Logic system input pins
Input capacitance	C_{IN}	Ta = 25 °C, f=1 MHz	—	—	25	pF	Logic system input pins
LOW level output voltage	V_{OL1}	I_{OL} = 0.06 mA	V_{SS}	—	V_{SS} + 0.3	V	Logic system input pins
HIGH level output voltage	V_{OH1}	I_{OH} = -0.06 mA	V_{DDI} - 0.3	—	V_{DDI}		
Output voltage deviation	ΔV_S	T_a = 25 °C	—	±10	±20	mV	S1 to S320

V_{SS} = 0 V, V_{DDI} = 2.7 to 5.5 V, V_{DD2} = 2.7 to 5.5 V, Ta=25°C

Parameter	Symbol	Condition	Rating			Unit	Applicable pin
			Min.	Typ.	Max.		
1st boosting ability (Internal impedance)	RV_{OUT1}	VDDI = VDD2 = 3.3V *1	—	50	75	Ω	V_{OUT}
2nd boosting ability (Internal impedance)	RV_{OUT2}		—	60	90	Ω	V_{OUTM}
3rd boosting ability (Internal impedance)	RV_{OUT3}		—	500	750	Ω	V_{EE}
4th boosting ability (Internal impedance)	RV_{OUT4}		—	800	1200	Ω	V_{DDHG}
Static current consumption	IDDIQ	VDDI = VDD2 = 3.3V *2	—	0.1	1.0	μA	V_{DDI}
	IDD2Q		—	70	150	μA	V_{DD2}
Dynamic current consumption 1	IDDI1	VDDI = VDD2 = 3.3V *3 *5	—	0.1	1.0	μA	V_{DDI}
	IDD21		—	6000	9000	μA	V_{DD2}
Dynamic current consumption 2	IDDI2	VDDI = VDD2 = 3.3V *4 *6	—	10	30	μA	V_{DDI}
	IDD22		—	1100	1650	μA	V_{DD2}

V_{SS} = 0 V, V_{DDI} = 2.7 to 5.5 V, V_{DD2} = 2.7 to 5.5 V, Ta = 10 to 40°C

Parameter	Symbol	Condition	Rating			Unit	Applicable pin
			Min.	Typ.	Max.		
Erase voltage	VME1	External power supply	21	22	23	V	VME1
Program voltage	VME2	External power supply	8.2	8.5	8.8	V	VME2
Erase current	IVME1	VME1 = 22V	-	-	3	mV	VME1
Program current	IVME2	VME2 = 8.5V	-	-	6	mV	VME2

*1 Capacitances of 1st and 2nd booster = 2.2uF, Capacitances of 3rd and 4th booster = 1uF, boosting clock frequency = 1H frequency * 1
CPSET1 = CPSET2 = VSS, 3rd booster: x (-2), VOFREG = 4.5V, VONREG = 2.0V

*2 Power consumption with default value of command set after RESET. Input level is V_{DDI} or V_{SS}.

*3 Current during still picture. (No display RAM access)

*4 Current during display RAM access ($\overline{WR}$). (Display is OFF)

*5 After reset, all commands are default value except "SLPOUT, PWRCTL/P1=5Fh, P2=04h, P3=00h, P4=00h, DISON"
RAM data are D0 to D7 = (10101010), (01010101) alternately.
CPSET1 = CPSET2 =VSS

*6 Current consumption when following data are written continuously and alternately with 300ns period.
D7: D0 = (10101010)
D7: D0 = (01010101)

*7 Schmidt trigger applied pins: $\overline{CS}$, A0, $\overline{RD}$, $\overline{WR}$, D0 to D7, SCL, SD, RESEN, TCEN, E2SI

(Notes) 1. Insert bypath capacitance at power pins for noise countermeasure.
2. It is not guaranteed to operate when voltage level are sudden changed.
3. Maximum of "V_{DDHG} – V_{EE}" is 32V.
4. Maximum operation range of "V_{DCCOM} – V_{OUTM}" is 6.2V.
5. Maximum operation range of "V_{OUT} – V_{COML}" is 8.1V.
6. Maximum operation range of "V_{COMH} – V_{OUTM}" is 8.1V.
7. Keep always condition "VDDHS - 0.1V >= V_{DDRH}".
8. Keep always condition of each regulator as following.
V_{OUT} − 0.3V >= VDDHS/V_{DDRH}/V_{OFREG}/V_{ONREG}/V_{COMH}
9. Keep always condition "V_{OUTM} + 0.3V =< V_{COML}"
10. Input level must be V_{DDI} or V_{SS}. Otherwise through current occurs at CMOS input buffer.

11. AC CHARACTERISTICS

11.1 Oscillation Frequency

The following defines clock frequency of built-in oscillator.

Table 41 Oscillation Frequency

V_{SS}=0V, V_{DDI}=2.7 to 5.5V, V_{DD2}=2.7 to 5.5V, T_a=-40 to 110°C

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation frequency	f_{OSC}	When built-in oscillator circuit is used	900	1000	1100	kHz
External clock input frequency	f_{OSCI}	—	900	1000	1100	kHz

*1 : External clock timing are specified based on the 20% and 80% of V_{DDI}
*2 : The rise and fall times (t_r and t_f) of the input signal are specified for less than 10ns.

11.2 Parallel Interface

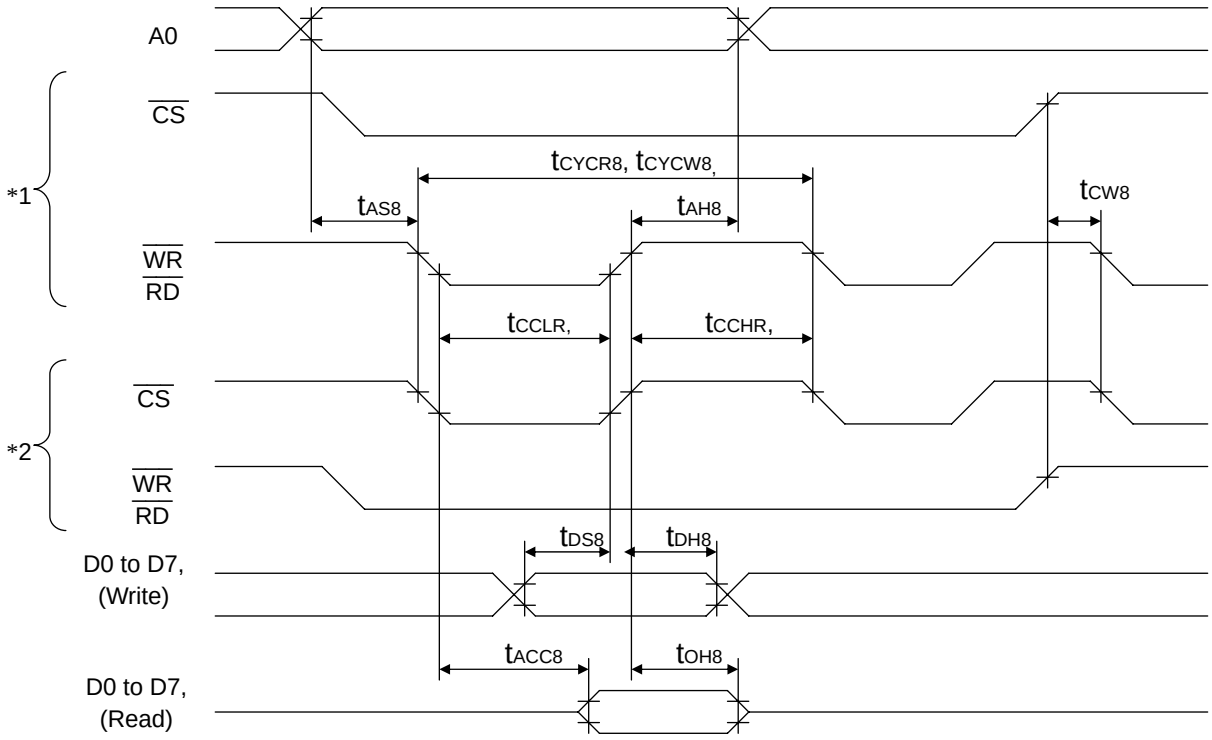


Fig.43 The 8bit parallel interface

*1 If $\overline{CS}$ = LOW and if accessed by $\overline{WR}$ or $\overline{RD}$ signal
*2 If $\overline{WR}$ = $\overline{RD}$ = LOW and if accessed by $\overline{CS}$ signal

V_{SS}=0V, V_{DDI}=2.7 to 5.5V, V_{DD}=1.65 to 1.95V, V_{DD2}=2.7 to 5.5V T_a=-40 to 110°C

Parameter		Symbol	Condition	Min.	Max.	Unit
A0 setup time	Write	t_{ASW3}	—	10	—	ns
	Read	t_{ASR3}	—	10	—	
A0 hold time	Write	t_{AHW3}	—	10	—	
	Read	t_{AHR3}	—	10	—	
Write system cycle time		t_{CYCW3}	—	300	—	
$\overline{WR}$ LOW level pulse width		t_{CCLW3}	—	150	—	
$\overline{WR}$ HIGH level pulse width		t_{CCHW3}	—	100	—	
Read system cycle time		t_{CYCR3}	—	500	—	
$\overline{RD}$ LOW level pulse width		t_{CCLR3}	—	200	—	
$\overline{RD}$ HIGH level pulse width		t_{CCHR3}	—	250	—	
$\overline{CS}$-$\overline{WR}$ time		t_{CWW3}	—	30	—	
$\overline{CS}$-$\overline{RD}$ time		t_{CWR3}	—	30	—	
Data setup time		t_{DS3}	—	20	—	
Data hold time		t_{DH3}	—	20	—	
$\overline{RD}$ access time		t_{ACC3}	CL=50pF	—	250	
Output disable time		t_{OH3}		10	150	

*3 : All timing are specified based on the 20% and 80% of V_{DDI}
*4 : The rise and fall times (t_r and t_f) of the input signal are specified for less than 10ns.

11.3 Serial Interface

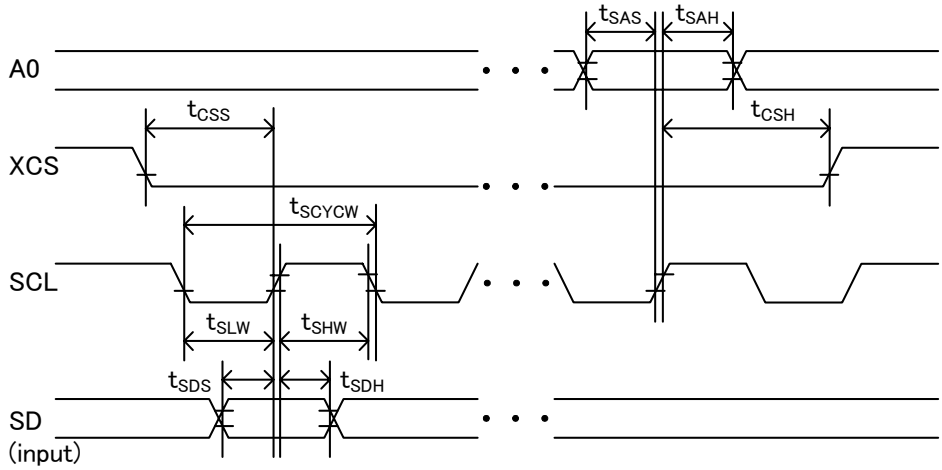


Fig.44 Serial Interface (write operation)

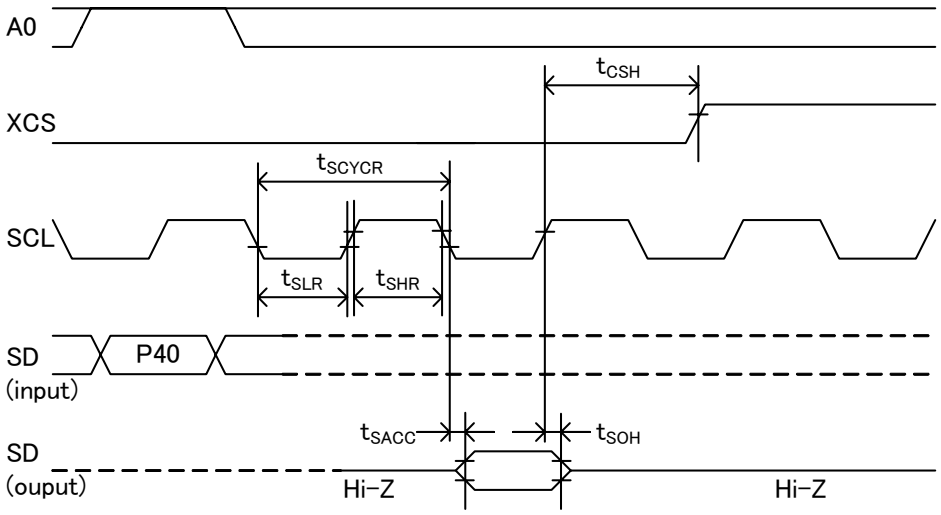


Fig.45 Serial Interface (Read operation)

V_{SS}=0V, V_{DDI}=2.7 to 5.5V, V_{DD}=1.65 to 1.95V, V_{DD2}=2.7 to 5.5V, T_a=-40 to 110°C

Parameter	Symbol	Condition	Min.	Max.	Unit
Write SCL cycle	t_{SCYCW}	—	300	—	ns
Write SCL LOW level pulse width	t_{SLW}	—	100	—	
Write SCL HIGH level pulse width	t_{SHW}	—	100	—	
Data setup time	t_{SDS}	—	20	—	
Data hold time	t_{SDH}	—	20	—	
Read SCL cycle	t_{SCYCR}	—	500	—	
Read SCL LOW level pulse width	t_{SLR}	—	200	—	
Read SCL HIGH level pulse width	t_{SHR}	—	250	—	
$\overline{CS}$ setup time	t_{CSS}	—	10	—	
$\overline{CS}$ hold time	t_{CSH}	—	10	—	
A0 setup time	t_{SAS3}	—	10	—	
A0 hold time	t_{SAH3}	—	10	—	
Read access time	t_{SACC}	CL=50pF	—	250	
Output disable time	t_{SOH}		10	150	

*1 All timings are specified based on the 20% and 80% of V_{DDI}.
*2 The rise and fall times (t_r and t_f) of the input signal are specified for less than 10ns.
*3 During final parameter(P10) of RDSTAT command to Read data XSC signal must be fixed to LOW.

11.4 EEPROM Interface

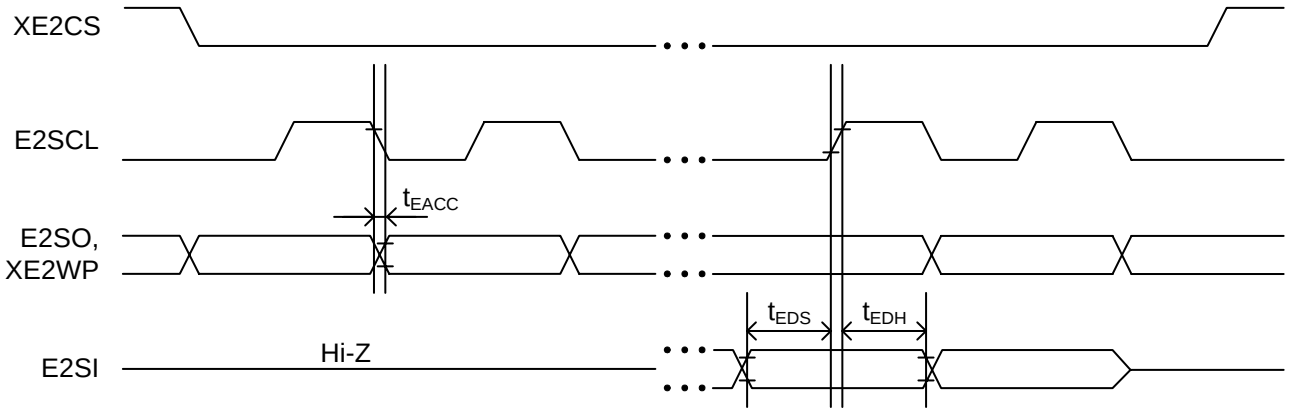


Fig 46 EEPROM interface

VSS =0 V, VDDI = 2.7 to 5.5 V, VDD = 1.65 to 1.95 V, VDD2 = 2.7 to 5.5 V, Ta = -40 to 110 °C

Parameter	Symbol	Condition	Min.	Max.	Unit
Data setup time	tEDS3	–	20	–	ns
Data hold time	tEDH3	–	20	–	
E2SO, XE2WP access time	tEACC3	CL = 50 pF	–	250	

*1 All timings are specified based on the 20% and 80% of V_{DDI}.
*2 The rise and fall times (t_r and t_f) of the input signal are specified for less than 10ns.

11.5 Resetting

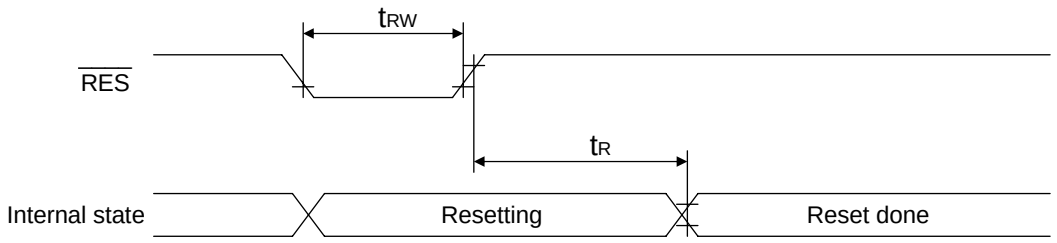


Fig.47 Resetting

V_{SS}=0V, V_{DDI} = 2.7 to 5.5V, V_{DD}=1.65 to 1.95V, V_{DD2}=2.7 to 5.5V, T_a=-40 to 110°C

Parameter	Symbol	Condition	Min.	Max.	Unit
Reset time	t_R	—	—	1	µs
Reset LOW level pulse width	t_{RW}	—	20	—	

*1 All timings are specified based on the 20% and 80% of V_{DDI}.
*2 All timings are specified based on the 20% and 80% of V_{DDI}.
*3 We recommend to hold the $\overline{RES}$ pin to LOW during power-on conditions.
*4 Applied when resetting while the power supply is stabilized.

11.6 ERR Output

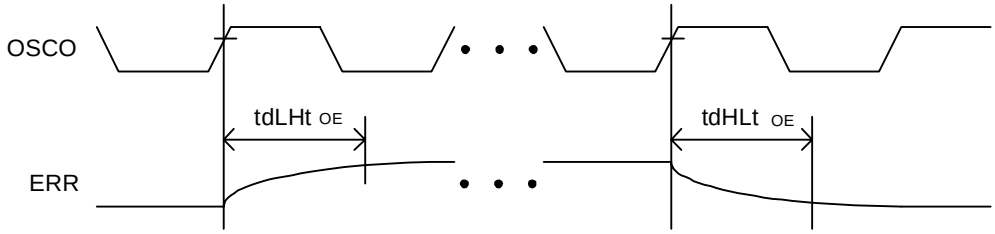


Fig.48 ERRout

V_{SS}=0V, V_{DDI} = 2.7 to 5.5V, T_a=-40 to 110°C

Parameter	Symbol	Condition	Min.	Max.	Unit
Output delay time OSCO to ERR (L→H)	t_{dLHtOE}	CL = 50 pF	—	100	µs
Output delay time OSCO to ERR (H→L)	t_{dHLtOE}	CL = 50 pF	—	100	

*1 Output delay time OSCO to ERR specified based on the 20% and 80% of set value.

11.7 OSCO output

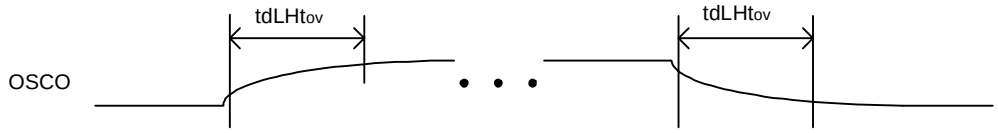


Fig.49 ERR output

V_{SS}=0V, V_{DDI} = 2.7 to 5.5V, T_a=-40 to 110°C

Parameter	Symbol	Condition	Typ.	Max.	Unit
OSCO rising time	tdLHto	CL = 50 pF	—	100	µs
OSCO falling time	tdHLto	CL = 50 pF	—	100	

*1 Output delay time OSCO to ERR specified based on the 20% and 80% of set value.

11.8 VSYNCO output

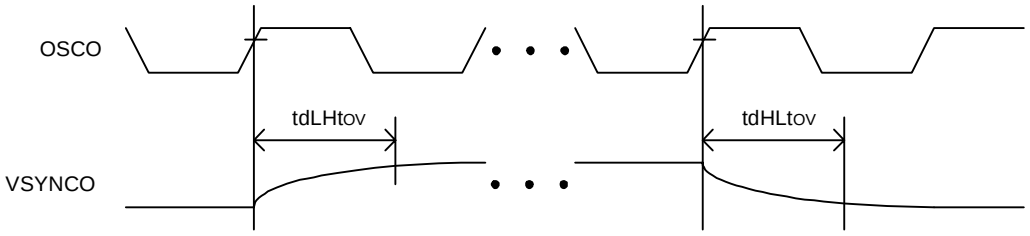


Fig.50 VSYNCO output

V_{SS}=0V, V_{DDI} = 2.7 to 5.5V, T_a=-40 to 110°C

Parameter	Symbol	Condition	Typ.	Max.	Unit
Output delay time OSCO to VSYNCO (L→H)	tdLHtov	CL = 50 pF	—	100	µs
Output delay time OSCO to VSYNCO (H→L)	tdHLtov	CL = 50 pF	—	100	

*1 Output delay time OSCO to ERR specified based on the 20% and 80% of set value.

11.9 Source output

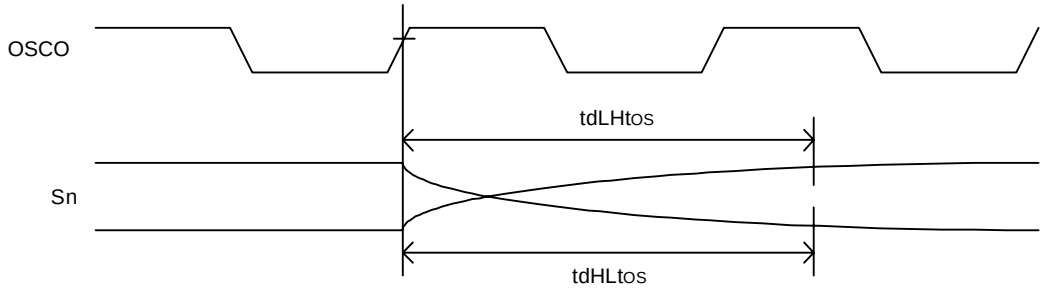


Fig.51 Source output

V_{SS} = 0 V, V_{DDHS} = 5.6 V, V_0 = 5.0 V, V_{15} = 0 V, T_a=-40 to 110°C

Parameter	Symbol	Condition	Typ.	Max.	Unit
Output delay time OSCO to Sn (L→H)	tdLHtos	RL = 35 kΩ CL = 60 pF	—	20	µs
Output delay time OSCO to Sn (H→L)	tdHLtos	RL = 35 kΩ CL = 60 pF	—	20	

*1 It is specified from OSCO rising edge which is set by P1 of DISSET2 command.
*2 Sn is S1 to S320 output
*3 Output shifting time from V_0 to V_{15} or from V_{15} to V_0.
*4 Output delay time OSCO to Sn is setting value±50 mV.

11.10 Gate output

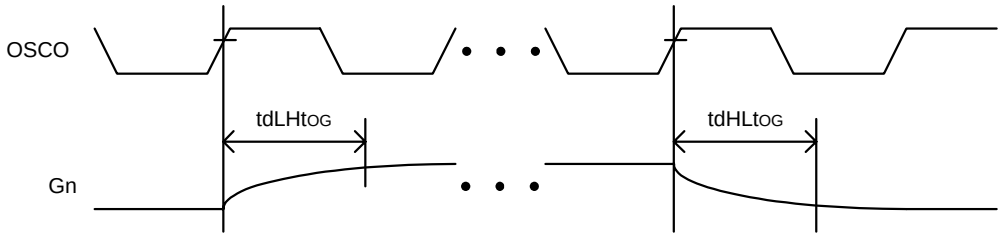


Fig.52 Gate output

V_{SS} = 0 V, V_{DDHG} = 16.0 V, V_{EE} = -12.0 V, T_a=-40 to 110°C

Parameter	Symbol	Condition	Typ.	Max.	Unit
Output delay time OSCO to Gn (L→H)	tdLHtog	RL = 5 kΩ CL = 100 pF	—	2	µs
Output delay time OSCO to Gn (H→L)	tdHLtog	RL = 5 kΩ CL = 100 pF	—	2	

*1 It is specified from OSCO rising edge which is set by P3 of DISSET2 command.
*2 Gn is G1 to G320 output
*3 Output delay time OSCO to Gn is specified based on the 5% and 95% of set value.

11.11 VCOM output

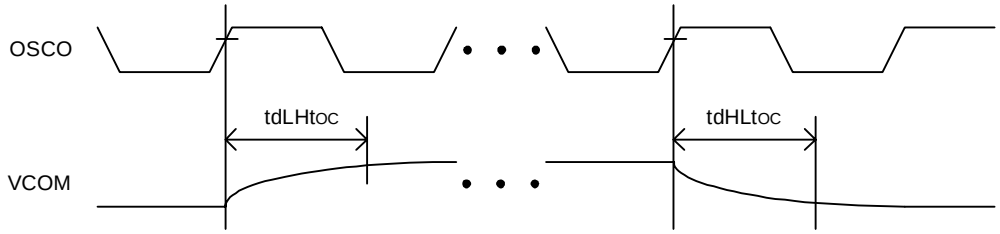


Fig.53 VCOM output

VSS = 0 V, VCOMH = 4.0 V, VCOML = -1.0 V, Ta=-40 to 110°C

Parameter	Symbol	Condition	Typ.	Max.	Unit
Output delay time OSCO to VCOM (LOW→HIGH)	tdLHtoc	RL = 50 Ω CL = 30 nF	—	15	μs
output delay time OSCO to VCOM (HIGH→LOW)	tdHLtoc	RL = 50 Ω CL = 30 nF	—	15	

*1 OSCO to VCOM output delay time is based on +/-50mV.
*2 Stabilized capacitance of VCOMH and VCOML is 4.7μF.

11.12 Multi Time PROM Erase

Fig 54 Multi Time PROM Erase

Ta = 10 to 40 °C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Erase voltage rising time	tRVE	–	0.1	–	5,000	Ms
Erase voltage falling time	tFVE	–	0.1	–	5,000	Ms

11.13 Multi Time PROM Programming

Fig 55 Multi Time PROM Programming

Ta = 10 to 40 °C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Programming voltage rising time	tRVP	–	0.1	–	5,000	us
Programming voltage falling time	tFVP	–	0.1	–	5,000	us

12. Revision History

Date	Rev.	Page	Type	Description
2012/2/29	1.1	All	New	Newly established

13. NOTES

When using these development specifications, note the following points.

1. The contents of these development specifications are subject to change without notice for improvement.

2. There is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party.

Examples shown in these development specifications are for understanding our products, and we are not responsible for any circuit problems that may occur when using them.

When using the S1D19600ries, note the following points:

IC handling notes against the light:

As a semiconductor chip is principally identical to a solar cell, its performance may change if exposed to bright light. Therefore, the IC may malfunction if exposed to light.

1. Design and mount the IC so that it is not exposed to light during actual operation.
2. In the test process, check the design and mounting of the IC so that it is not exposed to light.
3. Take all surfaces, top, bottom and sides, of the IC chip into consideration when blocking out light.

IC handling notes on ambient noise and others:

1. Though the S1D19600 series reserves the register settings, its internal state may change if excessive ambient noise is inserted. Measures are required to prevent noise generation or influence in terms of mounting and the system itself.
2. It is recommended that you set the software to refresh the operating state (register reset) periodically to avoid spike noise.

Precautions on use of Multi Time PROM

1. The reliability characteristics such as endurance (data rewriting frequency), light resistance, retention, etc. are those evaluated during development of the Multi-Time-Programmable ROM and are not tested at the time of shipment.
2. We are not in a position to guarantee the data after it is mounted. Therefore, we do not supply with the ROM data.
3. The Multi-time PROM is for temporary memory. The usage is data carrier such as that unique data of LCD module is stored to the Multi Time PROM of the S1D19600, and the data is stored to external non volatile memory on final application. After that, the access of Multi Time PROM is prohibited.

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