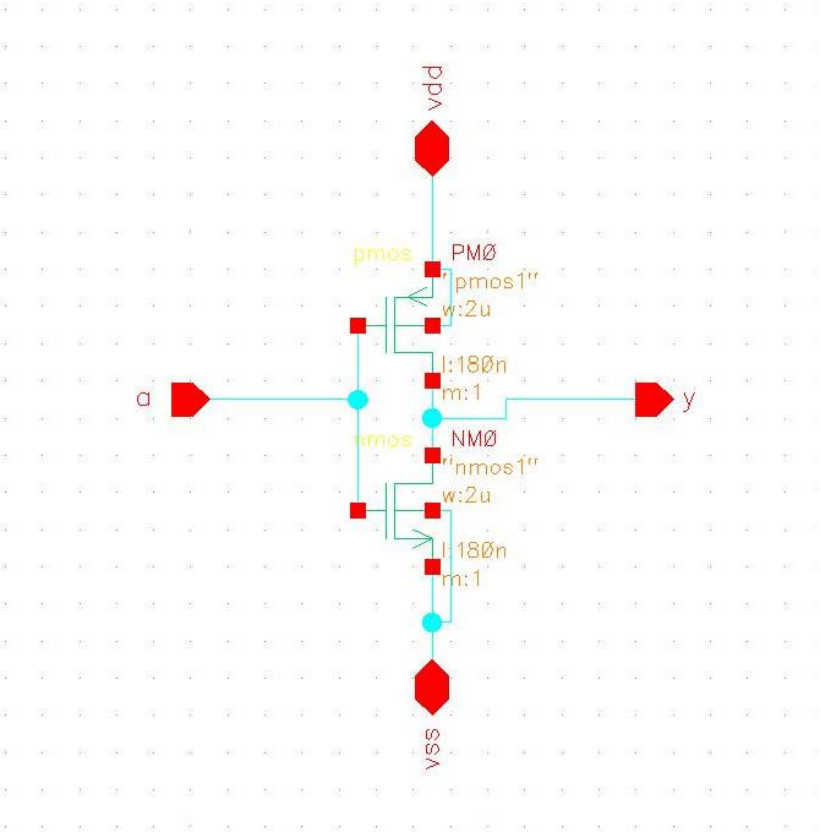


Fig: Schematic of Inverter

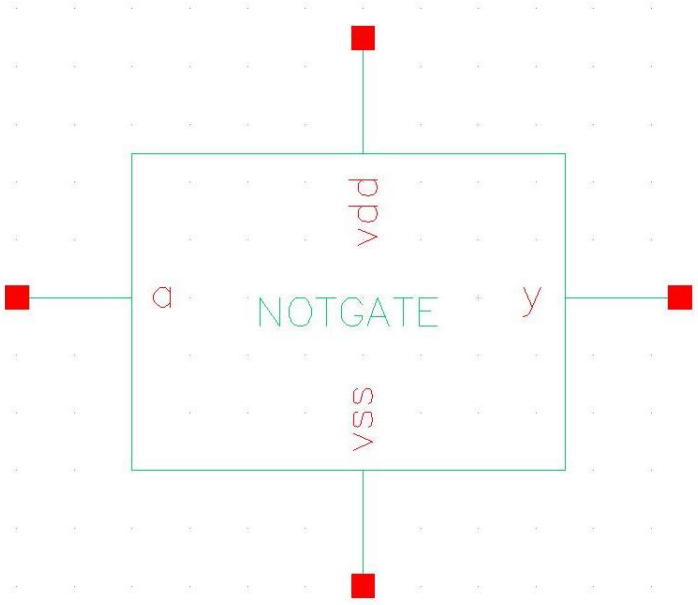


Fig: Symbol of Inverter

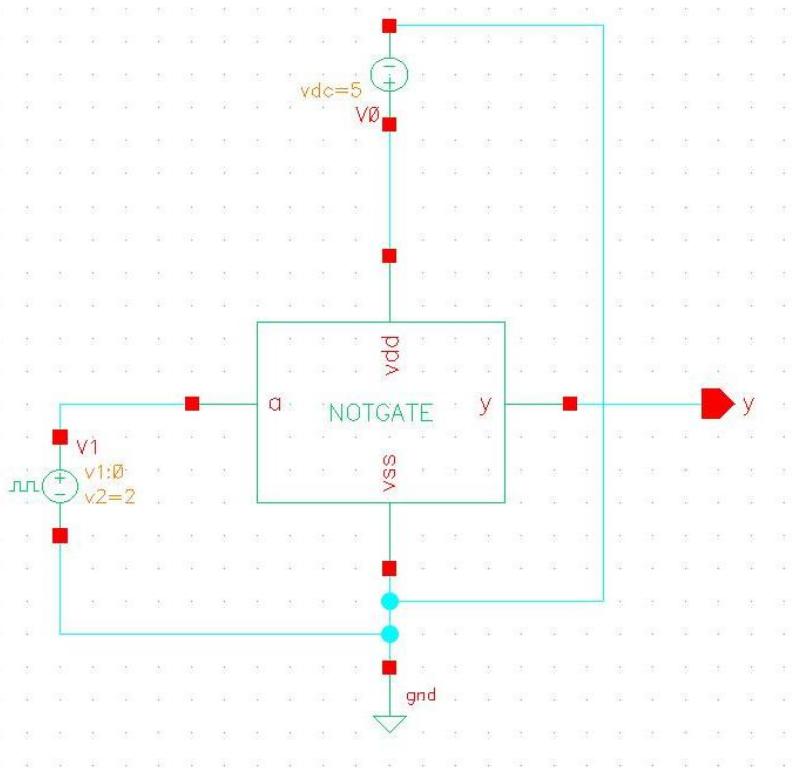


Fig: Test Circuit of Inverter

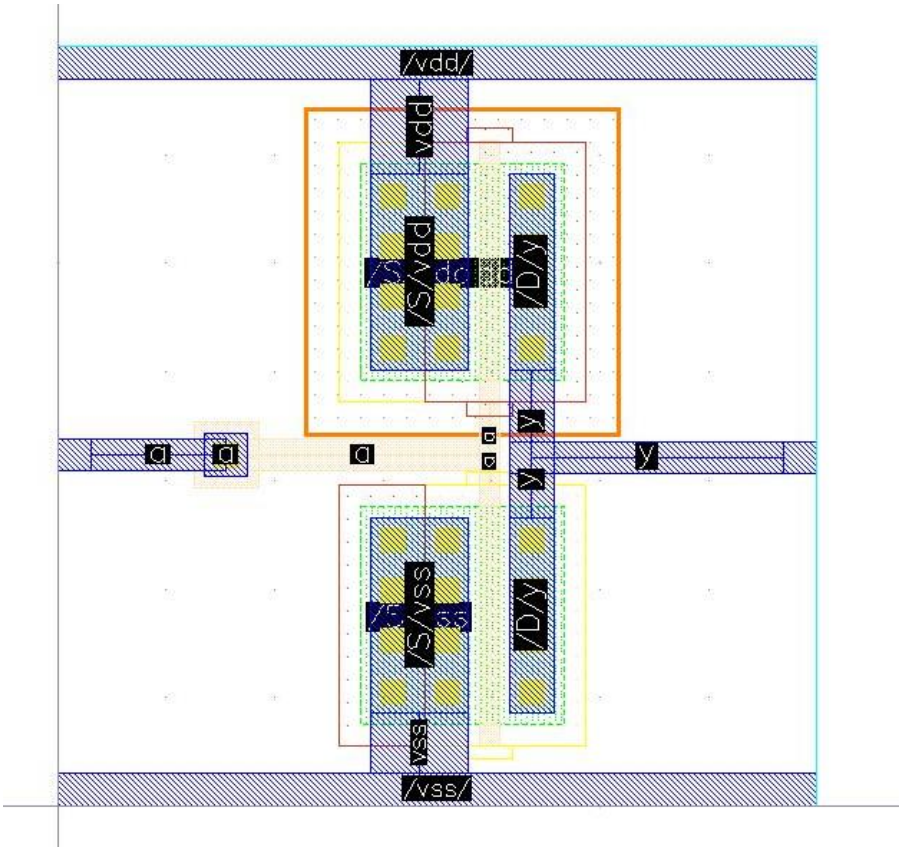


Fig: Layout of Inverter

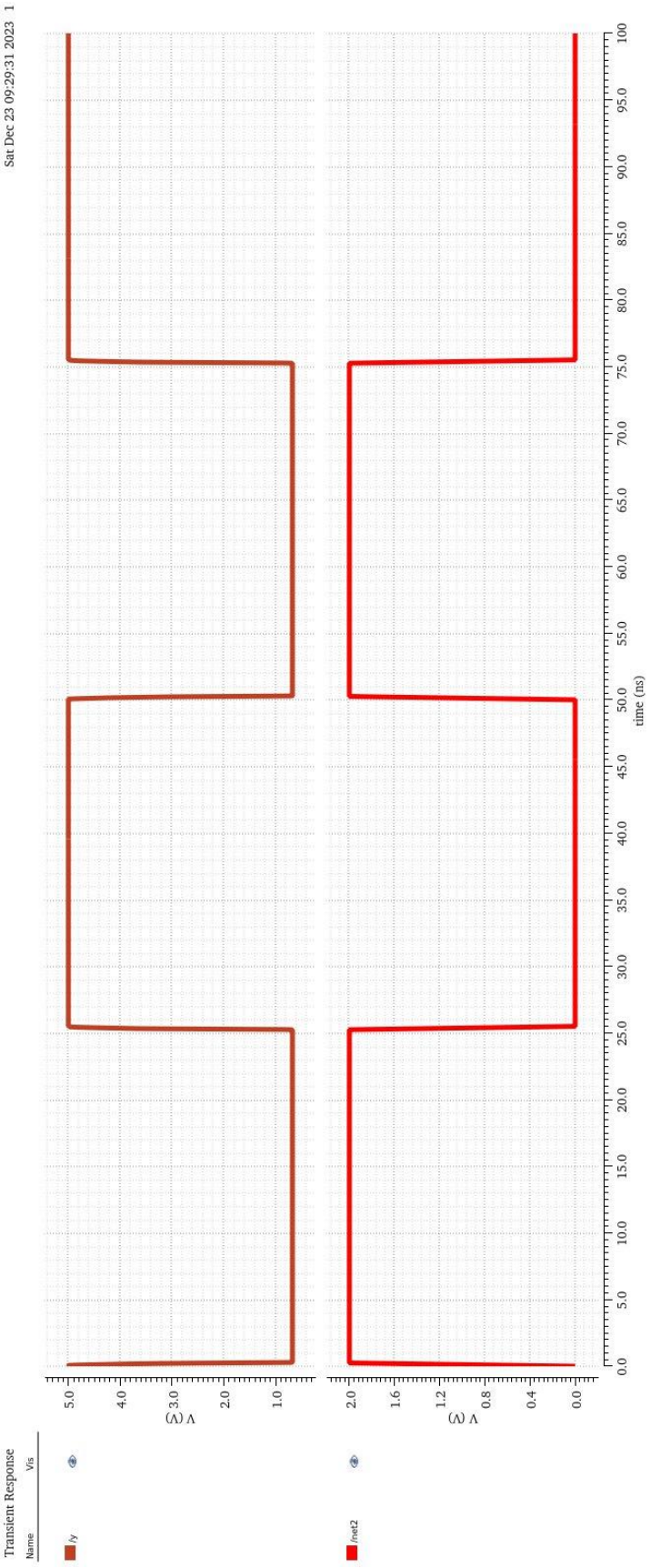


Fig: Output of Inverter

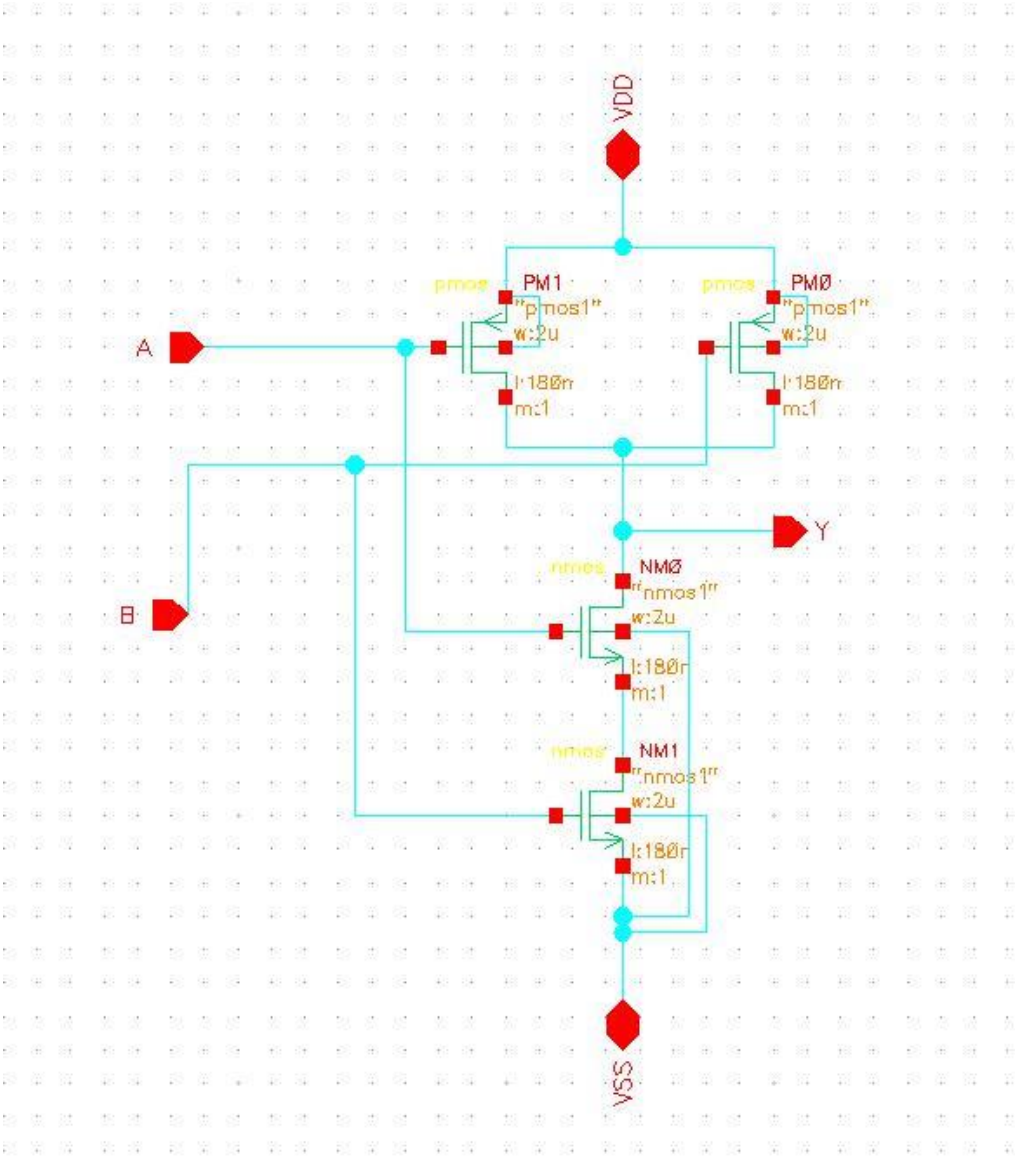


Fig: Schematic of NAND gate

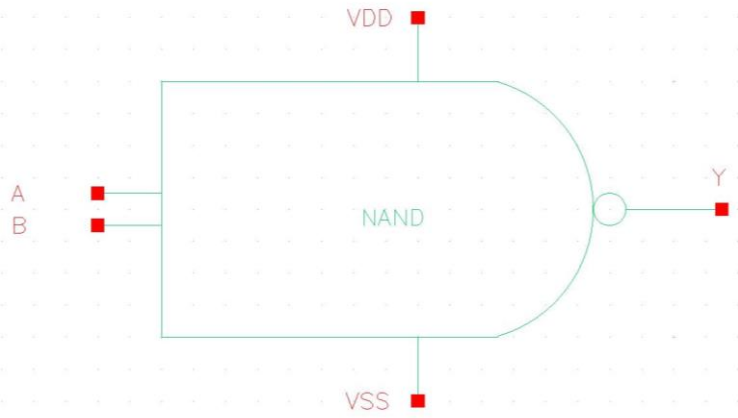


Fig: Symbol of NAND gate

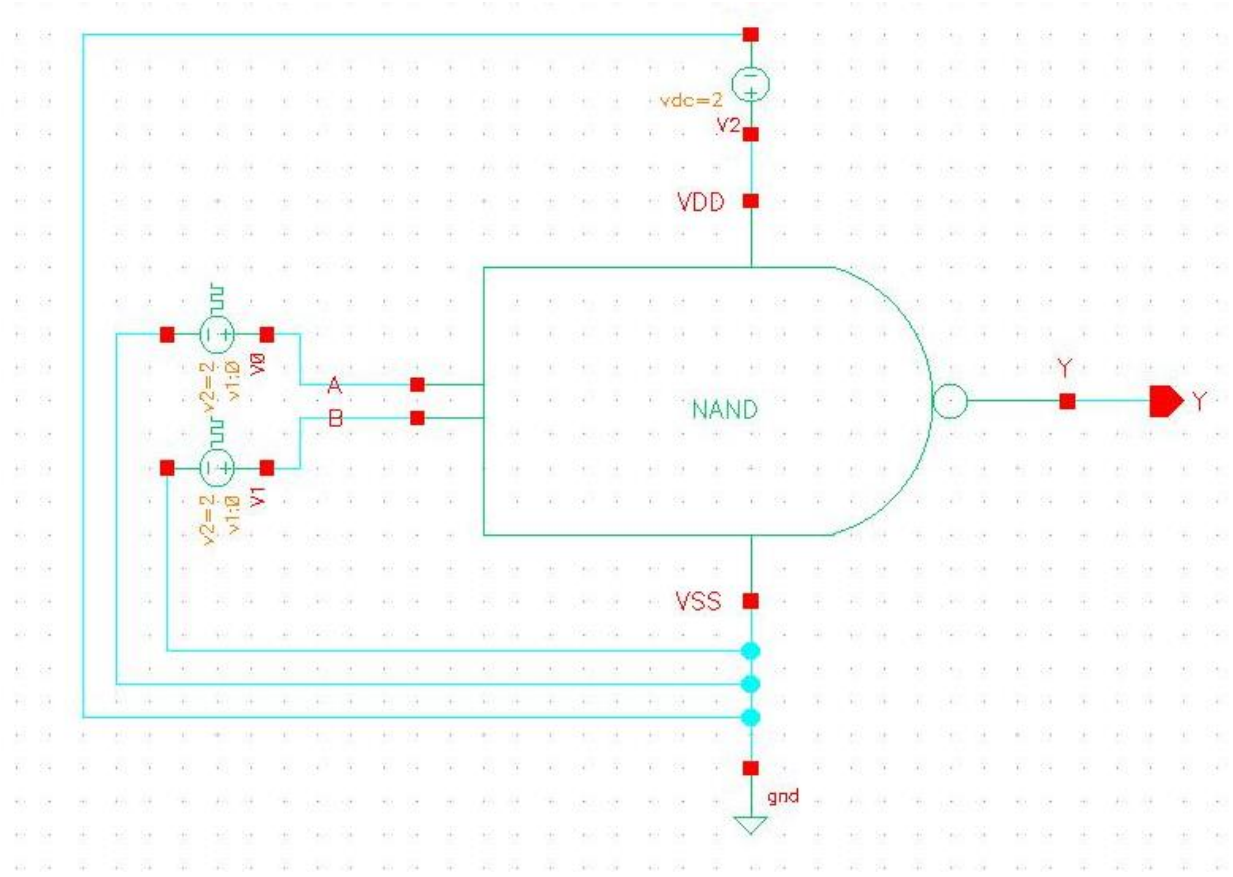


Fig: Test Circuit of NAND gate

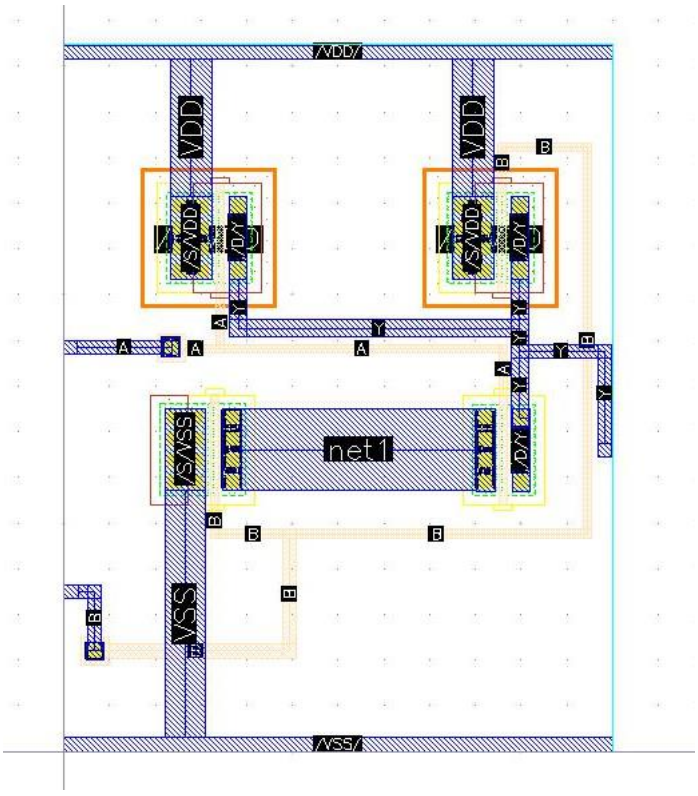


Fig: Layout of NAND gate

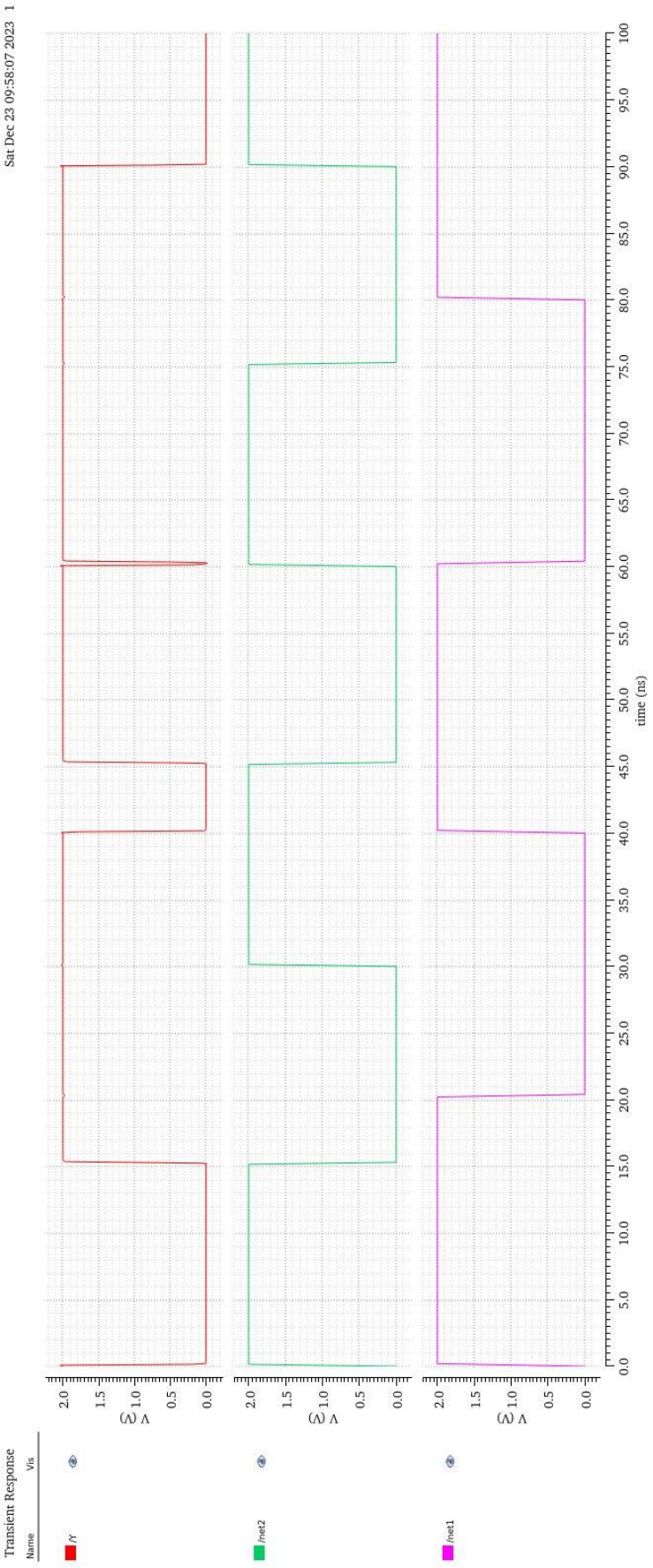


Fig: Output of NAND gate

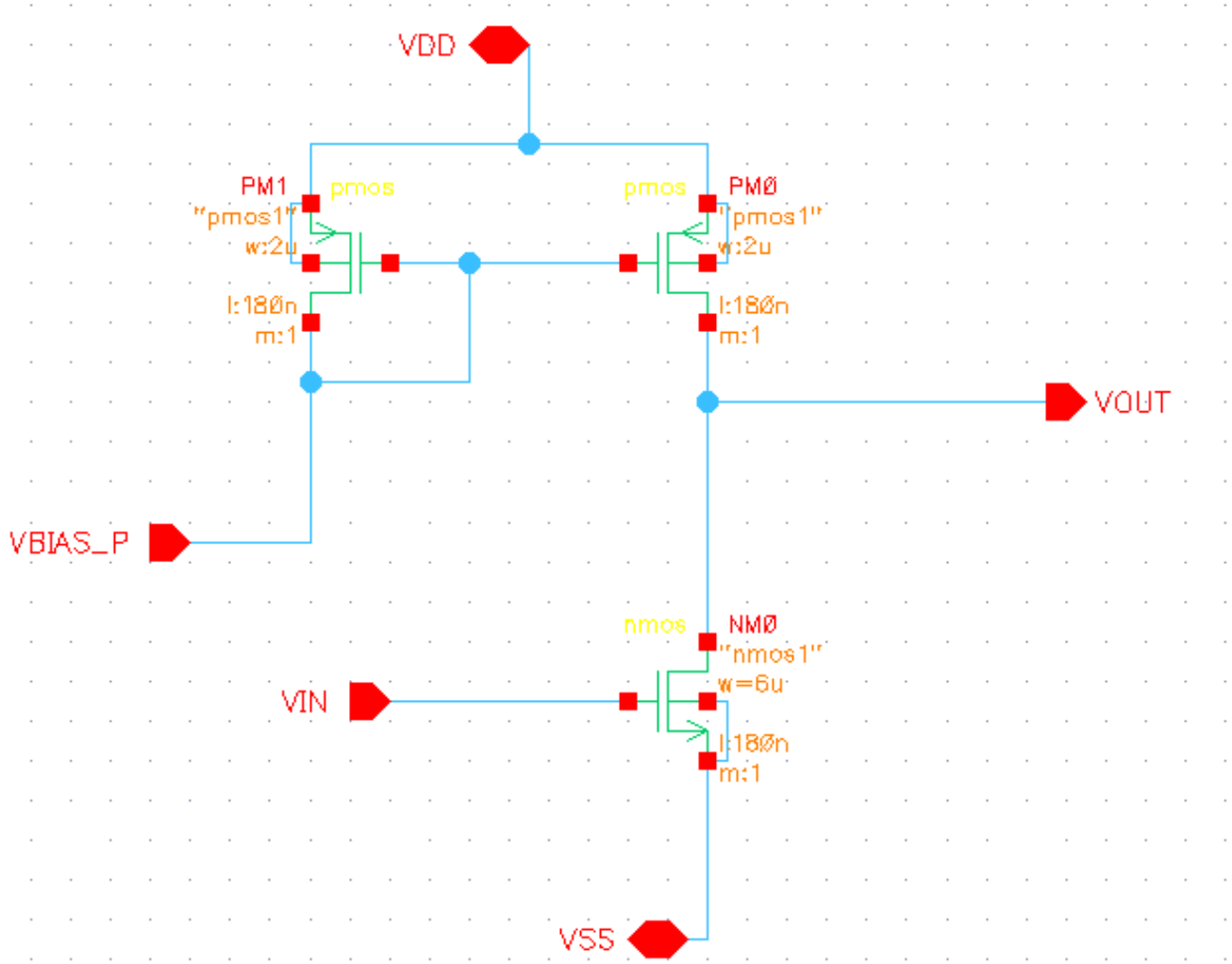


Fig: Schematic of CS amplifier

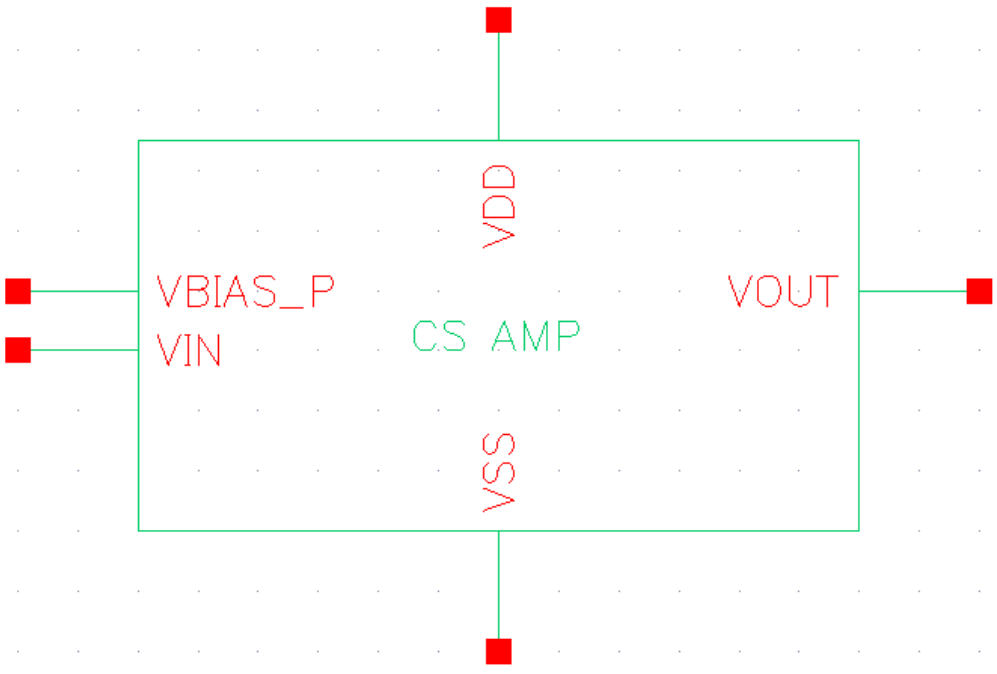


Fig: Symbol of CS amplifier

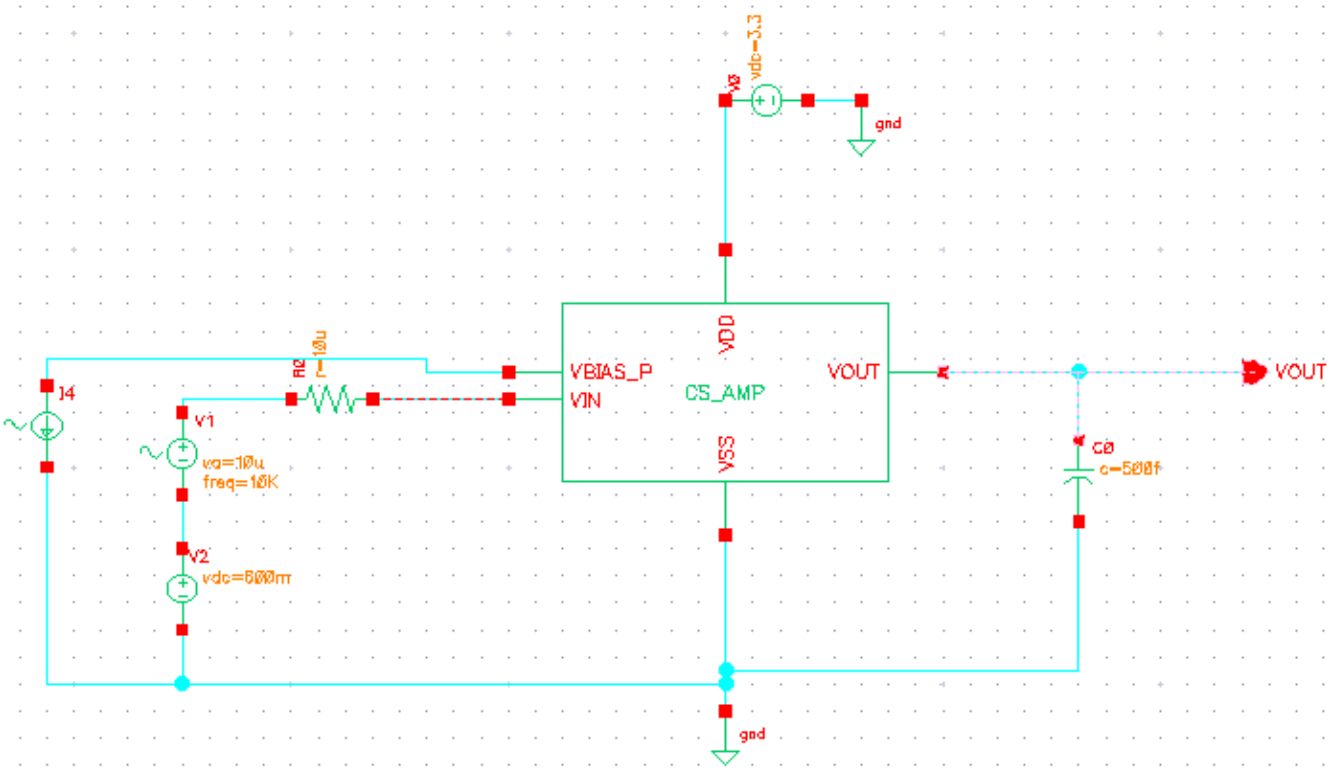


Fig: Test circuit of CS amplifier

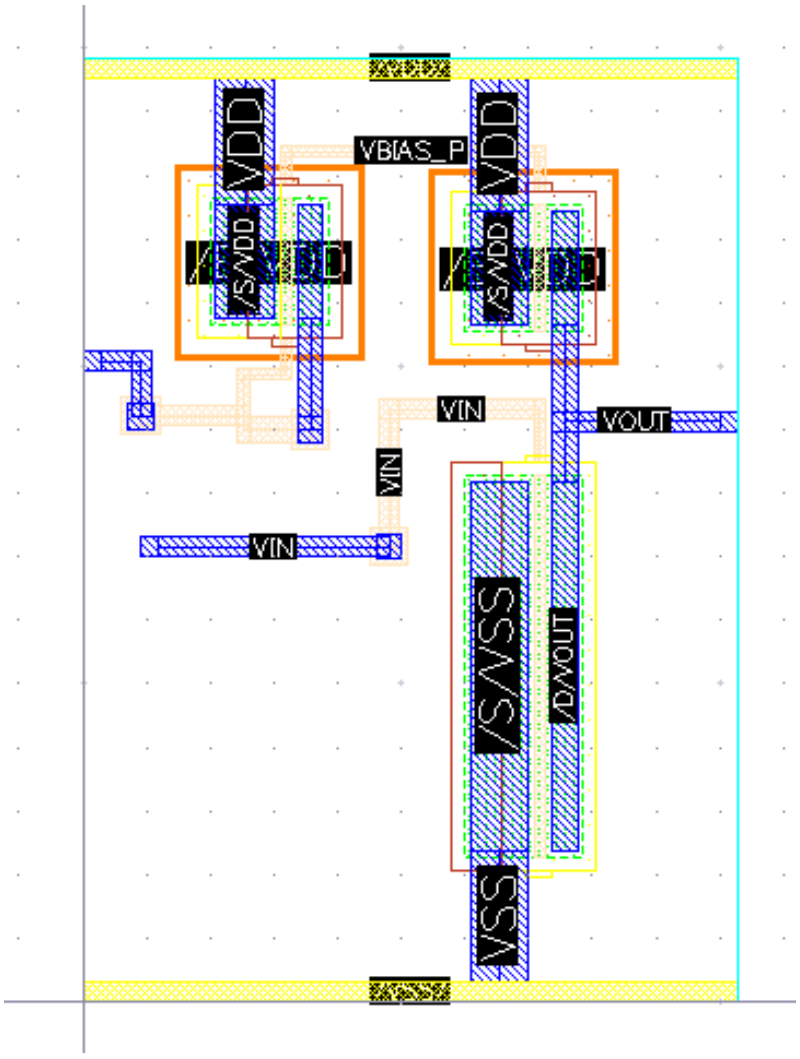
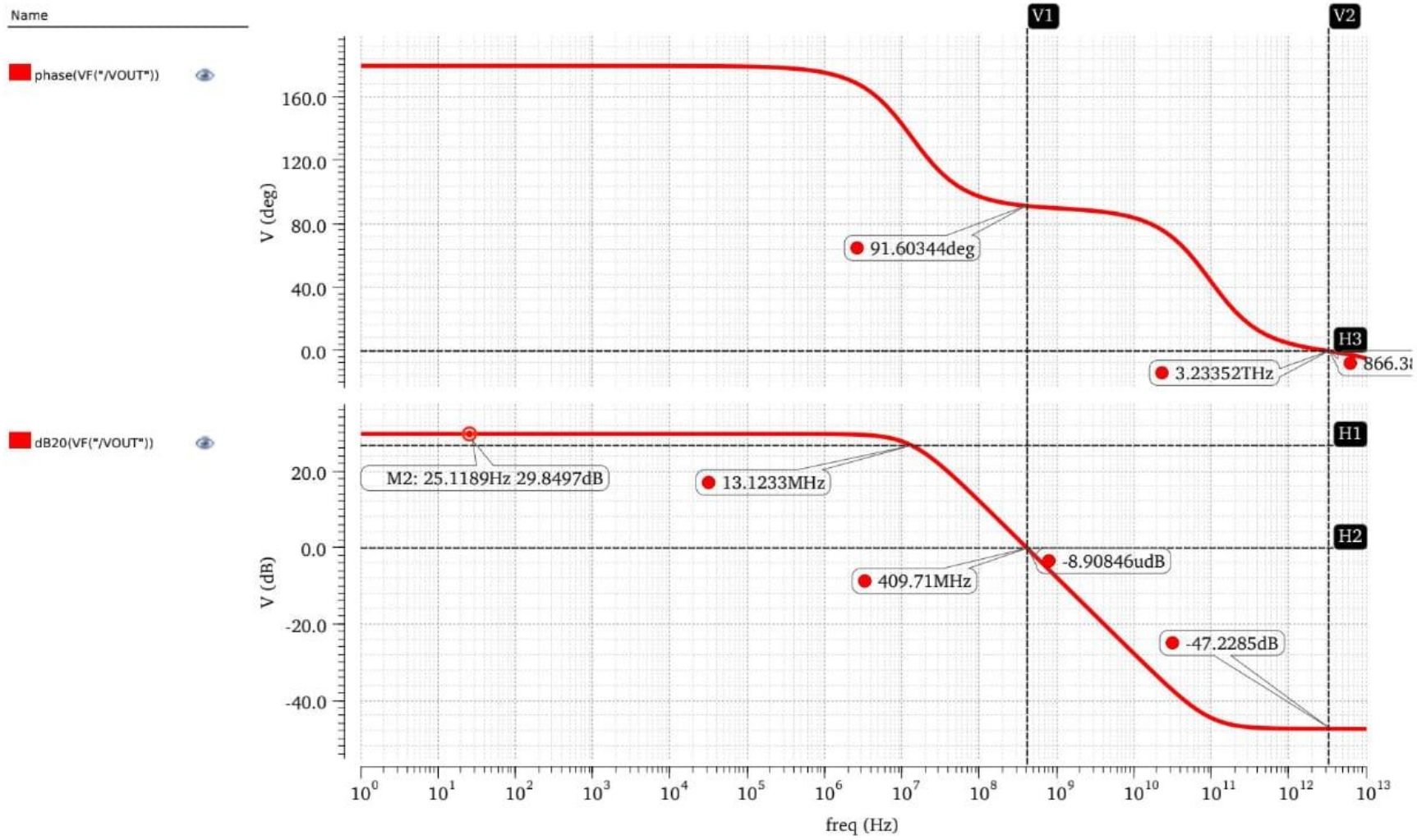


Fig: Layout of CS amplifier

AC Response



Markers

Fig: Output of CS amplifier

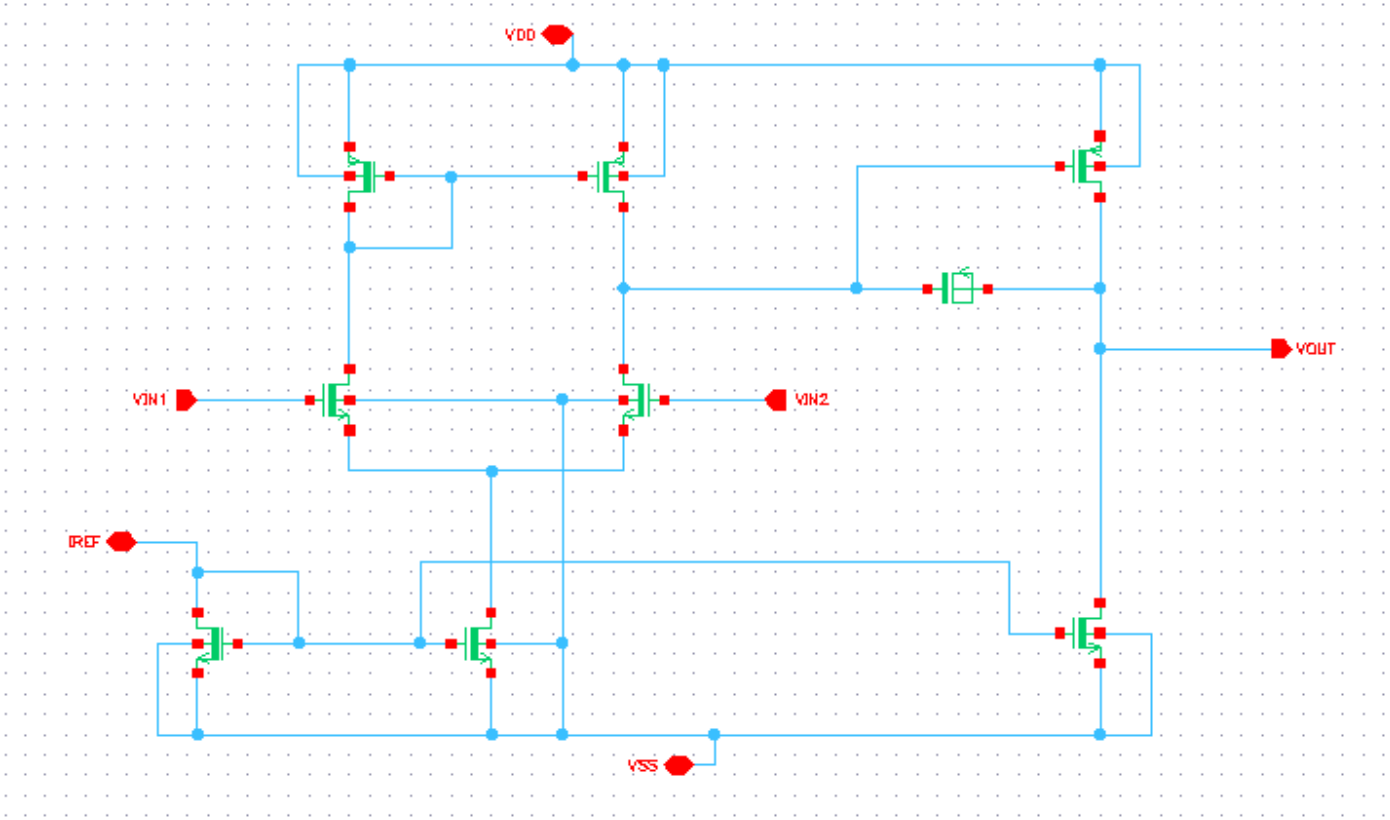


Fig: Schematic of Op-Amp

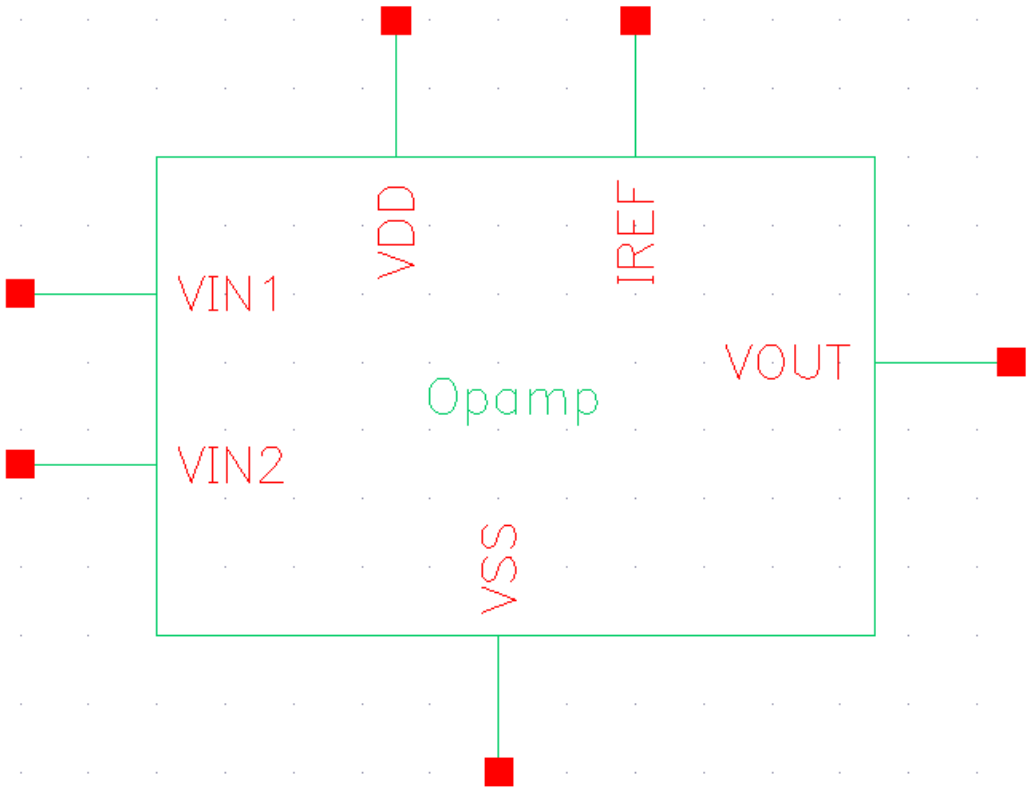


Fig: Symbol of Op-Amp

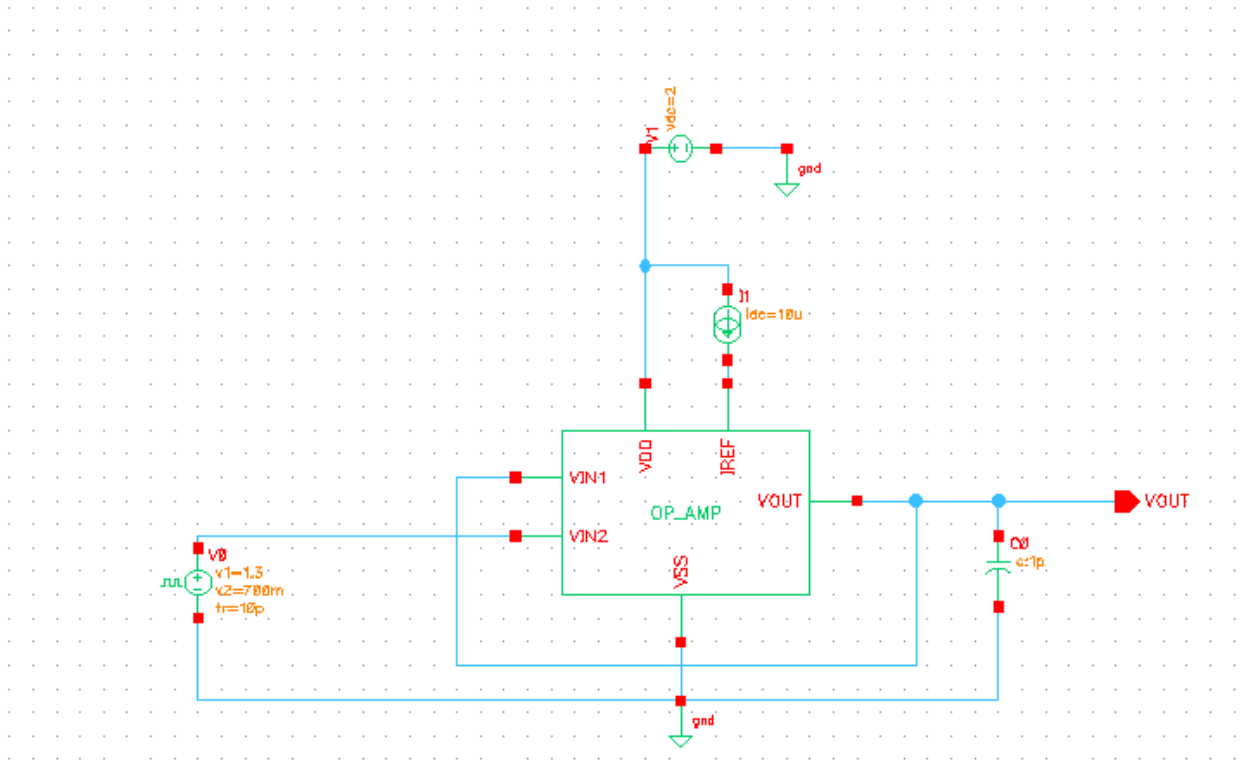
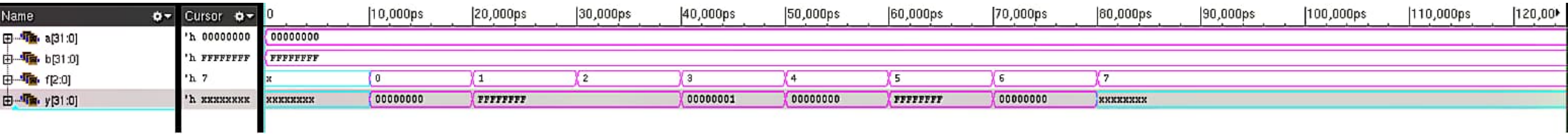


Fig: Test Circuit of Op-Amp

Fig: Output of Op-Amp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70,000ps
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100,000ps
110,000ps
120,000
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00000000
b[31:0]
'h FFFFFFFF
FFFFFFFF
f[2:0]
'h 7
x
0
1
2
3
4
5
6
7
y[31:0]
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00000001
00000000
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00000000
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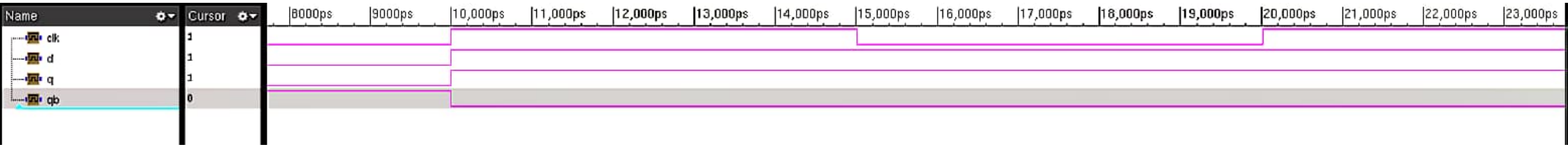
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d
q
qb
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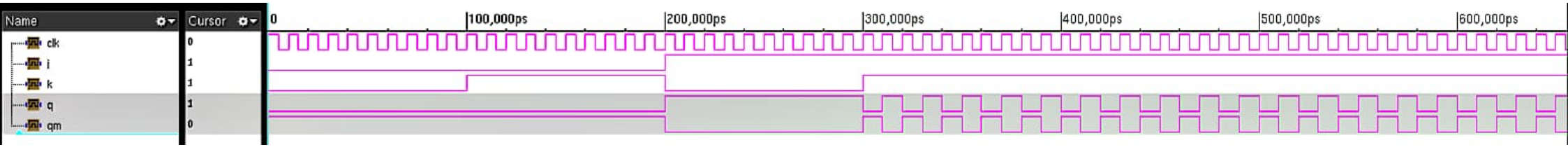
1
1
0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i
k
q
qm
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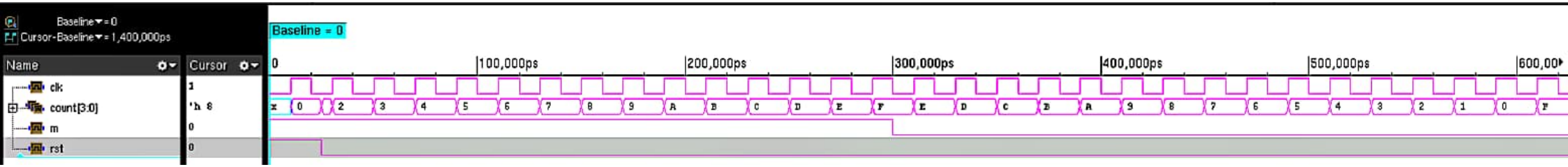
1
1
0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rst
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'h 8
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0
Baseline = 0
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200,000ps
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500,000ps
600,00
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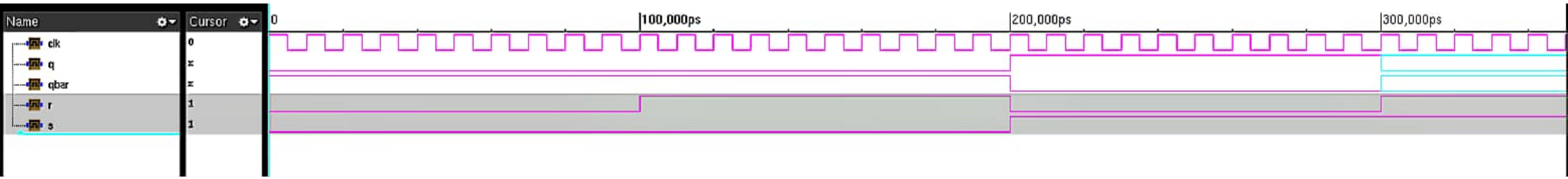
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x
x
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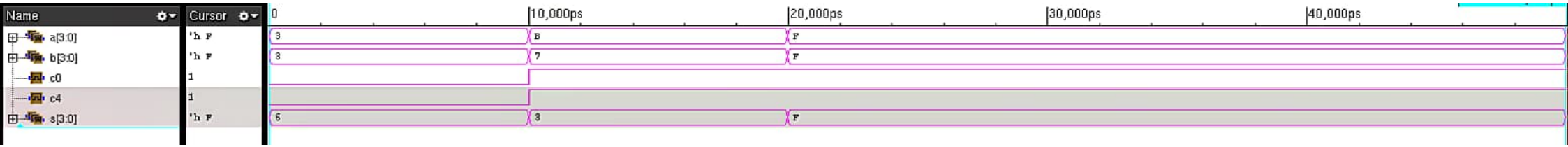
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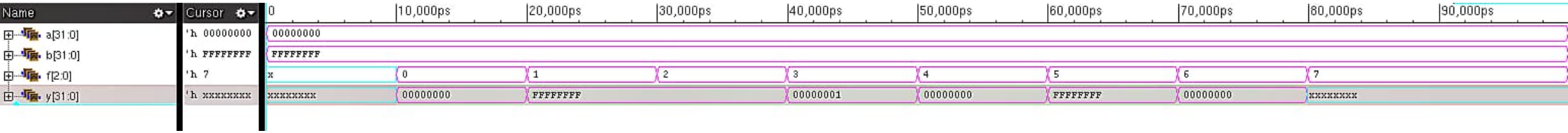
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00000000
b[31:0]
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FFFFFFFF
f[2:0]
'h 7
x
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2
3
4
5
6
7
y[31:0]
'h xxxxxxxx
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FFFFFFFF
00000001
00000000
FFFFFFFF
00000000
xxxxxxxx