PROJECT GROUP 10: Gagana Hirenallur Mohankumar

Rahul Jnanesh Gowda

Raksha Mairpady

Shashikirana Chinchandlahalli Ravanappa

DIMM	Specifications	Calculations
Total number of ranks	2 Ranks	
Total number of Channels	2 Channels	
Total Capacity of the DIMM	16GB	
Total Number of x8 DDR5 Chips	8 DDR5 chips	
Total number of output bits per chip	8 bits	
Total number of output bit from DIMM module	64 bits	
DDR5 chip		
Total Capacity of the chip	16Gb	16GB x 8= 128Gb/8= 16Gb
Organization of the chip	2G x 8	16Gb/8= 2G x 8
Page Size	1KB	Given
Burst Length	16	
Total number of bank groups	8	Given
Total number of banks per bank groups	4	Given
Total number of columns	2^10	Total number of columns = page size /internal access width
Number of column bit lines	10	
Total number of rows	2^16	Number of rows = total capacity of the chip / Number of columns x total bank groups x total banks per bank groups x internal access width
Number of address bit lines	16	

PHYSICAL TO TOPOLOGICAL ADDRESS MAPPING:

3318	1712	11 10	9 8 7	6	5 4 3 2	1 0
Row (16 bits)	Upper Column (6	Bank	Bank	Channel	Lower	Byte
	bits)	(2 bits)	Group (3	(1 bit)	Column (4	Select
			bits)		bits)	(2 bits)