

Openlane-Sky130-workshop

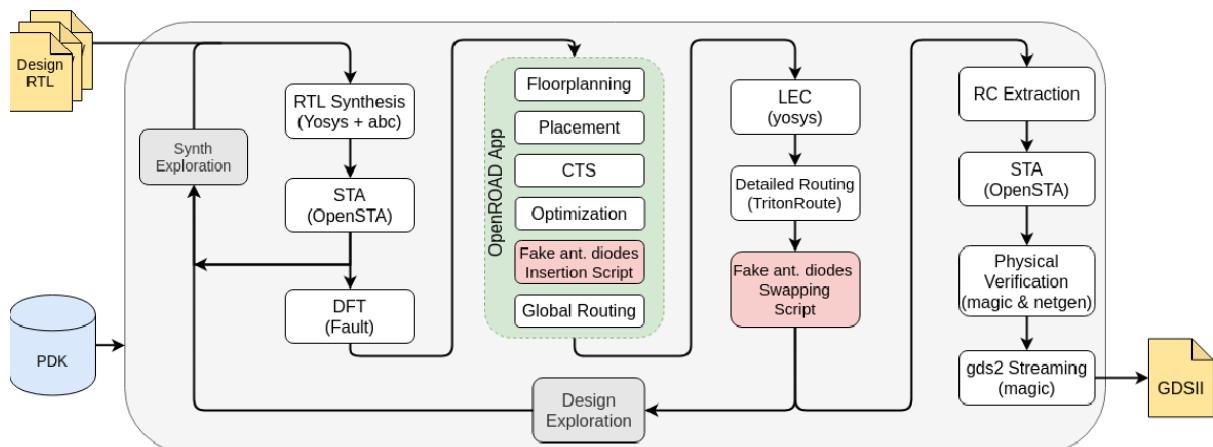
An informative workshop on advanced Physical Design using OpenLANE/Sky130 organized by VSD Corp. The workshop focused on building basics by imparting exposure to conceptual as well as practical approach. Learning's: Open source tools, Characterization of Cell, SPICE simulations, Static timing Analysis concepts, Commands of various OpenLANE tools, 16-mask CMOS Fabrication, Antenna Diode Concept, Decoupling Cap, Routing algorithm & Steps, Timing Characterization and familiarity with files like libs/db, LEF, DEF, SDC and SPEF. Tools used: Magic, Ngspice, OpenSTA, TritonRoute, yosys, SPEF extractor and OpenROAD.

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5. Day 4: Timing Analysis using Triton Clock Tree Synthesis (CTS).
6. Day 5: Creation of Power Distribution Network, Routing and SPEF Extraction.

Introduction to OpenLane

OpenLANE is an automated RTL to GDSII flow based on several components including OpenROAD, Yosys, Magic, Netgen, Fault, OpenPhySyn, SPEF-Extractor and custom methodology scripts for design exploration and optimization. It is a tool started for true open source tape-out experience and comes with APACHE version 2.0. The goal of OpenLANE is to produce clean GDSII without any human intervention. OpenLANE is tuned for Skywater 130nm open PDK and can be used to produce hard macros and chips.



The Flow of OpenLane EDA

OpenLane Design Stages

OpenLane flow consists of several stages. By default all flow steps are run in sequence. Each stage may consist of multiple sub-stages.

1. Synthesis

- a) Yosys/abc - Perform RTL synthesis and technology mapping.
- b) OpenSTA - Performs static timing analysis on the resulting Netlist to generate timing reports

2. Floorplaning

- a) init_fp - Defines the core area for the macro as well as the rows (used for placement) and the tracks (used for routing)
- b) ioplacer - Places the macro input and output ports
- c) pdngen - Generates the power distribution network
- d) tapcell - Inserts welltap and decap cells in the floorplan

3. Placement

- a) RePLace - Performs global placement
- b) Resizer - Performs optional optimizations on the design
- c) OpenDP - Performs detailed placement to legalize the globally placed components

4. CTS

- a) TritonCTS - Synthesizes the clock distribution network (the clock tree)

5. Routing

- a) FastRoute - Performs global routing to generate a guide file for the detailed router
- b) TritonRoute - Performs detailed routing
- c) OpenRCX - Performs SPEF extraction

6. Tapeout

- a) Magic - Streams out the final GDSII layout file from the routed def
- b) KLayout - Streams out the final GDSII layout file from the routed def as a back-up

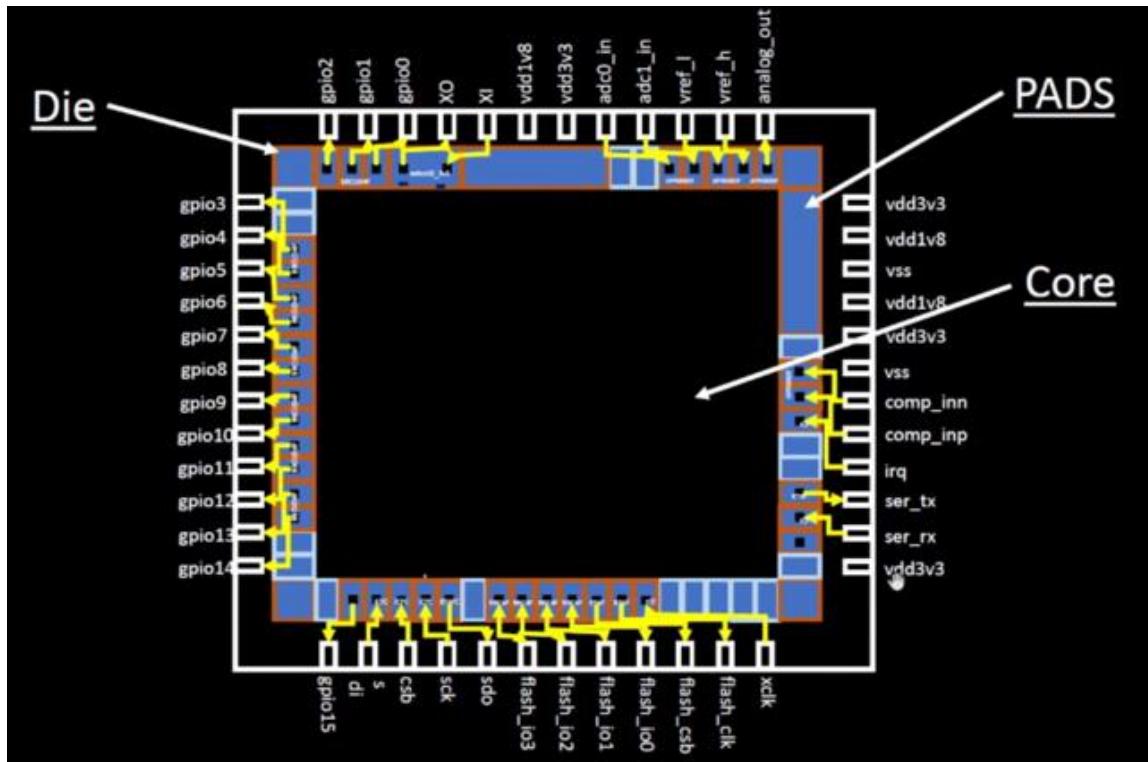
7. Signoff

- a) Magic - Performs DRC Checks & Antenna Checks
- b) KLayout - Performs DRC Checks
- c) Netgen - Performs LVS Checks
- d) CVC - Performs Circuit Validity Checks

Day 1: Introduction of chip architecture and insights into Physical Design.

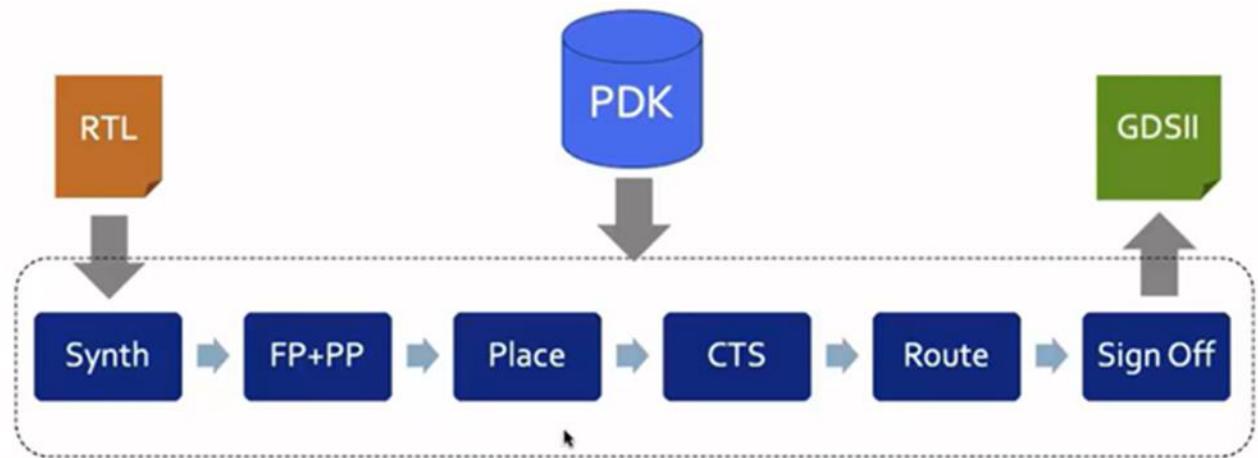
The chip will be sitting at the center of the package. Chip is connected to the package, as shown in the above figure.

- PADS – It is an I/O port which can be used send and receive the signals via PADS.
- CORE – The Foundry IP's as well as many other digital and analog blocks are placed in the chip.
- DIE – The size of the entire chip. Die will be manufactured on the silicon wafer.



Introduction into Physical Design:

In integrated circuit design, **physical design** is a step in the standard design cycle which follows after the circuit design. At this step, circuit representations of the components (devices and interconnects) of the design are converted into geometric representations of shapes which, when manufactured in the corresponding layers of materials, will ensure the required functioning of the components. This geometric representation is called integrated circuit layout. This step is usually split into several sub-steps, which include both design and verification and validation of the layout.



There are mainly six steps in Physical design:

1. Synthesis :

Physical design is based on a netlist which is the end result of the synthesis process. Synthesis converts the RTL design usually coded in VHDL or Verilog HDL to gate-level descriptions which the next set of tools can read/understand. This netlist contains information on the cells used, their interconnections, area used, and other details.

2. Floorplanning :

The second step in the physical design flow is floorplanning. Floorplanning is the process of identifying structures that should be placed close together, and allocating space for them in such a manner as to meet the sometimes conflicting goals of available space (cost of the chip), required performance, and the desire to have everything close to everything else. Based on the area of the design and the hierarchy, a suitable floorplan is decided upon. Floorplanning takes into account the macros used in the design, memory, other IP cores and their placement needs, the routing possibilities, and also the area of the entire design. Floorplanning also determines the IO structure and aspect ratio of the design. A bad floorplan will lead to wastage of die area and routing congestion.

3. Placement

Placement uses RC values from Virtual Route (VR) to calculate timing. VR is the shortest Manhattan distance between two pins. VR RCs are more accurate than WLM RCs.

Placement is performed in four optimization phases:

- Pre-placement optimization
- In placement optimization
- Post Placement Optimization (PPO) before clock tree synthesis (CTS)
- PPO after CTS.

Pre-placement Optimization optimizes the netlist before placement, HFNs (High Fanout Nets) are collapsed. It can also downsize the cells. In-placement optimization re-optimizes the logic based on VR. This can perform cell sizing, cell moving, cell bypassing, net splitting, gate duplication, buffer insertion, area recovery. Optimization performs iteration of setup fixing, incremental timing and congestion driven placement. Post placement optimization before CTS performs netlist optimization with ideal clocks. It can fix setup, hold, max trans/cap violations. It can do placement optimization based on global routing. It re does HFN synthesis. Post placement optimization after CTS optimizes timing with propagated clock. It tries to preserve clock skew.

4. Clock tree synthesis

The goal of **clock tree synthesis (CTS)** is to minimize skew and insertion delay. Clock is not propagated before CTS as shown in the picture. After CTS hold slack should improve. Clock tree begins at .sdc defined clock source and ends at stop pins of flop. There are two types of stop pins known as ignore pins and sync pins. 'Don't touch' circuits and pins in front end (logic synthesis) are treated as 'ignore' circuits or pins at back end (physical synthesis). 'Ignore' pins are ignored for timing analysis. If clock is divided then separate skew analysis is necessary.

5. Routing

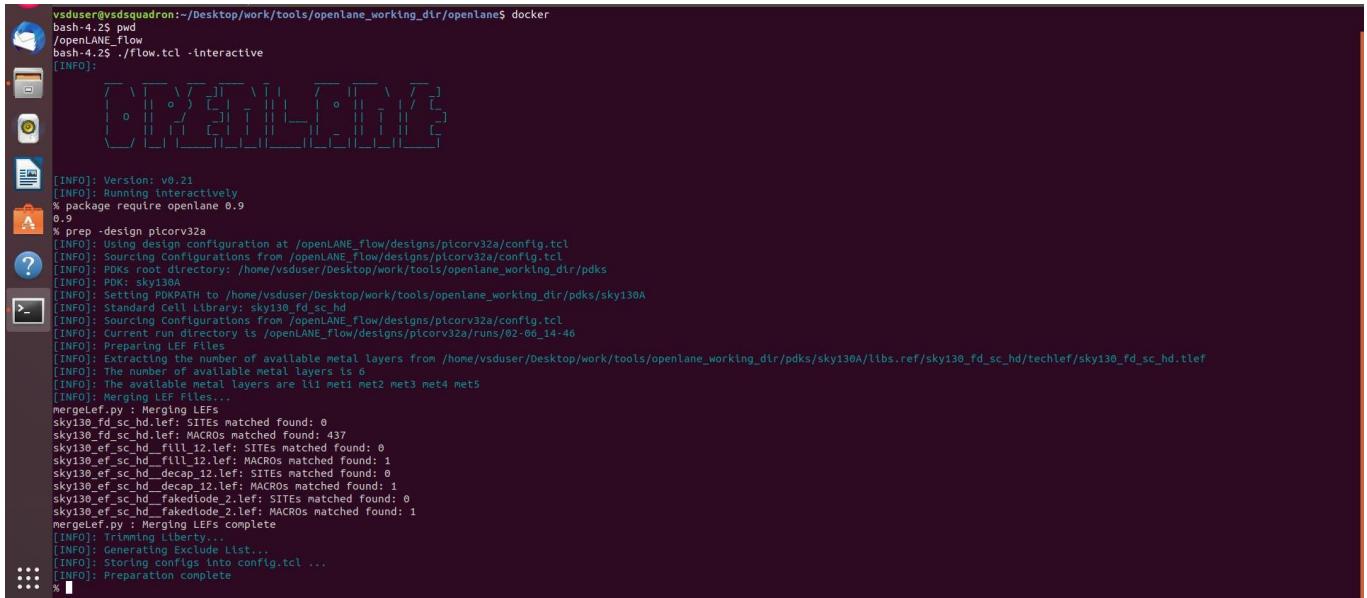
There are two types of routing in the physical design process, global routing and detailed routing. Global routing allocates routing resources that are used for connections. It also does track assignment for a particular net. Detailed routing does the actual connections. Different constraints that are to be taken care during the routing are DRC, wire length, timing etc.

OpenLANE LAB:

The working Directory will be,

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$
```

The commands used enter into OpenLANE directory is,

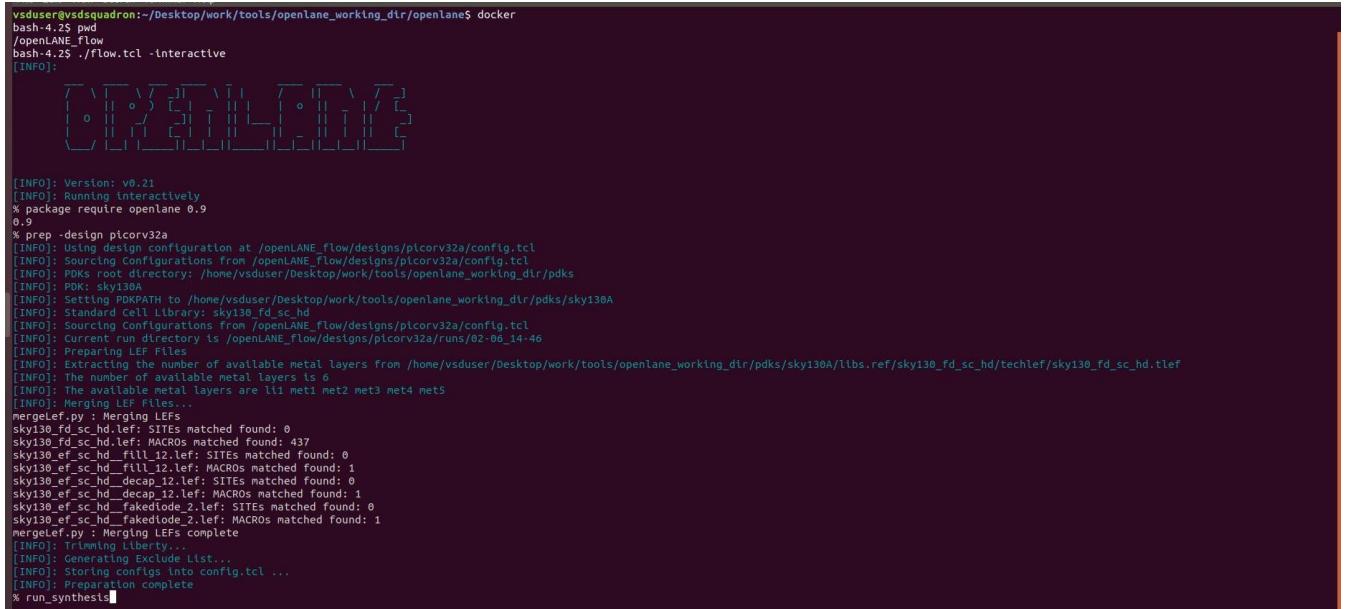


```

vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ docker
bash-4.2$ pwd
/openLANE_flow
bash-4.2$ ./flow.tcl -interactive
[INFO]:
[INFO]: Version: v0.21
[INFO]: Running interactively
% package require openlane 0.9
[INFO]: prep -design picorv32a
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations From /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations From /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/02-06_14-46
[INFO]: Merging LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.lef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1l met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergelef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITES matched found: 0
sky130_fd_sc_hd.lef: MACROS matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITES matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROS matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITES matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROS matched found: 1
sky130_ef_sc_hd_fakelioide_2.lef: SITES matched found: 0
sky130_ef_sc_hd_fakelioide_2.lef: MACROS matched found: 1
mergelef.py : Merging LEFs complete
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
%
```

To run synthesis,

Command: run_synthesis



```

vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ docker
bash-4.2$ pwd
/openLANE_flow
bash-4.2$ ./flow.tcl -interactive
[INFO]:
[INFO]: Version: v0.21
[INFO]: Running interactively
% package require openlane 0.9
[INFO]: prep -design picorv32a
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations From /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations From /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/02-06_14-46
[INFO]: Merging LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.lef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1l met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergelef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITES matched found: 0
sky130_fd_sc_hd.lef: MACROS matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITES matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROS matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITES matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROS matched found: 1
sky130_ef_sc_hd_fakelioide_2.lef: SITES matched found: 0
sky130_ef_sc_hd_fakelioide_2.lef: MACROS matched found: 1
mergelef.py : Merging LEFs complete
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% run_synthesis
```

After synthesis step,

```

Copyright © 1993-2013 Gnu GPL Version 3 <http://www.gnu.org/licenses/gpl.html>
This is free software, and you are free to change and redistribute it
under certain conditions; type `show_copyright' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type `show_warranty'.
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.9460000000000001
puts "\[INFO]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.9460000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -711.59
wns -23.89
[INFO]: Synthesis was successful
%
```

Day 2: Chip floorplan and Introduction to Library Cells

On Day 2, definition of width and height of core and die. Factors like Utilization factor and Aspect ratio important to understand a design were introduced and their effects were discussed. Steps involved to define location of pre-placed cell & it's advantage of enhancing reusability and de-coupling capacitor and how they help during switching to avoid failure explained. A fully charged De-coupling cap placed parallel to circuits to ensure proper supply of peak current Ipeak by decoupling them from main supply voltage. Hence de-coupling cap ensures proper local communication while multiple Vdd & Vss lines lead to proper global communication avoiding voltage droop and ground bounce conditions. Step of placing logical cell placement blockage to avoid PnR tool to place anything.

Characterization

Input information required by Characterization software's are PDKs, DRC & LVS rules and spice models. The design steps of it involve *Circuit Design* and *Layout design* characterization. The software GUNA used for characterization. The characterization can be classified as Timing characterization, Power characterization and Noise characterization.

Characterization flow steps

- Model file of CMOS containing basic property definitions
- Read extracted Spice Netlist
- Recognize the behaviour of cell
- Read the subcircuits
- Attract the power sources
- Apply input or stimulus

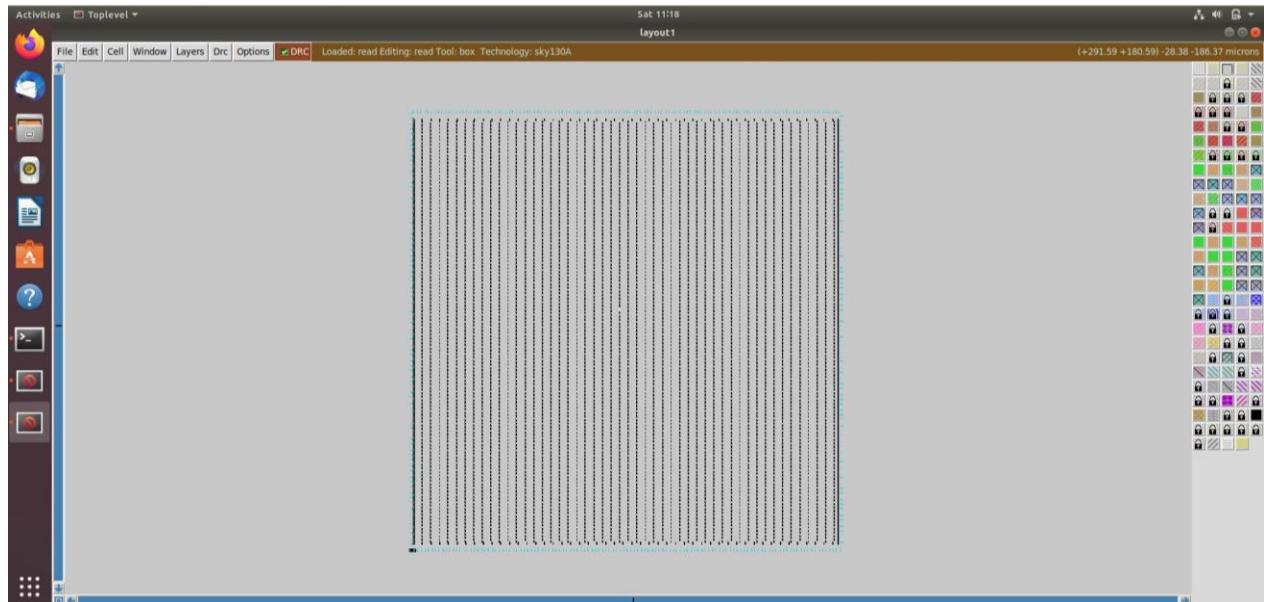
- Provide necessary output capacitance
- Provide necessary simulation commands

To run Floorplan stage

Command : run_floorplan

Floorplan Result

```
Running tapcell...
Step 1: Cut rows...
[INFO] Macro blocks found: 0
[INFO] #Original rows: 285
[INFO] #Cut rows: 0
Step 2: Insert endcaps...
[INFO] #Endcaps inserted: 570
Step 3: Insert tapcells...
[INFO] #Tapcells inserted: 10473
Running tapcell... Done!
```



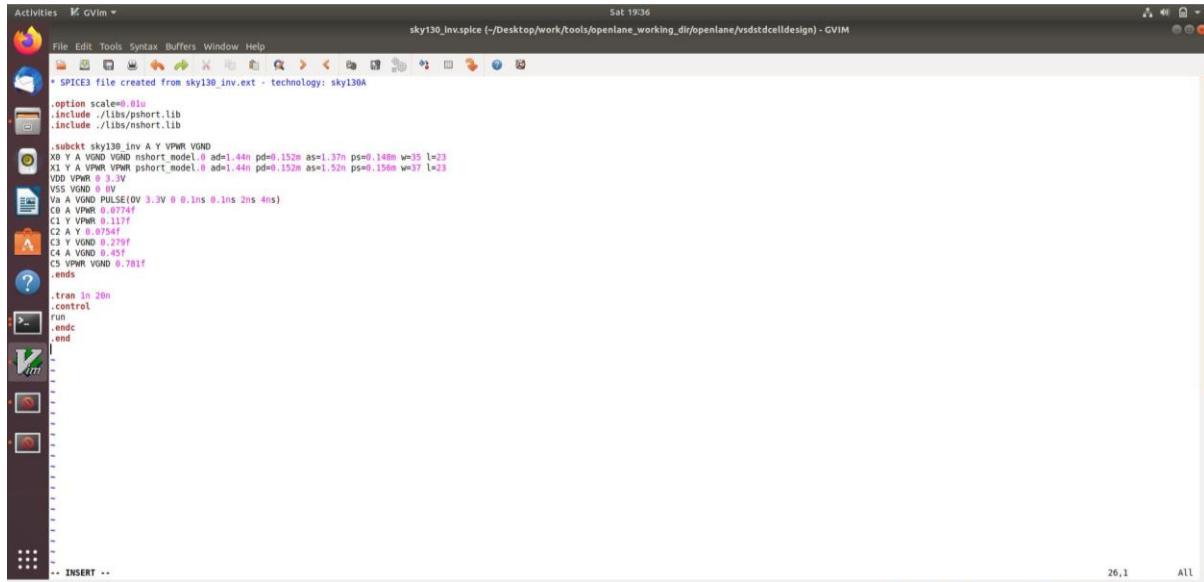
Floorplan of picorv32a

Day 3: Design and Characterization of cells using Magic Layout tool and Ngspice

OpenLANE offers an interesting feature of making changes into parameters on the go. This helps to deal with issues like congestion. SPICE deck formation contains information like components connectivity and values and information about nodes. It was showed how W/L ratio of MOS impacts its conductivity and hence reason of carefully defining W/L ratio of

MOS to ensure same *rise* and *fall* delay for clock signals. CMOS robustness defined with the help of parameter that is **Switching Threshold (Vm)**. Here name of inverter is vsdshinv.

Spice deck Description of vsdshinv:

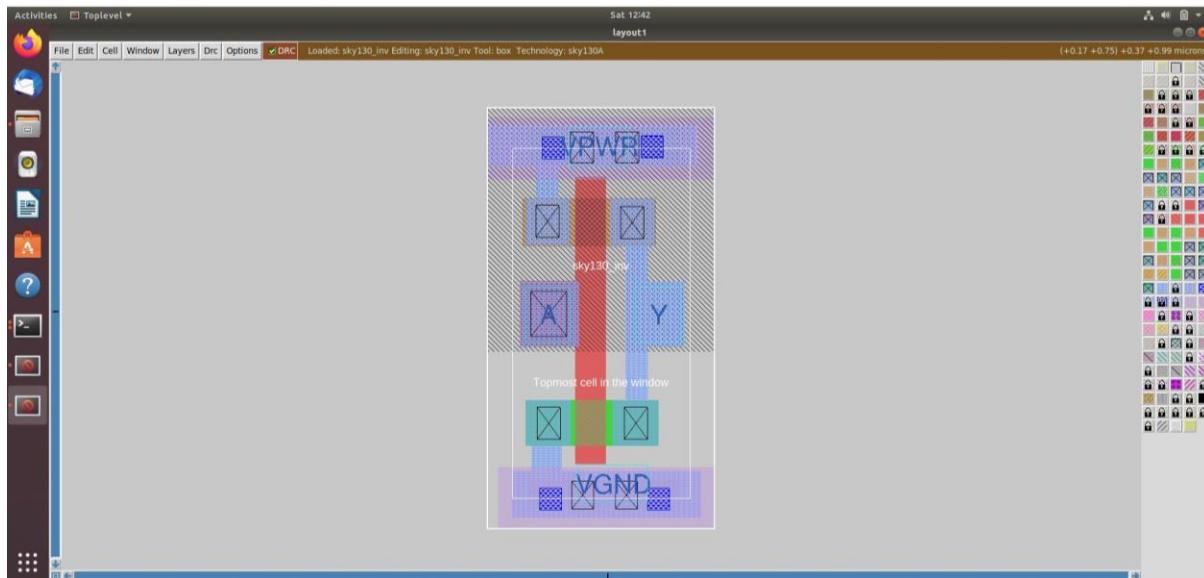


```

Activities  GVim *
File Edit Tools Syntax Buffers Window Help
* SPICE3 file created from sky130_inv.ext - technology: sky130A
.option scale=0.01u
.include ./Libs/pshort.lib
.include ./Libs/nshort.lib
.subckt sky130_inv A Y VDD VSS
  X0 Y A VDD VSS pshort_model.0 ad=1.44n pd=0.152n as=1.37n ps=0.148n ve=35 l=23
  X1 Y VSS VDD nshort_model.0 ad=1.44n pd=0.152n as=1.52n ps=0.156n ve=37 l=23
  VDD VDD 0 3.3V
  VSS VSS 0 0V
  Va A VDD PULSE(OV 3.3V 0 0.ns 0.ns 2ns 4ns)
  C0 A Y 0.117f
  C2 Y VDD 0.117f
  C3 A Y 0.0754f
  C4 A VDD 0.279f
  C5 VDD VDD 0.45f
  C6 VDD VDD 0.781f
.ends
.tran 1n 20n
.control
  run
.endc
.end

```

Layout view of vsdshinv:



16-Mask CMOS Process Steps

- **Substrate Selection:** Selection of base layer on which other regions will be formed.
- **Create active region for transistors:** SiO₂ and si3N₂ deposited. Pockets created using photoresist and lithography.
- **Nwell & Pwell formation:** Pwell uses boron and nwell uses phosphorous. Drive in diffusion by placing in high temp furnace.

- **Creating Gate terminal:** For desired *threshold value* NA (doping Concentration) and Cox to be set.
- **Lightly Doped Drain (LDD) formation:** LDD done to avoid *hot electron effect* and *short channel effect*.
- **Source and Drain formation:** Forming the source and drain.
- **Contacts & local interconnect Creation:** SiO₂ removed using HF etch. *Titanium* deposited using sputtering.
- **Higher Level metal layer formation:** Upper layers of metals deposited.

Ngspice environment:

To enter into Ngspice : command ngspice file_name.spice

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ gvim sky130_inv.spice
*****  

** ngspice-27 : Circuit level simulation program  

** The U. C. Berkeley CAD Group  

** Copyright 1985-1994, Regents of the University of California.  

** Please get your ngspice manual from http://ngspice.sourceforge.net/docs.html  

** Please file your bug-reports at http://ngspice.sourceforge.net/bugrep.html  

** Creation Date: Tue Dec 26 17:10:20 UTC 2017  

*****  

Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a  

Scale set  

Error on line 12 :  

  va vqnd pulse(0v 3.3v 0 0.1ns 0.1ns 2ns 4ns)  

no such parameter on this device  

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000  

Warning: va: has no value, DC 0 assumed  

Initial Transient Solution  

-----  

Node          Voltage  

----  

y            3.3  

a            0  

vgnd         0  

vpwr         3.3  

var#branch   0  

vss#branch   3.32336e-12  

vdd#branch   -3.32337e-12  

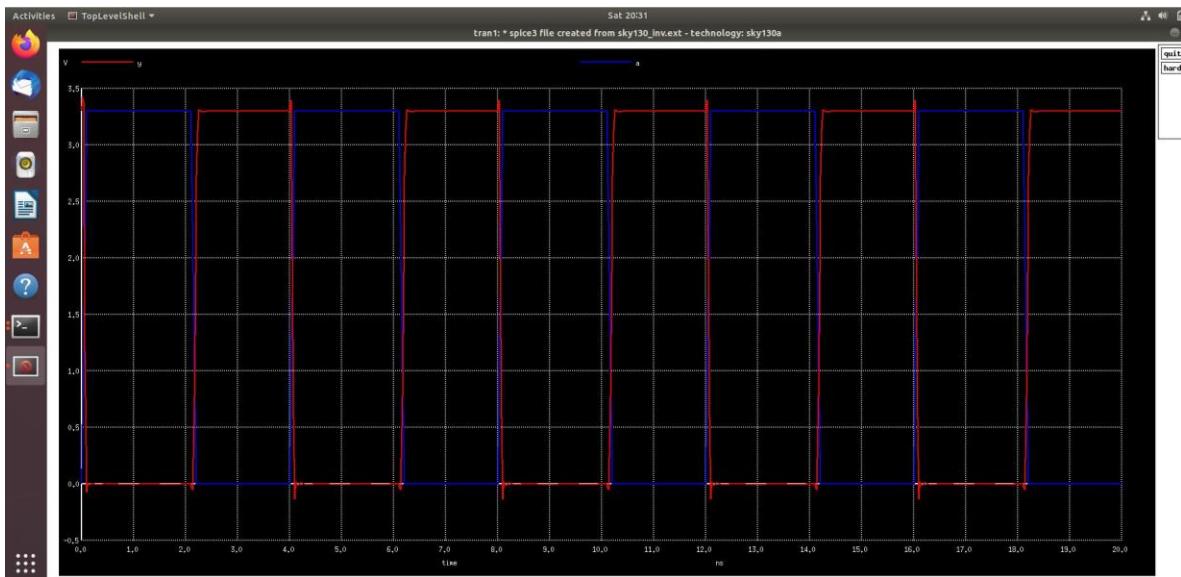
Reference value :  0.00000e+00  

::: No. of Data Rows : 59  

::: ngspice 1 -> |
```

:

Transient analysis of vsdshinv:



Day 4: Timing Analysis using Triton Clock Tree Synthesis (CTS).

Topic of Delay tables explored on Day 5. I learned that delay and output transition values of any particular cell are calculated with the help of values of *input transition* and *output load* values. Delay table and output transition table of a cell contain different value for each combination of input trans and output load, represented in form of lookup tables in liberty file. With the help of interpolation and extrapolation the values of point in range can also be calculated for precise result.

Setup & Hold Slack Analysis Setup and hold time define a window of time in which our data should remain unchanged for desired data transfer to take place. Factors like uncertainty and skew also play an important role in this. **Clock skew is the difference between Source Clock path and Destination Clock path.** Slack defined as difference between actual time and required time is monitored. Positive or zero Slack indicates no violation whereas negative slack value indicates violation of timing.

After adding vsdshinv to merged.lef file. The synthesis and floorplan is done again to get better timing results.

```

Activities Terminal Sun 15:54
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

File Edit View Search Terminal Help
sky130_fd_sc_hd_nor2_2 524
sky130_fd_sc_hd_nor2b_2 1
sky130_fd_sc_hd_nor3_2 42
sky130_fd_sc_hd_nord2_2 1
sky130_fd_sc_hd_o211a_2 2
sky130_fd_sc_hd_o211a_2 69
sky130_fd_sc_hd_o211a_2 6
sky130_fd_sc_hd_o211a_2 54
sky130_fd_sc_hd_o21a1_2 141
sky130_fd_sc_hd_o21ba_2 209
sky130_fd_sc_hd_o21ba1_2 1
sky130_fd_sc_hd_o221a_2 204
sky130_fd_sc_hd_o221a_2 7
sky130_fd_sc_hd_o221a_2 1312
sky130_fd_sc_hd_o22a1_2 59
sky130_fd_sc_hd_o22ba_2 119
sky130_fd_sc_hd_o2bb2a1_2 92
sky130_fd_sc_hd_o311a_2 8
sky130_fd_sc_hd_o31a_2 19
sky130_fd_sc_hd_o31a1_2 1
sky130_fd_sc_hd_o41a_2 109
sky130_fd_sc_hd_o41a_2 2
sky130_fd_sc_hd_or2_2 1088
sky130_fd_sc_hd_or2b_2 25
sky130_fd_sc_hd_or3_2 68
sky130_fd_sc_hd_or3b_2 5
sky130_fd_sc_hd_or4_2 93
sky130_fd_sc_hd_or4b_2 6
sky130_fd_sc_hd_or4b_2 2
sky130_vsdlnv 1554

Chip area for module '\picorv32a': 147712.918400
29. Executing Verilog backend.
Dumping module '\picorv32a'.

Warnings: 307 unique messages, 307 total
End of script. Logfile hash: 52fdd87cf0, CPU: user 48.42s system 0.36s, MEM: 96.04 MB peak
Yosys 0.9+3621 (git sha1 b4e9fa7, gcc 8.3.1 -fPIC -O5)
Time spent: 40s 2x abt (41 sec), 16% 33x opt_expr (14 sec), ...
[INFO]: Changing netlist from 0 to /openLANE_flow/designs/picorv32a/runs/04-06_10-21/results/synthesis/picorv32a.synthesis.v
[INFO]: Running static Timing Analysis...
[INFO]: Done with step layout 2
OpenSTA 2.3.0 3Bd403B3aB Copyright (c) 2019, Parallax Software, Inc.
License GPLv3+: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>
***
```

Commands to change configuration variables settings

set ::env(SYNTH_STRATEGY) 1

set ::env(SYNTH_SIZING) 1

OpenROAD Commands

read_lef /openLANE_flow/designs/picorv32a/runs/tmp/merged.lef

read_def /openLANE_flow/designs/picorv32a/runs/results/cts/picorv32a.cts.def

write_db pico12.db

read_verilog

/openLANE_flow/designs/picorv32a/runs/results/synthesis/picorv32a.synthesis_cts.v

read_liberty \$::env(LIB_SYNTH_COMPLETE)

link_design picorv32a

read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc

set_propagated_clock [all_clocks]

report_checks -path_delay min_max -digits 4

sky130_fd_sc_hd File containing layer information of Cell

```

lil X 0.23 0.46
lil Y 0.17 0.34
met1 X 0.17 0.34
met1 Y 0.17 0.34
met2 X 0.23 0.46
met2 Y 0.23 0.46
met3 X 0.34 0.68
met3 Y 0.34 0.68
met4 X 0.46 0.92
met4 Y 0.46 0.92
met5 X 1.70 3.40
met5 Y 1.70 3.40
~
~
```

Placement results of picorv32a:

```

Activities Terminal Sat 11:33
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdk/pdk5/clk...
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane...
```

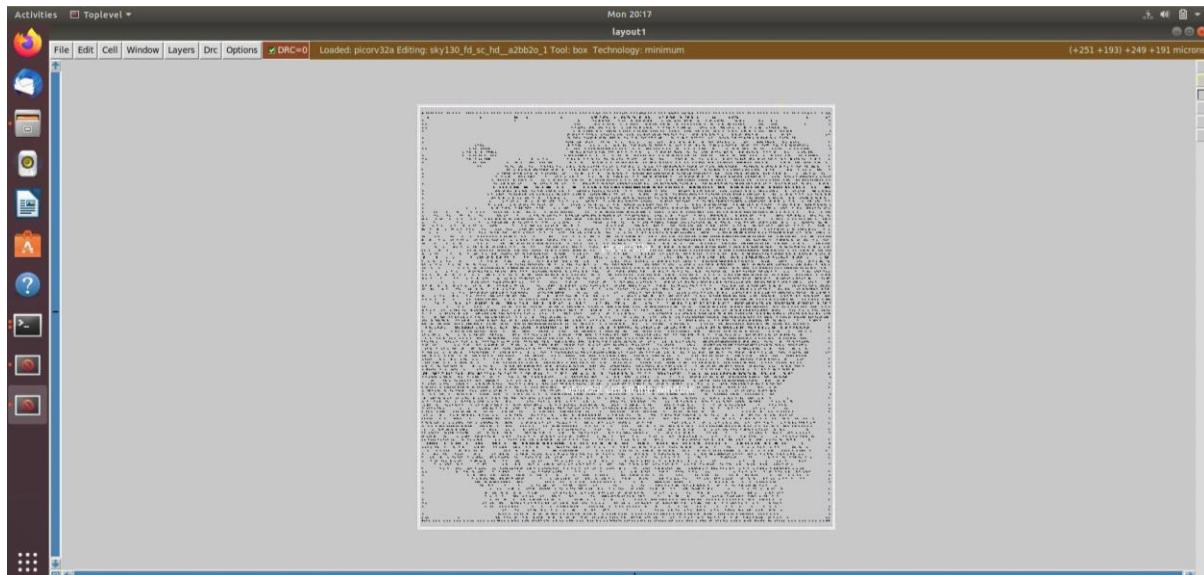
[WARNING PSM-0010] Vsrc location at (565.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 333.650um).
[WARNING PSM-0010] Vsrc location at (5.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 486.830um).
[WARNING PSM-0010] Vsrc location at (145.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 486.830um).
[WARNING PSM-0010] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 486.830um).
[WARNING PSM-0010] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 486.830um).
[WARNING PSM-0010] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 486.830um).
[WARNING PSM-0010] Vsrc location at (285.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 640.010um).
[WARNING PSM-0010] Vsrc location at (565.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 640.010um).
[INFO PSM-0031] Number of nodes on net VVWR = 20000.
[INFO PSM-0037] G matrix created sucessfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VVWR.
[WARNING PSM-0016] Voltage pad location (vsrc) file not specified, defaulting pad location to checkerboard pattern on core area.
[WARNING PSM-0017] X direction bump pitch is not specified, defaulting to 140um.
[WARNING PSM-0018] Y direction bump pitch is not specified, defaulting to 140um.
[WARNING PSM-0019] Voltage node net VGND is not explicitly set.
[WARNING PSM-0021] Using voltage 0.000V for ground network.
[INFO PSM-0026] Creating G matrix.
[INFO PSM-0028] Extracting power stripes on net VGND.
[WARNING PSM-0030] Vsrc location at (5.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 103.880um).
[WARNING PSM-0030] Vsrc location at (145.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 103.880um).
[WARNING PSM-0030] Vsrc location at (285.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 103.880um).
[WARNING PSM-0030] Vsrc location at (425.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 103.880um).
[WARNING PSM-0030] Vsrc location at (565.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 103.880um).
[WARNING PSM-0030] Vsrc location at (285.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 153.880um).
[WARNING PSM-0030] Vsrc location at (425.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 153.880um).
[WARNING PSM-0030] Vsrc location at (565.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 153.880um).
[WARNING PSM-0030] Vsrc location at (5.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 410.240um).
[WARNING PSM-0030] Vsrc location at (145.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 410.240um).
[INFO PSM-0031] Number of nodes on net VGND = 19223.
[INFO PSM-0037] G matrix created sucessfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO] pdk generation was successful.
[INFO] Changing layout from /openLANE_flow/designs/picorv32a/runs/03-06_05-05/results/floorplan/picorv32a.floorplan.def to /openLANE_flow/designs/picorv32a/runs/03-06_05-05/tmp/floorplan/7-pdn.def
1
%
% run_placement

After the run:

```

Mon 19:32
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Tabs Help
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
multi cells : 0
fixed cells : 0
total nets : 14978
design area : 4.05289e+11
total f_area : 0
total m_area : 1.4188e+11
design cell : 1.1014
num_rows : 234
row height : 2720
-----
non_group.cell_region.assign done ..
-----
non_group.cell_placement done ..
-----
Reading /openLANE_flow/designs/picorv32a/runs/04-06_07-58/tmp/placement/5-replace.def is Done
DEF file write success !!
location : /openLANE_flow/designs/picorv32a/runs/04-06_07-58/results/placement/picorv32a.placement.def
-----
tasks          Wtme   Ctime
Parmer        1.10
region assign 1.149   1.100
pre-placement 1.149   1.100
non Group cell placement 1.162   1.110
All           1.165   1.110
----- EVALUATION -----
AVG_displacement : 2242.55
SUM_displacement : 2.98753e+07
MAX_displacement : 10000
-----
GP_HPNL : 652337
HPNL : 678577
avg_Displ_site : 4.87512
avg_Displ_low : 1.82468
delta_HPNL : 4.9225
==== CHECK LEGALITY ====
row_check >>> PASS
site_check >>> PASS
power_check >>> PASS
edge_check >>> PASS
placed_check >>> PASS
overlapp_check >>> PASS
----- < Program END > -----
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/04-06_07-58/tmp/placement/5-replace.def to /openLANE_flow/designs/picorv32a/runs/04-06_07-58/results/placement/picorv32a.placement.def
%
```

Layout view of placement.def,



CTS run of Picorv32a:

Activities Terminal

TUE 16:47
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```

File Edit View Search Terminal Help
24.44  data required time
-24.85  data arrival time
-----  

-0.41  slack (VIOLATED)

wnt -16.89
tnc -346.03
Clock clk
Latency CRPR Skew
_27011 /CLK ^
4.57
_27666 /CLK ^
1.08 0.00 3.49

[INFO]: Clock Tree Synthesis was successful.
[INFO]: Cleaning Layout from /openLANE_flow/designs/picorv32a/runs/04-06_07-58/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/04-06_07-58/results/cts/picorv32a.cts.def
[INFO]: Writing Verilog...
[INFO]: current step index: 13
OpenROAD 0.9.0 1415572073
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/04-06_07-58/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 441 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/04-06_07-58/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/04-06_07-58/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 14081 components and 110827 component-terminals.
Notice 0: Created 15737 nets and 54461 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/04-06_07-58/results/cts/picorv32a.cts.def
[INFO]: Cleaning Layout from /openLANE_flow/designs/picorv32a/runs/04-06_07-58/results/synthesis/picorv32a.synthesis.cts.v
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 14
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/04-06_07-58/results/cts/picorv32a.cts.def
[INFO]: Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/klayout/sky130A.lyt
[INFO]: Reading Layout file: /openLANE_flow/designs/picorv32a/runs/04-06_07-58/results/cts/picorv32a.cts.def
[INFO]: Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/04-06_07-58/results/cts/picorv32a.cts.def.png'
Done.
[INFO]: Screenshot taken.

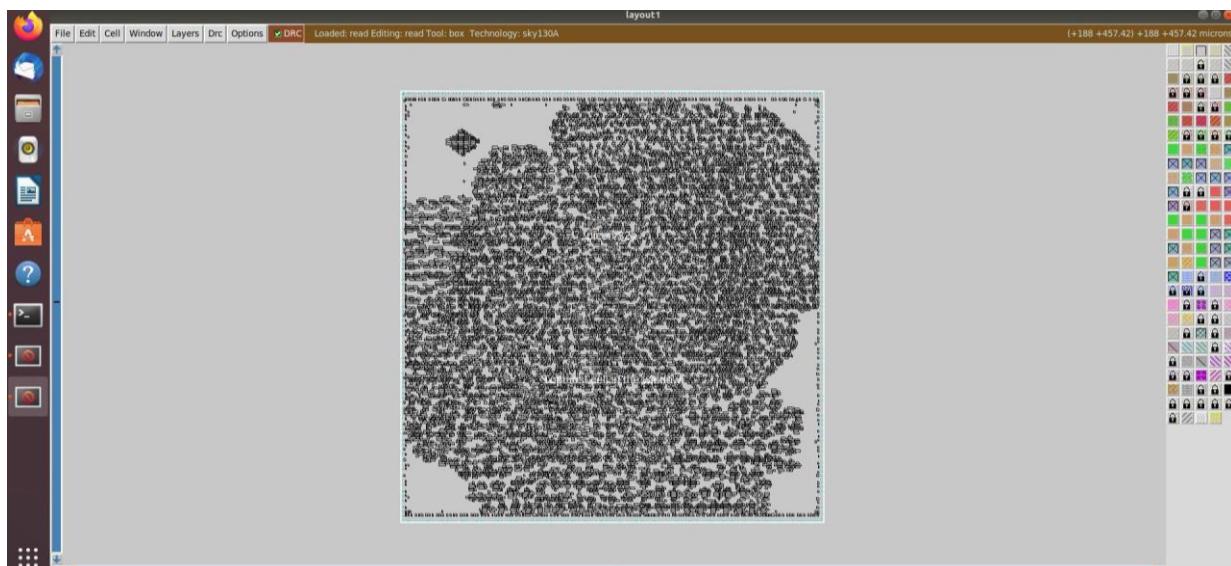
```

After CTS run,

```

%
%
%
% echo $::env(LIB_SYNTH_COMPLETE)
/openLANE_flow/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd_clkbuf_1 sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
% echo $::env(CTS_ROOT_BUFFER)
sky130_fd_sc_hd_clkbuf_16
% echo $::env(CURRENT_DEF)
/openLANE_flow/designs/picorv32a/runs/04-06_07-58/results/cts/picorv32a.cts.def
%
%
```

Layout view of picorv32a.cts.def



Day 5: Creation of Power Distribution Network, Routing and SPEF Extraction.

Routing method finds out best possible pattern for connection between two end points, of which one point is *target node* while the other is *source node*. **Maze Routing-Lee's Algorithm** was introduced. In this technique firstly routing grids are created and source & target nodes are identified. Then the blocks adjacent to one under consideration are assigned same numbers and this process is repeated till we reach the target node. Once this done the pattern with minimum number of turns preferably a L spaced pattern is finalised for route.

Typical DRC rules for pair of wires

1. Wire width
2. Wire pitch
3. Wire Spacing

These DRC rules exist because of limitations of the Lithography technique. Deviation takes place in lithography leading to changes which might lead to an unintended open circuit or short circuit and to avoid this the DRC rules are fixed. Another DRC Violation type is Signal short which can be dealt by changing layers.

Routing Technique Classified into

- **Global Route** : Performed using fast route. In this step route guides are formed.
- **Detailed Route** : Performed using *TritonRoute*.

Triton Route It performs *initial detailed route* and tries to route within the route guide provided by fast route. It works on MILF-based panel routing with intra-layer parallel route and inter-layer sequential route technique. Input files required for triton route are LEF,DEF and pre-processed route guide. Output is in form of detailed routing with optimum wire length and Via count.

Steps for pre-processed route guides

- **Initial route guide** : Basic connecting information using route guides.
- **Splitting** : Routes in non-preferred direction are split into unit width.
- **Merging** : Touching guides have edge orthogonal to the preferred route guide direction are merged.
- **Bridging** : Edges parallel to preferred one are bridged using additional layers.
- **Pre-processed Route** : Now all route guides are in preferred direction as required.



Routing result of picorv32a:

Command : run_routing

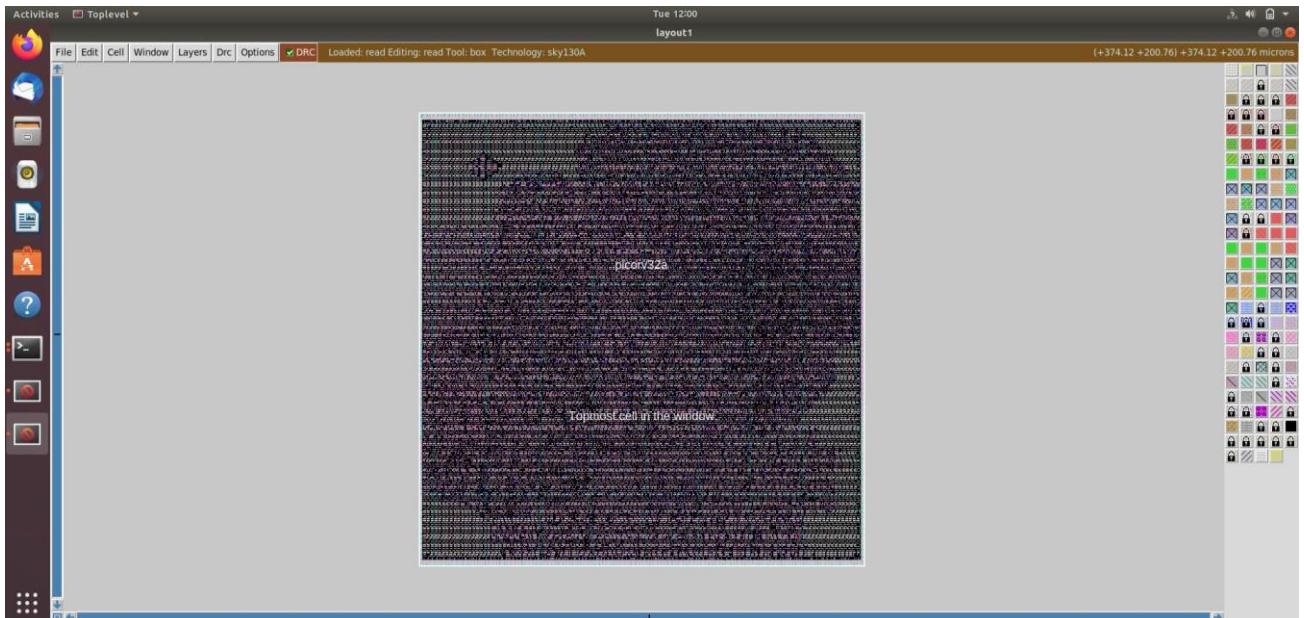
```

Activities Terminal Tue 1148
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Tabs Help
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane * vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/04-06_07-58/tmp
Edge Capacitance Factor: 1.0
Wire model: L

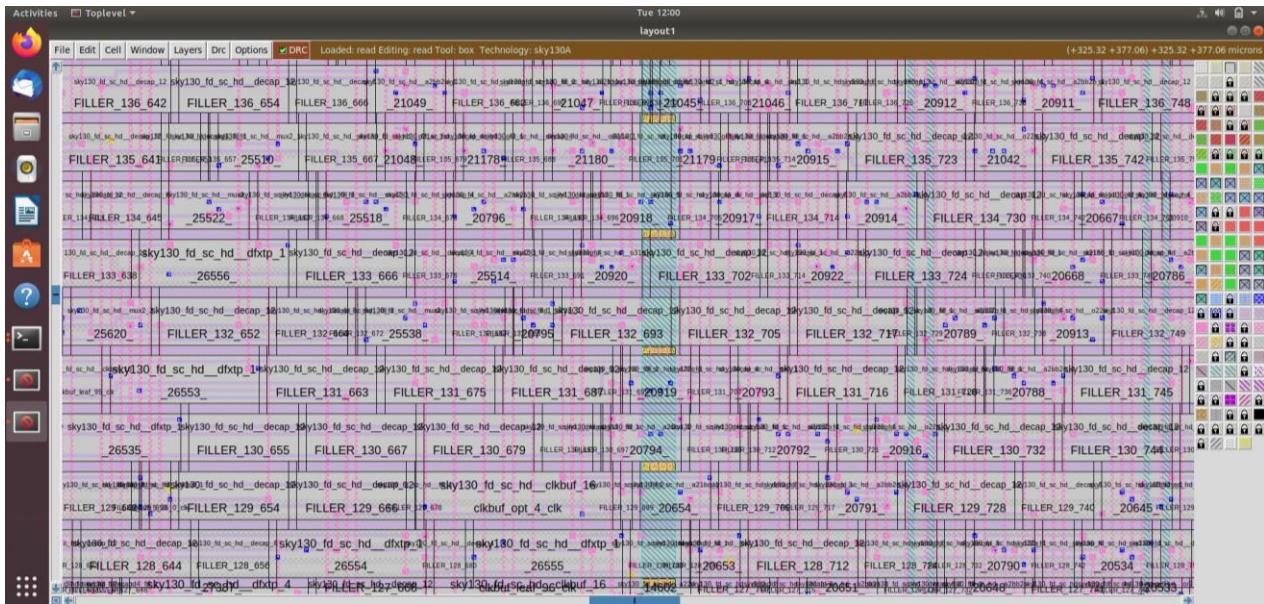
RC Extraction is done
Start writing SPICE file
Writing SPICE is done
[INFO]: Running Static Timing Analysis...
[INFO]: current step index: 22
OpenSTA 2.3.0 38b40303a8 Copyright (c) 2019, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type 'show_copyright' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type 'show warranty'.
Warning: /openLANE_flow/designs/picorv32a/runs/04-06_07-58/results/synthesis/picorv32a.synthesis_preroute.v line 54857, module sky130_fd_sc_hd_fill_2 not found. Creating black box for FILLER_0_8.
Warning: /openLANE_flow/designs/picorv32a/runs/04-06_07-58/results/synthesis/picorv32a.synthesis_preroute.v line 54859, module sky130_fd_sc_hd_fill_1 not found. Creating black box for FILLER_0_22.
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set_input_delay 0.0 [get_clocks $::env(CLOCK_PORT)] -clock $::env(CLOCK_PERIOD)
set_output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(TD_PCT)]
puts "[INFO]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.9466000000000001
puts "[INFO]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.9466000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_max_fanout $::env(SYNTH_MAX_FANOUT) [all_outputs [get_clocks $::env(CLOCK_PORT)]]
#set_rst_idx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_idx $clk_idx]
set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_idx $rst_idx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_max_cap_load [all_outputs]
tns -309.72
wns -14.97
[INFO]: Calculating Runtime From the Start...
[INFO]: Routing completed for picorv32a/05-06_13-33 in 16h45m2s
%
```

Layout view of picorv32a_routing.def,



Detailed view of design,



Acknowledgements

- Kunal Ghosh, Co-founder (VSD Corp. Pvt. Ltd).
 - Nickson Jose - Workshop Instructor