Microelectronics & VLSI design

Lab Assignment

By: -

SHASHWAT PRATAP

2019UGEC030R

EXPERIMENT-1

AIM: - To obtain Transient analysis of INVERTER using CMOS.

Components Required: - PMOS, NMOS, Voltage source, Tanner tools

Theory: -

In CMOS (Complementary Metal-oxide Semiconductor). technology, both N-type and P-type transistors are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type.

In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail (Vss or quite often ground). Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named Vdd).

Thus, if both p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be ON when the n-type MOSFET is OFF, and vice-versa. The networks are arranged such that one is ON and the other OFF for any input pattern.

NMOS-

NMOS is built on a p-type substrate with n-type source and drain diffused on it. In NMOS, the majority of carriers are electrons. When a high voltage is applied to the gate, the NMOS will conduct. Similarly, when a low voltage is applied to the gate, NMOS will not conduct. NMOS is considered to be faster than PMOS, since the carriers in NMOS, which are electrons, travel twice as fast as the holes.

PMOS-

P- channel MOSFET consists of P-type Source and Drain diffused on an N-type substrate. The majority of carriers are holes. When a high voltage is applied to the gate, the PMOS will not conduct. When a low voltage is applied to the gate, the

PMOS will conduct. The PMOS devices are more immune to noise than NMOS devices.

CMOS(INVERTER) Working Principle: -

A CMOS inverter is a field-effect transistor that is composed of a metal gate that lies on top of an insulating layer of oxygen, which lies on top of a semiconductor.

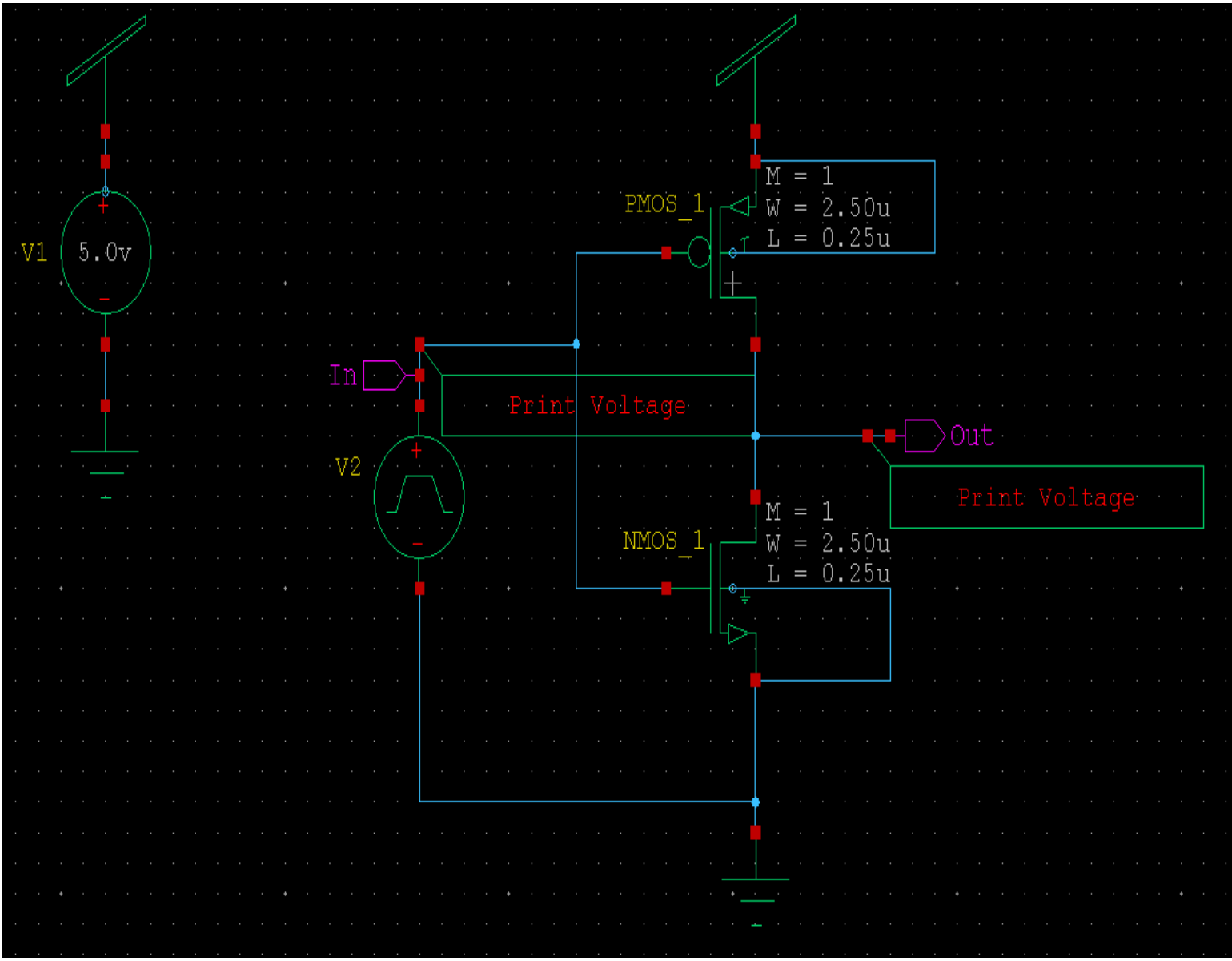
The inverter circuit consists of PMOS and NMOS. The input A serves as the gate voltage for both transistors.
The NMOS transistor has input from Vss (ground) and the PMOS transistor has input from Vdd. The terminal Y is output. When a high voltage (~ Vdd) is given at input terminal (A) of the inverter, the PMOS becomes an open circuit, and NMOS switched OFF so the output will be pulled down to Vss.

When a low-level voltage (<Vdd, ~0v) applied to the inverter, the NMOS switched OFF and PMOS switched ON. So the output becomes Vdd or the circuit is pulled up to Vdd.

INPUT	LOGIC INPUT	OUTPUT	LOGIC OUTPUT
0 v	0	Vdd	1
Vdd	1	0 v	0

Schematic: -

S-Edit



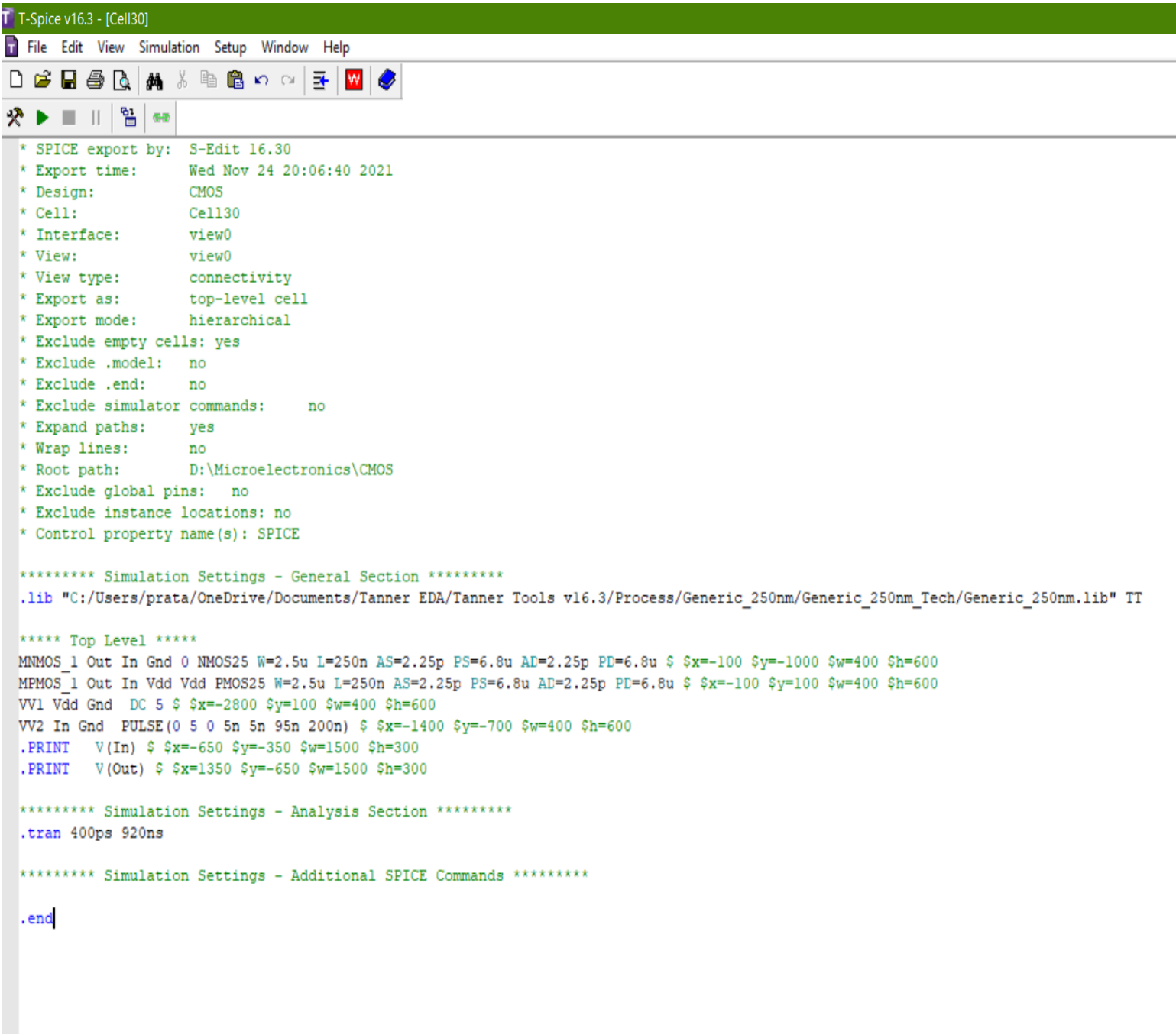
Transient Analysis: -

Maximum time step = 400 ps

Stop time = 920 ns

IN Voltage = 5V

T-Edit



Device and node counts:

MOSFETs - 2

MOSFET geometries - 2

Voltage sources - 2

Subckt Definitions - 1

Model Definitions - 6

Computed Models - 2

Independent nodes - 1

Boundary nodes - 3

Total nodes - 4

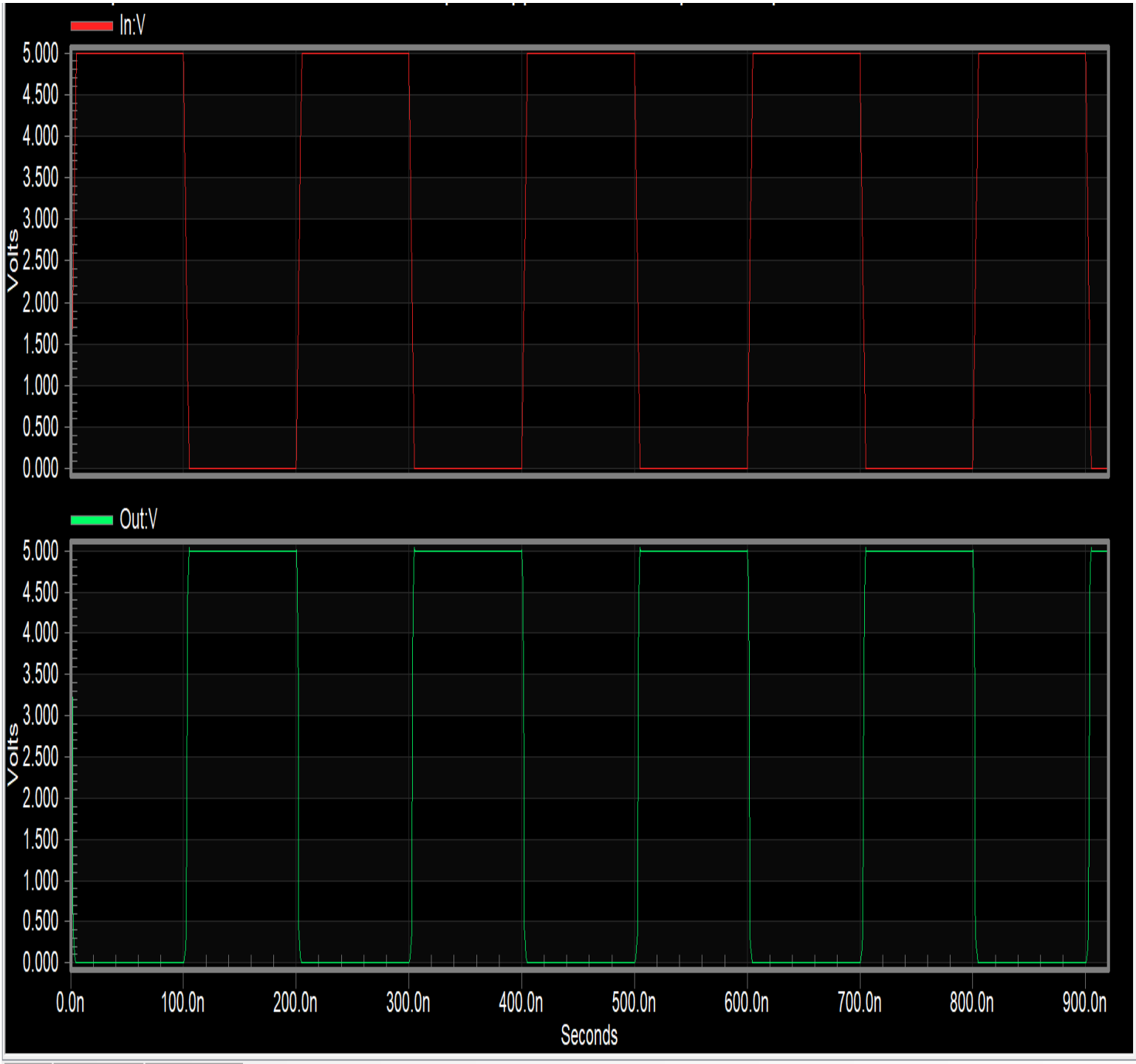
Opening simulation database "C:\Users\prata\AppData\Local\Temp\Cell30.tsim"

Parsing	0.13 seconds
Setup	0.04 seconds
DC operating point	0.02 seconds
Transient Analysis	0.14 seconds
Overhead	0.40 seconds

Total	0.74 seconds

Simulation completed

WAVEFORM- OUTPUT


In:V
5.000
4.500
4.000
3.500
3.000
2.500
2.000
1.500
1.000
0.500
0.000
Volts
Out:V
5.000
4.500
4.000
3.500
3.000
2.500
2.000
1.500
1.000
0.500
0.000
Volts
0.0n
100.0n
200.0n
300.0n
400.0n
500.0n
600.0n
700.0n
800.0n
900.0n
Seconds

EXPERIMENT-2

AIM: - To obtain DC sweep analysis of INVERTER using CMOS.

Components Required: - PMOS, NMOS, Voltage source, Tanner tools

Theory: -

In CMOS (Complementary Metal-oxide Semiconductor). technology, both N-type and P-type transistors are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type.

In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail (Vss or quite often ground). Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named Vdd).

Thus, if both p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be ON when the n-type MOSFET is OFF, and vice-versa. The networks are arranged such that one is ON and the other OFF for any input pattern.

NMOS-

NMOS is built on a p-type substrate with n-type source and drain diffused on it. In NMOS, the majority of carriers are electrons. When a high voltage is applied to the gate, the NMOS will conduct. Similarly, when a low voltage is applied to the gate, NMOS will not conduct. NMOS is considered to be faster than PMOS, since the carriers in NMOS, which are electrons, travel twice as fast as the holes.

PMOS-

P- channel MOSFET consists of P-type Source and Drain diffused on an N-type substrate. The majority of carriers are holes. When a high voltage is applied to the gate, the PMOS will not conduct. When a low voltage is applied to the gate, the PMOS will conduct. The PMOS devices are more immune to noise than NMOS devices.

CMOS(INVERTER) Working Principle: -

A CMOS inverter is a field-effect transistor that is composed of a metal gate that lies on top of an insulating layer of oxygen, which lies on top of a semiconductor.

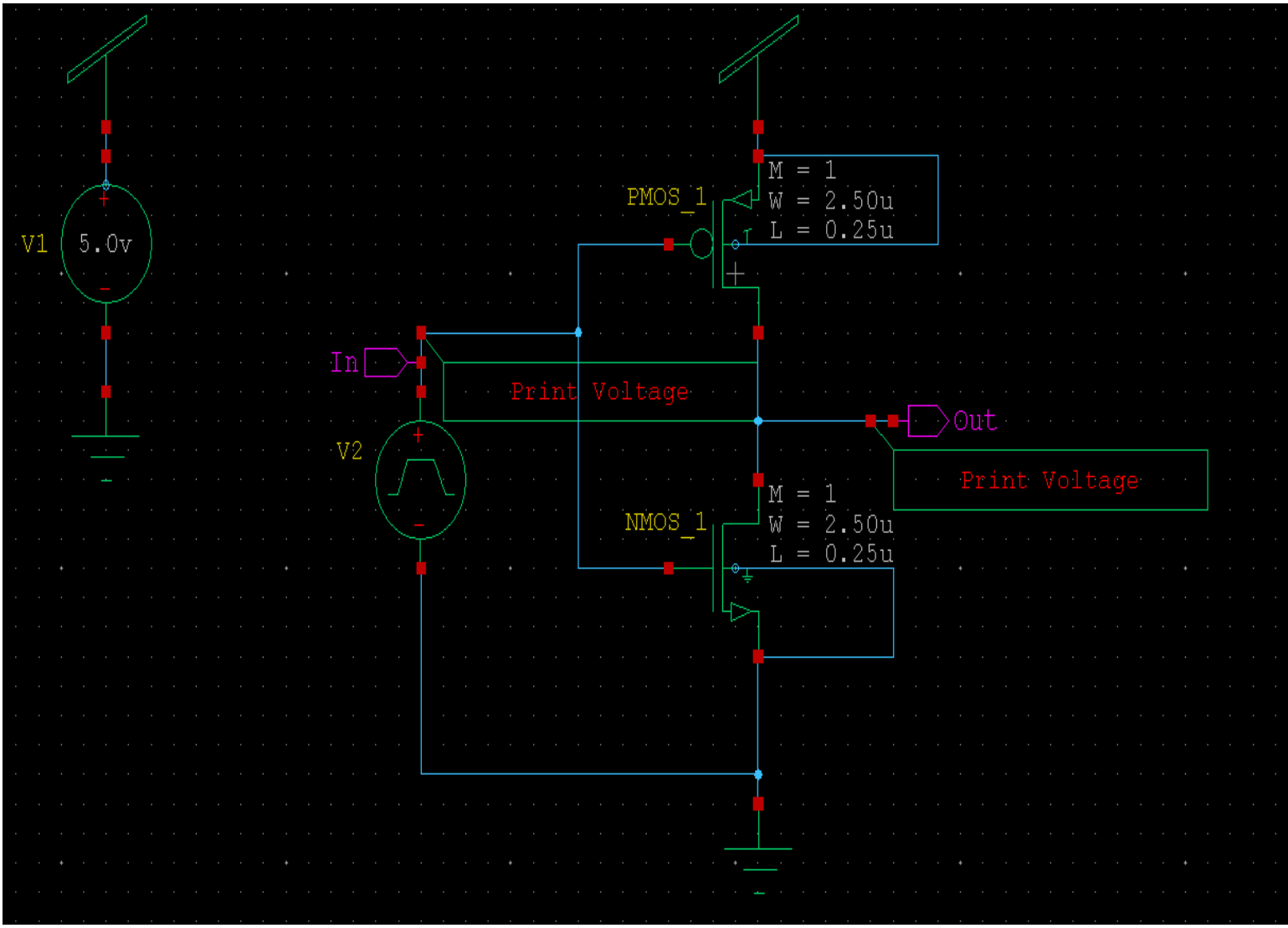
The inverter circuit consists of PMOS and NMOS. The input A serves as the gate voltage for both transistors.
The NMOS transistor has input from Vss (ground) and the PMOS transistor has input from Vdd. The terminal Y is output. When a high voltage (~ Vdd) is given at input terminal (A) of the inverter, the PMOS becomes an open circuit, and NMOS switched OFF so the output will be pulled down to Vss.

When a low-level voltage (<Vdd, ~0v) applied to the inverter, the NMOS switched OFF and PMOS switched ON. So the output becomes Vdd or the circuit is pulled up to Vdd.

INPUT	LOGIC INPUT	OUTPUT	LOGIC OUTPUT
0 v	0	Vdd	1
Vdd	1	0 v	0

Schematic: -

S-Edit



DC sweep Analysis: -

Source/parameter name = V2

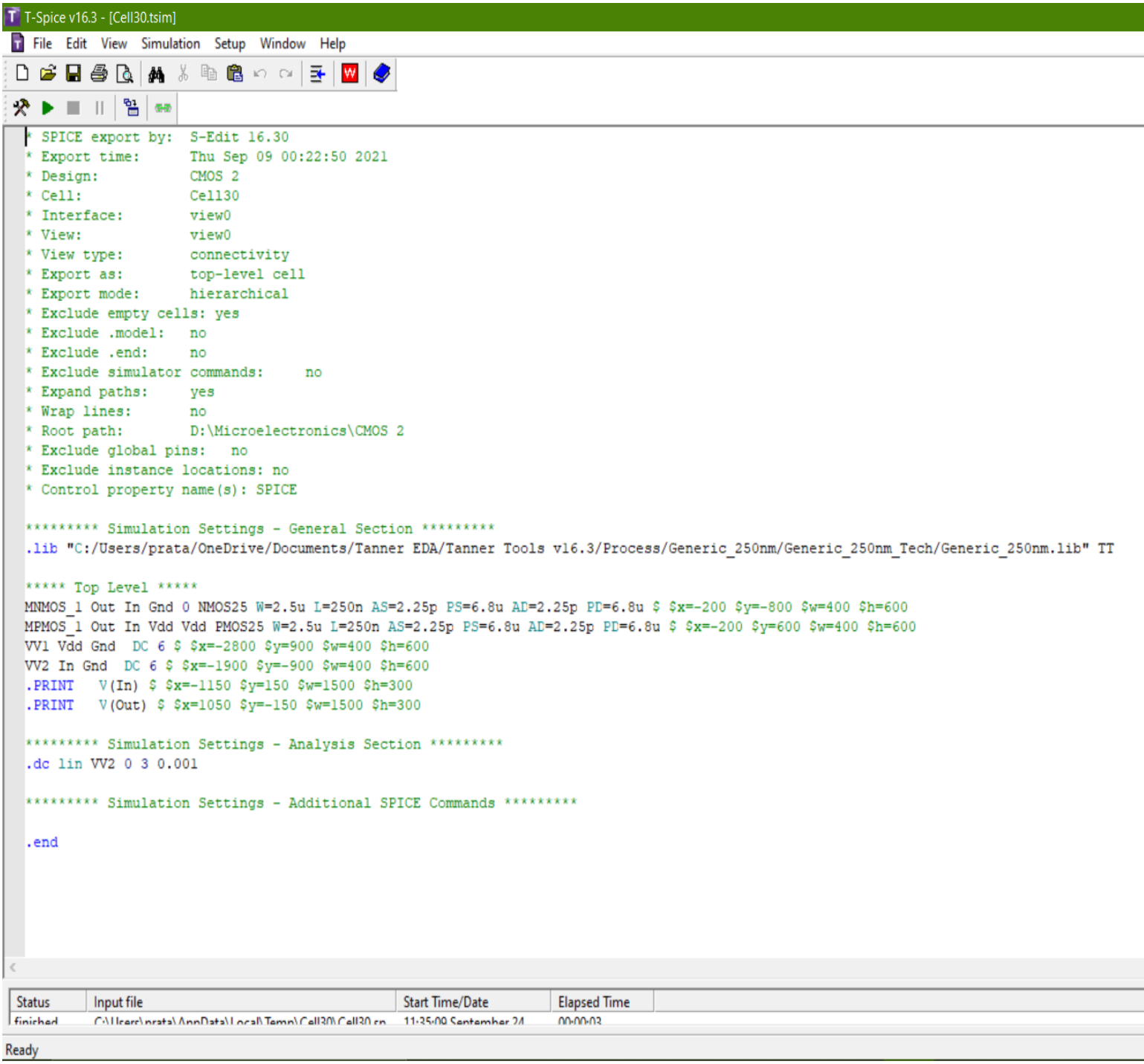
Start value = 0V

Stop value = 3V

Step = 0.001s

Sweep type = linear

T-Edit



Device and node counts:

MOSFETs - 2

MOSFET geometries - 2

Voltage sources - 2

Subckt Definitions - 1

Model Definitions - 6

Computed Models - 2

Independent nodes - 1

Boundary nodes - 3

Total nodes - 4

Opening simulation database "C:\Users\prata\AppData\Local\Temp\Cell30.tsim"

Parsing 0.26 seconds

Setup 0.04 seconds

DC operating point 0.03 seconds

DC Analysis 0.34 seconds

Overhead 0.29 seconds

Total 0.96 seconds

Simulation completed

WAVEFORM- OUTPUT

EXPERIMENT-3

AIM: - To obtain Transient analysis of NAND GATE using CMOS.

Components Required: - PMOS, NMOS, Voltage source, Tanner tools

Theory: -

In CMOS (Complementary Metal-oxide Semiconductor). technology, both N-type and P-type transistors are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type.

In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail (Vss or quite often ground). Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named Vdd).

Thus, if both p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be ON when the n-type MOSFET is OFF, and vice-versa. The networks are arranged such that one is ON and the other OFF for any input pattern.

NMOS-

NMOS is built on a p-type substrate with n-type source and drain diffused on it. In NMOS, the majority of carriers are electrons. When a high voltage is applied to the gate, the NMOS will conduct. Similarly, when a low voltage is applied to the gate, NMOS will not conduct. NMOS is considered to be faster than PMOS, since the carriers in NMOS, which are electrons, travel twice as fast as the holes.

PMOS-

P- channel MOSFET consists of P-type Source and Drain diffused on an N-type substrate. The majority of carriers are holes. When a high voltage is applied to the gate, the PMOS will not conduct. When a low voltage is applied to the gate, the PMOS will conduct. The PMOS devices are more immune to noise than NMOS devices.

CMOS (NAND GATE) Working Principle: -

It is a 2-input Complementary MOS NAND gate. It consists of two series NMOS transistors between OUT and Ground and two parallel PMOS transistors between OUT and VDD.

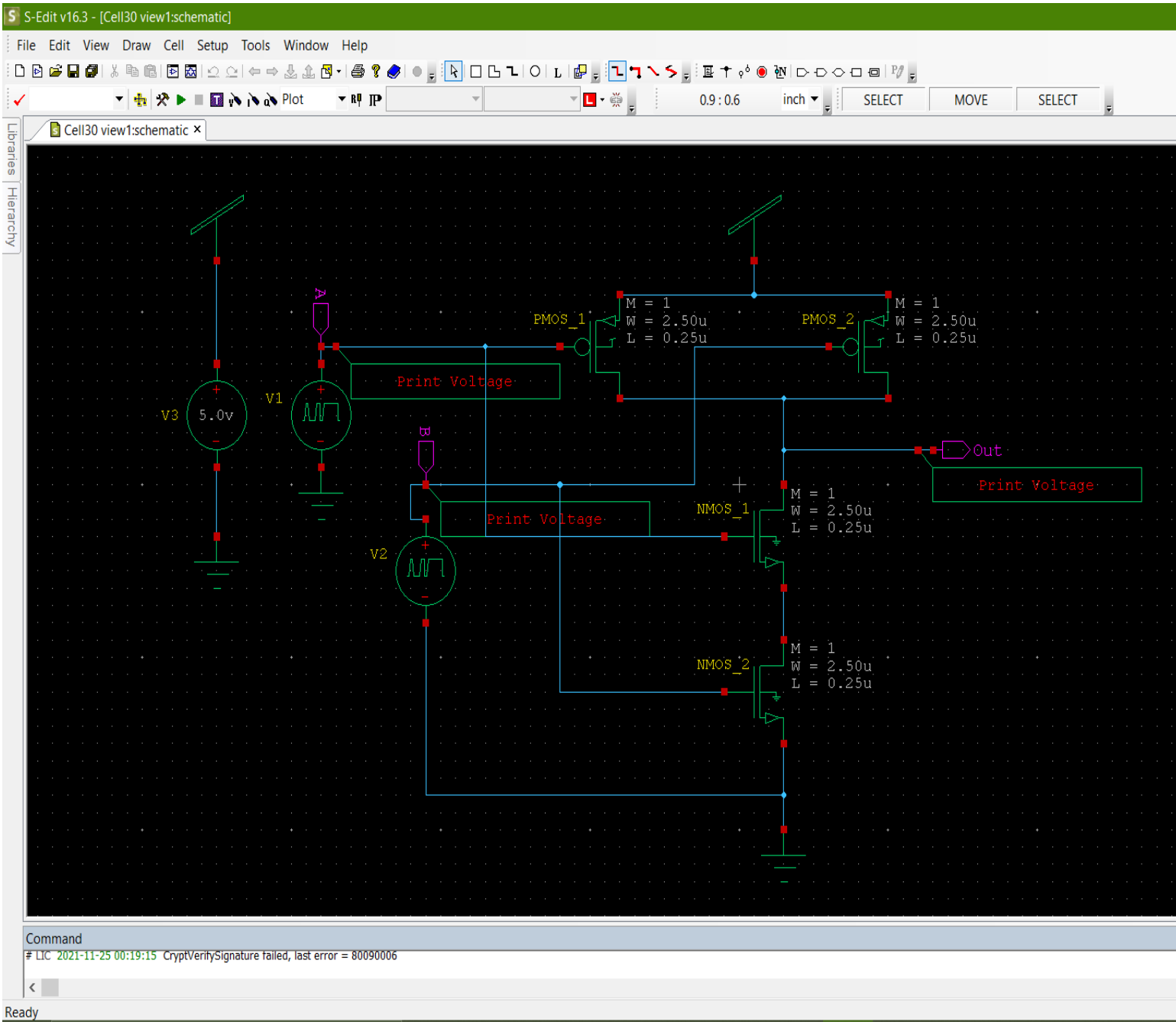
If either input A or B is logic 0, at least one of the NMOS transistors will be OFF, breaking the path from Y to Ground. But at least one of the pMOS transistors will be ON, creating a path from OUT to VDD.

Hence, the output (OUT) will be high. If both inputs are high, both of the nMOS transistors will be ON and both of the pMOS transistors will be OFF. Hence, the output will be logic low. The truth table of the NAND logic gate given in the below table.

A	B	Pull-Down Network	Pull-up Network	OUT
0	0	OFF	ON	1
0	1	OFF	ON	1
1	0	OFF	ON	1
1	1	ON	OFF	0

Schematic: -

S-Edit



Transient Analysis: -

Maximum time step = 10 ns

Stop time = 100 ns

IN Voltage(A) = 0110101111

IN Voltage (B)= 0110101011

T-Edit

T-Spice v16.3 - [Cell30 *]

File Edit View Simulation Setup Window Help

```
* SPICE export by:  S-Edit 16.30
* Export time:      Thu Nov 25 00:25:20 2021
* Design:           NAND
* Cell:             Cell30
* Interface:        view0
* View:             view1
* View type:        connectivity
* Export as:        top-level cell
* Export mode:      hierarchical
* Exclude empty cells: yes
* Exclude .model:   no
* Exclude .end:     no
* Exclude simulator commands:     no
* Expand paths:     yes
* Wrap lines:       no
* Root path:        D:\Microelectronics\NAND
* Exclude global pins:   no
* Exclude instance locations: no
* Control property name(s): SPICE

********* Simulation Settings - General Section *********
.probe
.option probev
.lib "C:/Users/prata/OneDrive/Documents/Tanner EDA/Tanner Tools v16.3/Process/Generic_250nm/Generic_250nm_Tech/Generic_250nm.lib" TT

***** Top Level *****
MNMOS_1 Out A N_1 0 NMOS25 W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=100 $y=-300 $w=400 $h=600
MNMOS_2 N_1 B Gnd 0 NMOS25 W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=100 $y=-1200 $w=400 $h=600
MPMOS_1 Out A Vdd Vdd PMOS25 W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=-1000 $y=800 $w=400 $h=600
MPMOS_2 Out B Vdd Vdd PMOS25 W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=800 $y=800 $w=400 $h=600
VV3 Vdd Gnd  DC 5 $ $x=-3500 $y=400 $w=400 $h=600
VV1 A Gnd  BIT({0110101111} ) $ $x=-2800 $y=400 $w=400 $h=600
VV2 B Gnd  BIT({0110101011} ) $ $x=-2100 $y=-500 $w=400 $h=600
.PRINT   V(A) $ $x=-1950 $y=650 $w=1500 $h=300
.PRINT   V(B) $ $x=-1350 $y=-150 $w=1500 $h=300
.PRINT   V(Out) $ $x=1950 $y=50 $w=1500 $h=300

********* Simulation Settings - Analysis Section *********
.tran 10n 100n

********* Simulation Settings - Additional SPICE Commands *********
```

Status	Input file	Start Time/Date	Elapsed Time
finished	C:\Users\prata\AppData\Local\Temp\Cell30\Cell30.sp	11:35:09 September 24	00:00:03

Ready

Device and node counts:

MOSFETs -	4
MOSFET geometries -	2
Voltage sources -	3
Subckt Definitions -	1
Model Definitions -	6
Computed Models -	2
Independent nodes -	2
Boundary nodes -	4
Total nodes -	**6**

Opening simulation database "C:\Users\prata\AppData\Local\Temp\Cell30.tsim"

Parsing	0.16 seconds
Setup	0.15 seconds
DC operating point	0.04 seconds
Transient Analysis	0.08 seconds
Output	0.02 seconds
Overhead	0.69 seconds
---	---
Total	**1.13 seconds**

Simulation completed

WAVEFORM- OUTPUT

EXPERIMENT-4

AIM: - To obtain Transient analysis of EXOR GATE using CMOS.

Components Required: - PMOS, NMOS, Voltage source, Tanner tools

Theory: -

In CMOS (Complementary Metal-oxide Semiconductor). technology, both N-type and P-type transistors are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type.

Thus, if both p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be ON when the n-type MOSFET is OFF, and vice-versa. The networks are arranged such that one is ON and the other OFF for any input pattern. In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail (Vss or quite often ground). Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named Vdd).

NMOS-

NMOS is built on a p-type substrate with n-type source and drain diffused on it. In NMOS, the majority of carriers are electrons. When a high voltage is applied to the gate, the NMOS will conduct. Similarly, when a low voltage is applied to the gate, NMOS will not conduct. NMOS is considered to be faster than PMOS, since the carriers in NMOS, which are electrons, travel twice as fast as the holes.

PMOS-

P- channel MOSFET consists of P-type Source and Drain diffused on an N-type substrate. The majority of carriers are holes. When a high voltage is applied to the gate, the PMOS will not conduct. When a low voltage is applied to the gate, the

PMOS will conduct. The PMOS devices are more immune to noise than NMOS devices.

CMOS (XOR GATE) Working Principle: -

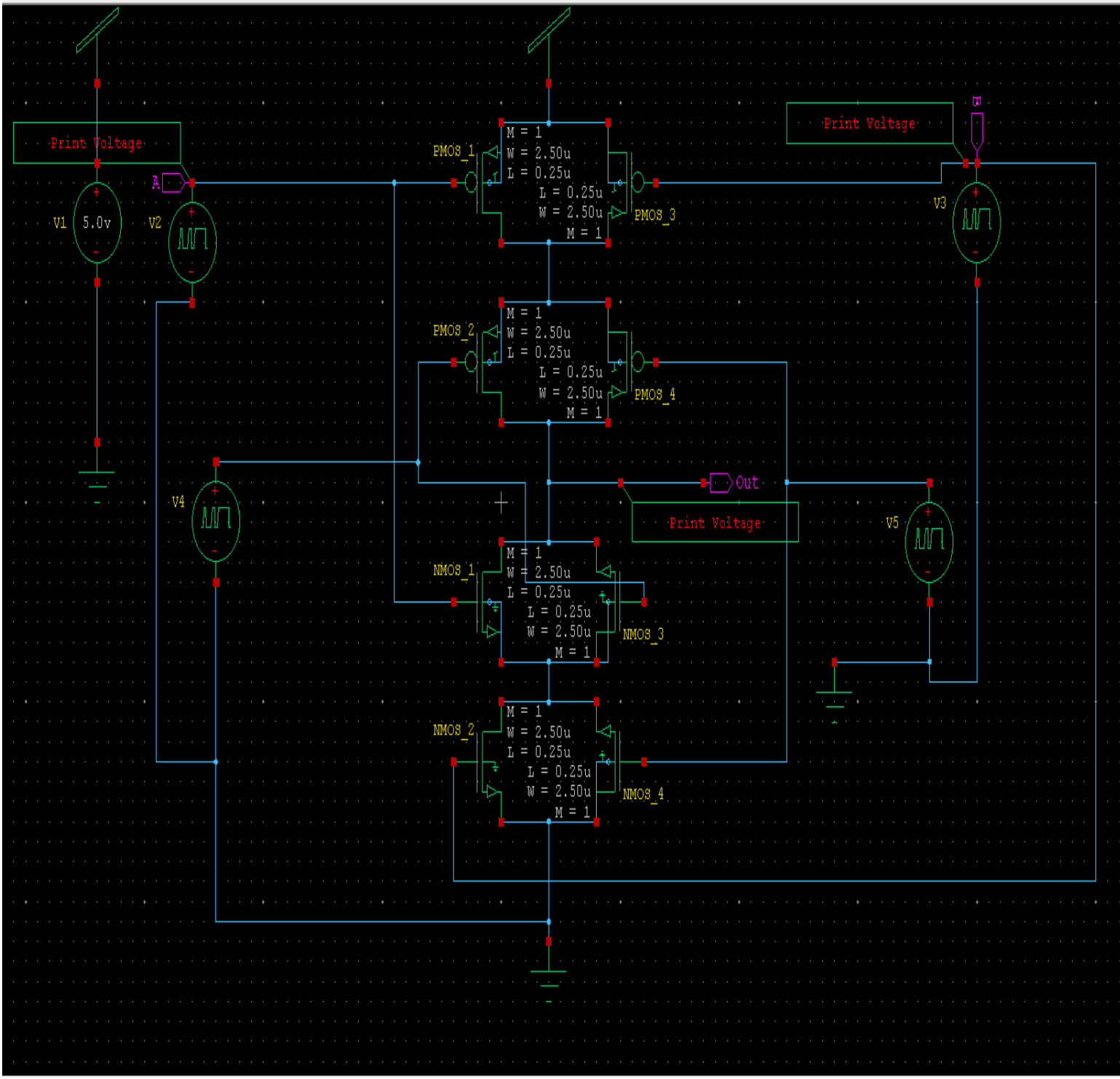
In an XOR circuit, the output is a logic 1 when one and only one input is a logic 1. Hence the output is logic 0 when both inputs are logic 1 or logic 0 simultaneously.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

A logic statement to express the XOR gate is as follows: If A = 1 and B = 0, or if B = 1 and A = 0, then Y = 1. In Boolean notation.

Schematic: -

S-Edit



Transient Analysis: -

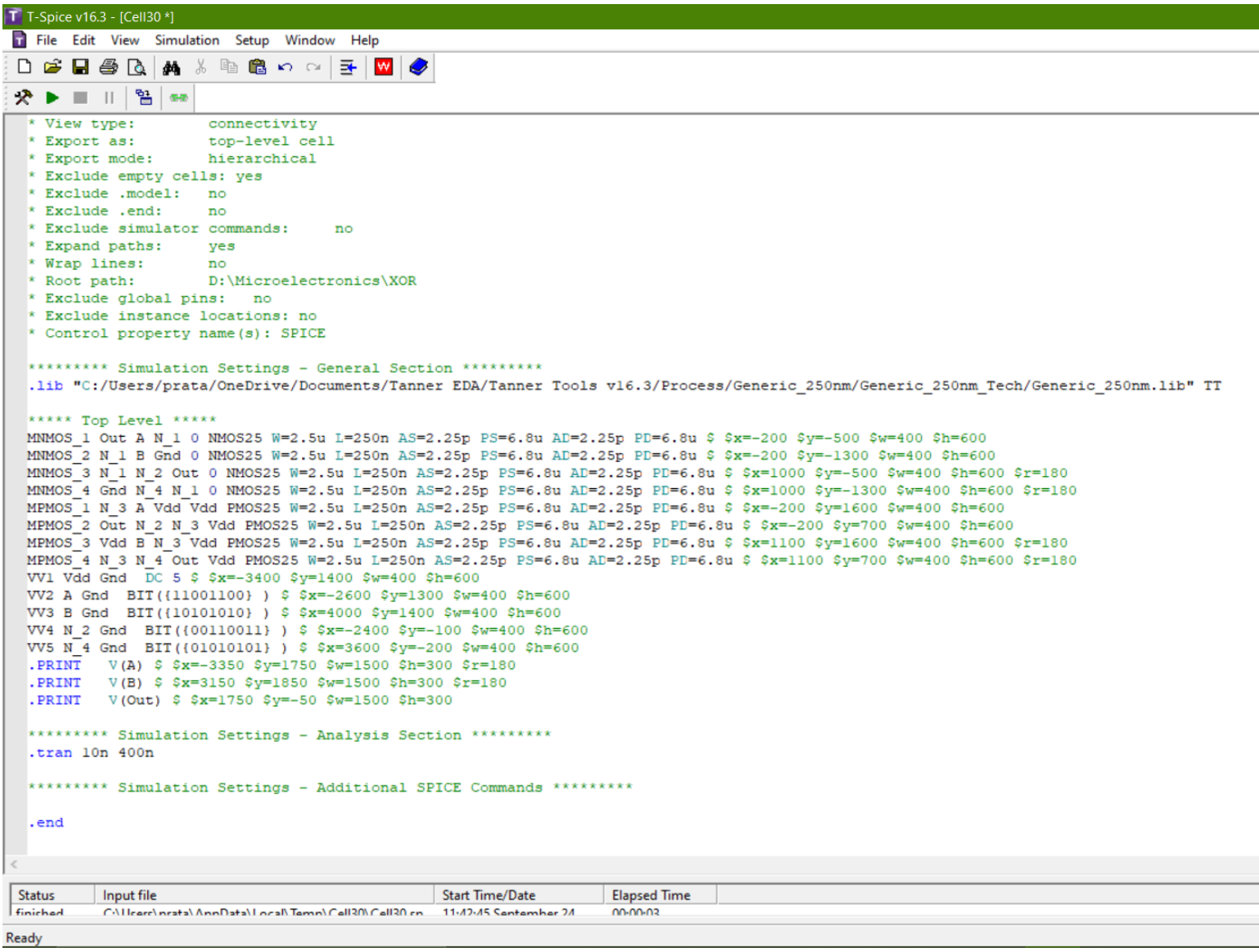
Maximum time step = 10 ns

Stop time = 400 ns

IN Voltage (A) = 11001100

IN Voltage (B) = 10101010

T-Edit



Device and node counts:

MOSFETs - 8

MOSFET geometries - 2

Voltage sources - 5

Subckt Definitions - 1

Model Definitions - 6

Computed Models - 2

Independent nodes - 3

Boundary nodes - 6

Total nodes - 9

Opening simulation database "C:\Users\prata\AppData\Local\Temp\Cell30.tsim"

Parsing 0.11 seconds

Setup 0.03 seconds

DC operating point 0.04 seconds

Transient Analysis 0.19 seconds

Overhead 0.38 seconds

Total 0.74 seconds

Simulation completed

WAVEFORM- OUTPUT

EXPERIMENT-5

AIM: - To obtain Transient analysis of 2:1 Multiplexer using Transmission Gate

Components Required: - PMOS, NMOS, Voltage source, Tanner tools

Theory: -

A **transmission gate** (**TG)**, or analog switch, is defined as an electronic element that will selectively block or pass a signal level from the input to the output. This solid-state switch is comprised of a pMOS transistor and nMOS transistor. The control gates are biased in a complementary manner so that both transistors are either on or off. It is an analog gate similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential. It is a CMOS-based switch, in which PMOS passes a strong 1 but poor 0, and NMOS passes strong 0 but poor 1. Both PMOS and NMOS work simultaneously.

Transmission gates are typically used as building blocks for logic circuitry, such as a D Latch or D Flip-Flop. As a stand-alone circuit, a transmission gate can isolate a component or components from live signals during hot insertion or removal.

In principle, a transmission gate is made up of two FET, in which – in contrast to traditional discrete field-effect transistors – the substrate terminal (bulk) is not connected internally to the source terminal. The two transistors, an n-channel MOSFET and a p-channel MOSFET, are connected in parallel with this, however, only the drain and source terminals of the two transistors are connected together. Their gate terminals are connected to each other by a NOT gate to form the control terminal.

TRANSMISSION GATE (TG) Working Principle: -

When the ***control input is a logic 0***, the gate of the n-channel MOSFET is also at a negative supply voltage potential. The gate terminal of the p-channel MOSFET is caused by the inverter, to the positive supply voltage potential. Regardless of on which switching terminal of the transmission gate a voltage is applied, the gate-source voltage of the n-channel MOSFETs is always negative, and the p-channel MOSFETs is always positive. Accordingly, neither of the two transistors will conduct and the transmission gate turns off.

When the ***control input is a logic 1***, the gate terminal of the n-channel MOSFETs is located at a positive supply voltage potential. By the inverter, the gate terminal of the p-channel MOSFETs is now at a negative supply voltage potential. As the substrate terminal of the transistors is not connected to the source terminal, the drain and source terminals are almost equal and the transistors start conducting at a voltage difference between the gate terminal and one of these conducts.

One of the switching terminals of the transmission gate is raised to a voltage near the negative supply voltage, a positive gate-source voltage (gate-to-drain voltage) will occur at the N-channel MOSFET, and the transistor begins to conduct, and the transmission gate conducts. The voltage at one of the switching terminals of the transmission gate is now raised continuously up to the positive supply voltage potential, so the gate-source voltage is reduced (gate-drain voltage) on the n-channel MOSFET, and this begins to turn off. At the same time, the p-channel MOSFET has a negative gate-source voltage (gate-to-drain voltage) builds up, whereby this transistor starts to conduct and the transmission gate switches.

Advantages of using transmission gate logic: -

- A CMOS transmission gate can be constructed by parallel combination of nMOS and pMOS transistors, with complementary gate signals.
- The main advantage of CMOS transmission gate compared to nMOS transmission gate is to allow the input signal to be transmitted to the output without the threshold voltage attenuation.
- It allows full rail transition i.e. ratioless logic
- The equivalent resistance is relatively constant during transition.
- Some gates are efficient implemented using transmission gate.

2:1 MUX (TG) Working Principle: -

A 2:1 multiplexer can be implemented using transmission gates. Figure below shows the connection diagram of the 2:1 multiplexer using transmission gates. The 2:1 MUX selects either A or B depending upon the **control signal C.** This is equivalent to implementing the Boolean function,

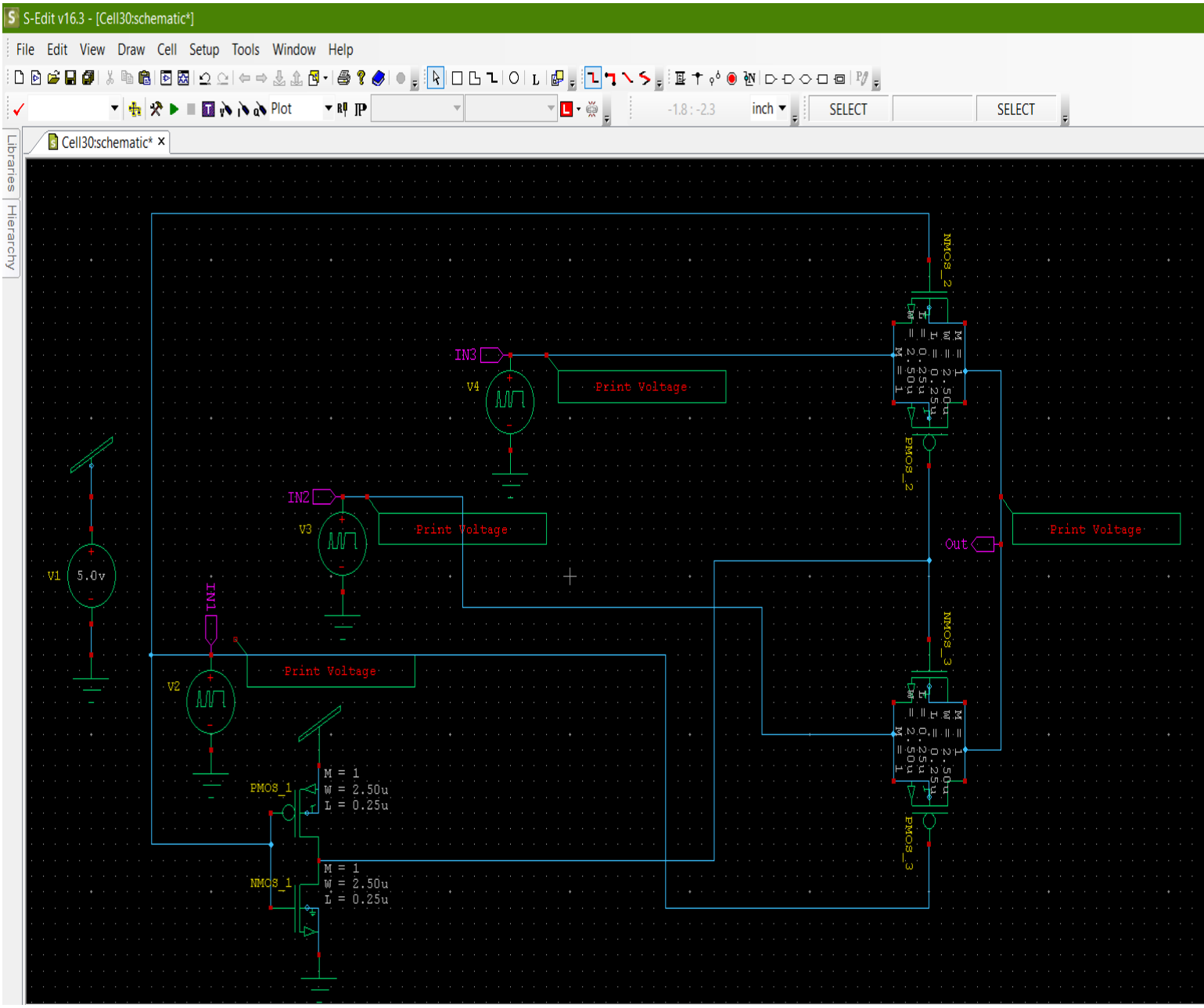
When the **control signal C is high** then the upper transmission gate is ON and it passes A through it so that **output = A.**

When the **control signal C is low** then the upper transmission gate turns OFF and it will not allow A to pass through it, at the same time the lower transmission gate is 'ON' and it allows B to pass through it so the **output = B**.

CONTROL	**A**	**B**	**LOGIC OUTPUT**
0	OPEN	CLOSED	A
1	CLOSED	OPEN	B

Schematic: -

S-Edit



Transient Analysis: -

Maximum time step = 10 ps

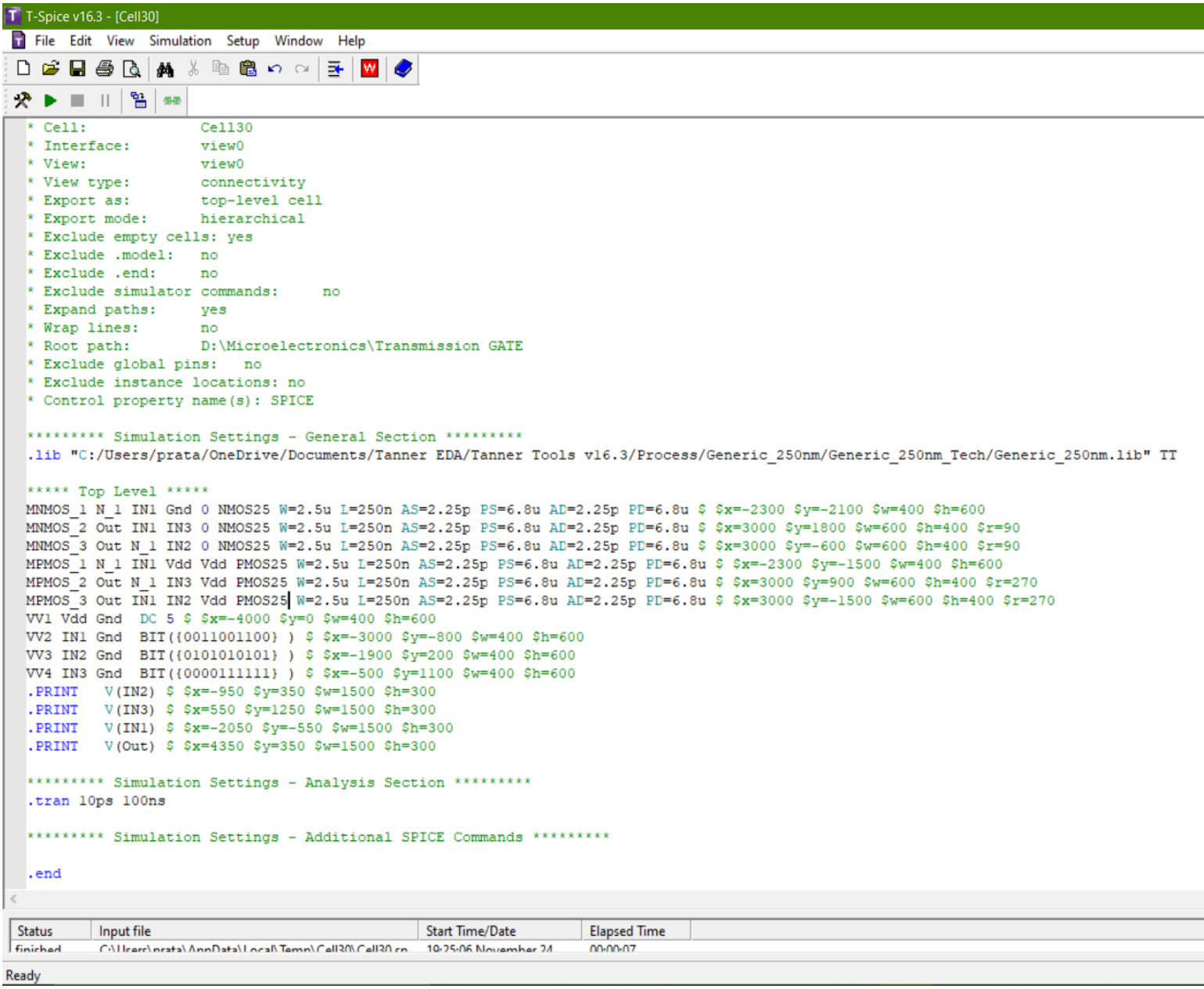
Stop time = 100 ns

IN Voltage (IN1) = 0011001100

IN Voltage (IN2) = 0101010101

IN Voltage (IN3) = 0000111111

T-Edit



Device and node counts:-

MOSFETs - 6

MOSFET geometries - 2

Voltage sources - 4

Subckt Definitions - 1

Model Definitions - 6

Computed Models - 2

Independent nodes - 2

Boundary nodes - 5

Total nodes - 7

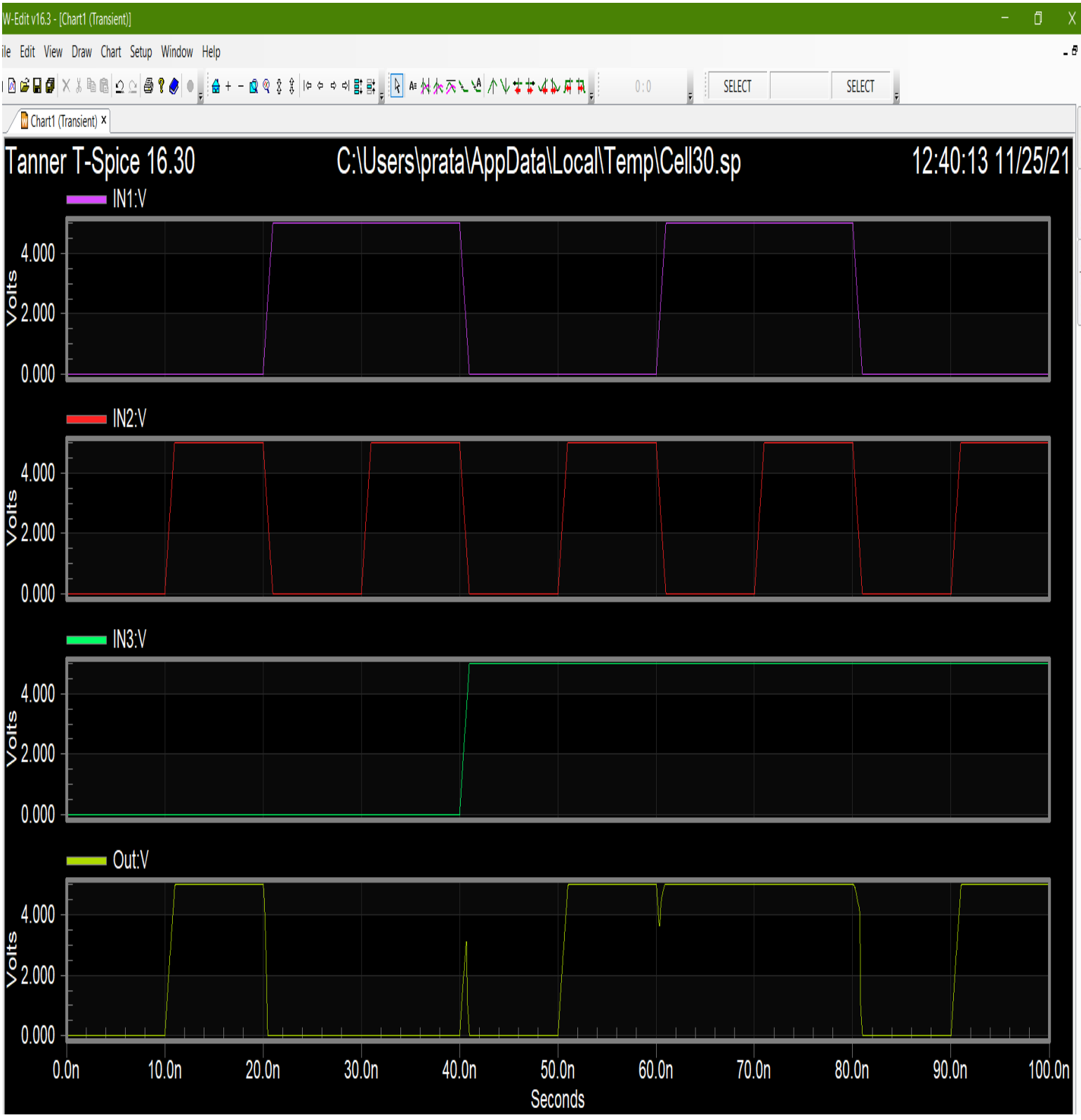
Opening simulation database "C:\Users\prata\AppData\Local\Temp\Cell30.tsim"

Parsing	0.15 seconds
Setup	0.05 seconds
DC operating point	0.02 seconds
Transient Analysis	0.42 seconds
Overhead	0.60 seconds

Total	**1.25 seconds**

Simulation completed

WAVEFORM- OUTPUT


W-Edit v16.3 - [Chart1 (Transient)]
ile Edit View Draw Chart Setup Window Help
SELECT
SELECT
Chart1 (Transient)
Tanner T-Spice 16.30
C:\Users\prata\AppData\Local\Temp\Cell30.sp
12:40:13 11/25/21
IN1:V
IN2:V
IN3:V
Out:V
Volts
4.000
2.000
0.000
0.0n
10.0n
20.0n
30.0n
40.0n
50.0n
60.0n
70.0n
80.0n
90.0n
100.0n
Seconds