Shashwat Khandelwal

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Professional objective

A highly motivated hardware engineer with a strong background in hardware acceleration like neural network deployment, image processing acceleration, and hardware verification. I am seeking a positions as an ASIC Design Engineer/ RTL Design Enginner where my expertise in designing and deploying quantised neural networks on FPGA accelerators, high-level synthesis, and digital systems design will contribute to developing cutting-edge hardware accelerated solutions.

Work Experience

Co-op Intern May '23 – Nov '23
AMD *Dublin, Ireland*

- **Manager** : Michaela Blott, Senior Fellow
- Extended the FINN framework by developing an end-to-end pipeline for deploying quantized recurrent neural networks (LSTMs) on FPGAs.
- **Key Technologies**: ONNX, Python, FINN, High Level Synthesis, Vitis-SDK, Pytorch, Brevitas, PYNQ
- Achievements: Deployed the first QLSTM layer based classification model (Intrusion detection system for automotive controller area network) deployed entirely using the FINN toolchain. This project is this first major step for the generalized QLSTM layer to become part of FINN.

Hardware Engineering Intern Apr '20 – Jun '20
NVIDIA *Hyderabad, India — Remote*

- **Manager** : Ranjith Nair, Sr. ASIC Manager
- Developed a Verification Testbench for a Parallel-to-Serial converter for the APB interface.
- **Key Technologies**: System Verilog, Verification Testbenches
- Achievements: Enabled robust verification of hardware modules, ensuring functional reliability and compliance with design specifications of the Parallel-to-Serial converter.

Education

Trinity College Dublin Dublin, Ireland
Ph.D. in Electronic and Electrical Engineering *Mar '21 – Feb '25(Expected)*

- **Ph.D. Supervisor**: Dr. Shreejith Shanker
- **Teaching Positions** : Deep Learning and it's applications, Digital System and Integrated Systems Design.
- **Coursework** : Deep Learning and it's applications, Data Structures

International Institute of Information Technology Hyderabad, India
B.Tech + M.S by Research in Electronics Engineering *Aug '16 – Aug '21*

- **M.S Grade | B.Tech Grade**: 9.5/10 | 7.96/10
- **M.S. Supervisor**: Dr. Suresh Purini
- **M.S. Coursework** : Complex Digital System Design, Digital VLSI Design.
- **B.Tech Coursework** : Statistical Methods in AI, Digital Logic and Processors, Computer System Organisation, Multivariate Analysis, Digital Signal Processing

Technical Skills

Hardware Design Languages: Verilog, System Verilog, BlueSpec System Verilog (BSV)
Programming Languages: Python, C
Machine Learning Frameworks: Pytorch, TensorFlow, Brevitas, ONNX
Operating Systems: Linux, Windows
FPGA Tools and Frameworks: Vivado, High-Level Synthesis (HLS), Vitis-SDK, FINN, Vitis-AI, PYNQ
Hardware Verification: Testbenches, Functional Verification
Miscellaneous: Github, Visual Studio Code

Selected Projects

IDS for CAN Bus on Edge FPGAs Mar '21 – Present

FINN, Vitis-AI, TensorFlow, Pytorch, Brevitas, Docker, ZCU104, Ultra96v2

- Deployed quantized ML models as intrusion detection engines for the Automotive Controller Area Network (CAN).
- **Outcome**: Enhanced real-time security features in automotive networks with FPGA acceleration of multiple QNNs (MLP's, CNN's, Autoencoders, LSTM's), optimizing power consumption and meeting latency deadlines, directly solving constraints posed by resource constrained vehicular systems.

U-Nets for Video Processing and Hyperspectral Image Analysis on FPGAs May '23 – Present

Vitis-AI, Pytorch, Brevitas, FINN, Alveo, ZCU104

- Optimized U-Nets and Autoencoders for image-to-image transformations in video processing applications and anomaly detection in satellite imagery.
- **Outcome**: Achieved high-performance processing of matting operations on Alveo FPGA platform (1.14× throughput improvement, 11× reduction in energy consumption)/ real-time analysis of HSI for anomaly detection on ZCU104 FPGA (1.27× latency reduction, 7.5× reduction in energy consumption).

Local Laplacian filters on FPGA Dec '18 – Apr '20

C, BSV, Matlab, Virtex-7 FPGA, Xillybus

- Developed the first FPGA implementation of the detail enhancing/smoothing local laplacian filter image processing algorithm. Proposed a novel high throughput shift operation based convolution engine to make the implementation amenable for FPGAs.
- **Outcome**: Achieved 7.5× speed-up against SOTA on the Virtex-7 FPGA.

Hardware Design Projects Apr '18 – Apr '22

Verilog, BSV, Vivado, Basys3

- FSM based Hardware Calculator Design, Parking System Design, Multiplier and Divider for hardware (Elastic and In-elastic variants)

Selected Publications

- **Exploring Highly Quantized Neural Networks for Intrusion Detection in Automotive CAN** - S. Khandelwal, S. Shanker, FPL 2023, Gothenburg, Sweden
- **Custom precision accelerators for energy-efficient image-to-image transformations in motion picture workflows** - E. Murphy, S. Khandelwal, S. Shanker, SPIE 2023, San Diego, US
- **An Energy-Efficient Artefact Detection Accelerator on FPGAs for Hyper-Spectral Satellite Imagery** - C. Castelino, S. Khandelwal, S. Shanker, DSD/SEAA 2024, Paris, France
- **Quantised Neural Network Accelerators for Low-Power IDS in Automotive Networks** - S. Khandelwal, A. Walsh, S. Shanker, DATE 2023, Antwerp, Belgium
- **Real-Time Zero-Day Intrusion Detection System for Automotive CAN on FPGAs** - S. Khandelwal, S. Shanker, ASAP 2023, Gothenburg, Sweden
- **A Lightweight FPGA-based IDS-ECU Architecture for Automotive CAN** -S. Khandelwal, S. Shanker, FPT 2022, Hong Kong, SAR
- **Accelerating Local Laplacian Filters on FPGAs** - S. Khandelwal, Z. Choudhury, S. Shrivastava, S. Purini, FPL 2020, Gothenburg, Sweden

Achievements

NVIDIA Academic Hardware Grant: Awarded an RTX A6000 GPU for advancing research in energy-efficient hardware design.
Dean's Merit List (IIIT Hyderabad): Recognized for academic excellence in Digital System Design and VLSI courses for undergraduate courses.
Joint Entrance Examination Score (227/360, 99.4 Percentile): Competitive score in India's prestigious engineering entrance exam, indicating strong problem-solving and analytical skills.

Extracurricular Activities

Volunteer at Aashakiran, providing academic support to underprivileged students.
Member of the Tennis Club and Cricket Team at Trinity College Dublin.