

# Exploring Highly Quantised Neural Networks for Intrusion Detection in Automotive CAN

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**Abstract**—Vehicles today comprise intelligent systems like connected autonomous driving and advanced driving assistance systems (ADAS) to enhance the driving experience, which is enabled through increased connectivity to infrastructure and fusion of information from different sensing modes. However, the rising connectivity coupled with the legacy network architecture within vehicles can be exploited for launching active and passive attacks on critical vehicle systems and directly affecting the safety of passengers. Machine learning-based intrusion detection models have been shown to successfully detect multiple targeted attack vectors in recent literature, whose deployments are enabled through quantised neural networks targeting low-power platforms. Multiple models are often required to simultaneously detect multiple attack vectors, increasing the area, (resource) cost, and energy consumption. In this paper, we present a case for utilising custom-quantised MLP's (CQMLP) as a multi-class classification model, capable of detecting multiple attacks from the benign flow of controller area network (CAN) messages. The specific quantisation and neural architecture are determined through a joint design space exploration, resulting in our choice of the 2-bit precision and the n-layer MLP. Our 2-bit version is trained using Brevitas and optimised as a dataflow hardware model through the FINN toolflow from AMD/Xilinx, targeting an XCZU7EV device. We show that the 2-bit CQMLP model, when integrated as the IDS, can detect malicious attack messages (DoS, fuzzing, and spoofing attack) with a very high accuracy of 99.9%, on par with the state-of-the-art methods in the literature. Furthermore, the dataflow model can perform line rate detection at a latency of 0.11 ms from message reception while consuming 0.23 mJ/inference, making it ideally suited for integration with an ECU in critical CAN networks.

**Index Terms**—Controller Area Network, Intrusion Detection System, Quantised Neural Nets, Machine Learning, FPGAs

## I. INTRODUCTION & RELATED WORKS

Automotive networks are evolving rapidly to cater to the high-data needs for novel/intelligent capabilities that have enabled safety, infotainment, and comfort for passengers. These interconnected networks (via multiple network protocols) facilitate high-speed communication/information exchange between over a hundred electronic computing units (ECUs), sensors, and actuators present in modern cars. Among the network protocols, Controller Area Network (CAN) is used for critical communication between ECUs and it continues to be the most widely used network protocol for in-vehicle networks owing to its cost-effective nature and ease of use in control applications [1]. Early ECUs and software functions deployed on the CAN were automatically siloed due to the limited connectivity of the vehicles then, to the external world. Novel capabilities in vehicles today rely on connectivity to infrastructure and other vehicles to enable real-time sensing

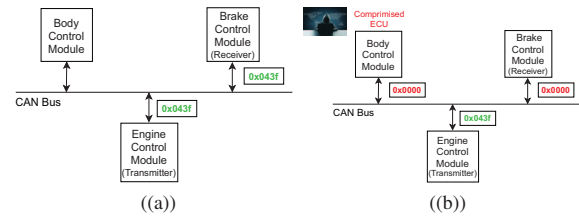


Fig. 1: An illustration of a simple DoS attack launched through a compromised ECU. Part (a) shows the normal communication between the ECUs, while in (b), the ECU is unable to transmit messages on the CAN bus as the compromised ECU floods the bus with high priority messages.

of the outside environment and also to enable unique features like remote monitoring and control of specific capabilities for diagnostics, and over-the-air upgrades. Researchers however have shown that such interfaces open up new avenues for injecting malicious code/messages into these previously siloed networks [2]–[4]. Figure 1 shows an example of a simple DoS attack on a standard CAN bus. Such attacks are largely enabled by the lack of inherent security and authentication mechanisms in CAN and similar automotive network protocols [5], [6].

To detect the onset of such intrusions on CAN, multiple intrusion detection approaches have been proposed in the literature allowing critical systems to enter into a ‘safe working’ mode when such threats are detected. Early intrusion detection systems (IDS) proposed were rule/specification based, which utilised a set of rules to compare known attack signatures to patterns captured from current network parameters/messages to detect unusual activity [7]–[9]. Recently, machine learning (ML) approaches have shown significant improvement in the detection accuracy of such threats and the ability to adapt to newer attack vectors [10]–[14] without incurring overheads of rule-based approaches. In addition to native precision ML models, quantised variants of the floating-point models have shown to be viable alternatives, reducing the computational complexity, resource, and energy consumption at the expense of a slight reduction in inference accuracy. Quantised models are then deployed on constrained devices such as low-end FPGAs or dedicated embedded platforms [15]. Frameworks such as Vitis-AI and FINN can convert the Pytorch/TensorFlow representations at native precisions to quantised models and dataflow-style hardware accelerators for deployment on the

FPGA [16], [17]. ECU architectures based on hybrid FPGAs are a promising platform for the deployment of such QNNs as IDS, while also enabling consolidation with standard ECU function(s), with clear isolation between them on the same die [18]. However, most methods so far relied on the integration of multiple accelerators, each fine-tuned to detect a subset of attacks, increasing the energy cost and area overhead.

In this paper, we explore the case for a custom quantised feed-forward network that can classify multiple attack vectors simultaneously and a dataflow-style custom quantised hardware implementation of the model. The dedicated hardware implements IDS capability as an Advanced eXtensible Interface (AXI) slave peripheral to the ARM cores, offering complete isolation from the software tasks on them, mimicking the model ECU architecture for deploying distributed IDS in CAN networks. Starting from a standard multi-layer perceptron (MLP) model, we analyse and evaluate different model configurations and quantisations for weights/biases/activations to arrive at our custom model with 2-, 3- & 4-bit precisions through a constrained design space exploration. Subsequently, the dataflow accelerator is generated and deployed using AMD/Xilinx's FINN framework [17]. This integration allows the software tasks on the ECU to invoke and fully control the operation of the IDS accelerator through APIs, similar to offloads enabled by AUTOSAR abstractions. The key contributions of this paper are as follows:

- A feed-forward custom quantised multi-layer-perceptron based-IDS for automotive CAN achieving state-of-the-art classification accuracy across multiple attack vectors using only a single model.
- Exploits the tightly-coupled ECU architecture with the dataflow implementation of IDS accelerating IDS operation in full isolation.
- Quantify the performance and energy savings of the proposed ML model and its integration using the open CAN dataset. Our results show that the proposed IDS achieves significant improvements in terms of per-message processing latency and power consumption against the state-of-the-art IDSs in the literature.

We evaluate our approach using the openly available CAR Hacking dataset [13] for training and validation across multiple attack vectors captured from an actual vehicle with the entire CAN data frame used as an input feature to improve the detection performance. We analyse the 2-, 3- & 4-bit precision models and utilise the inference accuracy and resource utilisation parameters to arrive at the most optimal model. Our experiments show that the proposed custom quantised (2-bit) MLP-based IDS (referred to as CQMLP-IDS) achieves an average accuracy of 99.91% across Denial of Service (DoS), Fuzzing, and RPM-spoofing attacks among the benign flow of messages, identical to or exceeding the detection accuracy achieved by state-of-the-art GPU- and CPU-based implementations. The tightly integrated ECU architecture reduces the per message execution latency by  $2.2\times$  and the energy consumed by  $3.9\times$  compared to state-of-the-art IDSs proposed in the research literature. We also show that our (fp32) MLP model on a Jetson Nano [19], mimicking a dedicated IDS ECU, incurs

$12\times$  higher energy consumption per inference, compared to the integrated IDS-ECU.

The remainder of the paper is organised as follows: Section II captures background information and state-of-the-art research in this area; section III describes the proposed MLP model and design choices for the implementation; section IV outlines the experiment setup and results; and we conclude the paper in section V.

## II. BACKGROUND AND RELATED WORKS

### A. Controller Area Network

In-vehicle networks enable distributed ECUs to exchange control and data messages to achieve the global functions of the vehicle. Multiple protocols are used in vehicular systems to cater to different functions based on their criticality and to optimise the cost of E/E systems. CAN [1] and CAN-FD [20] continue to be the most widely used protocol today due to their lower cost, flexibility, and robustness. The broadcast CAN bus uses carrier sense multiple access with the collision avoidance and arbitration priority (CSMA/CA-AP) access/arbitration mechanism to control access to the bus using the CAN ID allocated to each message. This enables higher priority messages to be processed first hence efficiently handling messages from safety-critical applications. CAN also supports multiple data rates (125 Kbps to 1 Mbps) and multiple modes of operation (1-wire, 2-wire) to cater to a range of critical and non-critical functions in vehicles. Despite this robustness, CAN is inherently insecure: there is no built-in mechanism (like message encryption) in the network to authenticate the transmitter, receiver, or the message content itself [21]. This makes CAN vulnerable to simple yet efficient active message injection attacks like fuzzing, spoofing, replay attacks, and Denial of Service (DoS) attacks [6], [22]–[24].

Researchers have explored different flavours of IDSs from rule-based approaches to machine learning-based methods to address CAN's existing vulnerabilities. Rule-based approaches are further classified into flow-based and payload-based. While flow-based approaches identify traits like message frequency and/or interval for the network to detect abnormalities [25], payload-based approaches use the data segment in CAN frames to detect abnormal sequences of instructions and or data [26]. Purely payload-based methods, however, fail to capture the timing/sequence of messages in an attack, leading to parts of attack messages being flagged as benign. Hybrid schemes use both the message timing/frequency and the payload information to capture a more holistic view of the network, allowing them to extract specific signatures of transmitting ECUs, receiving ECUs, and messages [27]. Machine learning-based techniques further generalises such techniques when trained with large datasets through classification approaches, sequential techniques, and deep learning-based schemes.

### B. Machine Learning based IDSs

ML-based IDSs discussed in the literature mostly use a combination of input features, as shown in table I. In [13], the authors propose a reduced inception net architecture as an

TABLE I: Input features used by the IDSs & IPSs proposed in the research literature.

Models	Input Features Used
GIDS [30]	CAN ID
DCNN [13]	CAN ID
Rec-CNN [38]	CAN ID
G-IDCS [28]	CAN ID
TAN-IDS [29]	CAN ID
iForest [35]	Data Field
MLIDS [36]	CAN ID + Data Field
NovelADS [32]	CAN ID + Data Field
TCAN-IDS [31]	CAN ID + Data Field
MTH-IDS [37]	CAN ID + Data Field
HyDL-IDS [33]	CAN ID + Data Field + DLC
GRU [34]	CAN ID + Data Field + DLC
<b>CQMLP-IDS (proposed)</b>	<b>CAN ID + Data Field</b>

IDS using deep convolutional neural networks. They achieve over 99% accuracy for DoS, fuzzing & spoofing attacks. In [28], authors present a graph based intrusion detection protocol and propose improvements over existing graph based IDS techniques. In [29], a transformer network-based IDS is proposed which demonstrates very high classification accuracy at the cost of higher detection latency. In [30], the authors propose a GAN-based IDS and achieve an average accuracy of 97.5% for the same attacks. More complex ML architectures like temporal convolution with global attention [31], a combination of convolutional neural networks (CNN) and long short-term memory (LSTM) cells using both supervised and unsupervised approaches [32], [33], gated recurrent units (GRU) networks [34] have been shown to improve detection accuracy. In [35], the authors use an iForest anomaly detection algorithm as an intrusion prevention system (IPS) to detect fuzzing and spoofing (RPM & Gear) attacks and mark the message as an error preventing its propagation to other ECUs; however, this can cause multiple messages to be dropped from the bus in case of false positives or DoS attacks. The key challenge of ML-based approaches is their deployment as an in-vehicle ECU. Most approaches rely on high-performance GPUs to meet the inference deadlines [13], [30]–[32], [34], [36], while others rely on dedicating full ECUs for IDS [35], [37]; both approaches incur additional overheads in energy budget and weight, making them less suited for distributing IDS among different network segments. Similarly, almost all methods presented in the literature require multiple uniquely trained models to detect all possible threat vectors, which incur much higher resources and energy than a singular model which can classify multiple threat vectors.

### III. SYSTEM ARCHITECTURE

#### A. MLP model for IDS

To determine the best ML model for IDS, we profiled different ML architectures to find a model with high classification accuracy which also offers low computational complexity. We observed that while CNNs were effective for classification when using only CAN IDs, MLPs provided more accurate detection (accuracy, false positives, and false negatives) when using the entire message contents at much lower computational complexity; since message data can contain malicious content,

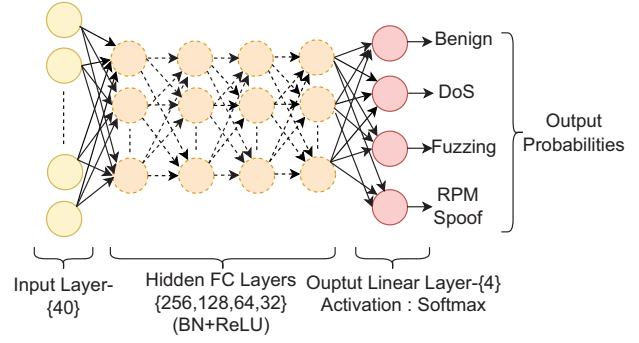


Fig. 2: The proposed MLP model as a multi-attack detection IDS.

we chose MLPs as our choice of architecture and entire message as the input feature [39], [40]. A concatenation of  $n = 4$  successive messages (CAN IDs + payload) is chosen as the input feature based on this testing. Note that during training/testing, if the block has even one attack message, the entire block is treated as an attack block. In a real system, this means that a window of 4 messages containing a single attack message will be detected as a malicious window, allowing a sequence of events leading to and after the attack message as potential threats. Though conservative, this approach enables the model to better capture normal operating sequences during training and provides a better balance to the dataset. We observed that using a block with a higher number of messages ( $> 4$ ) improves the classification accuracy as the model has more input data to make a decision; however, grouping more messages also affects the detection latency from the arrival of the 'infected' message, leading to our choice of  $n = 4$ .

Our final MLP model consists of 5 Linear layers implemented with the 256, 128, 64, 32 & 4 units at each layer as shown in Figure 2. The time-series data from the input feature buffer is fed as input to the input layer with 40 units. Subsequent layer(s) operate on the output of the previous layer, with increasing complexity to perform classification. Batch Normalisation was used between the linear layers to prevent over-fitting and to improve the learning efficiency during the training phase. The output linear layer uses a softmax activation at the output to estimate the probability of the message being benign, DoS, fuzzing, or RPM-spoofed. The model is defined in Pytorch using standard functions and nodes with the quantised versions of linear and relu activation layers imported from the brevis training library.

#### B. Design space exploration

To arrive at the optimum bit-precision for the quantised model, we trained our final MLP model at 2-bit, 3-bit, and 4-bit uniform quantisation on all the attacks to determine the trade-offs in detection accuracy and resource consumption (indirectly leading to power consumption and latency). Figures 3 & 4 show the training and validation losses when the model was trained for 1000 epochs at each quantisation. The 2-bit model converges to an optimum detection and is very close to the 3-bit & 4-bit variants (between epoch 810 and 820) in

TABLE II: Inference cost of the custom quantised models (CQMLP) inferred through the FINN library and normalised to the 4-bit model.

CQMLP Models	2-bit	3-bit	4-bit
Normalised inference cost	0.27	0.67	1

terms of validation loss. We observed 147 misclassifications out of the total 180,000 messages in the test set for the 2-bit variant. For the same test set, we found misclassifications to be 74 & 31 for the 3-bit & 4-bit variants respectively.

To capture the inference costs of the models further, we use the FINN utility function (inference cost) to estimate the memory footprint and operational complexity of each model. This function captures the *memory footprint* and *binary operations* cost for each version of the model; the costs are then normalised (against a baseline) and linearly combined to arrive at the normalised inference cost for each of the three quantisation levels. Table II shows these costs with the 4-bit version as the baseline. We find the cost of the 2-bit version is 40% & 27% of the 3-bit & 4-bit version respectively, without a significant drop in detection accuracy and was hence chosen as the optimal bitwidth for deploying the CQMLP.

### C. Dataset and Training

We use the open Car Hacking dataset for training our model and to test its performance [41]. The dataset provides a labelled set of benign and attack messages which were captured via the Onboard Diagnostic (OBD) port in an actual vehicle, with attack messages injected in real-time. The dataset includes DoS, Fuzzing, and RPM-Spoofing message injections allowing us to validate the detection accuracy across these different attacks. We split the dataset as 85:10:5 for training, validation, and testing respectively, allocating the large section to training and optimisation of the quantised network. The performance of the model on the validation set during training ensures that it is not over-fitting on any of the attacks. We pre-process the dataset before training to mimic the dataflow the model will obtain as its input when integrated into the ECU. Each message (ID and payload) is encoded into INT8 type vector, and an adjacent sequence of  $n = 4$  of these encoded messages form the input feature buffer content for the IDS (block shape of  $\{1, 10 \times n\}$  INT8 data).

The different bit models were trained using Brevitas, a quantisation-aware training (QAT) library from AMD/Xilinx [42]. We used the adam optimizer with binary cross-entropy as the loss function. The learning rate was set to 0.0001 to allow for slower learning which aids in efficient model training [43]. Each model has 54,824 learning parameters and was trained for 1000 epochs with a batch size of 128 for the DoS, Fuzzing, and RPM-Spoof attacks. The best model in terms of validation loss was saved and exported as an 'onnx' graph. This graph was then fed into the FINN hardware generation flow for the CQMLP-IDS IP generation.

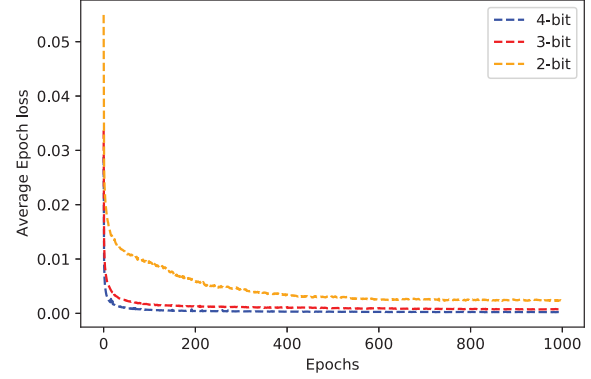


Fig. 3: Training loss of the model for different precision of weights and activations for all the attacks.

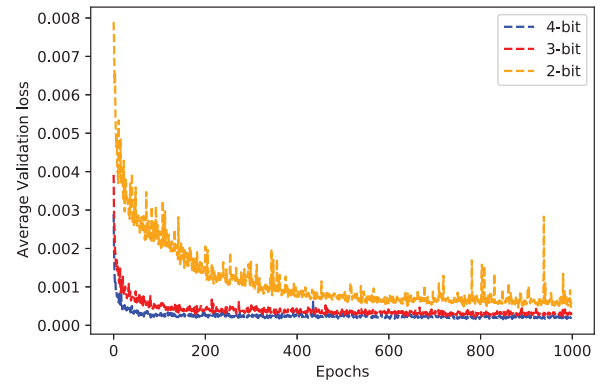


Fig. 4: Validation loss of the model for different precision of weights and activations for all the attacks.

### D. Dataflow hardware generation and integration to ECU ECU-IDS

We utilise the FINN compiler to synthesize and generate the RTL description of the hardware implementation of the model. Starting at the 'onnx' graph, FINN applies a series of streamlining and dataflow transformations to convert the ML model into a synthesizable graph. We further specify the parallelism to achieve our target latency (set to 100000 messages per second), matrix-vector activation unit widths (set to 80), and folding levels to generate the dataflow hardware with AXI interfaces for input and output. Subsequently, FINN invokes Vivado tools to stitch the accelerator as an AXI slave to a Zynq subsystem for our target device (XCZU7EU) and generates the final bitstream along with the software drivers for our hardware ML engine. This integration allows us to model the Zynq-based hybrid ECU architecture, where our custom hardware is accessible from the ECU and performs IDS in complete isolation from the tasks on the ARM cores as shown in Figure 5. We build on the proposed architecture from our previous works which contain detailed information of the same [18], [44]. For our experiments, we use the PYNQ runtime on top of a Linux kernel on the ARM cores to interact



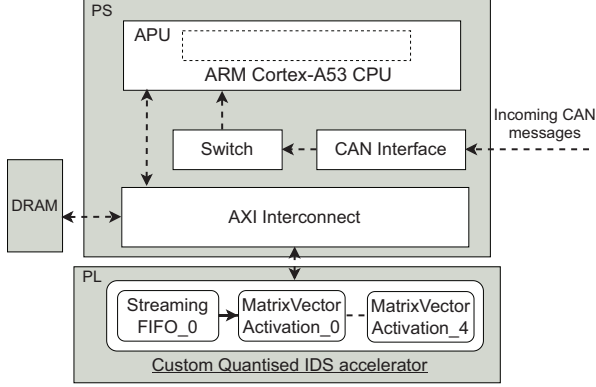


Fig. 5: The proposed IDS-ECU architecture. The ML model is accelerated on the PL part of the FPGA.

with our hardware model on the PL.

#### IV. EXPERIMENTAL RESULTS

To quantify the performance and energy benefits of a dedicated dataflow accelerator implementing our CQMLP-IDS integrated with ECU function(s), we use a Zynq Ultrascale+ ZCU104 development board as the test ECU platform. The ZCU104 board features an XCZU7EV Ultrascale+ device with quad-core ARM A53 cores and dual-core ARM R5 cores on the PS as our target platform. The A53 cores on the PS are configured to run at 1.2 GHz peak, and the dataflow hardware was synthesized for a clock frequency of 200 MHz by FINN. The ARM cores run Linux OS with petalinux tools and PYNQ runtime to provide APIs to interface to the CQMLP-IDS IP in the PL. When testing, the hardware CQMLP model is fed with inputs message from the ECU mimicking the standard message flow within ECUs, and use our test split from the Car Hacking dataset to perform inference. We quantify the inference accuracy by evaluating the precision, recall, and F1 rates of our CQMLP models when inference is performed on the Zynq-IDS-ECU. We also quantify the per-message processing latency and power consumption for each incoming CAN message on the Zynq-IDS-ECU. The results, in terms of inference accuracy and message processing latency, are compared against the state-of-the-art IDSs/IPs presented in the research literature. We also compare the per-block processing latency and the per-inference energy consumption when the FP32 version of the proposed model is executed on an NVIDIA Jetson Nano 4GB GPU. In the case of schemes where inference is performed on a block of CAN messages, we use these metrics along with the block size for the comparison. We also compare our active power consumption against ML-based IDS approaches in literature where power consumption has been reported.

##### A. Inference accuracy

We evaluate the classification performance of the model in identifying *DoS*, *Fuzzy* and *RPM-Spoofing* attacks from the Car Hacking dataset and compare them against state-of-the-art techniques in the literature. Table III captures the classification

TABLE III: Confusion matrix capturing the classification results of the CQMLP.

CQMLP	Predicted Values			
	Benign	DoS	Fuzzing	RPM-Spoof
<b>Benign</b>	103142	17	17	0
<b>DoS</b>	27	23666	0	0
<b>Fuzzing</b>	78	0	28003	8
<b>RPM-Spoof</b>	0	0	0	25042

performance of our model in isolation across our test set as a confusion matrix. The misclassifications in our test set can be attributed to scenarios where nearly identical attack and benign message patterns are observed in a block at a given time which leads to an overall false positive rate (FPR) of 0.03% (34 messages falsely classified as attacks out of the total 103176 benign messages). We compare the inference performance of our 2-bit CQMLP model integrated within the ECU against the state-of-the-art IDSs and IPSs proposed in the literature: GIDS [30], DCNN [13], MLIDS [36], HyDL-IDS [33] NovelADS [32], TCAN-IDS [31], IForest [35], MTH-IDS [37], GRU [34], G-IDCS [28], TAN-IDS [29] and Rec-CNN [38] which are captured in table IV, comparing them in terms of inference precision, recall, F1 score and false negative rate. For the *DoS* attack the 2-bit CQMLP performs equally among the proposed IDSs in terms of F1 score. In the case of *fuzzing* attack, the 2-bit CQMLP model performs identically to DCNN [13] while performing better than iForest [35], TCAN-IDS [31], and GRU [34] by 2.3%, 0.6% and 0.6% respectively in terms of F1 score. The 2-bit CQMLP also achieves almost perfect classification for the *RPM-spoofing* attack and performs better than or equal to the other methods proposed in the literature. Our prior work using two 8-bit variants of the feed-forward model achieved 99.96%, 99.76% & 100% F1 scores for the *DoS*, *Fuzzing*, and *RPM spoofing* attacks, when deployed as two concurrent accelerators for detecting them simultaneously [18]. In contrast, our 2-bit CQMLP variant achieves almost identical F1 scores (99.90%, 99.81% & 99.98% respectively) for the same attacks (from the same dataset) while performing multi-class classification using a single inference model. By adopting QAT training and conservative block-based labelling, our low precision model is able to match the inference performance of the MLP variant at 8-bit quantisation discussed in [18].

##### B. Inference latency

We quantify the per-message processing latency of the model, starting from the arrival of the CAN message at the interface to determine the detection delay incurred by the approach. Table V compares our result against other approaches in the literature, which utilise different platforms (GPUs, Jetson edge accelerators, Raspberry Pi) and approaches (block of CAN messages v/s individual messages). It should be noted that the latency metric in the case of block-based IDS does not consider the delay in acquiring the number of CAN messages required, and hence could result in potentially larger delays in detection of the onset of an attack. The tightly integrated CQMLP-IDS achieves 0.11 ms per CAN frame, which is a

TABLE IV: Accuracy metric comparison (%) of our CQMLP accelerators against the reported literature on the DoS, Fuzzing and RPM-Spoof attacks.

Attack	Model	Precision	Recall	F1	FNR
DoS	GIDS [30]	-	99.9	-	-
	DCNN [13]	100	99.89	99.95	0.13
	MLIDS [36]	99.9	100	99.9	-
	G-IDCS [28]	99.81	98.86	99.33	-
	TAN-IDS [29]	100	100	100	-
	HyDL-IDS [33]	100	100	100	0
	NovelADS [32]	99.97	99.91	99.94	-
	TCAN-IDS [31]	100	99.97	99.98	-
	iForest [35]	-	-	-	-
	GRU [34]	99.93	99.91	99.92	-
	<b>CQMLP-IDS</b>	99.92	99.88	99.90	0.11
Fuzzing	GIDS [30]	-	98.7	-	-
	DCNN [13]	99.95	99.65	99.80	0.5
	MLIDS [36]	99.9	99.9	99.9	-
	G-IDCS [28]	99.71	99	99.35	-
	TAN-IDS [29]	99.99	99.99	99.99	-
	HyDL-IDS [33]	99.98	99.88	99.93	-
	NovelADS [32]	99.99	100	100	-
	TCAN-IDS [31]	99.96	99.89	99.22	-
	iForest [35]	95.07	99.93	97.44	-
	GRU [34]	99.32	99.13	99.22	-
	<b>CQMLP-IDS</b>	99.93	99.69	99.81	0.27
RPM-Spoof	GIDS [30]	-	99.6	-	-
	DCNN [13]	99.99	99.94	99.96	0.05
	MLIDS [36]	100	100	100	-
	G-IDCS [28]	99.85	98.69	99.27	-
	TAN-IDS [29]	99.99	99.93	99.96	-
	HyDL-IDS [33]	100	100	100	0
	NovelADS [32]	99.9	99.9	99.9	-
	TCAN-IDS [31]	99.9	99.9	99.9	-
	iForest [35]	98.9	100	99.4	-
	<b>CQMLP-IDS</b>	99.96	100	99.98	0

TABLE V: Per-message latency comparison against other state-of-the-art IDSs reported in literature.

Models	Latency	Frames	Platform
GRU [34]	890 ms	5000 CAN frames	Jetson Xavier NX
MLIDS [36]	275 ms	per CAN frame	GTX Titan X
Rec-CNN [38]	117 ms	128 CAN frames	Jetson TX2
NovelADS [32]	128.7 ms	100 CAN frames	Jetson Nano
GIDS [30]	5.89 ms	64 CAN frames	GTX 1080
TAN-IDS [29]	11.6 ms	128 CAN frames	-
DCNN [13]	5 ms	29 CAN frames	Tesla K80
TCAN-IDS [31]	3.4 ms	64 CAN frames	Jetson AGX
MTH-IDS [37]	0.574 ms	per CAN frame	Raspberry Pi 3
QMLP-IDS [18]	0.24 ms	per CAN frame	Zynq Ultrascale+
<b>CQMLP-IDS</b>	0.11 ms	per CAN frame	Zynq Ultrascale+

2.18 $\times$  improvement over the dedicated line-rate QMLP-IDS ECU proposed in [18]. We also observe the inference latency of the (fp32) model on the Jetson Nano (modeling a dedicated IDS ECU) to be 1.2ms when averaged over 10000 runs. This is 10.9 $\times$  slower than the proposed CQMLP-IDS on the integrated IDS-ECU on the Zynq Ultrascale platform. In terms of raw throughput, our dataflow implementation of CQMLP coupled to the ECU can process over 9090 messages per second at the highest payload capacity, achieving near-line-rate detection on high-speed critical CAN networks.

TABLE VI: Resource utilisation breakdown of our proposed CQMLP (XCZU7EV).

Node	LUT	FF	BRAM/URAM	DSP
2-bit-CQMLP-IDS	3999	4524	4/0	0
% Usage	1.74%	0.98%	1.28%/ 0%	0%

### C. Power consumption, Resource Utilisation (PS/PL)

We further quantify the active power consumption of our dataflow accelerator to determine the average energy consumption per inference and the hardware resources incurred by the dataflow design on the XCZU7EV device. We observe that our model consumed 2.15 W when measured directly from the device's power rails (using the PYNQ-PMBus package) while performing inference and other tasks on the ECU (with Linux OS), thus consuming 0.23 mJ of energy per inference. This is a 3.9 $\times$  improvement compared to QMLP-IDS which report a per-inference energy consumption of 0.9 mJ. In comparison, we also observed the per-inference energy consumption of our (fp32) CAE model on the Jetson Nano to be 2.76 mJ when averaged over 10000 inference runs which is 12 $\times$  more than the proposed CQMLP-IDS on the tightly integrated IDS-ECU on a hybrid FPGA device. Among other reported results in the literature, our approach improves the active power consumption by 4.6 $\times$  when compared to the GRU [34] model on an Nvidia Jetson Xavier as a dedicated IDS node. In terms of resources, the dataflow CQMLP model consumes less than 2% of resources on the device, leaving behind enough resources to integrate dedicated accelerators for the ECU function.

We also quantify the utilisation of the ARM cores for managing the dataflow CQMLP accelerator to estimate the overhead in consolidating the IDS capability on the ECU. It was observed that a single core utilisation peaked at 40% when processing the completion interrupt from the IDS core (at the highest message rate modelling the worst case scenario), while other cores remained at IDLE ( $\leq 2\%$  utilisation). We believe that this could be further refined by processing the classification results using hardware logic, interrupting the ECU only when a threat is detected, while also improving the detection latency.

## V. CONCLUSION

In this paper, we present a dataflow-style hardware accelerator that implements a custom quantised MLP (CQMLP) model for detecting and classifying multiple attack vectors on an automotive CAN network. The accelerator generated through the FINN flow is quantised to 2-bit precision for weights and activations and is tightly integrated to the ARM core on a Zynq Ultrascale+ platform, mimicking a standard ECU. We show that the dataflow integration achieves a 2.2 $\times$  speed-up in per-message processing latency and almost 3.9 $\times$  reduction in energy consumption with 0.23mJ per inference when compared to the state-of-the-art IDSs. The quantised model also maintains high detection and classification accuracy across a range of attacks including DoS, fuzzing, and RPM-Spoofing attacks, making it an ideal approach for distributing IDS capabilities across ECUs in a vehicle network.

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