National Institute of Technology Agartala

B.Tech Odd Semester Midd-Term Examination, September 2022

Enrolment No. | | | | | | | |

Subject: Digital Electronics

Code: UEE03B13

Full Marks: 20

Time: 1 Hr.

Group A (Answer any four)

1. Which gates are known as universal gates? (1)
2. Represent XOR gate using Vann Diagram. (1)
3. What is associative law? (1)
4. Draw the circuit diagram of a half subtractor circuit. (1)
5. What is the drawback of a half adder? (1)

Group B (Answer any four)

6. Convert the following decimals to binary : 118, 255, 1023, 2049. (2)
7. Convert the following binary numbers to hexadecimal numbers : 1100101, 11111, 10101, 1111. (2)
8. Simplify the expression : (A+C)(AD+AD')+AC+C (2)
9. Prove De-morgan's law using truth table. (2)
10. Draw the circuit diagram for 1 bit comparator with truth table. (2)

Group C (Answer both questions)

11. Construct basic gates using universal gates. (4)
12. Justify the statement " a full adder is made up of two half adders". (4)