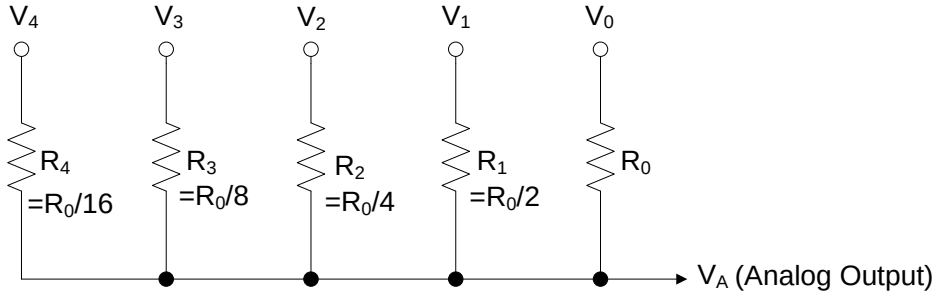
Q1. Explain 5-bit resistive divider with diagram.

Answer: 5-bit resistive divider is shown below:



A resistive divider can be build to change a digital voltage to an equivalent analog voltage. The following criterion can be applied to resistive divider.

- There must be one input resistor for each digital bit.
- Beginning with the LSB, each following resistor value is one half of the previous resistor.
- The LSB has weight of $\frac{1}{2^n - 1}$, where n is the number of input bits.
- The change in output voltage due to a change in the LSB is equal to $\frac{V}{2^2 - 1}$ where V is the digital input voltage.
- The output voltage can be obtained for any digital input signal by following equation. $V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + V_3 2^3 + ... + V_{n-1} 2^{n-1}}{2^n - 1}$, where $V_0, V_1, V_2, ..., V_{n-1}$ are the digital voltage (0 or V) and n is the number of input bits.

Q2. For a 5-bit resistive divider, determine the following (a) the weight assigned to the LSB (b) the weight assigned to the second and the third LSB (c) the change in output voltage due to a change in the LSB, the second LSB, and the third LSB (d) the output voltage for a digital input 10101. Assume 0= 0 V and 1=+10 V.

Answer:

(a) The LSB weight is $\frac{1}{2^5 - 1} = \frac{1}{31}$

(b) The second LSB weight is $\frac{2}{31}$ and third LSB weight is $\frac{4}{31}$

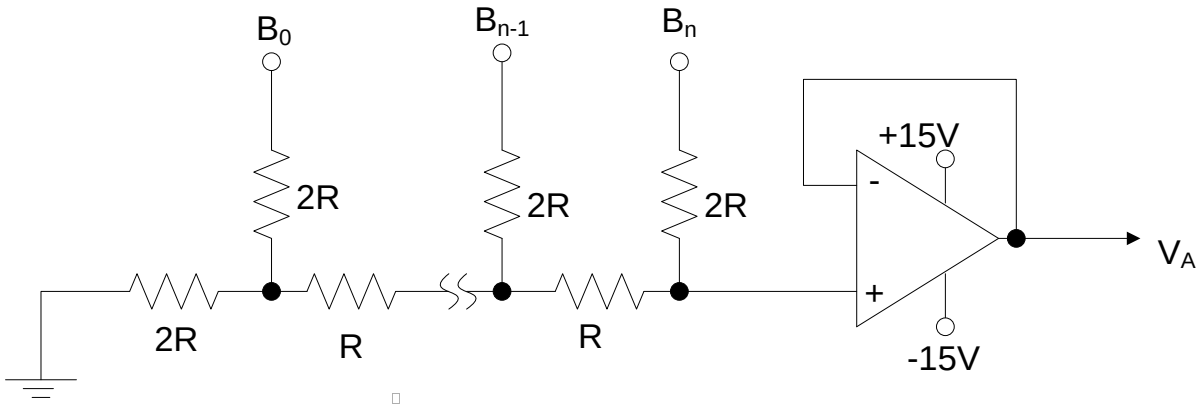
(c) The LSB causes a change in the output voltage of $\frac{10}{31}$ V. The second LSB causes an output voltage change of $\frac{20}{31}$ V and third LSB causes an output voltage change of $\frac{40}{31}$ V.

(d) The output voltage for a digital input of 10101 is

$$V_A = \frac{10\times 2^0 + 0\times 2^1 + 10\times 2^2 + 0\times 2^3 + 10\times 2^4}{2^5 - 1} = \frac{10(1+4+16)}{31} = \frac{210}{31} = 6.77 \text{ V}$$

Q3. Explain binary ladder with diagram.

Answer: Binary ladder is shown below.



B_n , B_{n-1} , ….,B_0 are the digital inputs, whose values are either 0 (0 Volt) or 1(V Volt).

B_n is MSB and B_0 is the LSB.

$$V_A = V(B_n \times \frac{1}{2} + B_{n-1} \times \frac{1}{4} + ... + B_0 \times \frac{1}{2^n})$$

Q4. Find the output voltage from a 5-bit ladder that has a digital input of 11010. Assume that 0=0 V and 1=+10 V.

Answer:

$$V_A = 10(1\times\frac{1}{2} + 1\times\frac{1}{4} + 0\times\frac{1}{8} + 1\times\frac{1}{16} + 0\times\frac{1}{32}) = 10(\frac{1}{2} + \frac{1}{4} + \frac{1}{16}) = 8.125 \text{ V}$$

Q5. Explain the terms accuracy and resolution for D/A converter.
Answer:
Accuracy is a measure of how close the actual output voltage is to the theoretical output value. For example, suppose the theoretical output voltage for a particular input is +10 V.
For accuracy of 1 percent, the actual output voltage must lies between +9.9 V and +10.1 V.
Resolution defines the smallest increment in voltage that can be recognized. Resolution is a function of number of bits in the digital input signal. In a 4-bit ladder system, the LSB weight of 1/16. This means that the smallest increment in output voltage is 1/16 of the input voltage. If the input voltage is +16 V, then the output voltage changes in steps of 1 V. This converter cannot resolve voltages smaller than 1 V. This converter is not capable of distinguishing voltages finer than 1 V which is the resolution of the converter.

Q6. What is the resolution of a 9-bit D/A converter which uses a ladder network? What is the resolution expressed as a percentage? If the full scale output voltage of this converter is +5 V, What is the resolution in volts?
Answer:

In a 9-bit system, the LSB has a weight of $\frac{1}{2^9} = \frac{1}{512}$.

Hence, the resolution of the converter expressed in percentage= $\frac{1}{512} \times 100\% \cong 0.2\%$

The resolution in volt= $\frac{1}{512} \times 5 \cong 10mV$

Q7. How many bits are required at the input of a converter if it is necessary to resolve voltage to 5 mV and the ladder has +10 V full scale?
Answer:

Resolution= $\frac{1}{2^n} \times$ full scale voltage where n is the number of bits

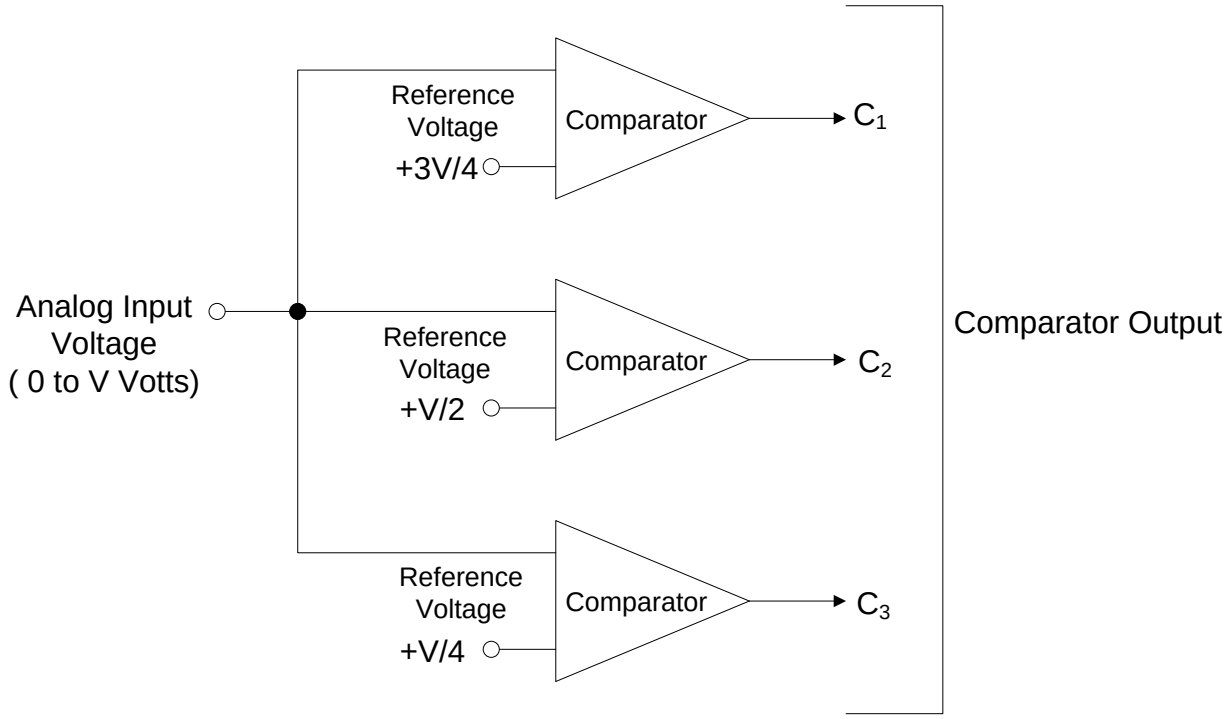
$\Rightarrow 5 \times 10^{-3} = \frac{1}{2^n} \times 10$

$\Rightarrow 2^n = 2000$

$\Rightarrow n \cong 11$

Q8. Explain simultaneous A/D converter with diagram.

Answer: Following is the logical diagram for 2-bit simultaneous A/D converter.



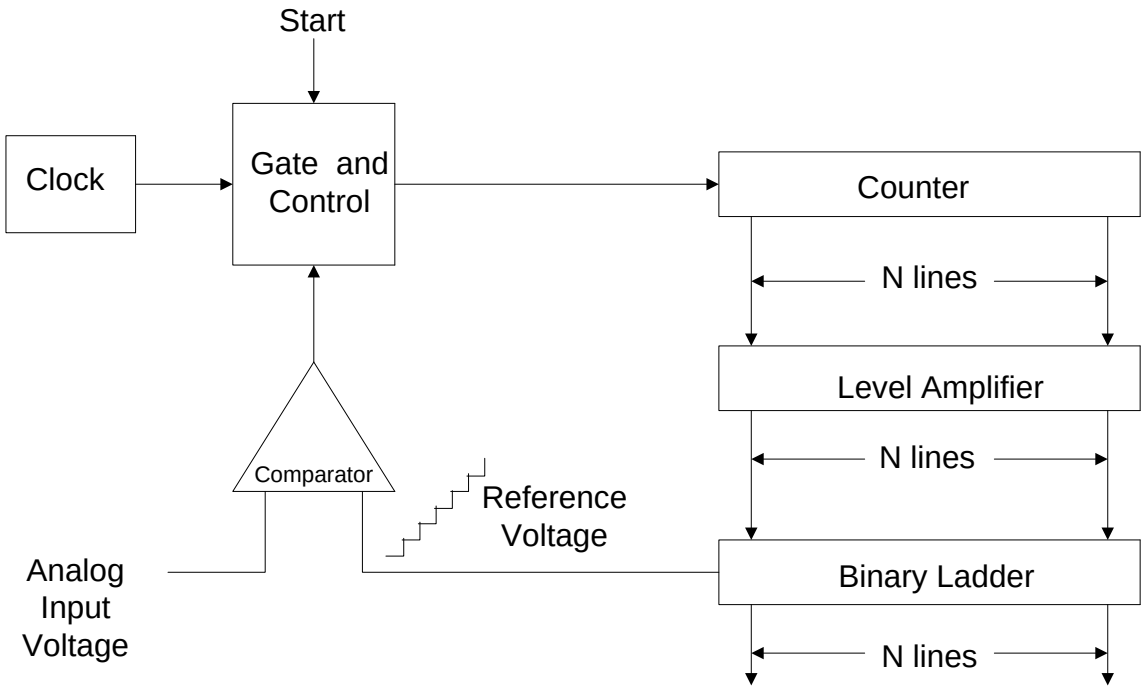
Following table shows the comparator output for input voltage ranges

Input Voltage	Comparator Output		
	C_3	C_2	C_1
0 to +V/4	Low	Low	Low
+V/4 to +V/2	Low	Low	High
+V/2 to +3V/4	Low	High	High
+3V/4 to V	High	High	High

The simultaneous method of A/D conversion using three comparators is shown in the above figure. The analog signal to be digitized serves as one of the inputs to each comparator. The second input is a standard reference voltage. The reference voltages used are +V/4, +V/2 and +3V/4. The system is then capable of accepting an analog input voltage between 0 and +V.

If the analog signal exceeds the reference voltage to any comparator, that comparator turns on. Now, if all the comparator are off, the analog input signal must be between 0 and +V/4. If C_1 is high and C_2 and C_3 are low, the input must be between +V/4 and +V/2. If C_1 and C_2 are high and C_3 is low, the input must be between +V/2 and +3V/4. If all the comparator outputs are high, the input signal must be between +3V/4 and +V.

Q9. Explain counter type A/D converter with diagram.
Answer: Following is the counter type A/D converter



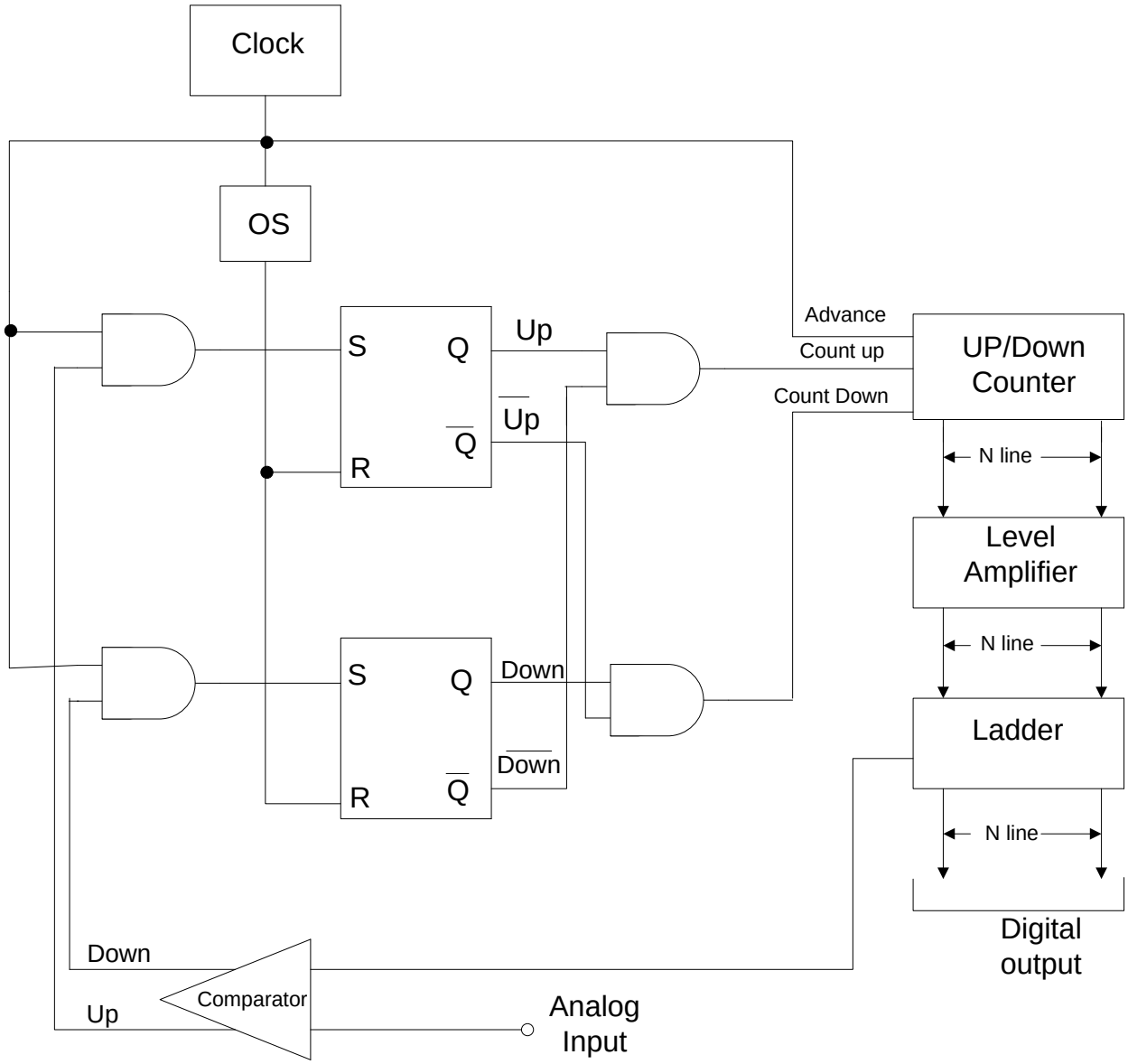
This type of A/D converter consists of binary counter. The digital output signal of this counter is connected to a standard binary ladder D/A converter. If a clock is applied to the input of the counter, the output of the binary ladder D/A converter is the staircase waveform. This waveform is the reference voltage signal for the comparator.

First, the counter is reset to all 0s. Then, when a convert signal appears on the START line,

the gate opens and the clock pulses are allowed to pass through to the input of the counter.

The counter advances through a normal binary count sequence, and the staircase waveform is generated at the output of the ladder. This waveform is applied to one side of the comparator and analog input voltage is applied to the other side. When the reference voltage equals (or exceeds) the input analog voltage, the gate is closed, the counter stops and the conversion is complete. The number stored in the counter is now the digital equivalent of the analog input voltage.

Q10. Explain continuous A/D converter with diagram.
Answer: Following is the continuous A/D converter:

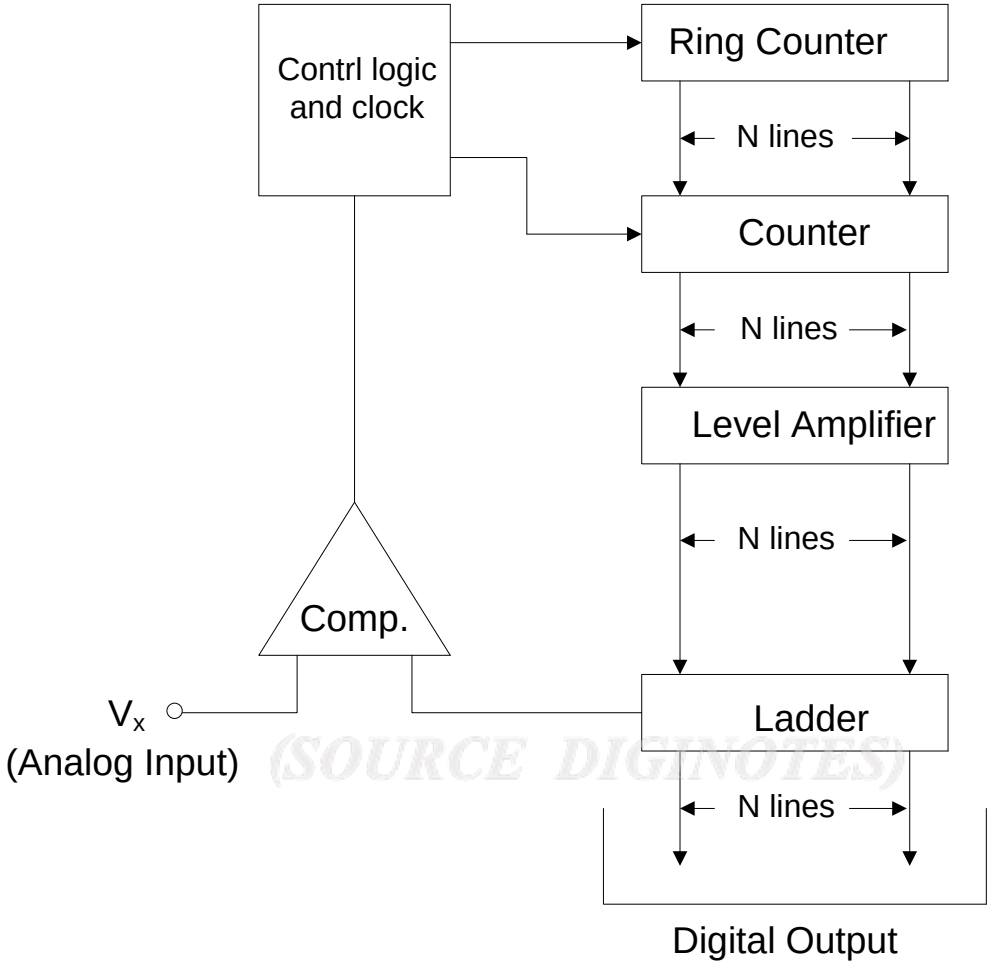


This type of A/D converter consists of binary up/down counter. The digital output signal of this counter is connected to a standard binary ladder to form a D/A converter. Output of the ladder is fed into a comparator which has two outputs. When the input analog voltage is more positive than the ladder output, Up output of the comparator is high. When the input analog voltage is more negative than the ladder output, the down output is high.

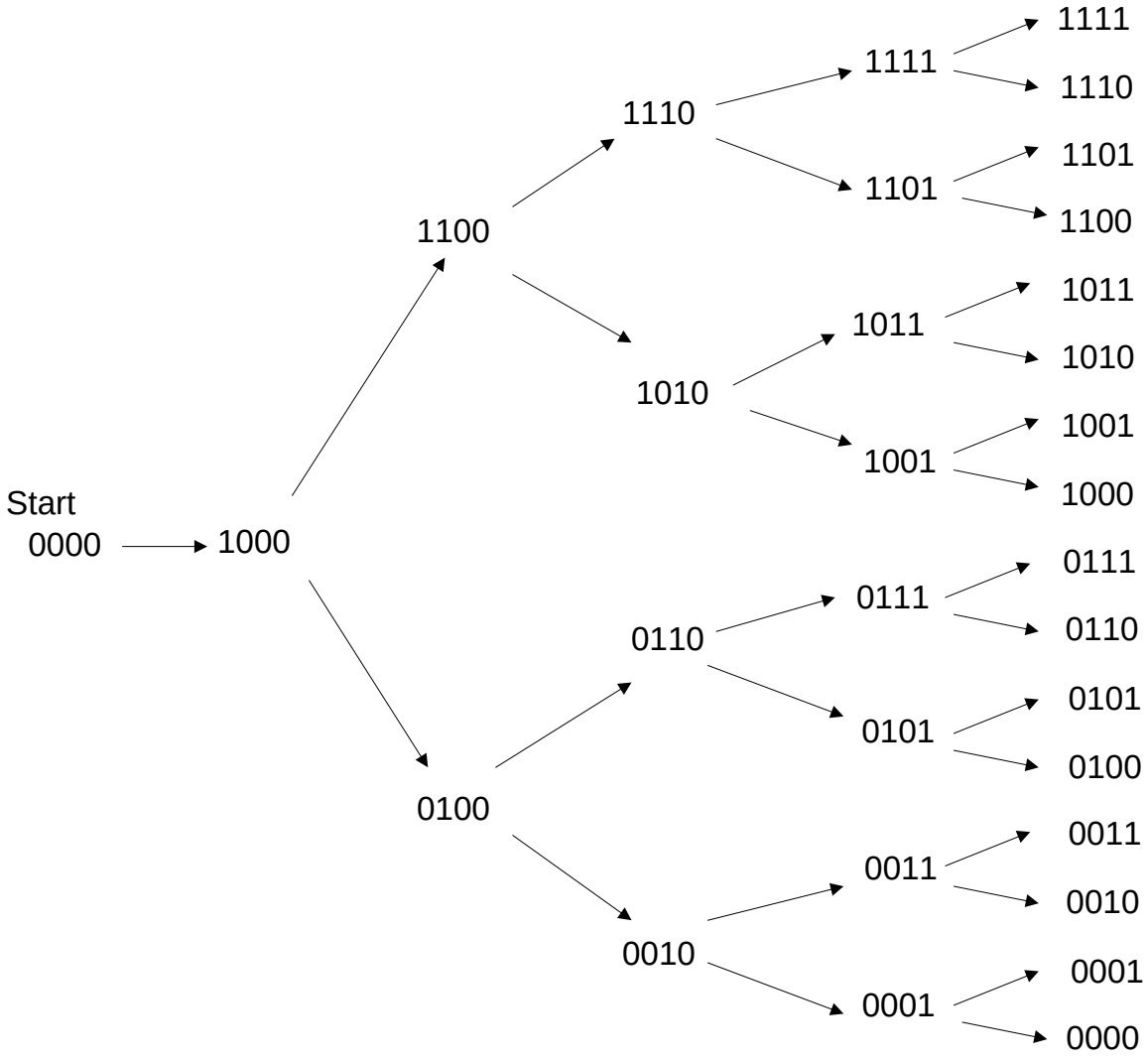
If the Up output of the comparator is high, the AND gate at the input of the Up flipflop open, and the first time the clock goes positive, the flipflop is set. At moment down flipflop is reset, the AND gate which controls the count-up line of the counter will be true and the counter advance one count. As long as the Up line out of the comparator is high, the converter continues to operate and advances its count.

At the point where the ladder voltage becomes more positive than the input voltage, the Up line of the comparator goes low and the Down line goes high. The converter then goes through a count-down conversion cycle.

Q11. Explain successive approximation converter with diagram.
Answer: Following shows the block diagram for successive approximation converter.



Following shows the operation performed in successive approximation converter



Successive approximation converter consists of counter which is first reset to all 0s. The MSB of the counter is then set. The MSB is then left in or taken out (by resetting the MSB flipflop) depending on the output of the comparator. Then the second MSB is set in, and comparator is made to determine whether to reset the second MSB flipflop. The process is repeated down to LSB and at this time desired number is in the counter. The converter operates by successive dividing the voltage ranges in half. The successive approximation method is the process of approximating the analog voltage by trying 1 bit at a time beginning with MSB. The operation is shown in the above diagram.