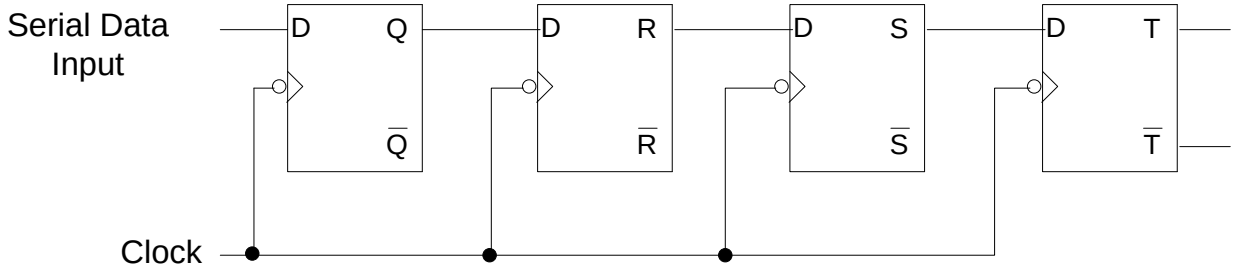
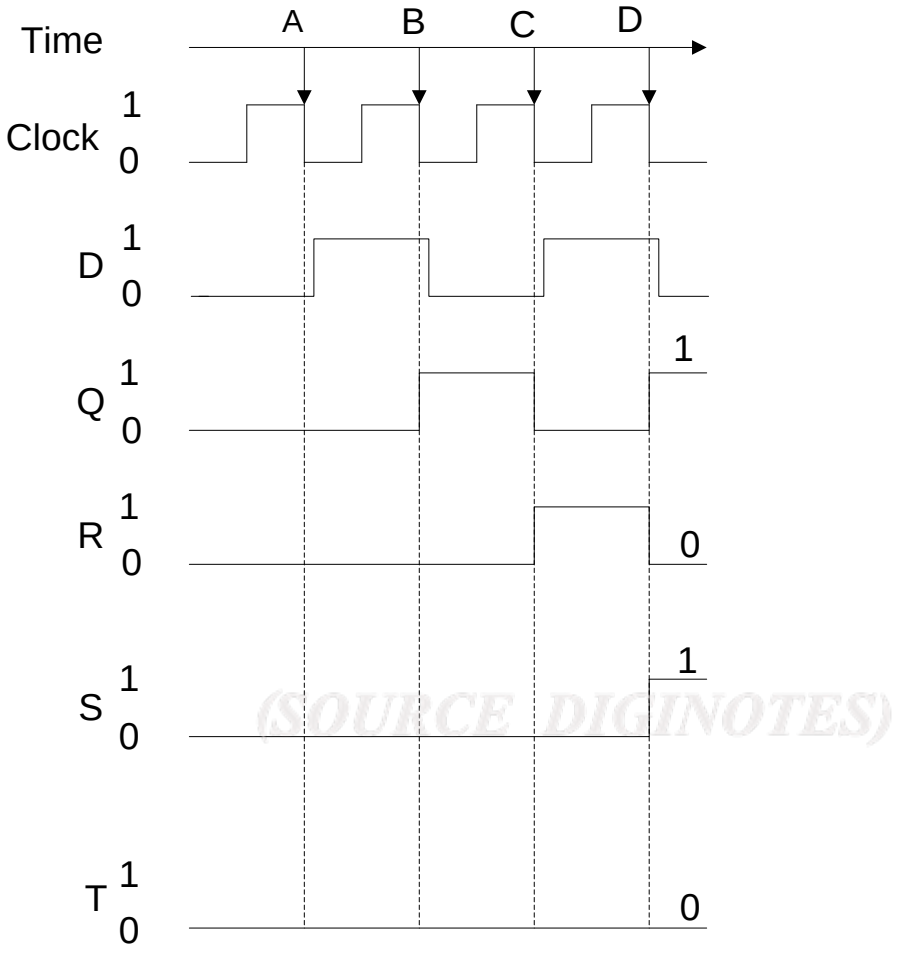
Q1. Explain 4-bit Serial in-Serial out register.

Answer: 4-bit serial in-serial out register is shown below:



The waveform for the above circuit is shown below:

It has been assumed that initially Q=0, R=0, S=0 and T=0.



At clock edge A: DQRS=0000. As the clock trigger at A, the values at DQRS is transferred to QRST and QRST=0000.

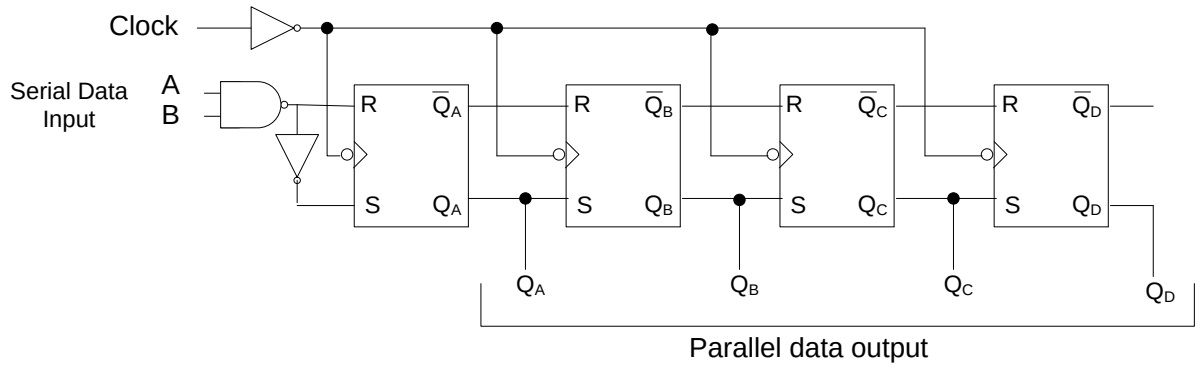
At clock edge B: DQRS=1000. As the clock trigger at B, the values at DQRS is transferred to QRST and QRST=1000.

At clock edge C: DQRS=0100. As the clock trigger at C, the values at DQRS is transferred to QRST and QRST=0100.

At clock edge D: DQRS=1010. As the clock trigger at B, the values at DQRS is transferred to QRST and QRST=1010.

Q2. Explain 4-bit Serial in-parallel out register.

Answer: 4-bit serial in-parallel out register is shown below:



Data shifted in serially, but shifted out in parallel as shown in the figure above. In order to shift the data out in parallel, output of each flip flop is connected to output pin.

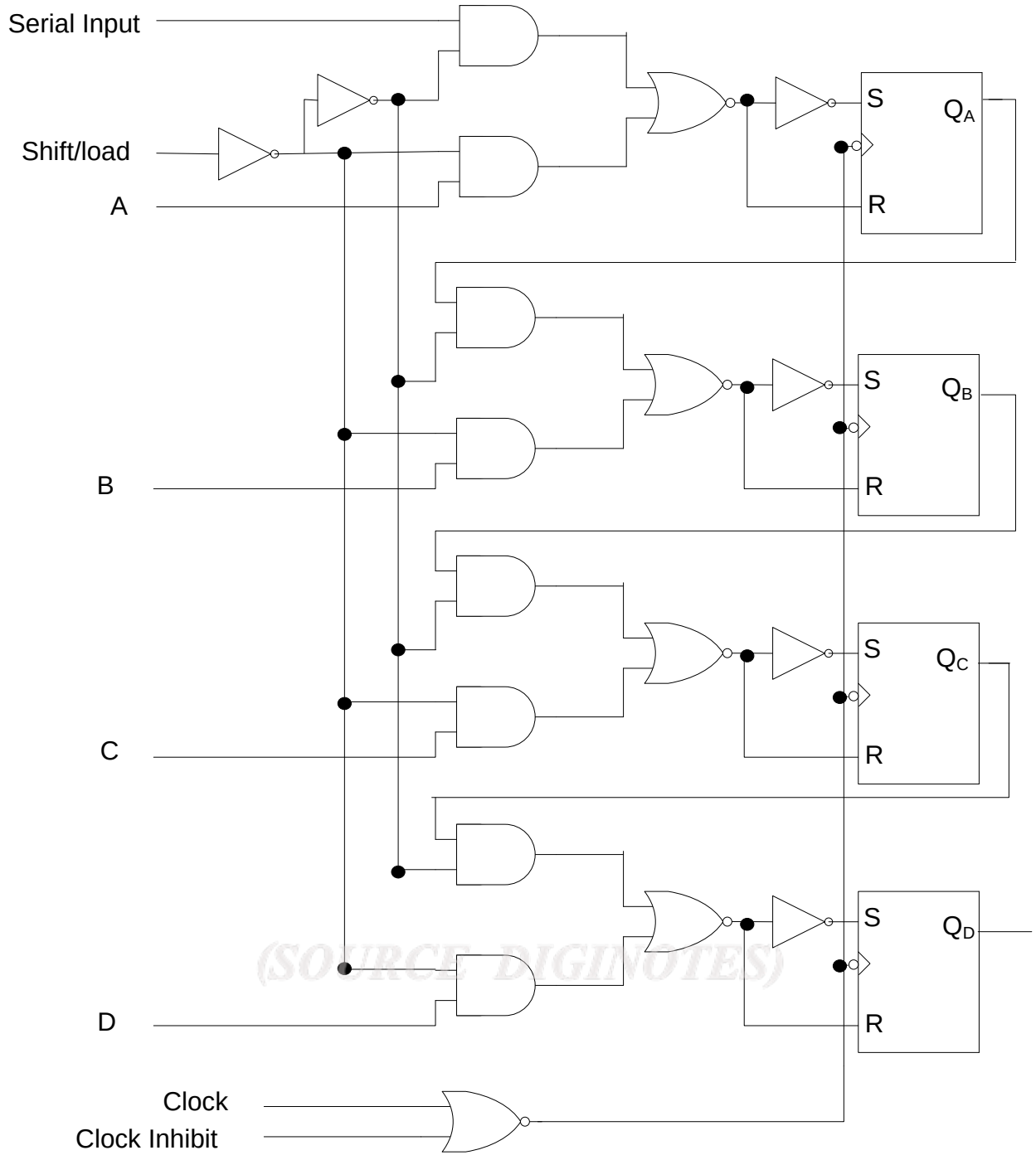
Suppose that the serial data is connected to A, and then B can be used as a control line.

If B is held high, then the NAND gate is enabled and the serial input data passes through the NAND gate is inverted. The input data is shifted serially into the register.

If B is held low, then the NAND gate output is high irrespective of input data.

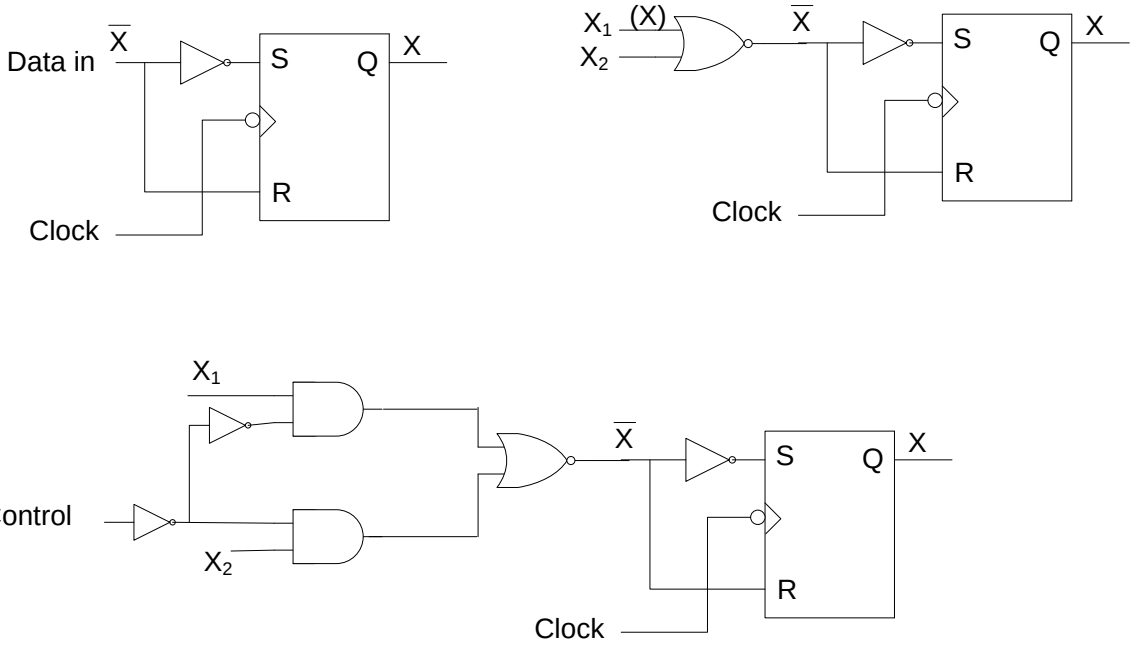
Q3. Explain 4-bit parallel in-Serial out register.

Answer: 4-bit parallel in serial out is shown below.



The above logic block diagram shows 4-bit parallel in (A, B, C and D) and serial out register. This can also be used as serial in if data is entered at Serial Input terminal as shown.

Analysis of the above circuit is given below:



The clocked RS flip flop and the attached inverter form a type D flip flop. If a data bit X is to be clocked into the, the complement of X must be present at the input.

If one leg of the NOR gate is at ground level, a data bit X at the other leg is inverted. This NOR gate provide option of entering data from two different sources, either X_1 or X_2 .

Addition of two AND gates and two inverters allow the selection of data selection of data X_1 or data X_2.

If the control line is high, the upper AND gate is enabled and lower AND gate is disabled.

If the control line is low, upper AND gate is disabled and the lower AND gate is enabled.

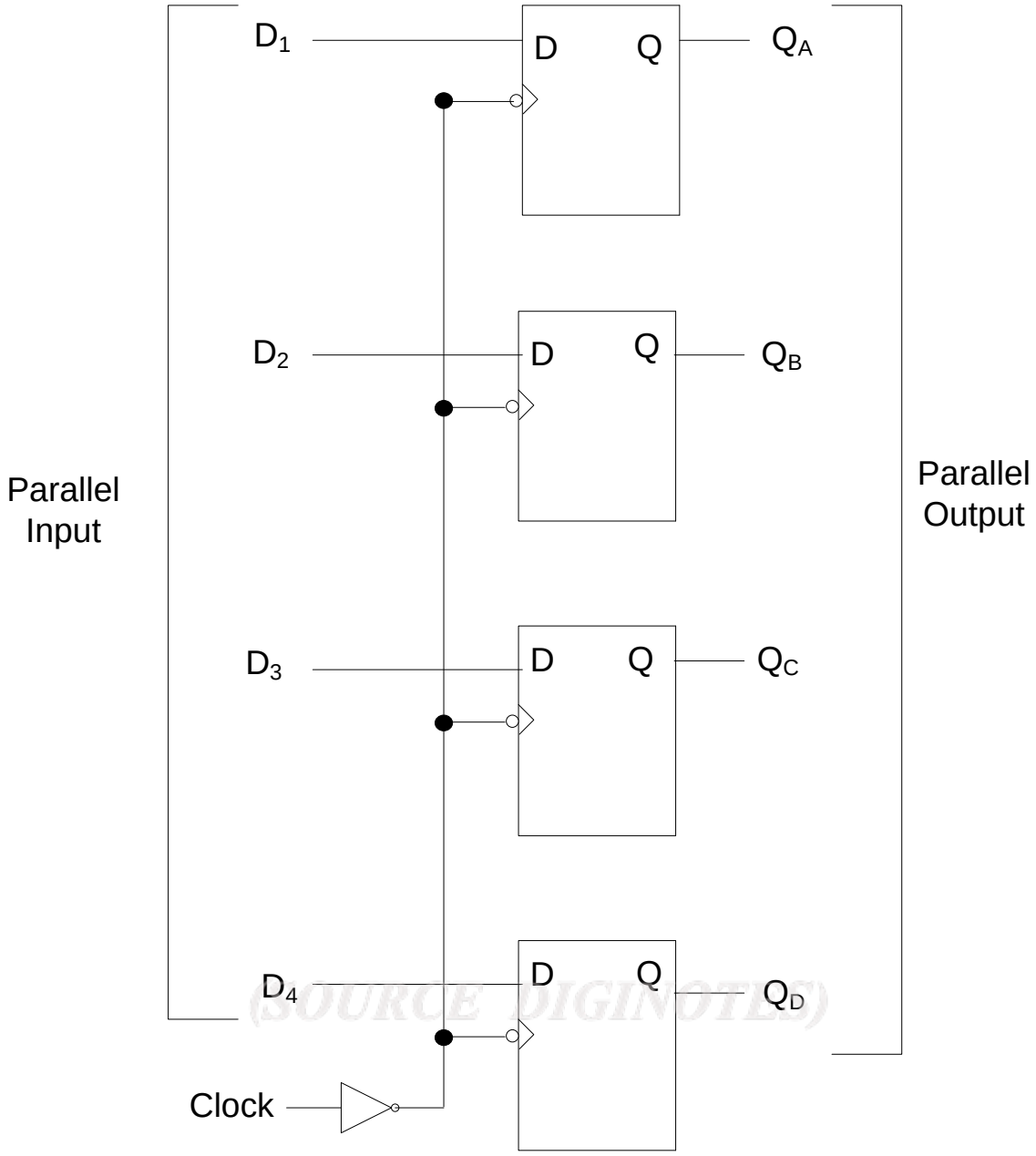
Control line is high: Data bit at X_1 will be shifted into the flip flop at the next clock pulse.

Control line is low: Data bit at X_2 will be shifted into the flip flop at the next clock pulse.

Shift/Load is low: A single clock transition load data into the register in parallel.

Q4. Explain 4-bit parallel in-parallel out register.

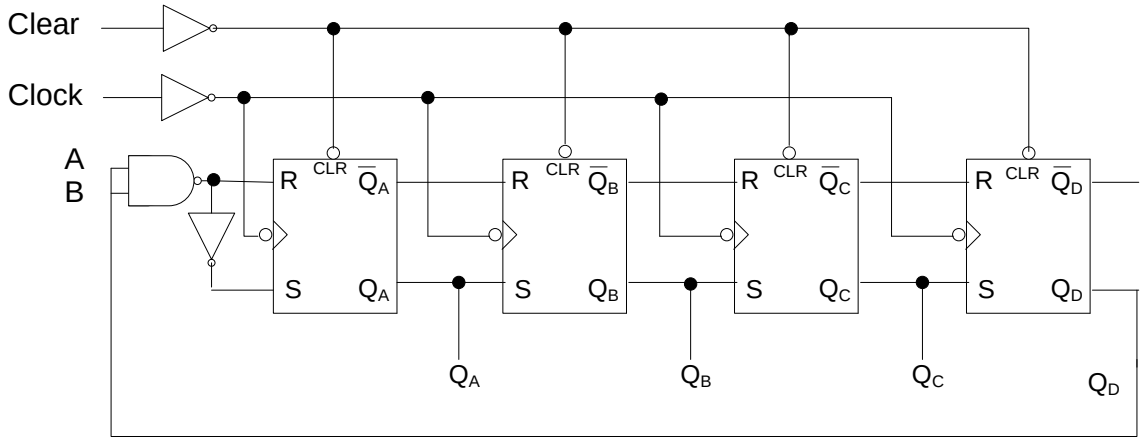
Answer: 4-bit parallel in parallel out is shown below.



Data D_1 through D_4 are shifted into the register with clock pulse. The stored data is immediately available in parallel at the output Q_1 through Q_4. This type of register is used to store data is called data latch or data register..

Q5. Explain 4-bit Ring Counter.

Answer: Following is the 4-bit ring counter.



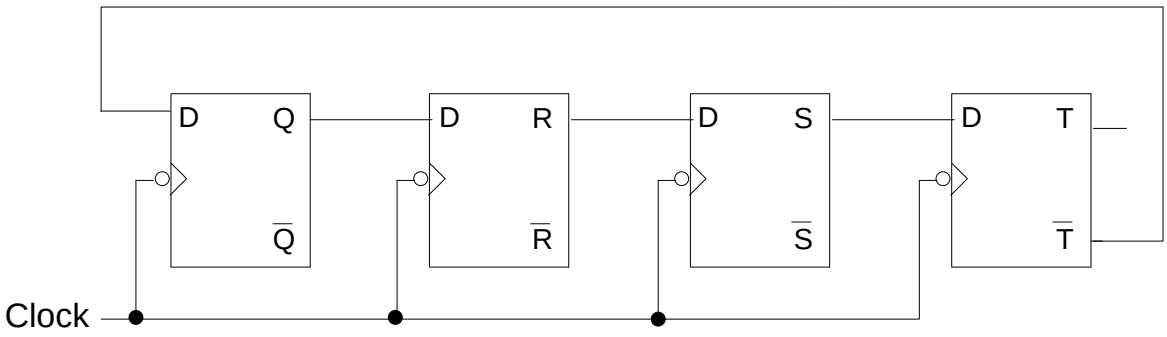
Output of the last flip flop Q_D is feedback to the input of the first flip flop.

State table of Ring Counter is shown below:

Clock	Q_A	Q_B	Q_C	Q_D
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0
5	0	1	0	0
6	0	0	1	0
7	0	0	0	1
8	1	0	0	0

Q6. Design 4-bit Johnson counter (Switch Tail Counter) with state table.

Answer: 4-bit Johnson counter is shown below.



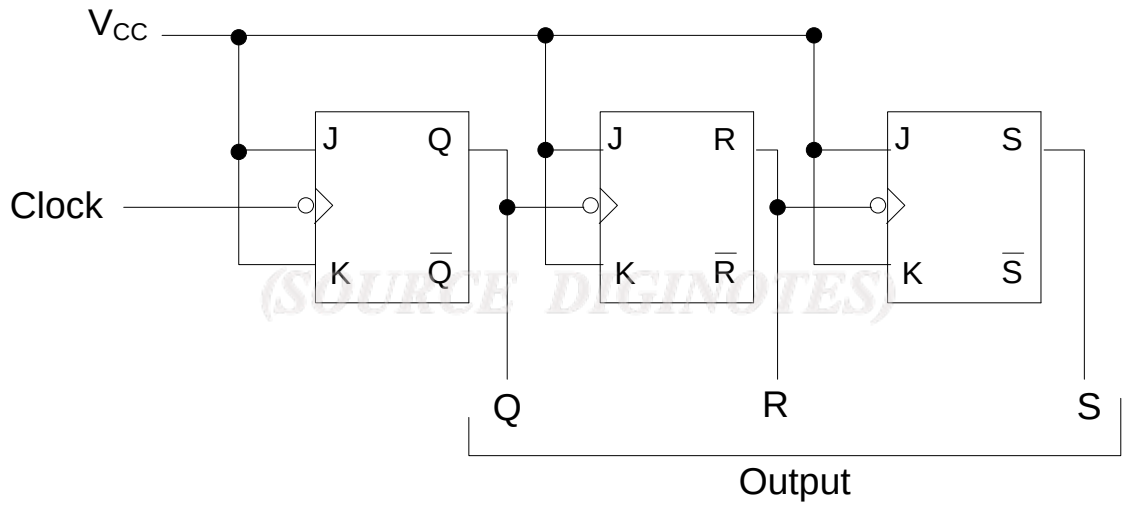
Inverting output of the last flip flop is feedback to the first flip flop.

State table of Johnson Counter is shown below:

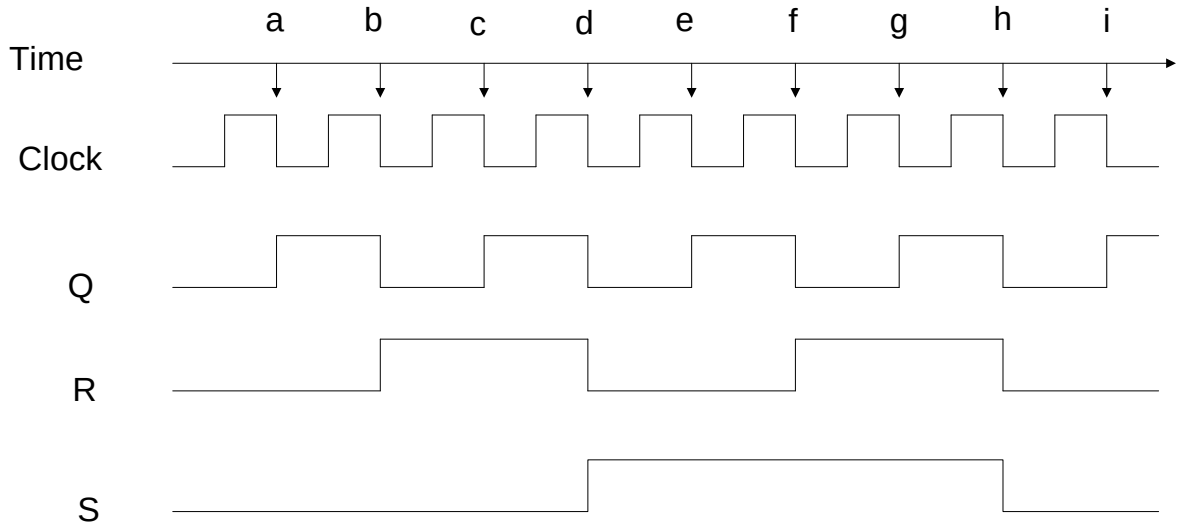
Clock	Serial in=T'	Q	R	S	T
0	1	0	0	0	0
1	1	1	0	0	0
2	1	1	1	0	0
3	1	1	1	1	0
4	0	1	1	1	1
5	0	0	1	1	1
6	0	0	0	1	1
7	0	0	0	0	1
8	1	0	0	0	0
9	1	1	0	0	0

Q7. Explain a 3-bit binary Ripple up counter, give the block diagram, truth table and output waveforms.

Answer: Following is a Ripple Up Counter (or Asynchronous UP Counter).



Waveforms:

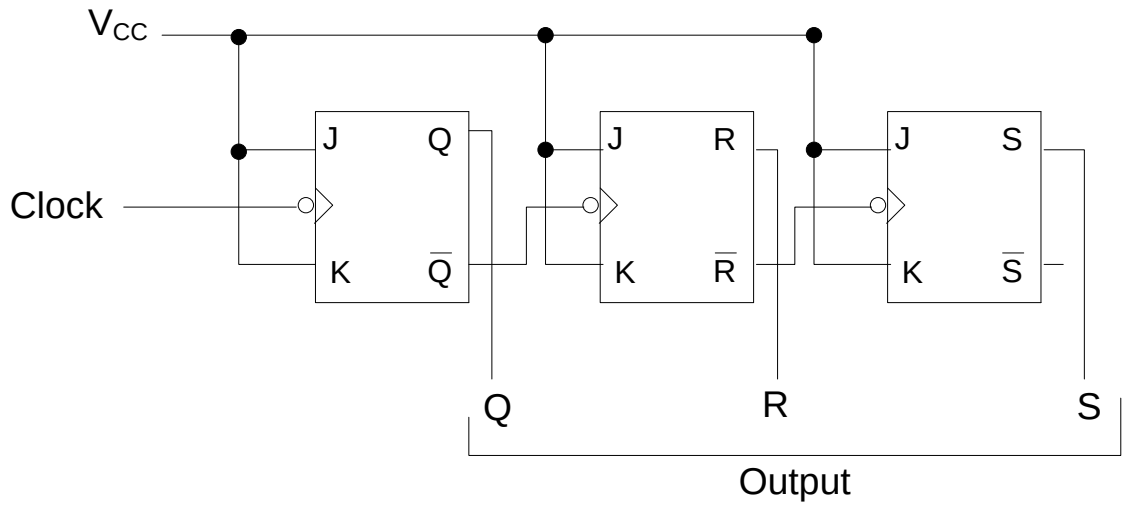


Truth Table:

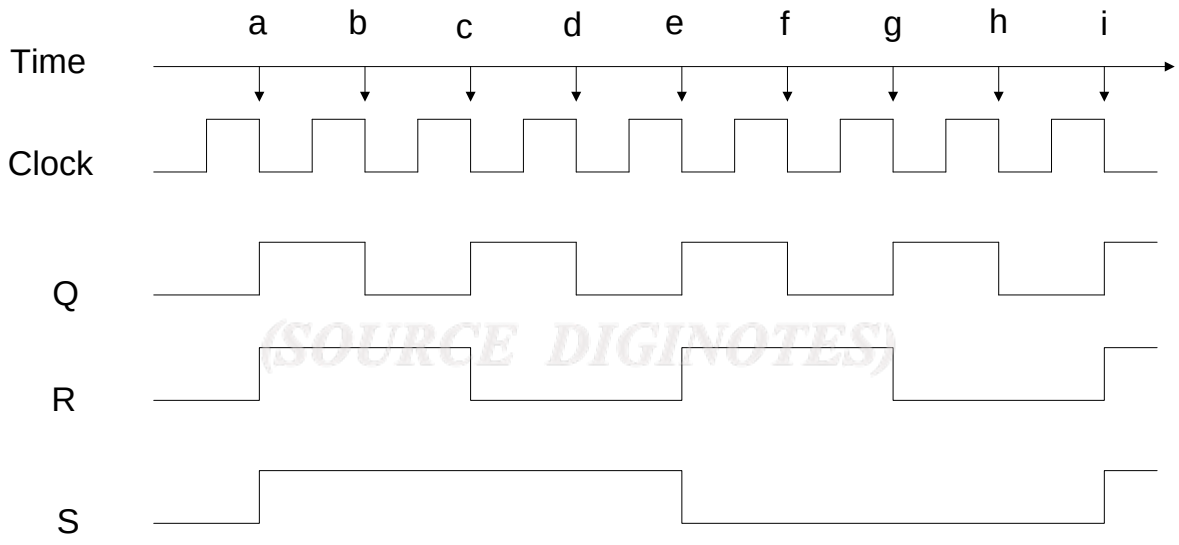
Negative Edge Triggered Clock	Q	R	S	Count
---	0	0	0	0
a	0	0	1	1
b	0	1	0	2
c	0	1	1	3
d	1	0	0	4
e	1	0	1	5
f	1	1	0	6
g	1	1	1	7
h	0	0	0	0
i	0	0	1	1

Q8. Explain a 3-bit binary Ripple down counter, give the block diagram, truth table and output waveforms.

Answer: Following is a Ripple Down Counter (or Asynchronous Down Counter).



Waveforms:

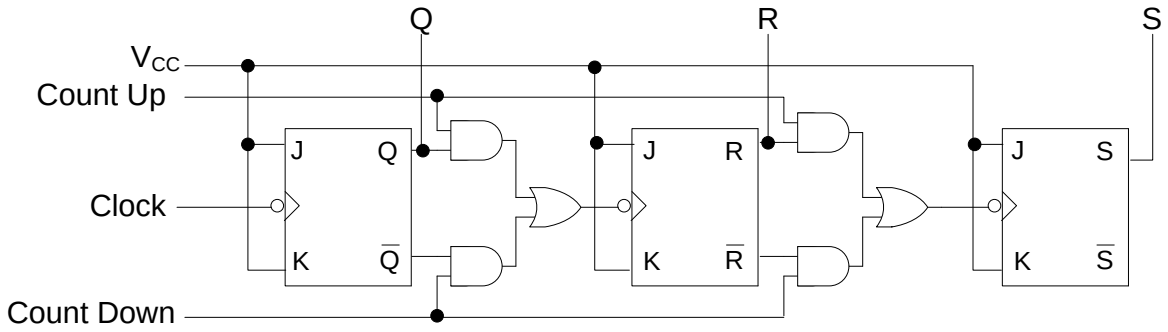


Truth Table:

Negative Edge Triggered Clock	Q	R	S	Count
---	0	0	0	0
a	1	1	1	7
b	1	1	0	6
c	1	0	1	5
d	1	0	0	4
e	0	1	1	3
f	0	1	0	2
g	0	0	1	1
h	0	0	0	0
i	1	1	1	7

Q9. Explain a 3-bit Ripple Up Down Counter.

Answer: Following is a Ripple Up Down Counter.



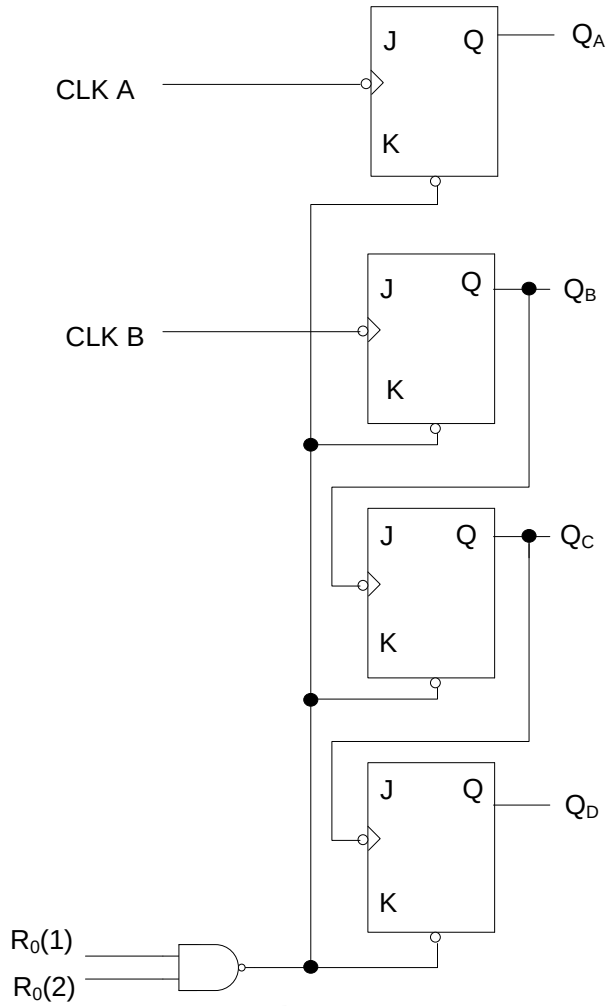
Ripple Up Down Counter is combination Ripple Up Counter and Ripple Down Counter.

If Count Up control is high and Count Down control is low, the above counter will be Up Counter.

If Count Up control is low and Count Down control is high, the above counter will be Down Counter.

Q10. Explain the 7493 IC.

Answer: Following is the 7493 IC



7493 IC is a 4 bit binary counter that can be used in either mod-8 or mod-16.

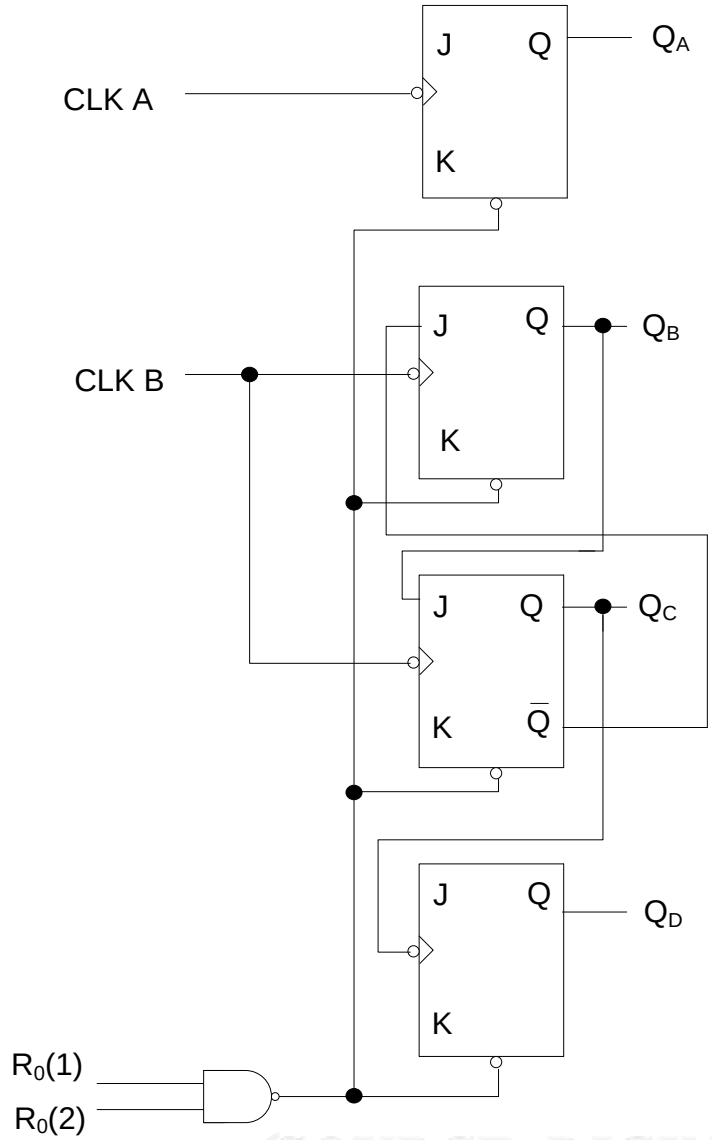
If the clock is applied at CLK B, the counter will be mod-8 counter and the output appear at Q_B, Q_C and Q_D.

If the clock is applied at CLK A and QA is connected to CLK B, the counter will be mod-16 Counter and the output appear at Q_A, Q_B, Q_C and Q_D.

$R_0(1)$ and $R_0(2)$ are used to reset all flip flops simultaneously.

Q11. Explain IC 7492.

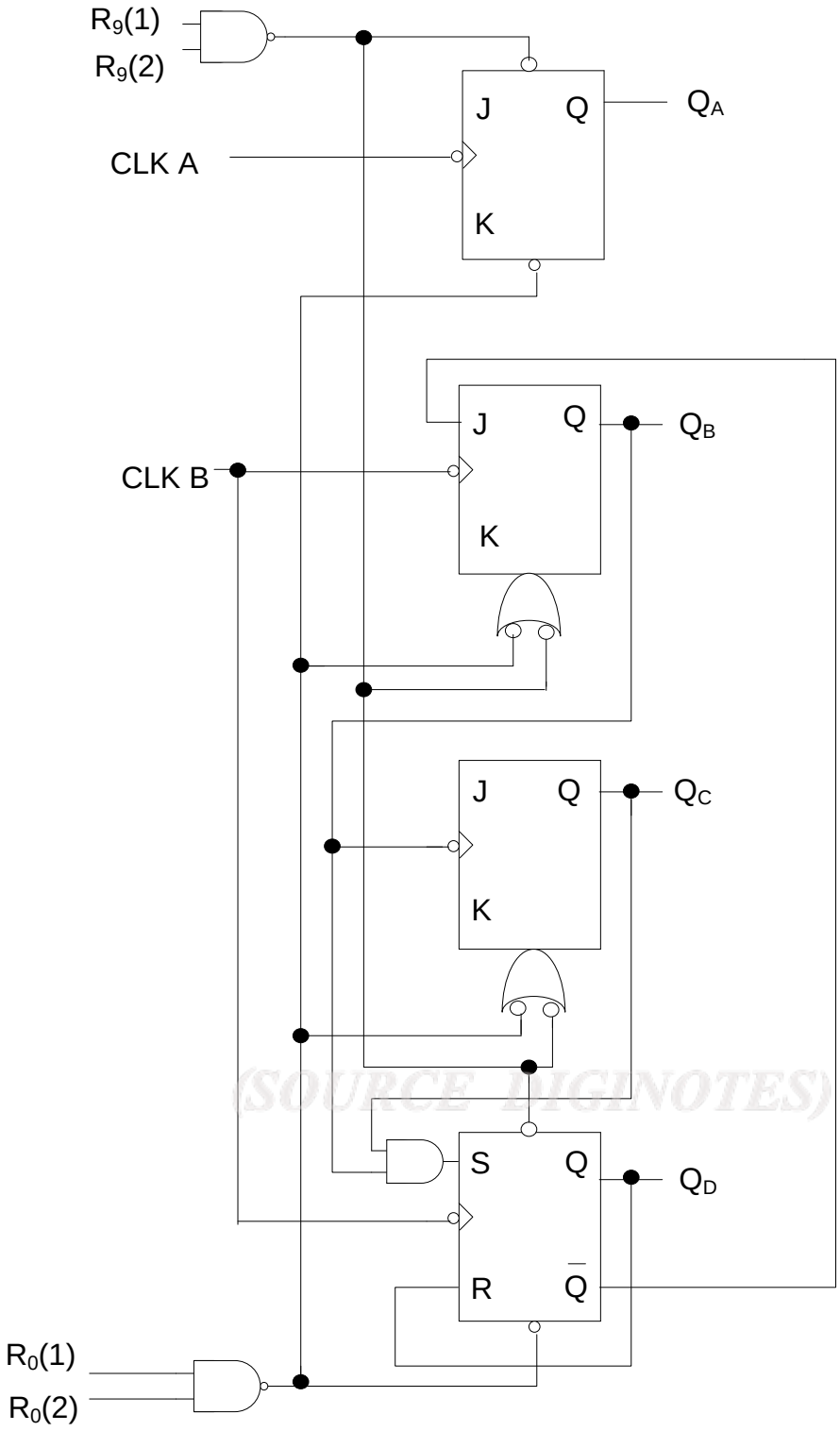
Answer: Following is the logical diagram for IC 7492



IC 7492 can be used as divide by 12 counter or as divide by 6 counter.
If the clock is applied at input B and the outputs are taken at Q_B, Q_C and Q_D, then the counter is divide by 6 counter.
If the clock is applied at input A, Q_A is connected to input CLK B and the outputs are taken at Q_A, Q_B, Q_C and Q_D, then the counter is divide by 12 counter.
$R_0(1)$ and $R_0(2)$ are used to reset all flip flops simultaneously.

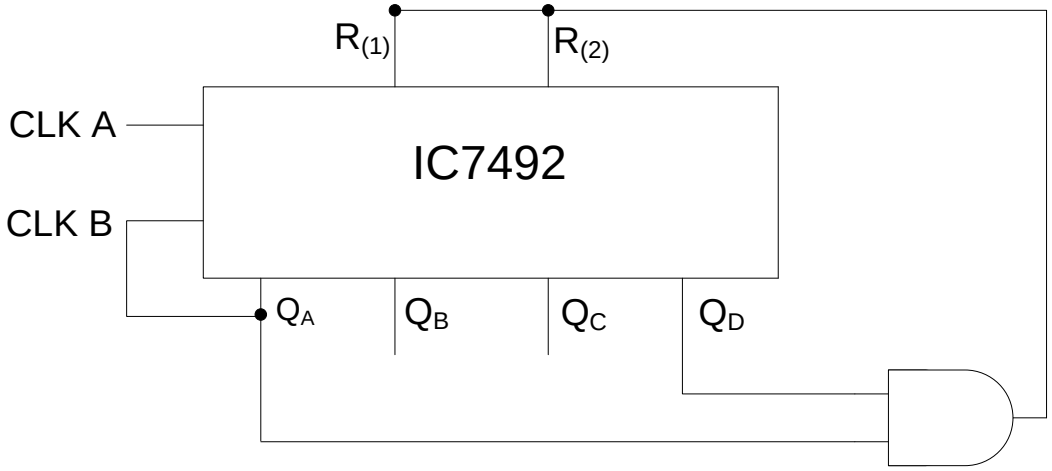
Q12. Explain IC 7490.

Answer: Following is the logical diagram for IC 7490



IC 7490 is a decade counter. If the system clock is applied at CLK A and Q_A is connected to CLK B, then the counter is a decade counter.
$R_0(1)$ and $R_0(2)$ are used to reset all flip flops simultaneously.

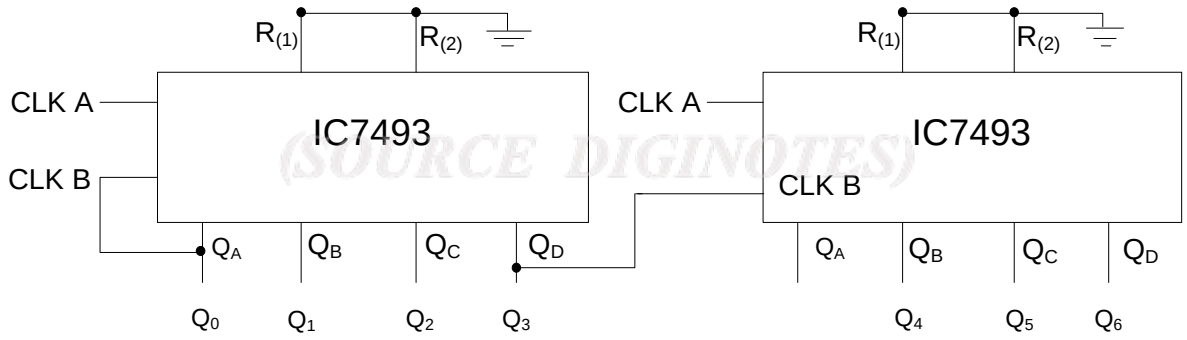
Q13. Design divide by 9 counter using IC 7492.
Answer: Following is the logic diagram to implement divide by 9 counter using IC 7492.



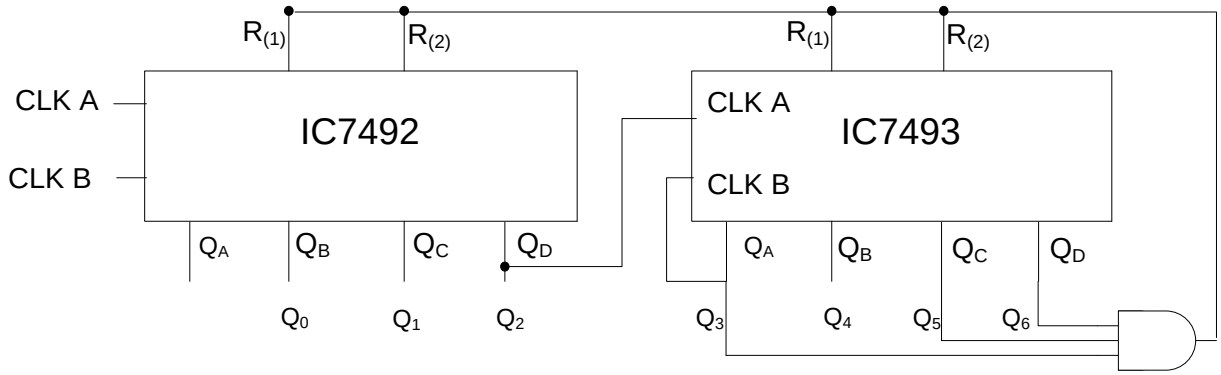
IC 7492 is a mod-12 counter when Q_A is connected to CLK B.
In the above diagram, when $Q_DQ_CQ_BQ_A$=1001, output of the AND gate is high and as a result, the counter reset as $Q_DQ_CQ_BQ_A$=0000. Thus, the above circuit is a divide by 9 counter.

Q14. Design a divide by 128 counter using 7493 ICs.
Answer: Following is the logic diagram divide by 128 counter.

128=16x8. First IC 7493 is used as divide by 16. The CLK B is input from Q_A and the external clock is applied at CLK A.
Second IC 7493 is used as divide by 8. CLK A is unused. CLK B is input from Q_D of the first IC.



Q15. Design a divide by 78 counter using 7493 and 7492 counter ICs.
Answer: Following is the logic diagram divide by 78 counter.



78=6x13.
IC 7492 is used as divide by 6 counter.CLK A is unused and the external clock is applied to the CLK B.
IC 7493 is to be used as divide by 13 counter. To make this as divide by 13 counter, Q_D of IC 7492 is connected to the CLK A of IC 7493. Q_A, Q_C and Q_D are connected as input to a AND gate and output of the AND gate is connected reset pins.

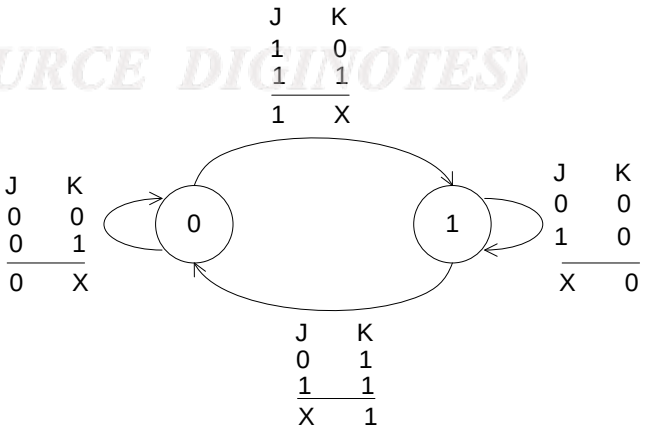
Q16. Design mod-3 synchronous counter.
Answer:
Truth Table

Clock	Counter Output	
	Q_2	Q_1
0	0	0
1	0	1
2	1	0
3	0	0

Truth Table for JK Flip Flop

J	K	Q_{n+1}	Action
0	0	Q_n	No Change
0	1	0	Reset
1	0	1	Set
1	1	$\overline{Q}_n$	Toggle

State Transition Diagram for JK Flip Flop



State table for the design of Modulo-3 synchronous counter

Present State		Next State		J_2	K_2	J_1	K_1
Q_2	Q_1	Q_2+	Q_1+				
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	0	0	X	1	0	X

K- Map for J_2

Q_2 \ Q_1	0	1
0	0	1
1	X	X

$J_2=Q_1$

K- Map for K_2

Q_2 \ Q_1	0	1
0	X	X
1	1	X

$K_2=1$

K- Map for J_1

Q_2 \ Q_1	0	1
0	1	X
1	0	X

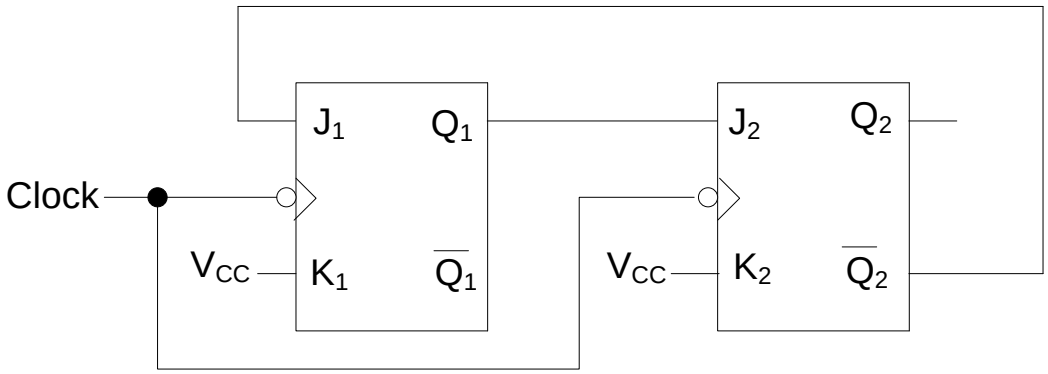
$J_1=\overline{Q}_2$

K- Map for K_1

Q_2 \ Q_1	0	1
0	X	1
1	X	X

$K_1=1$

Logic diagram:



Q17. Design mod-5 synchronous counter.

Answer:

Truth Table:

Clock	Counter Output		
	Q_3	Q_2	Q_1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	0	0	0

Truth Table for JK Flip Flop

J	K	Q_{n+1}	Action
0	0	Q_n	No Change
0	1	0	Reset
1	0	1	Set
1	1	$\overline{Q_n}$	Toggle

State Transition Diagram for JK Flip Flop

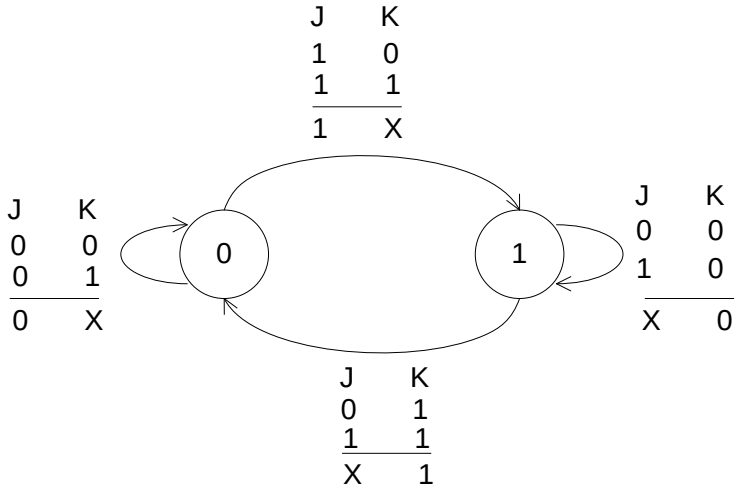
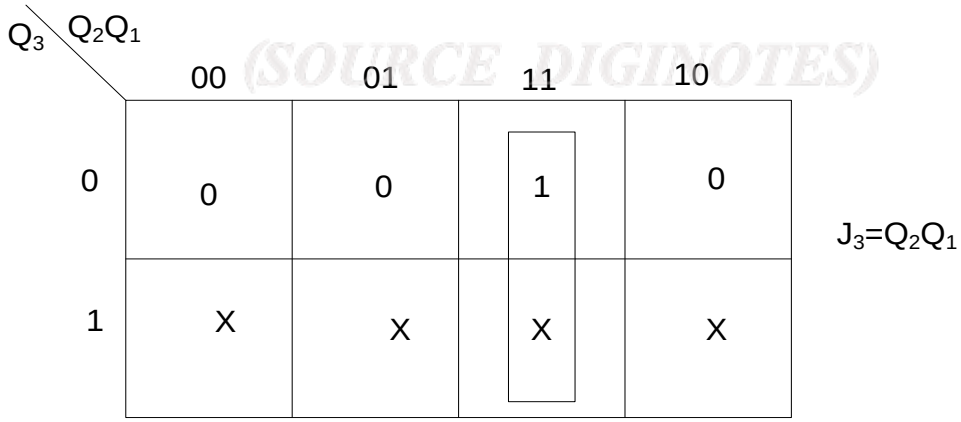


Table for the design of Modulo-5 synchronous counter

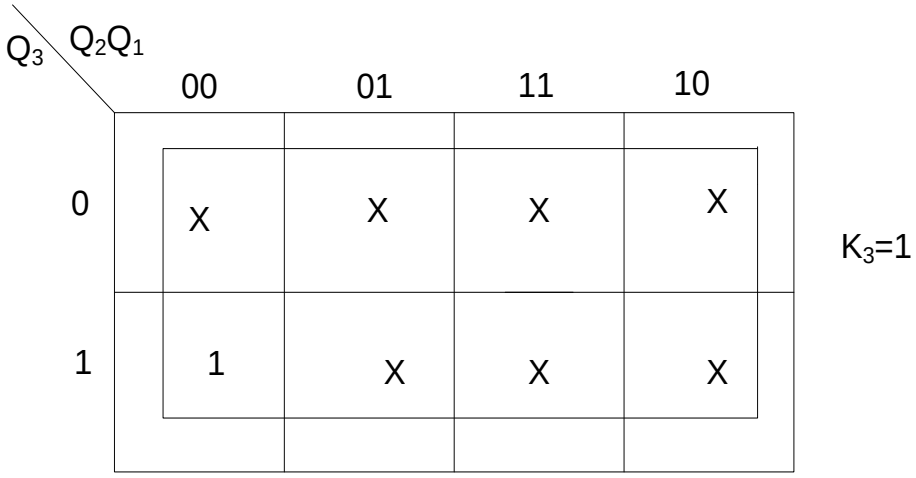
Present State			Next State			J_3	K_3	J_2	K_2	J_1	K_1
Q_3	Q_2	Q_1	Q_3+	Q_2+	Q_1+						
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X

K-map for J_3:

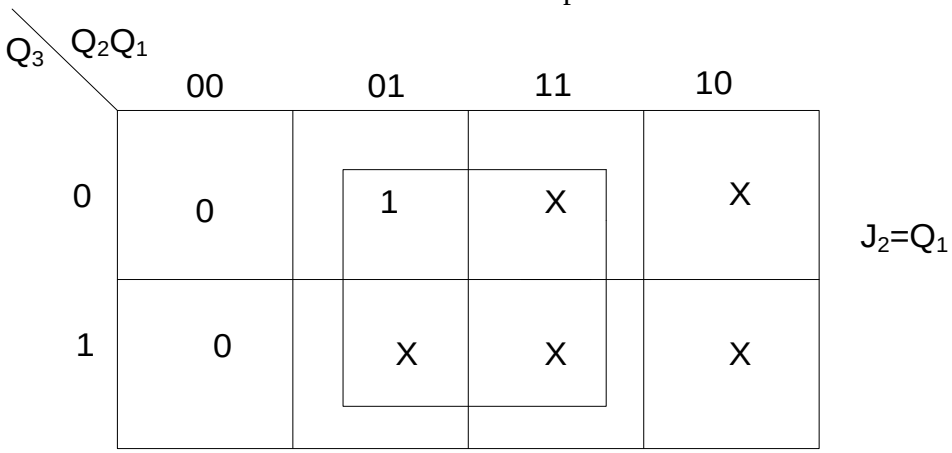


$J_3=Q_2Q_1$

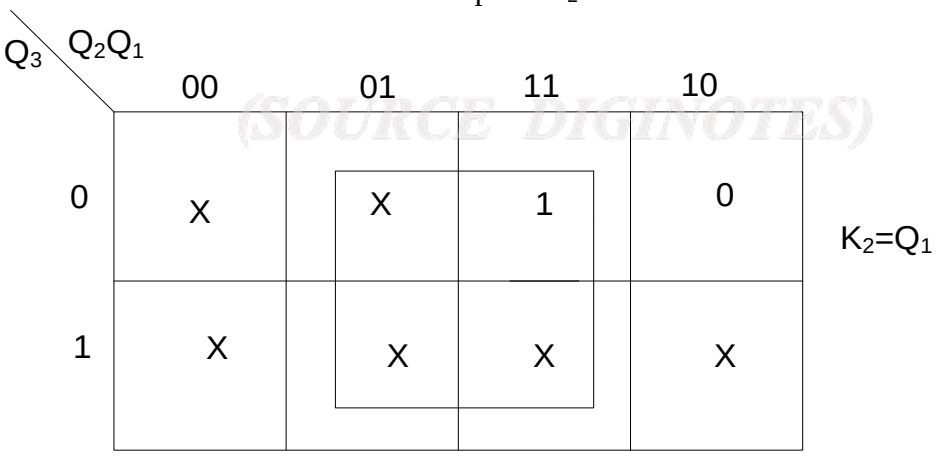
K-map for K_3:



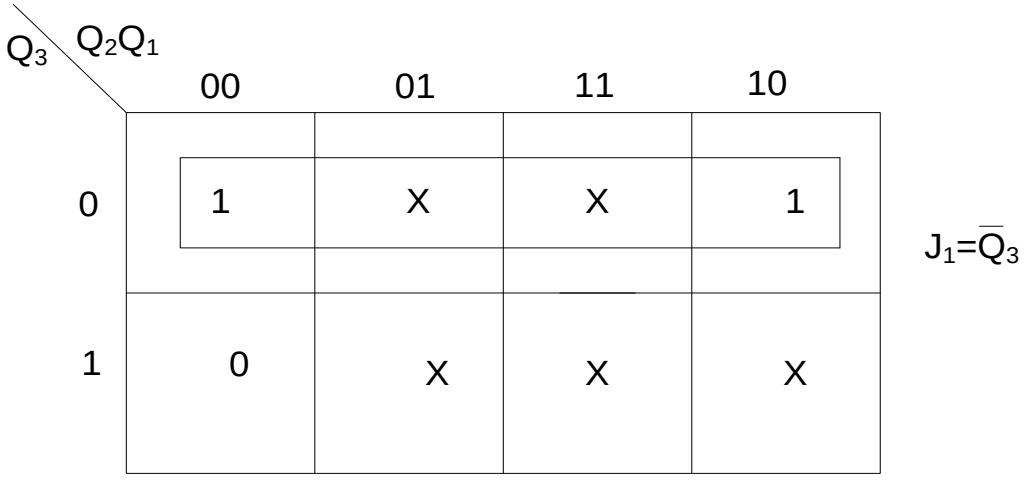
K-map for J_2:



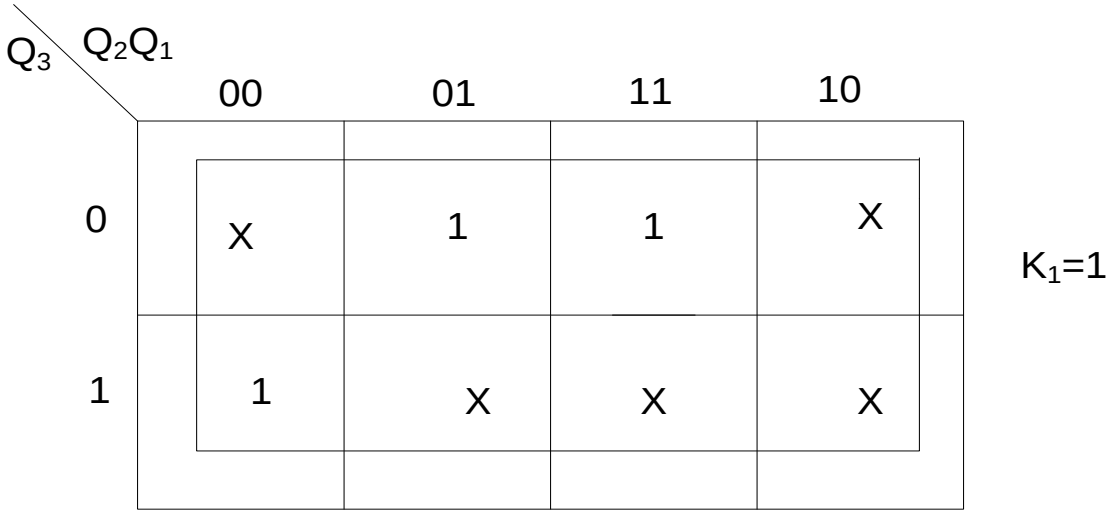
K-map for K_2



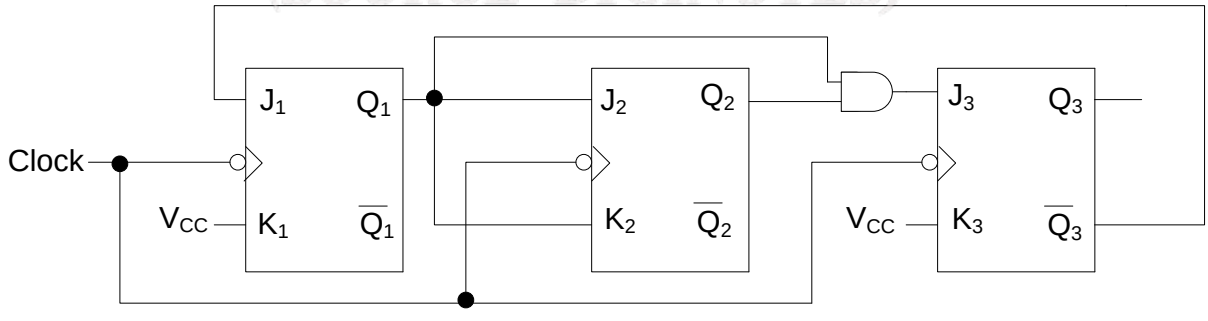
K-map for J_1:



K-map for K_1:



Logic Diagram:



Q18. Design synchronous mod-6 counter.

Answer:

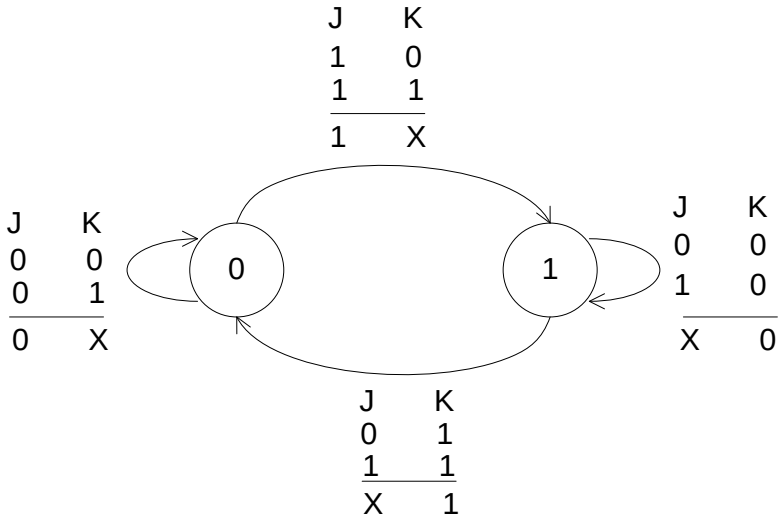
Truth Table:

Clock	Counter Output		
	Q_3	Q_2	Q_1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	0	0	0

Truth Table for JK Flip Flop

J	K	Q_{n+1}	Action
0	0	Q_n	No Change
0	1	0	Reset
1	0	1	Set
1	1	$\overline{Q}_n$	Toggle

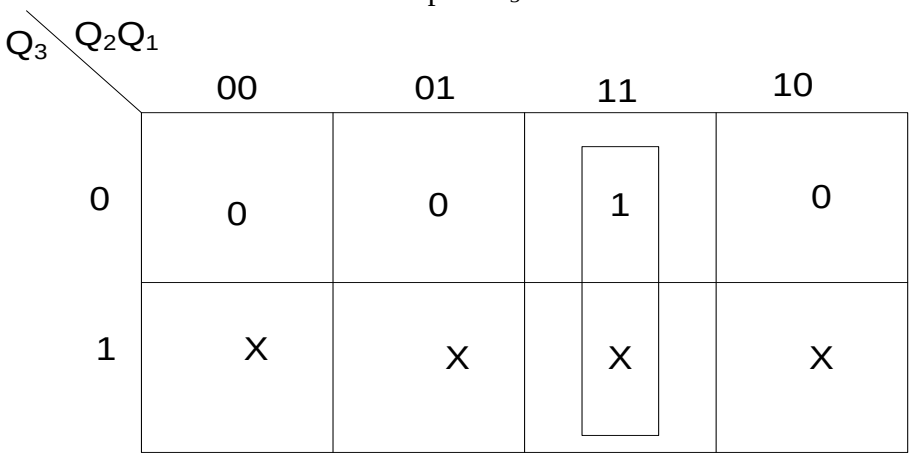
State Transition Diagram for JK Flip Flop



State Table for the design of Modulo-5 synchronous counter

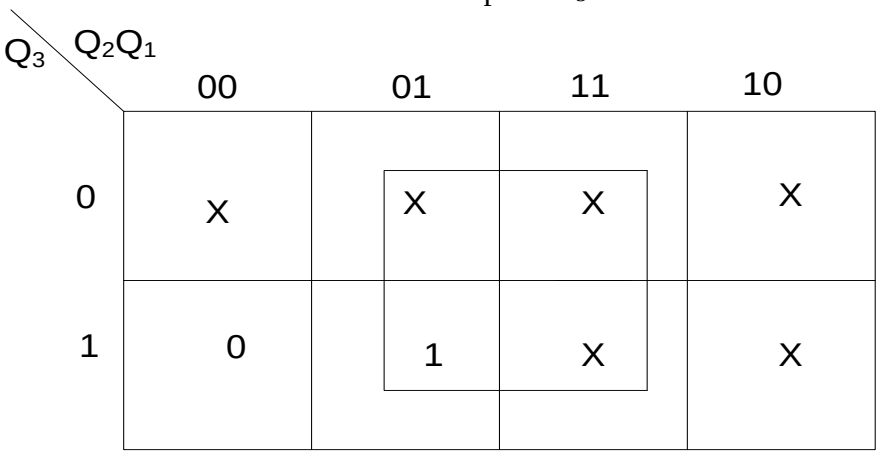
Present State			Next State			J_3	K_3	J_2	K_2	J_1	K_1
Q_3	Q_2	Q_1	Q_3+	Q_2+	Q_1+						
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1

K-map for J_3:



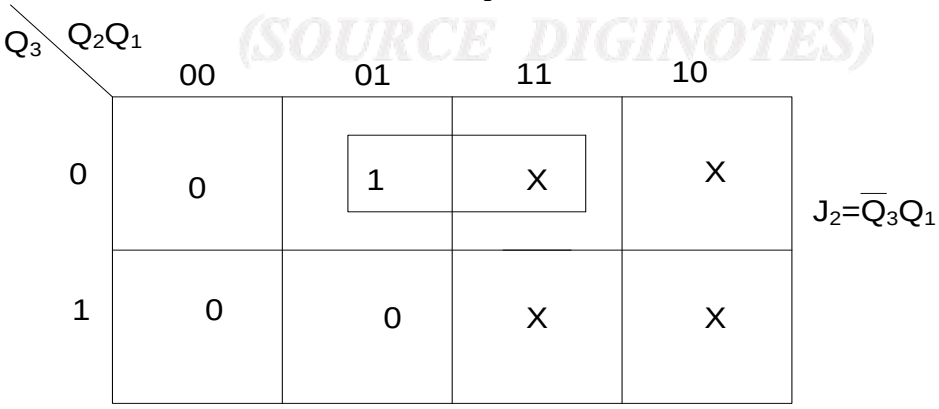
$J_3=Q_2Q_1$

K-map for K_3:



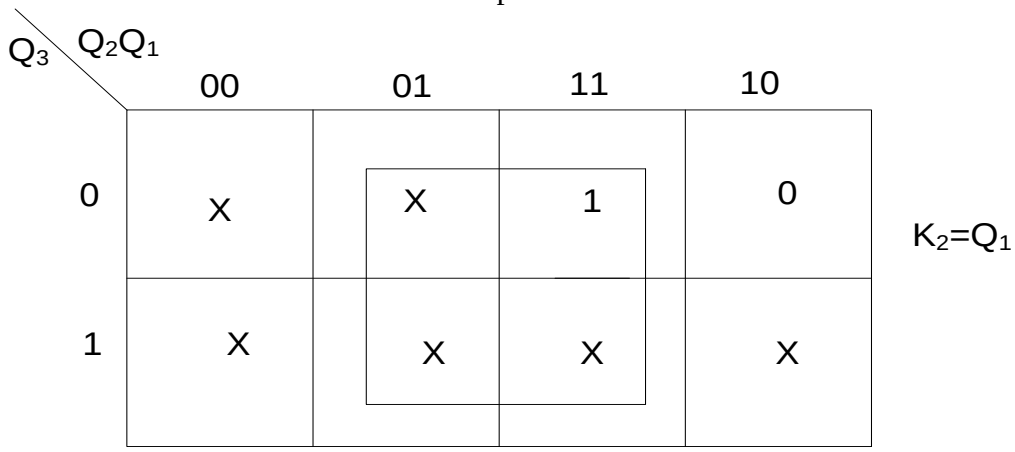
$K_3=Q_1$

K-map for J_2:

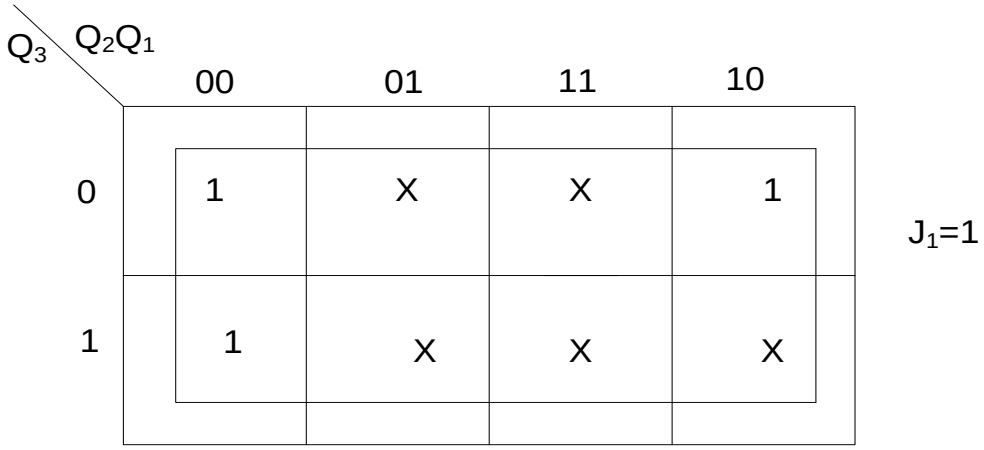


$J_2=\overline{Q}_3Q_1$

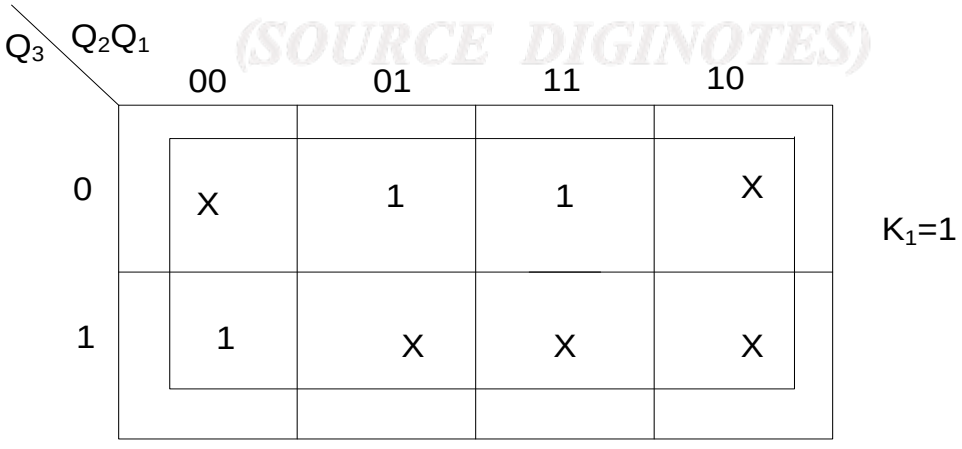
K-map for K_2:



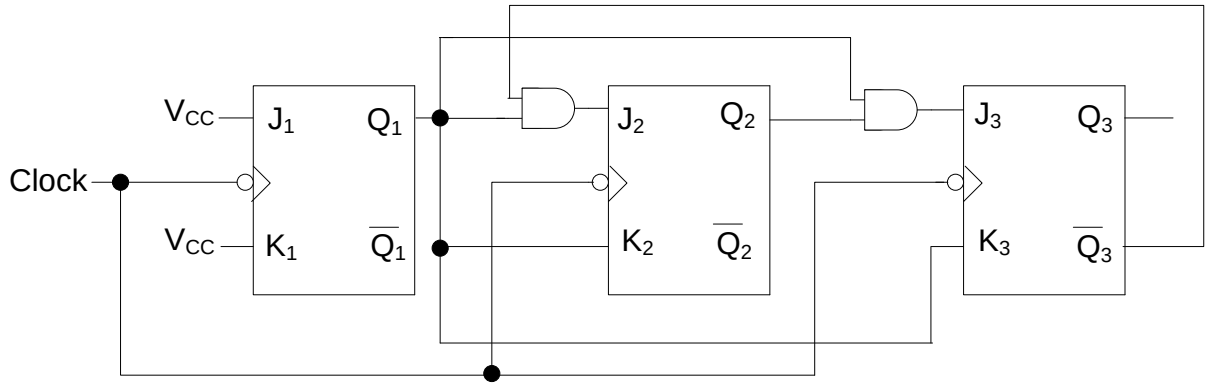
K-map for J_1:



K-map for K_1:



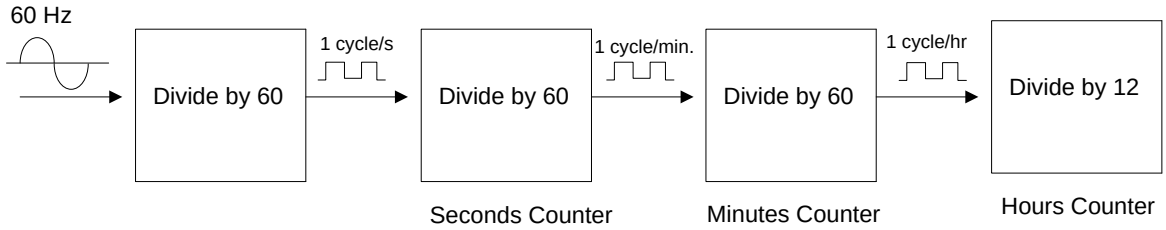
Circuit diagram:



Q19. Explain Digital Clock with block diagram.

Answer: In several countries power supply is 50Hz. There one can use standard variable frequency signal generator to get 60Hz.

Block diagram of a digital clock:



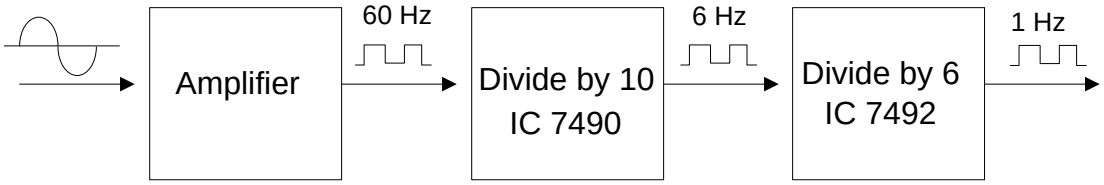
Block diagram shows the functions to be performed. The first divide by 60 counter divides the 60 Hz power signal down to a 1 Hz square wave. This 1 Hz square wave is the input to the second counter.

The second divide by 60 counter changes its state once each second and has 60 discrete states. It can be decoded to provide signal to display second. This counter produces output square wave of 1 cycle per minute and this is the input to the third counter.

The third divide by 60 counter changes its state once each minute and has 60 discrete states. It can be decoded to provide signal to display minute. This counter produces output square wave of 1 cycle per hour and this is input to the fourth counter.

The last counter changes its state once each hour and has12 discrete states. It can be decoded to provide signal to display hour. The last counter reset at every 12 hours.

Divide by 60 counter can be implemented by cascading divide by 10 counter (IC 7490) and divide by 6 counter (IC 7492). This is in the block diagram below.



.Display of Second, Minute and Hour can be implemented by the IC 7447 and 7 segment display.

This is shown below in the following diagram.