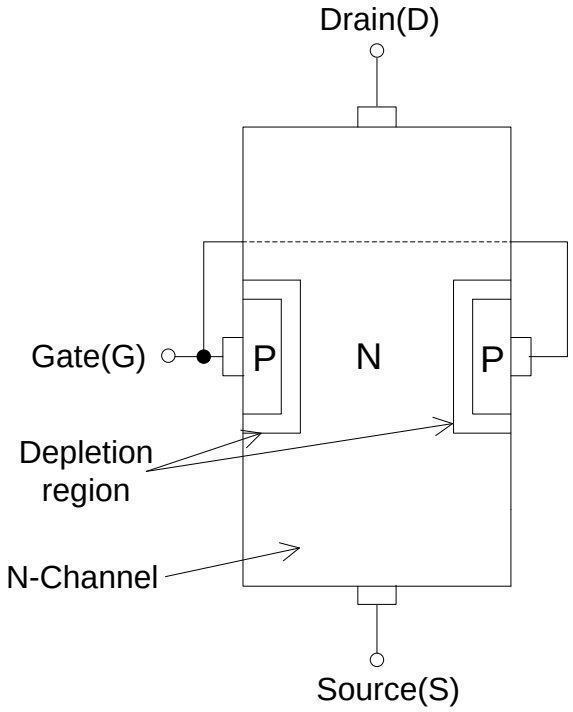
Q1. Explain the construction and principle of operation of N-Channel and P-Channel Junction Field Effect Transistor (JFET).

Answer: N-Channel Junction Field Effect Transistor (JFET)

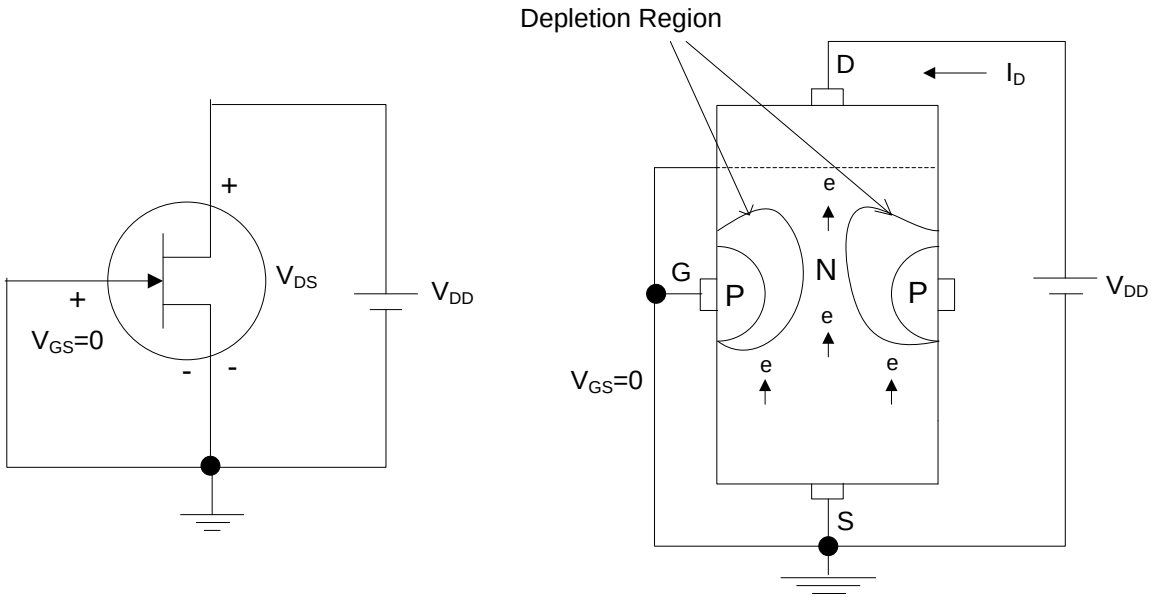
Construction:



The above figure shows the cross sectional view of the N-Channel JFET. P-type semiconductor material are embedded into the N-type semiconductor material as shown in the figure. N-type semiconductor material form a channel between embedded layers of P-type material. Two P-N junctions are formed. Contracts at the top and bottom are referred as Drain (D) and Source (S) respectively. Both the P-type are connected together to form Gate (G).

(Note: For P-Channel JFET, embedded material is N-type. Construction of P-Channel is left to you. In the remaining section, only N-Channel types are explained. P-channel types are left to you.)

Principle of Operation:



When a positive Drain (D)-Source (S) voltage(V_{DS}) is applied with Gate(G) shorted with the Source (S) terminal (V_{GS}=0), the electrons in the N-Channel are attracted to the Drain (D) terminal and due to the flow of electrons, Drain Current (I_D) is established. The value I_D depends on the applied V_{DS} and the resistance of the N-Channel. There is uniform voltage drop across the channel and the two P-N junctions are reversed biased. This results in increase of width of the depletion regions. The depletion regions are wider near the drain region.

I_D increases linearly with the increase of V_{DS} till saturation effect sets in. The value of V_{DS} where the saturation effect sets in is referred to as Pinch-Off (V_P) voltage. When V_{DS} reaches V_P, the value of I_D remain same with the further increase of V_{DS}.

The Gate–Source voltage (V_{GS}) is to control the value I_D. When a negative voltage is applied between Gate and Source terminals, there is an increase of width of the depletion layers and as a result the value of Drain Current (I_D) decreases. As the value V_{GS} is made further negative, at a certain value of negative V_{GS}, the Drain Current become zero. This voltage is referred as Gate-Source pinch-Off voltage.

The relation between the Drain Current, I_D for a given value of V_{GS} is given by

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

Where I_{DSS} is the Drain to Source Current when Gate is shorted with the Source.

V_P is the Pinch –Off voltage.

The drain resistance (r_d) in the saturation region is given by

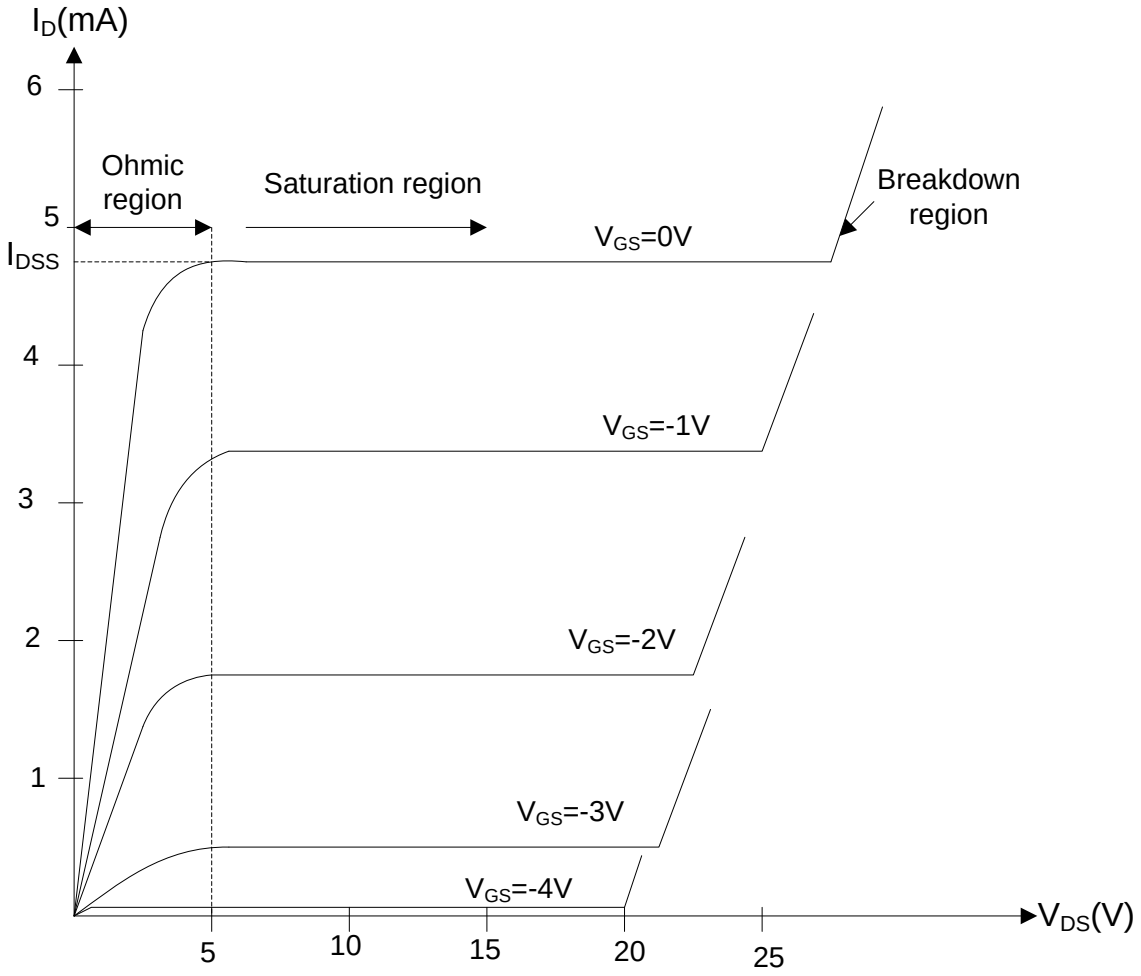
$$r_d = \frac{r_0}{\left(1-\frac{V_{GS}}{V_P}\right)^2}$$

Where r_0 is the resistance at V_{GS}=0 and V_P is the Pinch –Off voltage.

Q2. Explain the Characteristics of N-Channel and P-Channel Junction Field Effect Transistor.

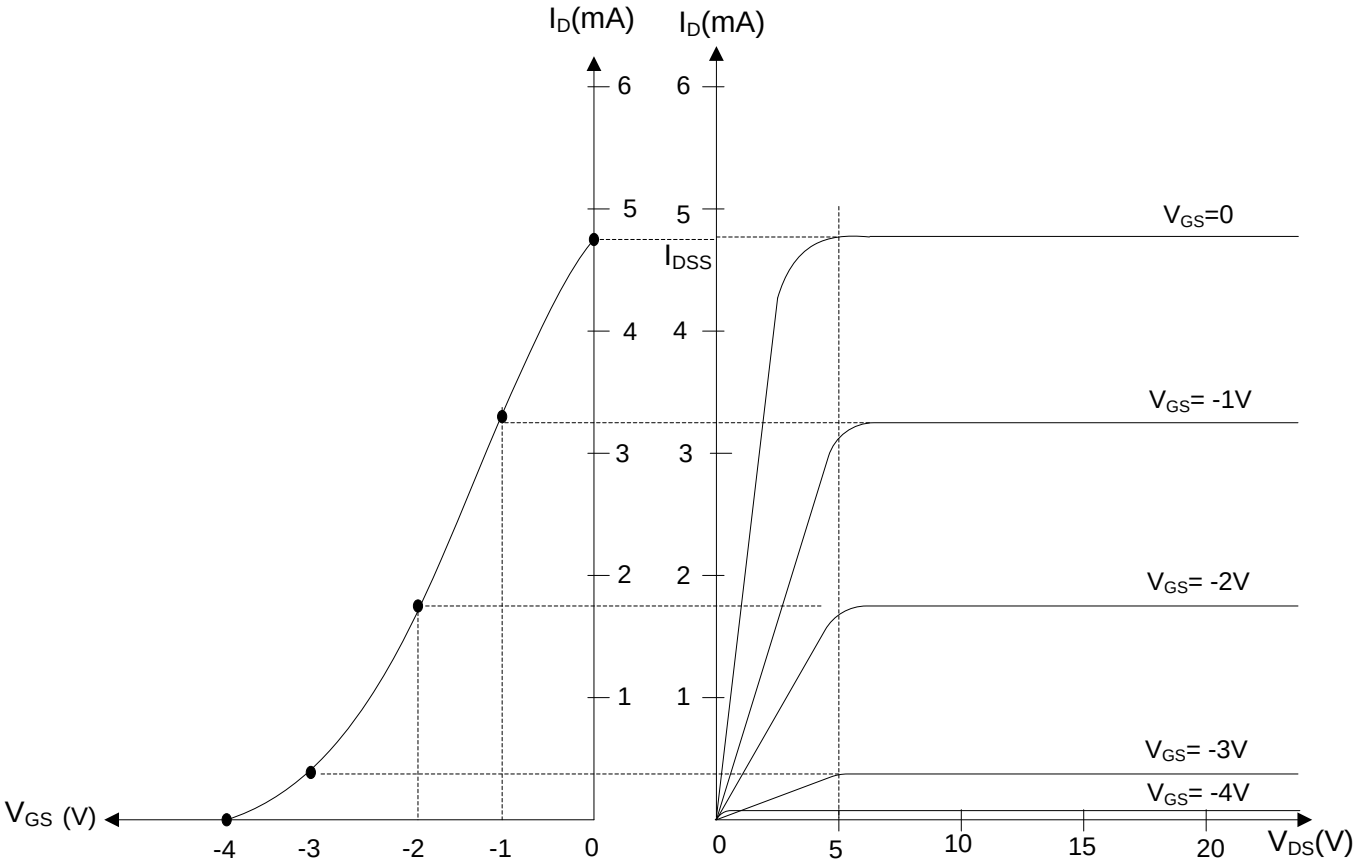
Answer: N-Channel Junction Field Effect Transistor (JFET)

Output Characteristic



The output characteristic of the N-Channel JFET is shown in the above diagram. Drain Current (I_D) is plotted against Drain-Source voltage (V_{DS}) keeping the Gate-Source voltage (V_{GS}) constant. As shown in the diagram, at lower value of Drain-Source voltage (V_{DS}), the Drain Current (I_D) is proportional Drain-Source voltage(V_{DS}) and it follows the Ohm's law. This region is referred as Ohmic region. As Drain-Source voltage (V_{DS}) increases further, at a certain value Drain Current (I_D) does not increase and this region as shown in the diagram is referred as Saturation region. If Drain-Source voltage(V_{DS}) is goes on increase, then after certain value of Drain-Source voltage(V_{DS}), the Drain Current (I_D) increases rapidly with small increase of Drain-Source voltage(V_{DS}) as shown in the diagram. This region is referred as breakdown region.

Transfer Characteristic



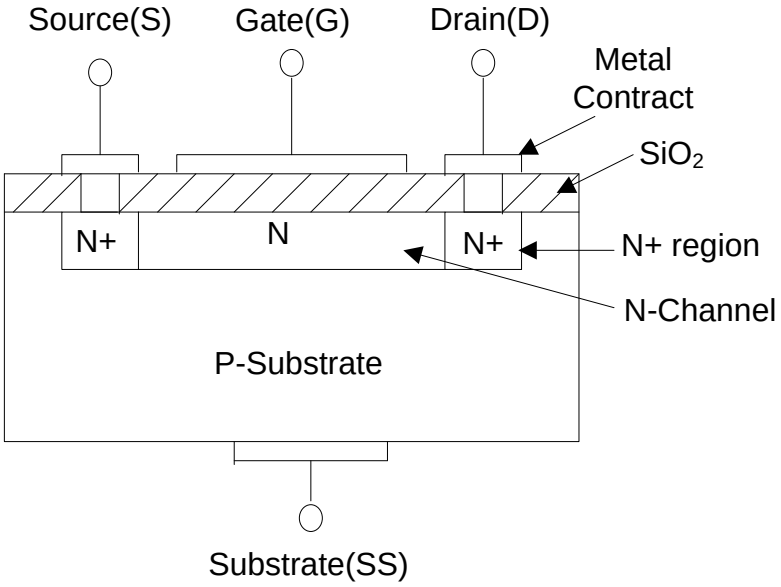
The transfer characteristic of the N-Channel DE-MOSFET is shown in the above diagram. Drain Current (I_D) is plotted against Gate-Source voltage (V_{GS}) keeping the Drain-Source (V_{DS}) voltage constant.

Q3.Explain the construction and principle of operation of N-Channel and P-Channel Depletion Metal Oxide Semiconductor Field Effect Transistor (DE-MOSFET).

Answer: N-Channel Depletion Metal Oxide Semiconductor Field Effect Transistor (DE-MOSFET)

Construction:

Cross Section of an N-Channel DE-MOSFET



The above figure shows the construction of DE-MOSFET. It consists of a P-type substrate. Two N+ type regions linked by an N-channel are formed in the substrate. The source and the drain terminals are formed by connecting metal contacts to the two N+ regions. The gate terminal is connected to the insulating silicon dioxide (SiO_2) layer on the top of the N-channel. There is no direct connection between the gate terminal and the channel.

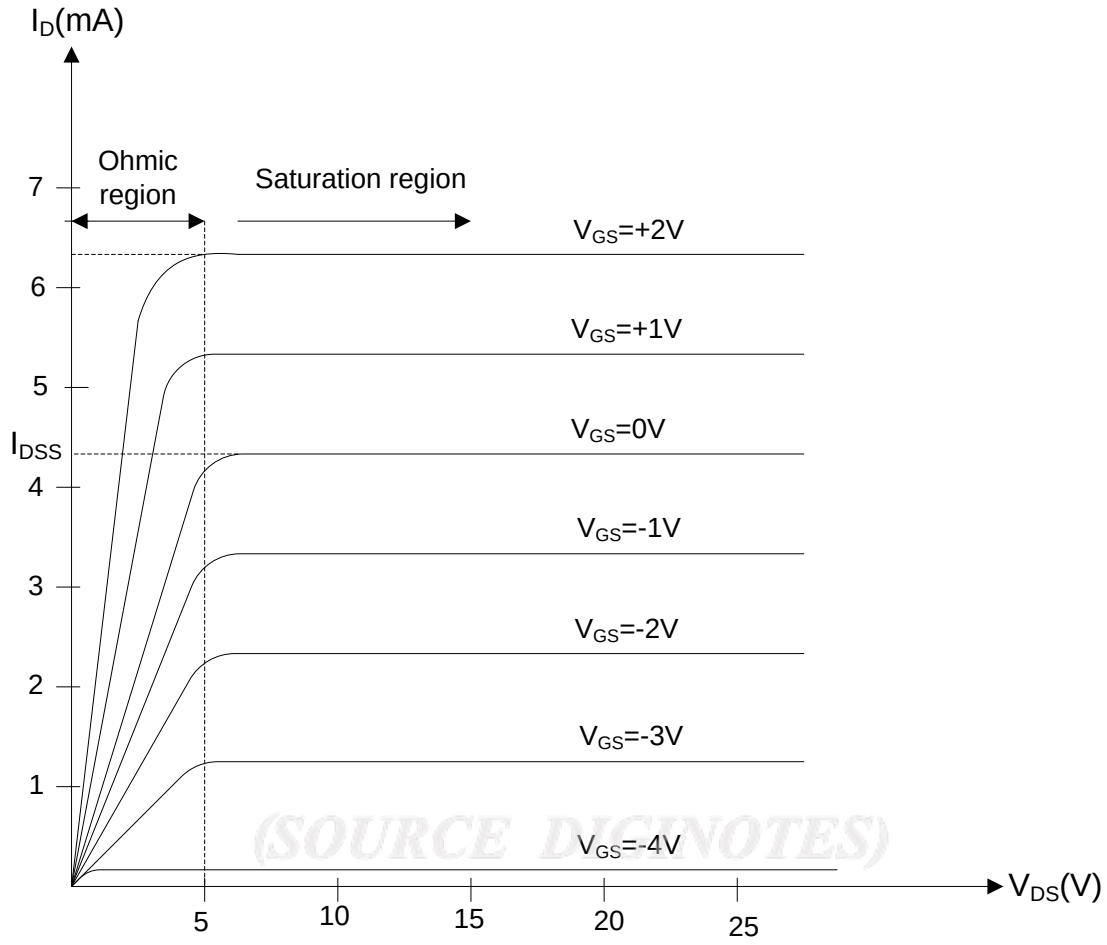
Principle of Operation:

When a positive voltage is applied between drain and source terminals ($+V_{DS}$), with gate shorted to the source ($V_{GS}=0$), then there is a flow of electrons towards drain terminal through N-channel as the electrons are attracted to the positive terminal at drain. This constitute Drain Current (I_D). The value of I_D increases with increase of V_{DS} up to a certain value of V_{DS}. After that value of V_{DS}, the I_D remain constant and this value is referred as I_{DSS} (Drain Current with Drain shorted with the source).

For positive gate to source voltage, the electrons (minority carrier) in the P-Substrate are attracted towards the gate terminal and concentration of electrons at the N-channel increases. As a result, the drain current increases. As the application of positive drain to source voltage

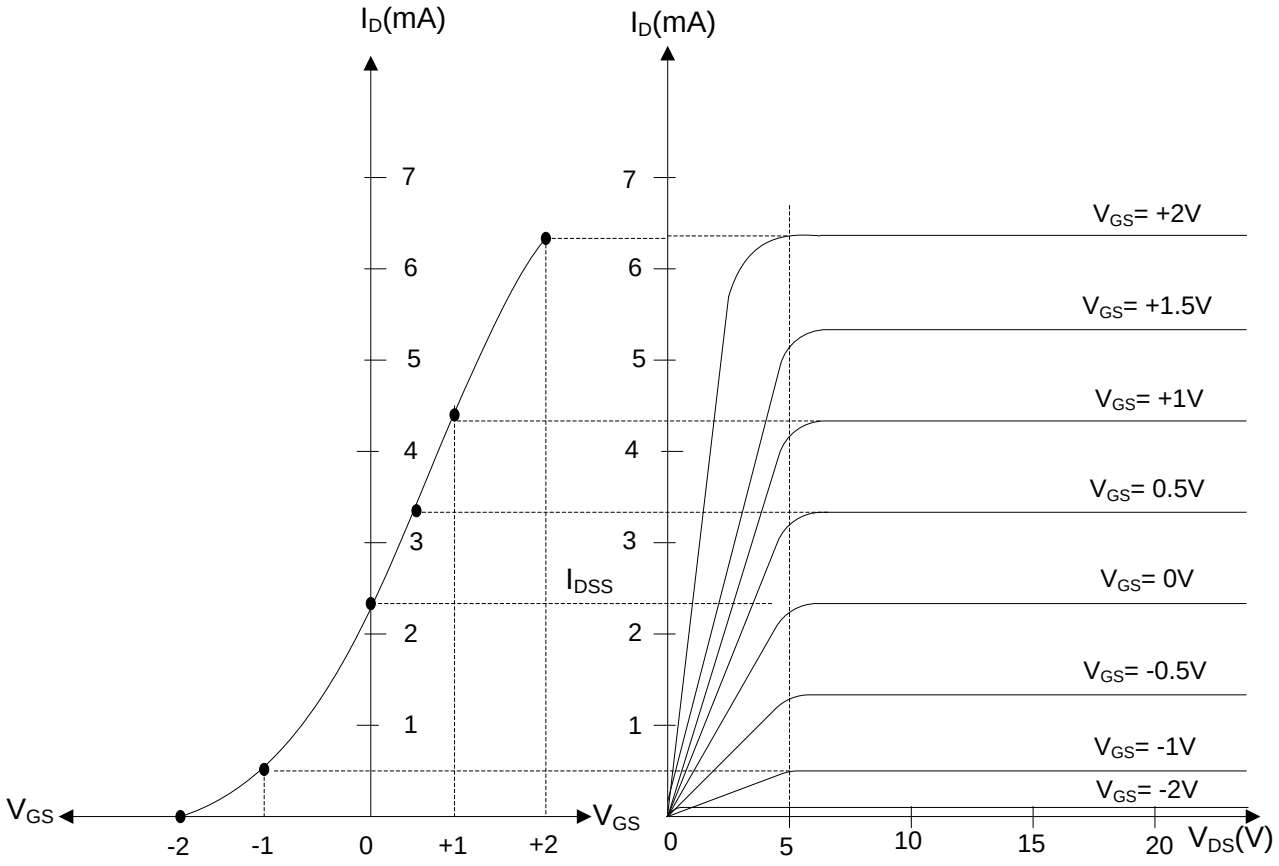
increases the drain current, the region of positive gate-source voltage is referred to as the enhancement region.
For negative gate to source voltage, the electrons in the N-channel are repelled towards the P-substrate and the concentration of electrons at the N-channel decreases. As a result, the drain current decreases. As the application of negative drain to source voltage decreases the drain current, the region of negative gate-source voltage is referred to as the depletion region. Therefore, gate to source voltage is used to control the gate current.

Q.4 Explain the characteristics of N-channel DE-MOSFET.
Answer: Output Characteristics of N-channel DE-MOSFET



The output characteristic of the N-Channel DE-MOSFET is shown in the above diagram. Drain Current (I_D) is plotted against Drain-Source voltage (V_{DS}) keeping the Gate-Source (V_{GS}) voltage constant. As shown in the diagram, at lower value of Drain-Source voltage (V_{DS}), the Drain Current (I_D) is proportional Drain-Source voltage(V_{DS}) and it follows the Ohm's law. This region is referred as Ohmic region. As Drain-Source voltage (V_{DS}) increases further, at a certain value Drain Current (I_D) does not increase and this region as shown in the diagram is referred as Saturation region.

Transfer Characteristics of N-channel DE-MOSFET



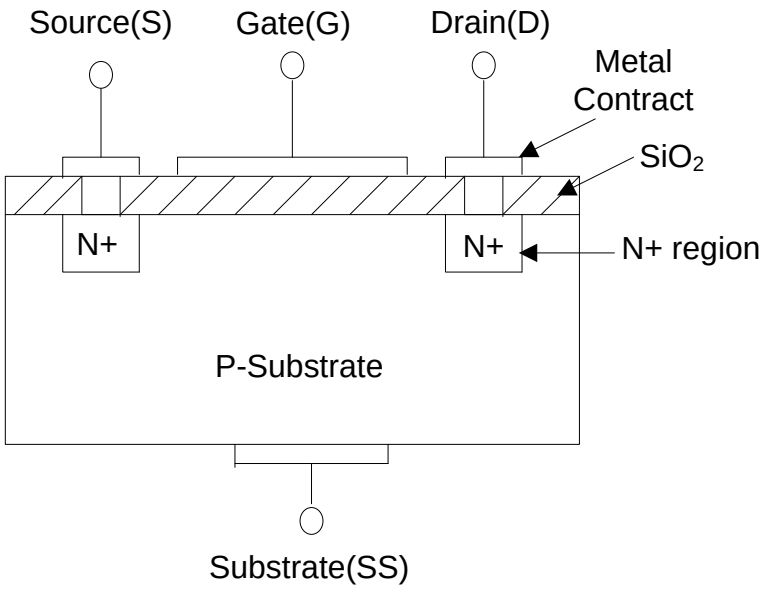
The transfer characteristic of the N-Channel DE-MOSFET is shown in the above diagram. Drain Current (I_D) is plotted against Gate-Source voltage (V_{GS}) keeping the Drain-Source (V_{DS}) voltage constant.

Q5.Explain the construction and principle of operation of N-Channel and P-Channel Enhacement Metal Oxide Semiconductor Field Effect Transistor (E-MOSFET).

Answer: N-Channel Enhancement Metal Oxide Semiconductor Field Effect Transistor (E-MOSFET)

Construction:

Cross Section of an N-Channel E-MOSFET



The above figure shows the construction of E-MOSFET. It consists of a P-type substrate. The source and the drain terminals are formed by connecting metal contacts to the two N+ regions. The gate terminal is connected to the insulating silicon dioxide (SiO_2) layer . There is no direct connection between the gate terminal and the semiconductor.

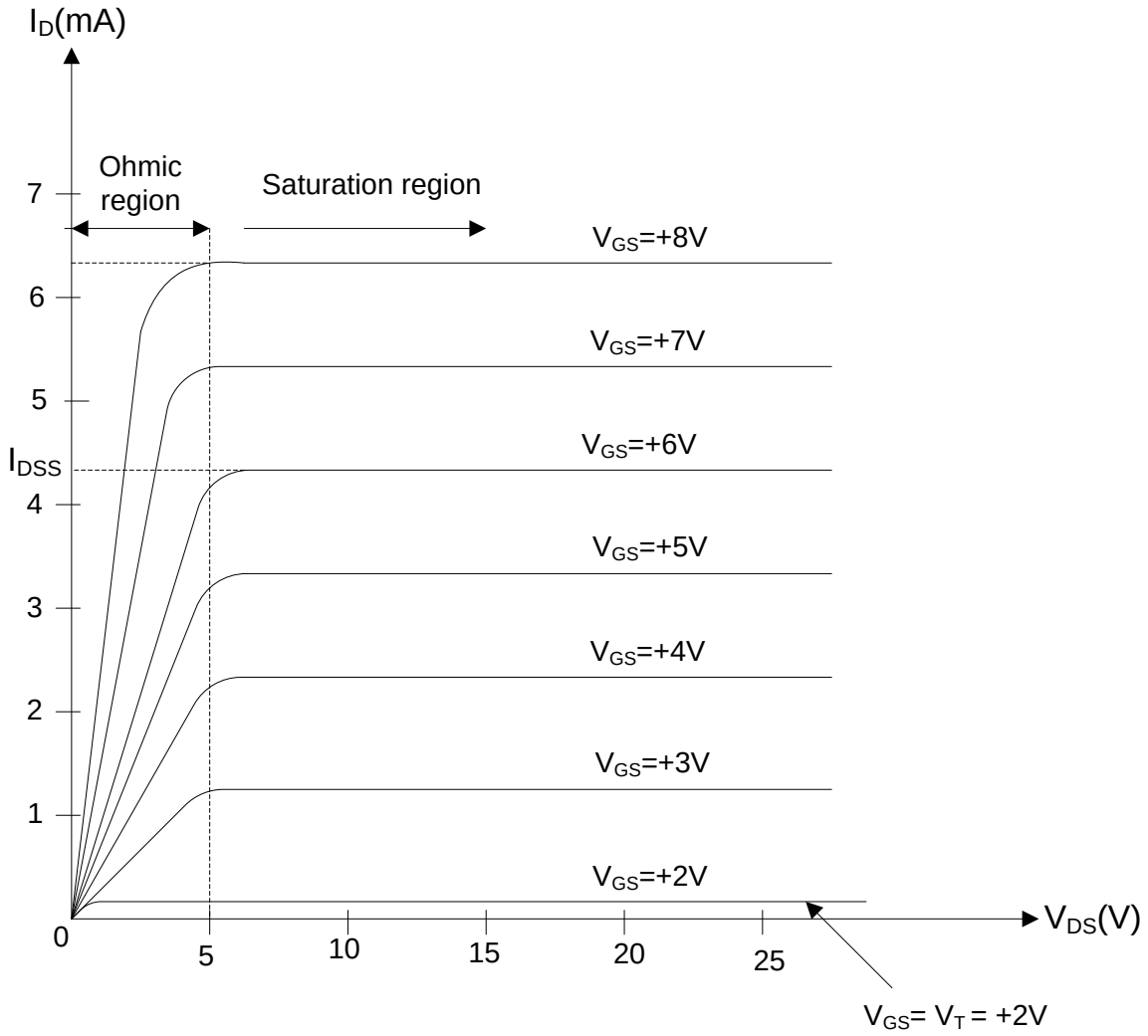
Principle of Operation:

When a positive voltage is applied between drain and source terminals ($+V_{DS}$), with gate shorted to the source (V_{GS}=0), then there is no flow of electrons towards drain terminal as N-channel is absent.

For positive gate to source voltage, the electrons (minority carrier) in the P-Substrate are attracted towards the gate terminal and concentration of electrons between the two N+ region increases. As a result, the drain current starts only when sufficient gate to source is applied. The minimum gate to source voltage required for the significant starting drain current is referred as threshold voltage (V_T).

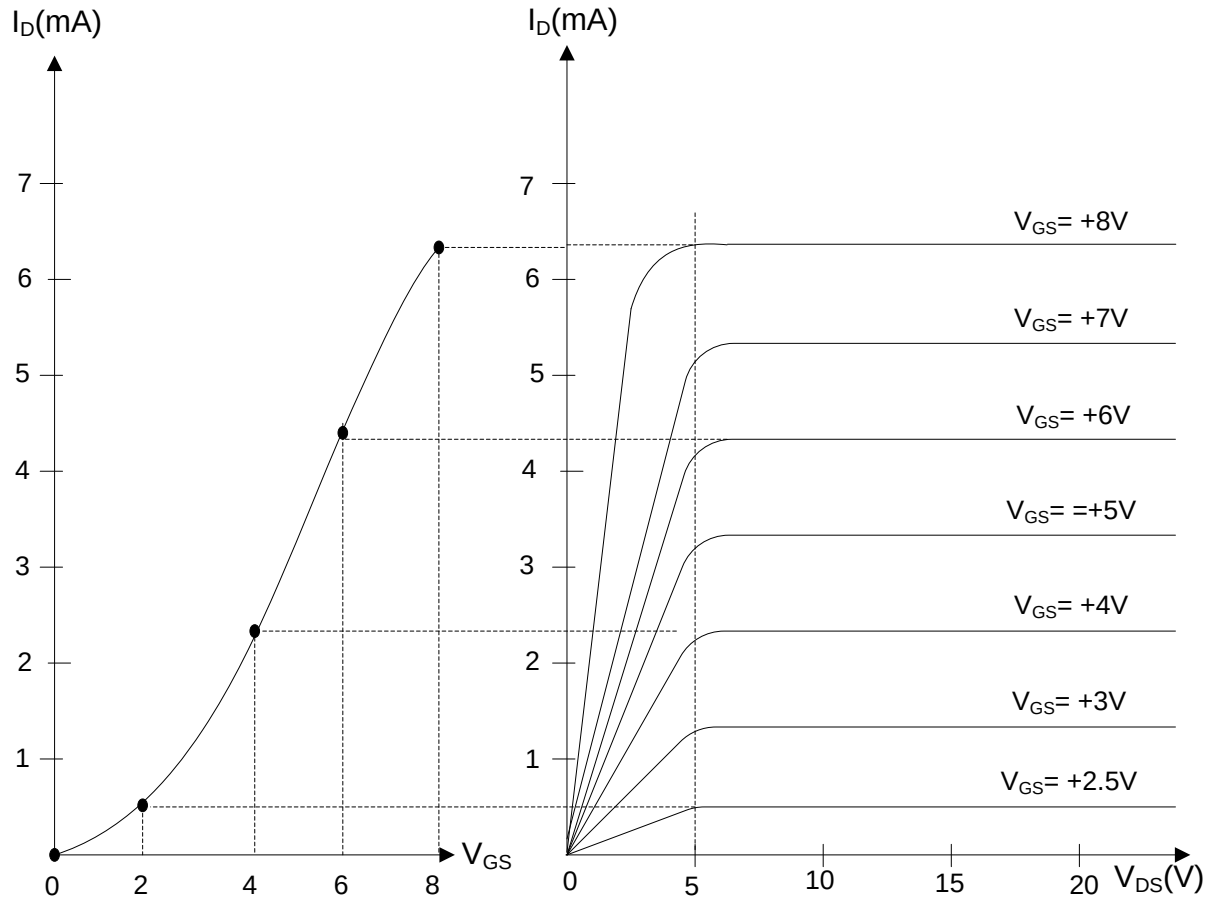
Q.6 Explain the characteristics of N-channel E-MOSFET.

Answer: Output Characteristics of N-channel E-MOSFET



The output characteristic of the N-Channel E-MOSFET is shown in the above diagram. Drain Current (I_D) is plotted against Drain-Source voltage (V_{DS}) keeping the Gate-Source (V_{GS}) voltage constant. As shown in the diagram, at lower value of Drain-Source voltage (V_{DS}), the Drain Current (I_D) is proportional Drain-Source voltage(V_{DS}) and it follows the Ohm's law. This region is referred as Ohmic region. As Drain-Source voltage (V_{DS}) increases further, at a certain value Drain Current (I_D) does not increase and this region as shown in the diagram is referred as Saturation region.

Transfer Characteristics of N-channel E-MOSFET

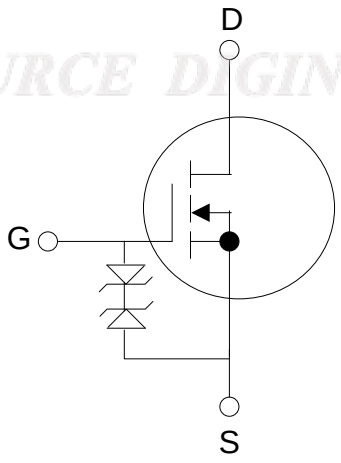


The transfer characteristic of the N-Channel E-MOSFET is shown in the above diagram. Drain Current (I_D) is plotted against Gate-Source voltage (V_{GS}) keeping the Drain-Source (V_{DS}) voltage constant.

Q7.Mention the difference between JFET and MOSFET,
Answer:

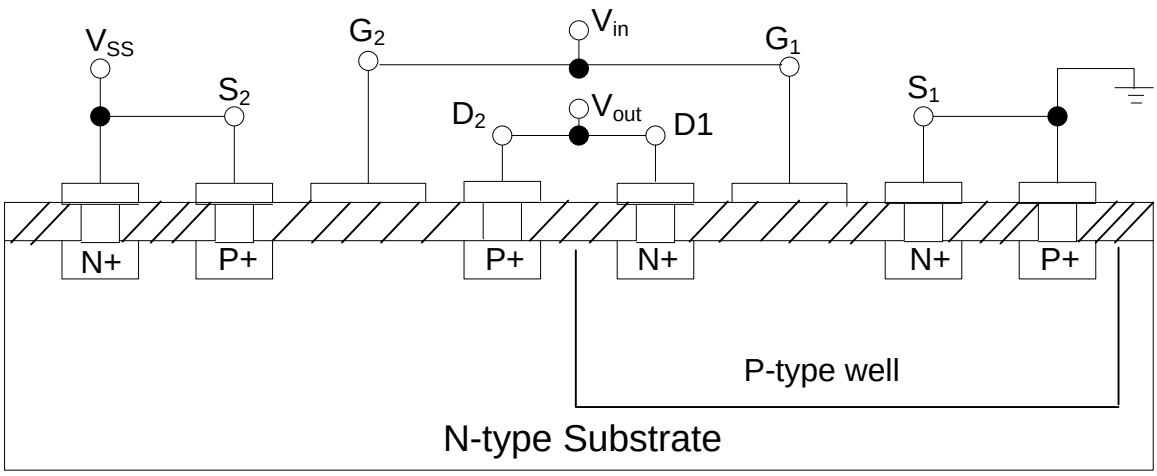
JFET	MOSFET
1. JFETs are operated in depletion mode only.	1.DE-MOSFET can be operated in both depletion and enhancement mode and E-MOSFET are operated in enhancement mode only.
2. Input resistance of JFET is around $10^9\Omega$.	2. Input resistance of MOSFET is much higher than JFET. Input resistance of MOSFET is around $10^{13}\Omega$.
3. Drain resistance of JFET is much higher than MOSFET. Drain resistance of JFET is in the range of 100 KΩ to 1MΩ.	3. Drain resistance of MOSFET is in the range of 1 KΩ to 50 KΩ
4. Leakage gate current for JFET is much higher than MOSFET. Leakage gate current for JFET is in the range of 100 μA to 100nA.	4. Leakage gate current for MOSFET is smaller than JFET. Leakage gate current for MOSFET is in the range of 100nA to 10 pA.
5. Construction of JFETs are more difficult than MOSFET and JFET are less widely used than MOSFET.	Construction of MOSFET are easier than JFET and MOSFET are widely used than JFET.

Q8. Discuss about the handling of MOSFET.
Answer: Due to the presence of thin Silicon dioxide (SiO_2) layer in MOSFET, they are easily get damaged if not properly handled.
A person accumulates static charge from surrounding. When that person handles a MOSFET, that charge may create a potential difference across the SiO_2 layer and that potential difference may breakdown the insulation of SiO_2 layer.
An effective method to prevent MOSFET from damage is to connect Zener diodes back to back between the gate and the source terminal as shown in the figure below. Connecingt Zener diodes back to back between the gate and the source terminal prevent the rise potential difference across Silicon dioxide(SiO_2) layer to a specified maximum limit.



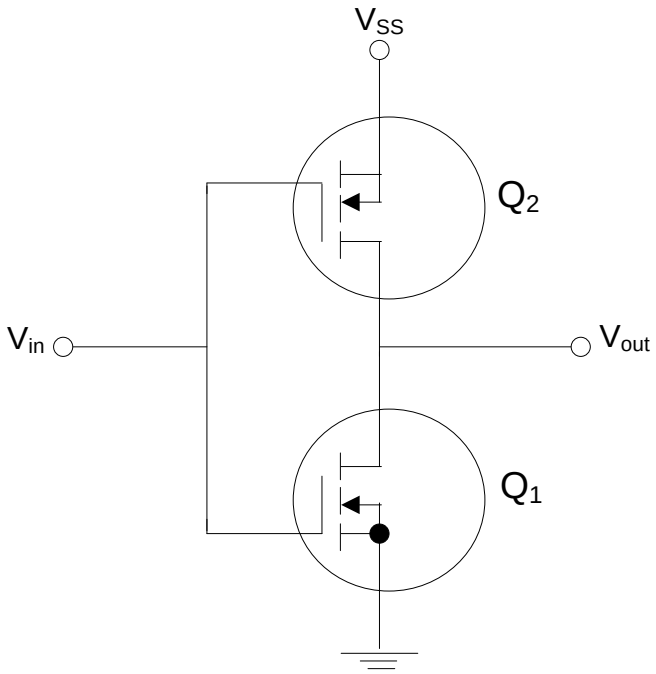
Q9. Discuss the application of Field Effect Transistors (FET).
Answer: Applications Field Effect Transistors (FET) are mentioned below:
(i) Amplifiers: FET devices are commonly used as low-noise amplifiers and as buffer amplifiers.
(ii) Analog Switch: FETs are used as analog switches.
(iii) Multiplexer: FET devices are used in multiplexer circuits where each FET device acts as a single-pole single-throw switch.
(iv) Current Limiters: FETs can be used as current limiter in an electronic circuit.
(v) Voltage-variable resistors: FETs when operated in the ohmic region, acts as voltage- variable resistor.
(vi) Oscillators: FETs are used in phase shift oscillators.

Q.10 Explain the working of CMOS inverter device.
Answer: Construction of CMOS Inverter



Complementary metal oxide semiconductor (CMOS) is those in which both P–type and N-type E-MOSFETs are diffused onto the same chip. The above figure shows the basic CMOS Inverter.

CMOS Inverter Circuit Diagram

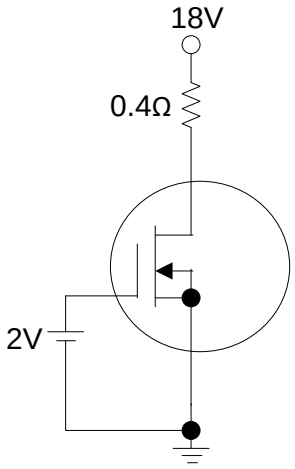


The basic inverter circuit using CMOS is shown above. Inverter is a logic circuit that inverts the applied input signal. The complementary N-type and P-type E-MOSFETs are connected in series with their gate terminals tied together to form input terminal. The drain terminals are connected together to form output terminal.

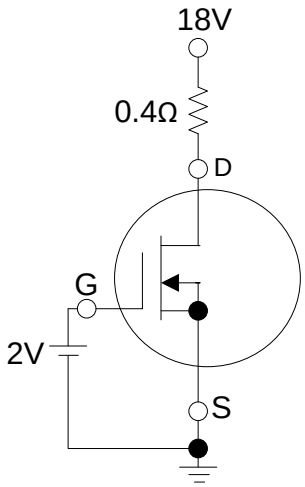
When the input voltage V_{in} is at logic LOW, the gate-source voltage of Q_2 (P-channel E-MOSFET) is $-V_{SS}$ which makes Q_2 in ON state resulting low resistance path between V_{SS} and V_{out} . The gate-source voltage for Q_1(N-channel E-MOSFET) is zero which makes Q_1 is in OFF state resulting very high resistance between output terminal and ground. As a result the output voltage is equal to V_{SS} , that is, V_{out} is HIGH.

When the input voltage V_{in} is at logic HIGH, the gate-source voltage of Q_2 (P-channel E-MOSFET) is zero which makes Q_2 in OFF state resulting high resistance path between V_{SS} and V_{out} . The gate-source voltage for Q_1(N-channel E-MOSFET) is HIGH which makes Q_1 is in ON state resulting low resistance between output terminal and ground. As a result the output voltage ,V_{out} is HIGH.

Q11. Figure below shows a biasing configuration using DE-MOSFET. Given that the saturation drain current is 8mA and the pinch-off voltage is -2V, determine the value of gate-source voltage, drain current and the drain-source voltage.



Answer: The figure below shows the circuit along with terminals.



From the above figure, Gate-source voltage (V_{GS}) is 2V.

We know, in a DE-MOSFET, $I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$

Here, given that I_{DSS}=8mA and V_P=-2V

Hence, $I_D = 8\times10^{-3}\times\left(1-\frac{2}{-2}\right)^2 = 32\times10^{-3} = 32\text{mA}$

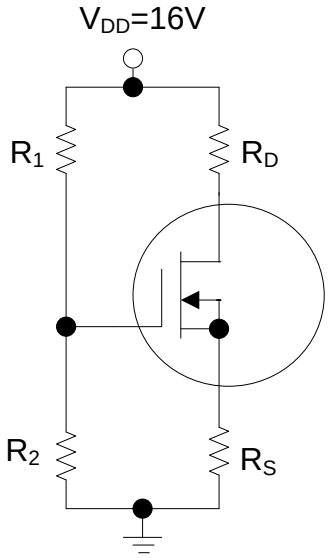
Now, applying Kirchhoff's voltage law to output section, we have

$18 - 0.4\times10^{3}\times32\times10^{-3} - V_{DS} = 0$

$\Rightarrow V_{DS} = 5.2\text{V}$

Therefore, Gate-source voltage=2V, Drain current=32mA and Drain-source voltage=5.2V

Q12. Design a voltage-divider–bias network using a DE-MOSFET with the supply voltage V_{DD}=16V, I_{DSS}=10mA and V_P = -5V to have a quiescent drain current of 5mA and gate voltage of 4V. (Assume the drain resistor R_D to be four times the source resistor R_S).
Answer: The following is a voltage divider bias network using DE-MOSFET.



Given V_{DD}=16V, Gate Voltage (V_G)=4V, Drain current (I_D)=5mA, I_{DSS}=10mA and V_P = -5V
As the quiescent drain current (I_D) is less than the saturation drain current (I_{DSS}), the MOSFET is operated in the depletion mode.
We know, in a DE-MOSFET,

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \Rightarrow 5\times10^{-3} = 10\times10^{-3}\times[1+\frac{V_{GS}}{5}]^2 \Rightarrow [1+\frac{V_{GS}}{5}]^2 = 0.5$$

$$\Rightarrow 1+\frac{V_{GS}}{5} = \pm\sqrt{0.5} \Rightarrow 1+\frac{V_{GS}}{5} = 0.7 \text{ (Only +ve is considered, otherwise } V_{GS} \text{ will be large negative)}$$

$$\Rightarrow V_{GS} = -1.5V$$

The gate-source voltage,

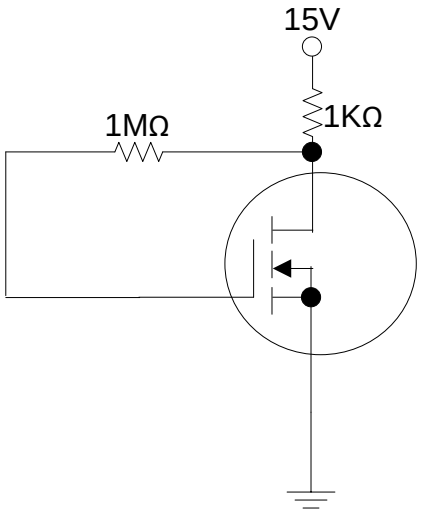
$$V_{GS} = V_G - V_S \Rightarrow V_{GS} = V_G - I_D R_S \Rightarrow -1.5 = 4 - 5\times10^{-3}\times R_S \Rightarrow R_S = 1.1K\Omega$$

$$R_D = 4\times R_S \text{ (Given)} \Rightarrow R_D = 4.4K\Omega$$

Assume $R_2 = 1K\Omega$

$$\text{Again, } V_G = \frac{R_2}{R_1+R_2}\times V_{DD} \Rightarrow 4 = \frac{1000}{R_1+1000}\times16 \Rightarrow R_1 = 3000\Omega = 3K\Omega$$

Q13. Figure below shows a circuit using E-MOSFET. Given that the threshold voltage for the MOSFET is 2V and $I_{D\,(on)}$ =6mA for $V_{GS\,(on)}$ =5V, determine the value of the operating point.



Answer: Drain current(I_D) in an E-MOSFET is given by

$I_D = K(V_{GS} - V_T)^2 \Rightarrow 6\times10^{-3} = K(5-2)^2 \Rightarrow K = \frac{2}{3}\times10^{-3}\ A/V^2$

$V_{GS} = V_{DD} - I_D R_D \Rightarrow V_{GS} = 15 - I_D \times 1\times10^3 \Rightarrow V_{GS} = 15 - 1000I_D$

Now, $I_D = K(V_{GS} - V_T)^2 \Rightarrow I_D = \frac{2}{3}\times10^{-3}(15 - 1000I_D - 2)^2 \Rightarrow 1500I_D = (13 - 1000I_D)^2$

$\Rightarrow 1500I_D = 169 - 26000I_D + 10^6 I_D$

$\Rightarrow 10^6 I_D - 27500I_D + 169 = 0$

$\Rightarrow I_D = \frac{27500 \pm \sqrt{(27500)^2 - 4\times10^6 \times 169}}{2\times10^6}$

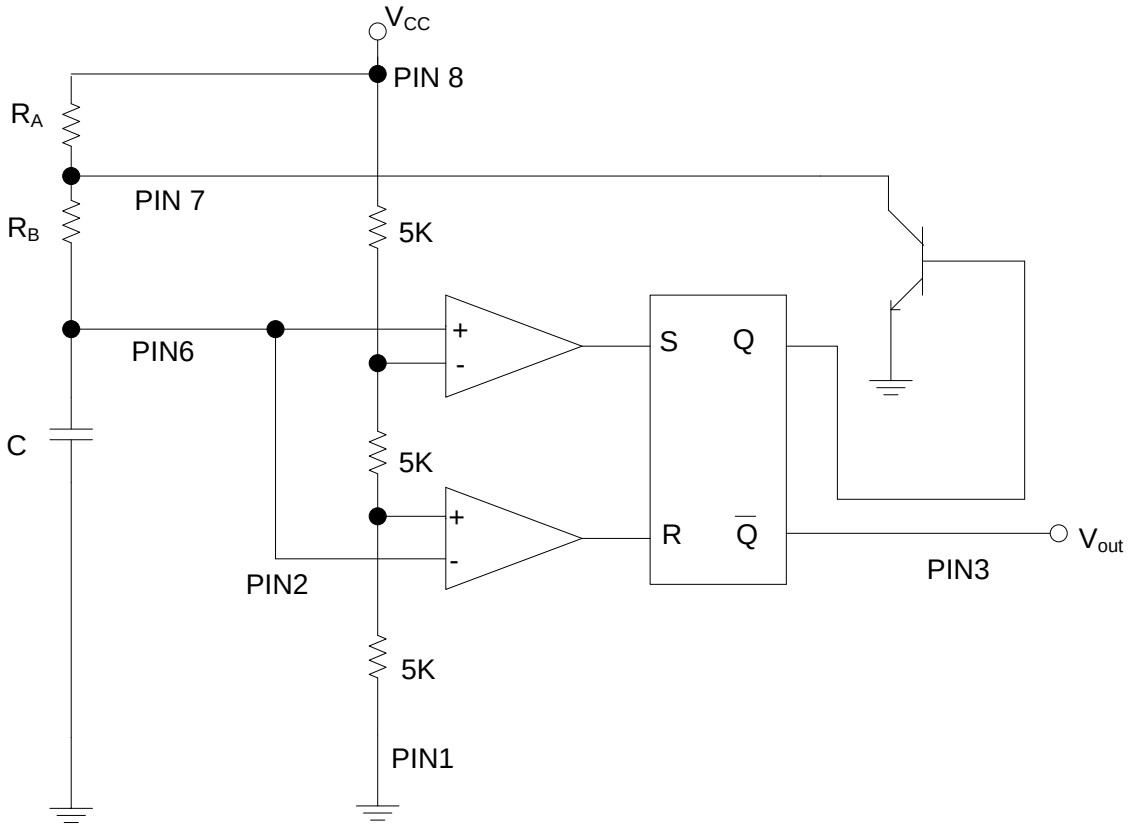
$\Rightarrow I_D = \frac{27500 \pm \sqrt{80250000}}{2\times10^6} = \frac{27500 \pm 8958.24}{2\times10^6} = 9.27\text{mA or } 18.23\text{mA}$

For $I_D = 9.27\text{mA}$, $V_{GS} = 15 - 1000I_D = 15 - 1000\times9.27\times10^{-3} = 5.73\text{V}$ which is selected

For $I_D = 18.23\text{mA}$, $V_{GS} = 15 - 1000I_D = 15 - 1000\times18.23\times10^{-3} = -3.23\text{V}$ which is rejected since V_{GS} should be positive and more than threshold voltage for E-MOSFET

Therefore, the operating point is (9.27mA, 5.73V)

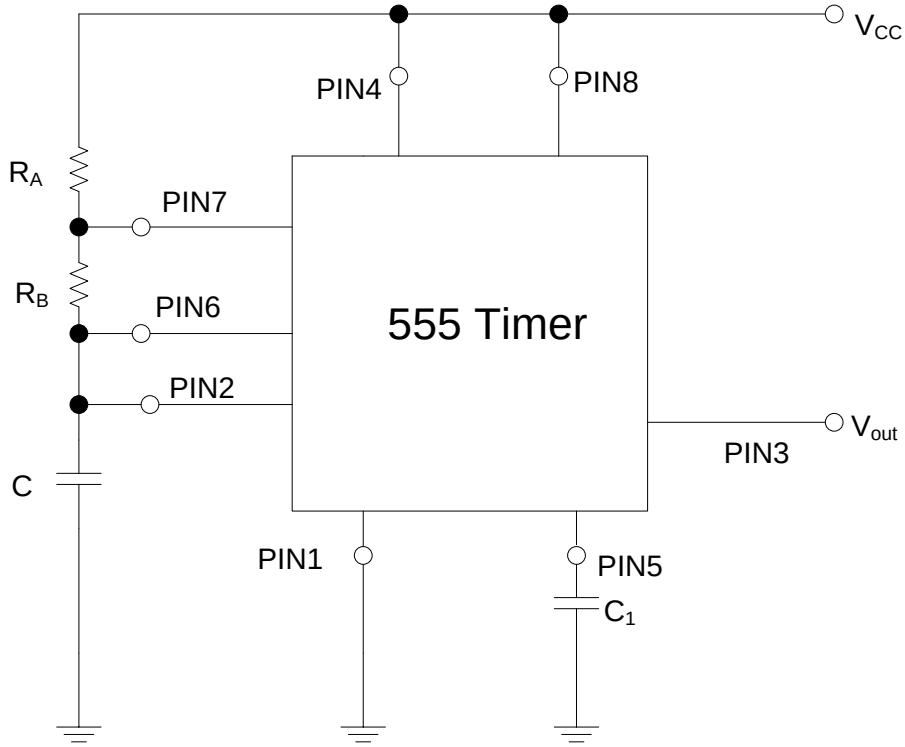
Q14. Explain the Astable Operation of multivibrator using 555 Timer IC.
Answer: The following figure shows the 555 Timer connected for astable operation.



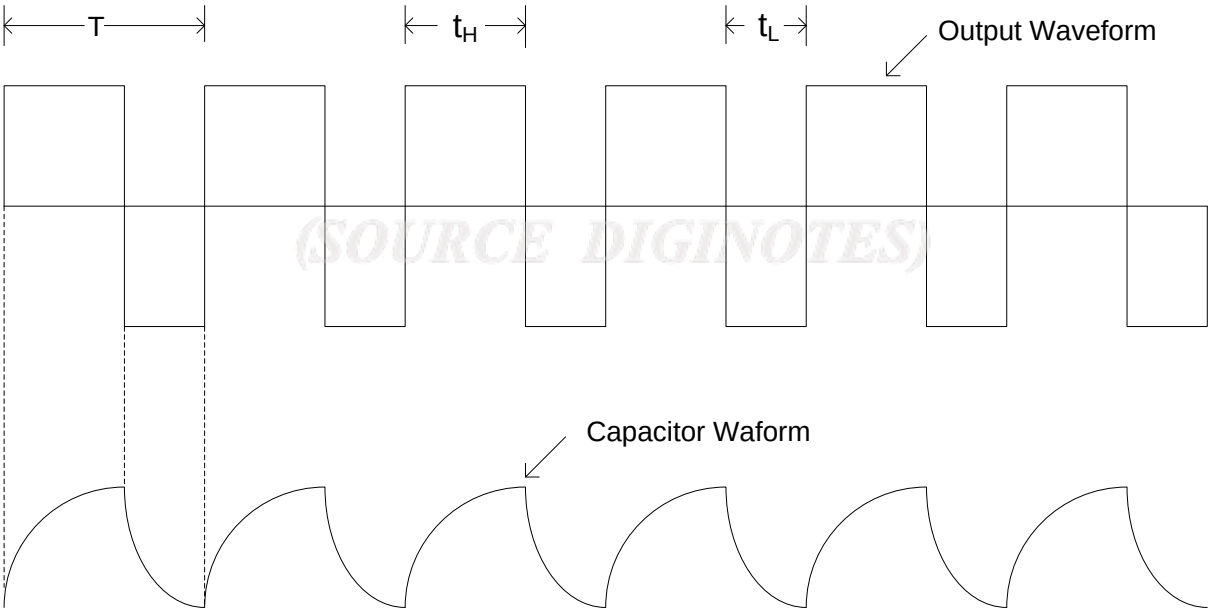
As shown in the figure, the 555 Timer contains a voltage divider, two comparators, an RS flip flop, and an npn transistor. Since the voltage divider has equal resistors, the top comparator has a trip point of $UTP=\frac{2V_{CC}}{3}$ and the lower comparator has a trip point of $LTP=\frac{V_{CC}}{3}$. The Pin 6 is connected to the upper comparator. The voltage on the pin 6 is called threshold voltage. Initially, the Q output of the RS flip-flop is LOW and V_{out} is HIGH. The transistor is in CUT OFF and there is no collector current through R_A. This makes the capacitor to start charging from V_{CC}. As the capacitor plate voltage starts rising and reaches $UTP=\frac{2V_{CC}}{3}$, trip occurs and the output of the upper comparator SET the RS flip-flop. At this point, Q the output of RS flip is HIGH and V_{out} is LOW. This forces the transistor in saturation and saturated current flows through the collector resistor R_A and the capacitor stop charging. The capacitor start discharge through R_B and the transistor. When the capacitor voltage falls and reaches $LTP=\frac{V_{CC}}{3}$, trip occurs and the output of the lower comparator RESET the RS flip-flop. At this point, Q the output of RS flip is LOW and V_{out} is HIGH.

This process repeats. V_{out} remains HIGH while capacitor charges and remains LOW while capacitor discharges.

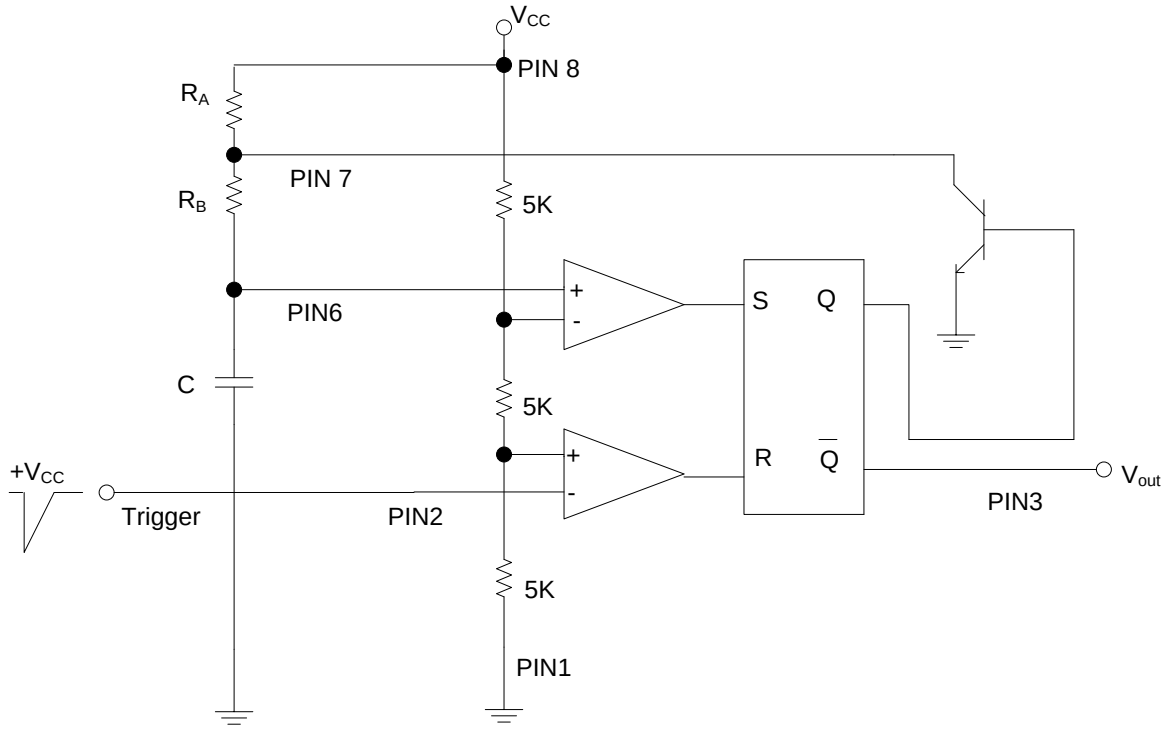
The following figure shows the block diagram of 555 Timer connected for astable operation.



The following figure shows output waveform and the capacitor waveform.

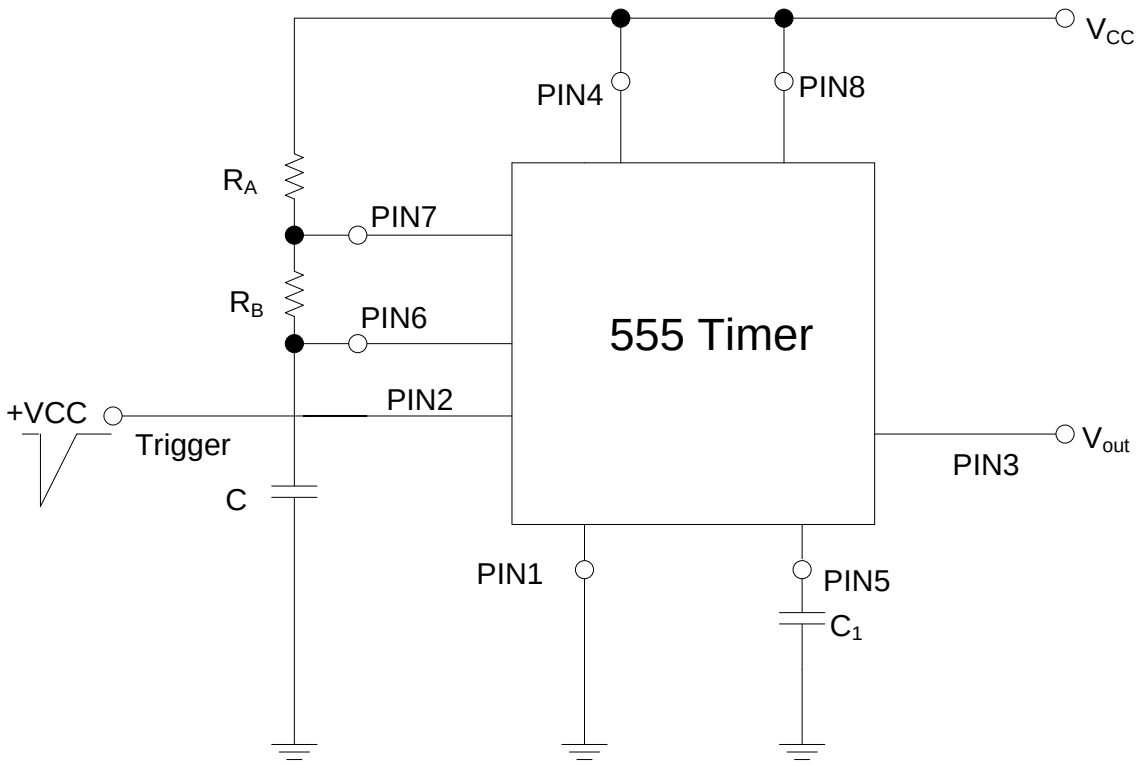


Q15. Explain the Monostable Operation of multivibrator using 555 Timer IC.
Answer: The following figure shows the 555 Timer connected for monostable operation.



As shown in the figure, the 555 Timer contains a voltage divider, two comparators, an RS flip flop, and an npn transistor. Since the voltage divider has equal resistors, the top comparator has a trip point of $UTP=\frac{2V_{CC}}{3}$ and the lower comparator has a trip point of $LTP=\frac{V_{CC}}{3}$.
Initially, the Q output of the RS flip-flop is HIGH and V_{out} is LOW. This saturates the transistor and capacitor is at ground. This circuit remains in this stage until a trigger arrives.
When the trigger input falls less than $V_{CC}/3$, the lower comparator reset theflip-flop and the Q the output of the flip-flop changes to LOW, the transistor goes to cut off, allowing the capacitor to charge. At this point, V_{out} is HIGH. The capacitor charges and when the capacitor voltage reaches $2V_{CC}/3$, the upper comparator sets the flip-flop. The Q the output of the flip-flop changes to HIGH and turns on the transistor. The capacitor starts discharging through the transistor. At this point, V_{out} is LOW. Therefore, the V_{out} remains HIGH only for the period while capacitor charges after a trigger is made. V_{out} again comes back to LOW until another trigger is made.

The following figure shows the block diagram of 555 Timer connected for monostable operation.



Q16. Discuss the Ideal Opamp versus practical Opamp.

Answer: The following is the comparison between Ideal Opamp and Practical Opamp

Ideal Opamp	Practical Opamp
Internal Impedence is infinite	Input Impedance range 100KΩ to 1000MΩ
Output Impendence is zero	Output impedance range from 10Ω to 100Ω
Open loop differential voltage gain is infinite	Open loop gain is in the range of 10,000 to 100,000
Bandwidth is infinite	Bandwidth is limited.
DC input and output offset voltage is zero	Finite DC input and output offset voltage
Input differential voltage is zero	Finite differential voltage is finite

Q17. Discuss the performance parameters of operational amplifier.

Answer: The following are the performance parameters of operational amplifier:

(i) Bandwidth: Bandwidth of operational amplifier is the range frequencies it can amplify for a given amplifier gain.

(ii) Slew rate: It is defined as the rate of change of output voltage time. It gives the idea as to how well the opamp output follows a rapidly changing waveform at the input.

(iii) Open-Loop Gain: Open-loop gain is the ratio of single-ended output to the differential input.

(iv) Common Mode Rejection Ratio (CMRR): It is the ratio of the desired differential gain (A_d) to the undesired common mode gain(A_c). CMRR is a measure of the ability of the opamp to suppress common mode signal. The ratio of CMRR is usually expressed 20log (A_d/A_c)dB.

(v) Power Supply rejection Ratio (PSRR): PSRR is defined as the ratio of change in the power supply voltage to corresponding change output voltage. PSRR is also defined as the ratio of change in one of the power supply voltage to the change in the input offset voltage with the other power supply voltage held constant.

(vi) Input Impedance: Input Impedance is the impedance looking into the input terminals of the opamp and mostly expressed in terms of resistance only.

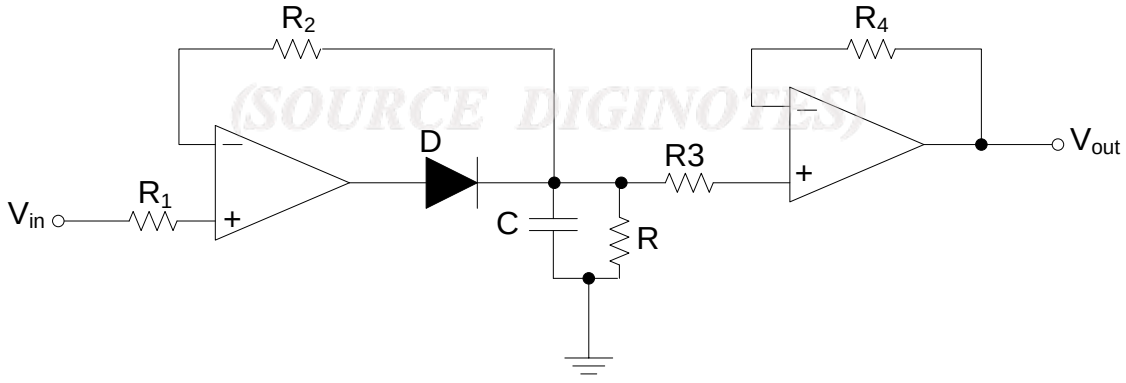
(vii) Output Impedance: Output Impedance is defined as the impedance between the output terminal of the opamp and the ground.

(viii) Settling Time: Settling Time is expressed as the time taken by the opamp output to settle within a specified percentage of the final value in response to a step input. It gives the response of the opamp to large step input.

(ix) Offset and Offset Drifts: An ideal opamp should produce a zero output for a zero differential input. But it is not so in the case of practical opamps. It is observed that a DC differential voltage is to be applied externally to get a zero output. This externally applied input is referred to as the input offset voltage. Output offset voltage is the voltage at the output with the both input terminals grounded. Input offset current is the difference between the two bias current flowing towards the inputs of the opamp. Input bias current defined as the average of the two bias currents flowing into the two input terminals of the opamp.

Q18. Explain the Peak Detector Circuit.

Answer: The following is the circuit diagram for a Peak Detector Circuit:



Peak detector circuit produces a voltage at the output equal to peak amplitude of the input signal. During the positive half cycle, the diode D is forward biased. The capacitor charges rapidly to

the peak from the output of the opamp. As the input starts decreasing beyond the peak, the diode gets reversed biased, thus isolating the capacitor the capacitor from the output of the opamp. The capacitor can now discharge only through resistor (R) connected across it. The value of R is much large. The purpose of the resistor is to allow a discharge path so that output can respond to changing amplitudes of the signal peak. The buffer circuit connected ahead of the capacitor prevents any discharge of the capacitor. The capacitor voltage, that is, the peak of the input is the output voltage.

Q19. Explain the following comparators:

(a) Zero crossing detector

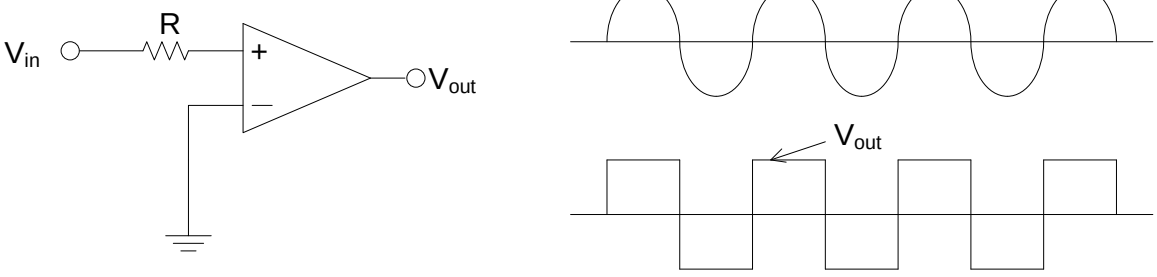
(b) Comparator with reference

(c) Comparator with hysteresis

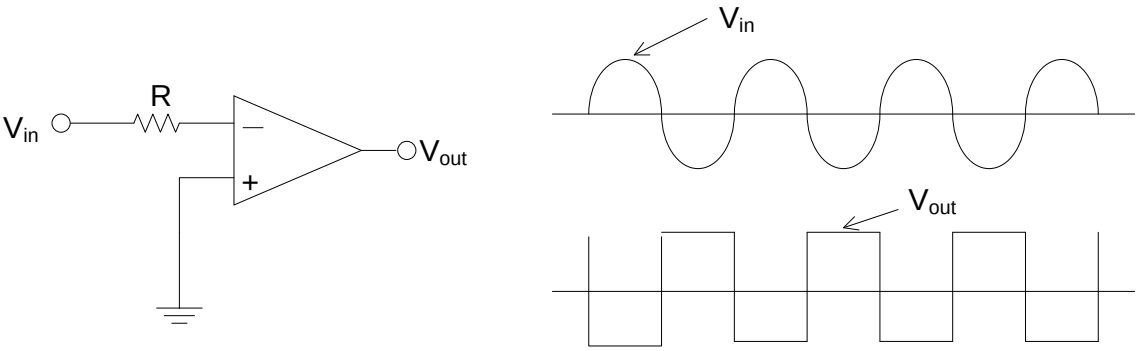
(d) Window comparator

Answer: (a) The following is the circuit diagram and waveform of the Zero crossing detector.

Non-Inverting zero crosing detector



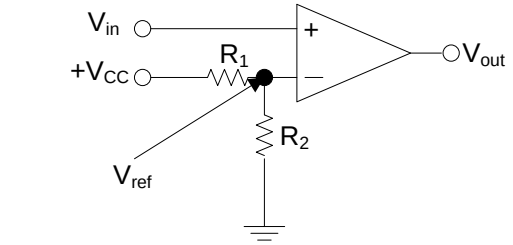
Inverting zero crosing detector



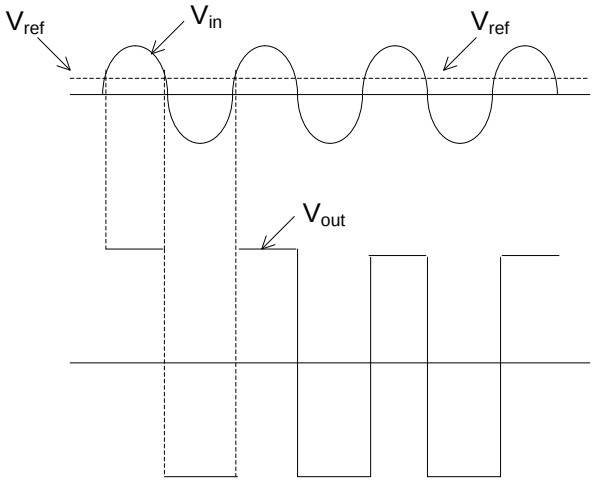
Non-Inverting Zero Crossing Detector: As shown in waveform, output (V_{out}) of the operational amplifier is $+V_{sat}$ during the positive half cycle. As the input wave crosses zero voltage, the output (V_{out}) changes from $+V_{sat}$ to $-V_{sat}$. That is, output (V_{out}) of the operational amplifier is $-V_{sat}$ during the negative half cycle.
Inverting Zero Crossing Detector: As shown in waveform, output (V_{out}) of the operational amplifier is $-V_{sat}$ during the positive half cycle. As the input wave crosses zero voltage, the output (V_{out}) changes from $-V_{sat}$ to $+V_{sat}$. That is, output (V_{out}) of the operational amplifier is $+V_{sat}$ during the negative half cycle.

(b) The following is the circuit diagram and waveform of the comparator with reference.

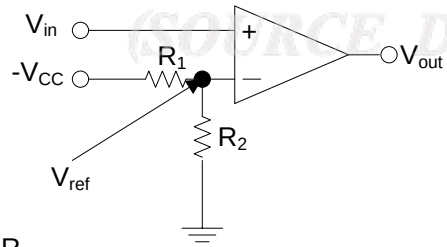
Non-Inverting comparator with positive reference



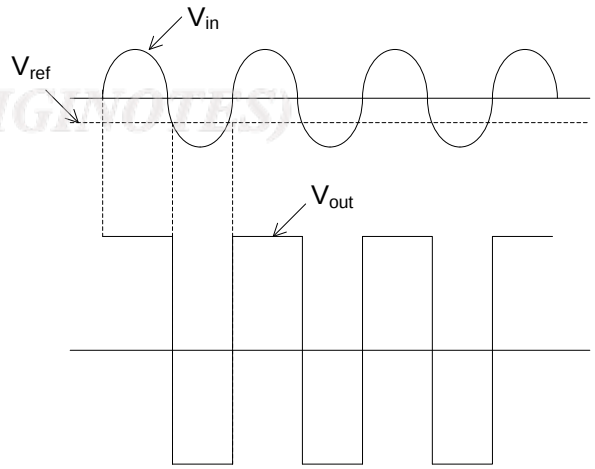
$$V_{ref} = + \frac{R_2}{R_1 + R_2} . V_{CC}$$



Non-Inverting comparator with negative reference



$$V_{ref} = - \frac{R_2}{R_1 + R_2} . V_{CC}$$



Non-inverting comparator with positive reference:

The potential at non-inverting terminal is $V_{ref} = +\frac{R_2}{R_1 + R_2}.V_{CC}$

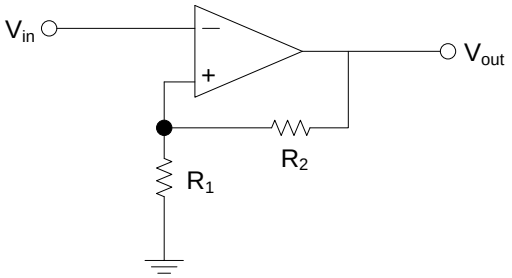
If $V_{in}>V_{ref}$, the output $V_{out}=+V_{sat}$ and If $V_{in}<V_{ref}$, the output $V_{out}=-V_{sat}$

Non-inverting comparator with negative reference:

The potential at non-inverting terminal is $V_{ref} = -\frac{R_2}{R_1 + R_2}.V_{CC}$

If $V_{in}>V_{ref}$, the output $V_{out}=+V_{sat}$ and If $V_{in}<V_{ref}$, the output $V_{out}=-V_{sat}$

(c) Following is the circuit diagram and waveform of comparator with hysteresis:

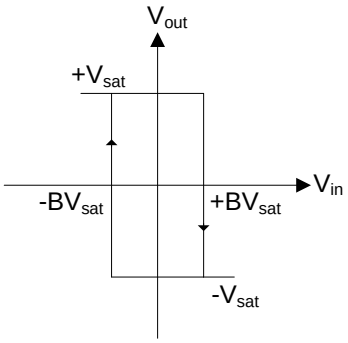


$B=\frac{R1}{R1+R2}$

$UTP=+BV_{sat}$

$LTP=-BV_{sat}$

$H=2BV_{sat}$

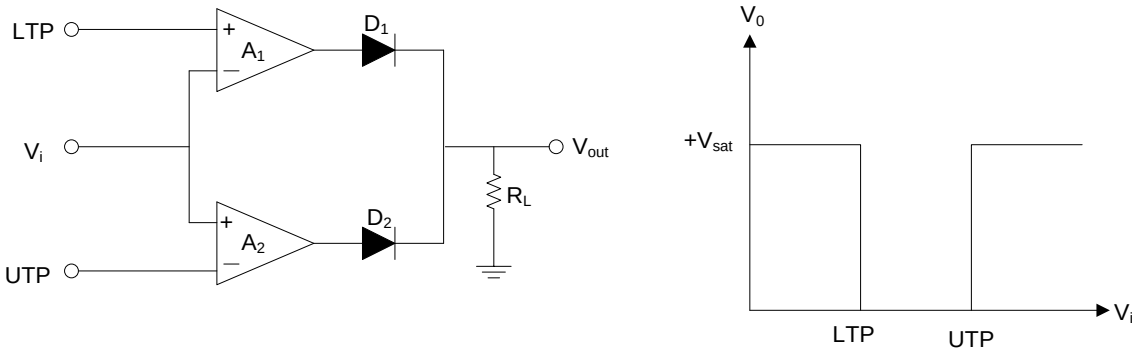


Let us assume $V_{out}=+V_{sat}$, then voltage at non-inverting terminal is $UTP=\frac{R_1}{R_1 + R_2}.V_{CC}$

When the input signal (V_{in}) exceeds this voltage, the output $V_{out}=-V_{sat}$ .Then then voltage at non-inverting terminal is $LTP=-\frac{R_1}{R_1 + R_2}.V_{CC}$

When the input signal (V_{in}) goes below this voltage, the output $V_{out}=+V_{sat}$ .Then then voltage at non-inverting terminal is $UTP=+\frac{R_1}{R_1 + R_2}.V_{CC}$ again

(d) Following is the circuit diagram and waveform for window comparator:



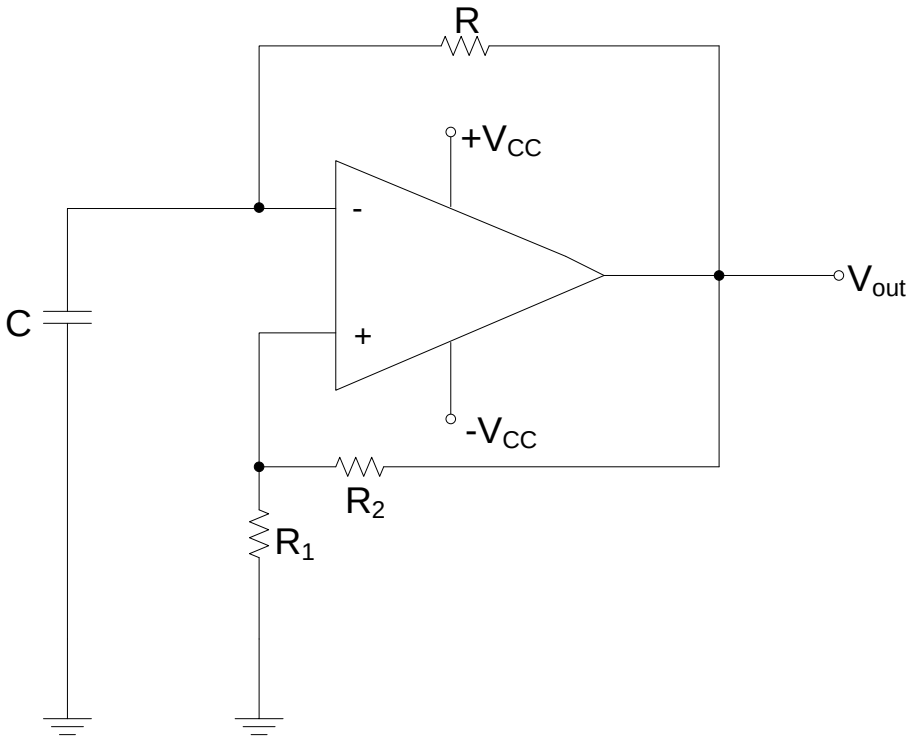
In a window comparator, there are two reference voltages called lower trip point (LTP) and upper trip point (UTP).

When the input voltage is less than the lower trip point (LTP), the output of the upper operational amplifier (A_1) is $+V_{sat}$ and the output of the lower operational amplifier (A_2) is $-V_{sat}$. Therefore, diode D_1 is forward biased and the diode D_2 is reversed biased. As a result, the output across R_L is $V_{out}=+V_{sat}$.

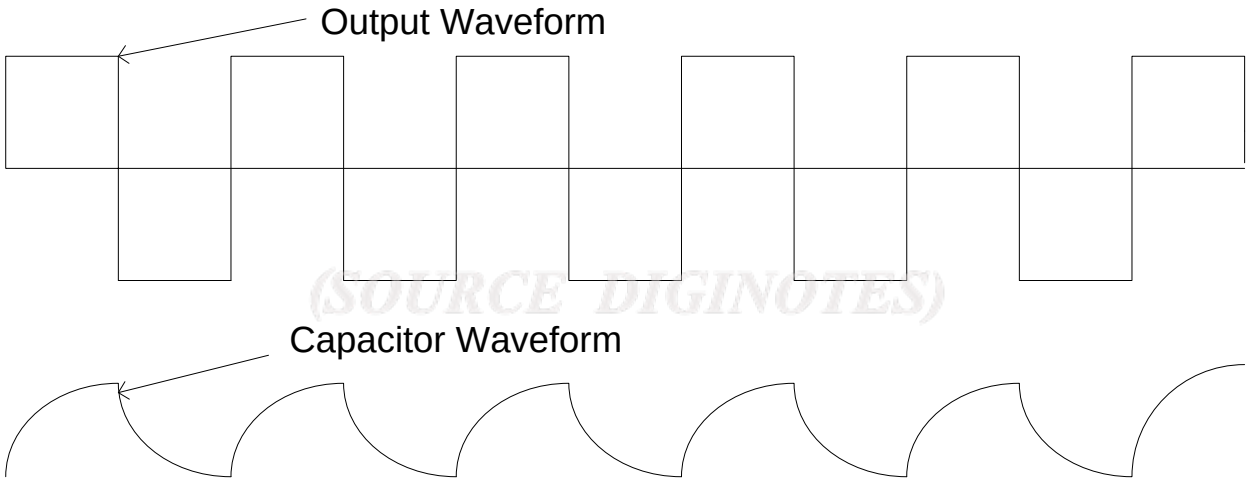
When the input voltage is greater than upper trip point (UTP), the output of the upper operational amplifier (A_1) is $-V_{sat}$ and the output of the lower operational amplifier (A_2) is $+V_{sat}$. Therefore, diode D_1 is reversed biased and the diode D_2 is forward biased. As a result, the output across R_L is $V_{out}=+V_{sat}$.

When the input voltage is greater than the lower trip point (LTP) and lower than upper trip point (UTP), output of both operational amplifiers (A_1 and A_2) is $-V_{sat}$. Therefore, both diode D_1 and the diode D_2 are reversed biased. As a result, the output across R_L is $V_{out}=0$.

Q20. Explain the Relaxation Oscillator using operational amplifier.
Answer: Following is the circuit diagram and wave form of the relaxation oscillator using operational amplifier.
Circuit diagram:



Waveform:



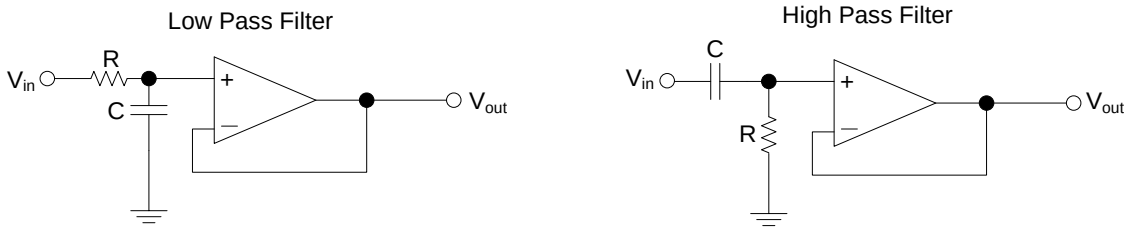
Relaxation oscillator is an oscillator circuit that produces an non-sinusoidal output. Time period of the oscillator is dependent on the charging time of a capacitor connected in the oscillator circuit.

Let us assume V_{out} =+V_{sat} , then voltage at non-inverting terminal is $\frac{R_1}{R_1+R_2}.V_{CC}$

At this point, the capacitor starts charging towards +V_{sat} through R and as the capacitor voltage reaches the voltage at non-inverting terminal, the output V_{out}=-V_{sat}. At the same time, the voltage at the non-inverting terminal changes to –(R_1/(R_1+R_2).V_{sat}. The capacitor starts discharging towards -V_{sat}. As voltage reaches –(R_1/(R_1+R_2).V_{sat} , the output is V_{out}=+V_{sat} and the cycle repeats.

The time period of the output wave form is $T=2RC\ln(\frac{1+B}{1-B})$ where $B=\frac{R_1}{R_1+R_2}$

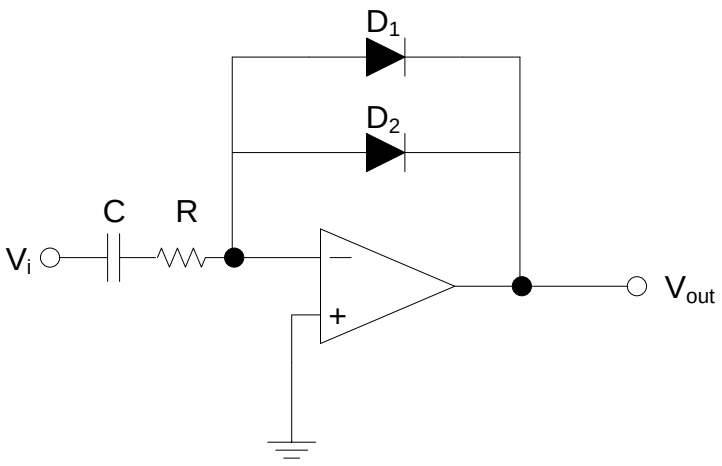
Q21. Explain the Active Filters.
Answer: Following are circuits diagram for Low Pass filter and High Pass filter;



Low Pass filter: At low frequencies, the reactance of the capacitor is much higher than the resistance of the R-C circuit and hence, the output voltage is nearly equal to the applied input voltage. The operational amplifier is acting as voltage follower.
High Pass filter: At high frequencies, the reactance of the capacitor is much lower than the resistance of the R-C circuit and hence, the output voltage is nearly equal to the applied input voltage. The operational amplifier is acting as voltage follower.

Q22. Explain the non-linear amplifier.

Answer: The following is the circuit diagram for non linear amplifier.



In a non-linear amplifier, the gain value is a non-linear function of the amplitude of the input signal. A simple method to achieve non-linear amplification is by connecting a non-linear device such as PN junction diode in the feedback path.

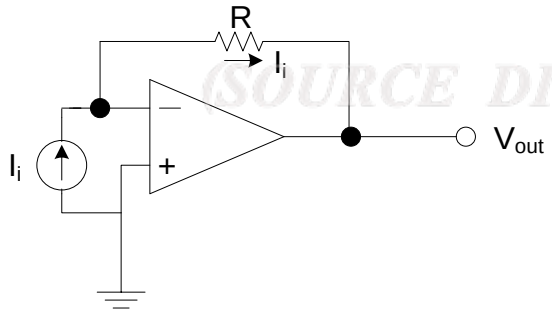
In the above circuit, the diodes act as open circuit and the gain is high due to minimum feedback when the value of the input signal is small. The diodes offer very small resistance and the gain is low when the value of the input signal is large. Such a circuit typically may cause the output voltage to change in the ratio of 2:1 for an input change of 1000:1. Resistance R_1 decides the compression ratio. Higher the value of R_1 , lesser the compression ratio.

A common application of such a non-linear amplifier is in AC bridge balance detectors.

Q23. Explain the current to voltage converter and the voltage to current converter.

Answer: Current to voltage converter:

Following is circuit diagram for current to voltage converter.



Current to voltage converter is transimpedance amplifier. An ideal transimpedance amplifier has zero input impedance and zero output impedance.

The circuit shown above is transimpedance amplifier having voltage shunt feedback with a feedback factor of unity.

$$V_0 = I_i \times R \times \left(\frac{A_{OL}}{1 + A_{OL}} \right)$$

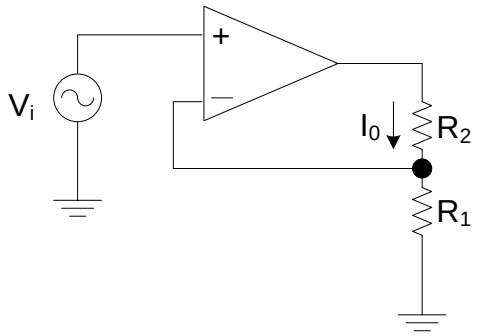
For, $A_{OL} >> 1,\ V_0 = I_i \times R$

The output voltage, $Z_{in} = \frac{R}{1 + A_{OL}}$

$Z_o = \frac{R_o}{1 + A_{OL}}$ where R_o is the output resistance of the opamp

Voltage to current converter:

Following is circuit diagram for voltage to current converter.



Voltage to current converter is transconductance amplifier. An ideal transconductance amplifier has infinite input impedance and infinite output impedance.

The circuit shown above is transconductance amplifier.

$I_0 = \frac{V_i}{R_1 + \frac{R_1 + R_2}{A_{OL}}}$, If $A_{OL} >> 1$ then $I_0 = \frac{V_i}{R_i}$

Closed loop input impedance is given by $Z_{in} = R_i \times \left(1 + A_{OL} \times \frac{R_1}{R_1 + R_2} \right)$

Closed loop output impedance is given by $Z_o = R_1 \times \left(1 + A_{OL} \times \frac{R_1}{R_1 + R_2} \right)$