Q1. What is Gate? State and prove De Morgan's theorems.

Answer: A digital circuit having one or more input signals but only one output signal is called a gate.

De Morgan's first theorem: The complement of a sum is equal to the product of the complements.

$\overline{A+B} = \overline{A}.\overline{B}$

Proof: We know from Boolean Algebra

$X + \overline{X} = 1,\ X.\overline{X} = 0,\ X + YZ = (X+Y)(X+Z)$

$Let\ P = A + B\ and\ Q = \overline{A}.\overline{B}$

$P + Q = (A+B) + (\overline{A}.\overline{B})$

$= (A + B + \overline{A})(A + B + \overline{B})\ [X + YZ = (X+Y)(X+Z)]$

$= (B+1)(A+1)$

$= 1.1 = 1$

$Therefore,\ Q = \overline{P} \Rightarrow \overline{A}.\overline{B} = \overline{A+B} \Rightarrow \overline{A+B} = \overline{A}.\overline{B}$

OR

$P.Q = (A+B).\overline{A}\overline{B} = A.\overline{A}.\overline{B} + B.\overline{A}.\overline{B} = 0 + 0 = 0$

$Therefore,\ Q = \overline{P} \Rightarrow \overline{A}.\overline{B} = \overline{A+B} \Rightarrow \overline{A+B} = \overline{A}.\overline{B}$

De Morgan's second theorem: The complement of a product is equal to the sum of the complements.

$\overline{A.B} = \overline{A} + \overline{B}$

Proof: We know from Boolean Algebra

$X + \overline{X} = 1,\ X.\overline{X} = 0,\ X + YZ = (X+Y)(X+Z)$

$Let\ P = AB\ and\ Q = \overline{A} + \overline{B}$

$P + Q = Q + P = (\overline{A} + \overline{B}) + AB = (\overline{A} + \overline{B} + A)(\overline{A} + \overline{B} + B) = (1 + \overline{B})(1 + \overline{A}) = 1.1 = 1$

$Therefore,\ Q = \overline{P} \Rightarrow \overline{A} + \overline{B} = \overline{AB} \Rightarrow \overline{AB} = \overline{A} + \overline{B}$

OR

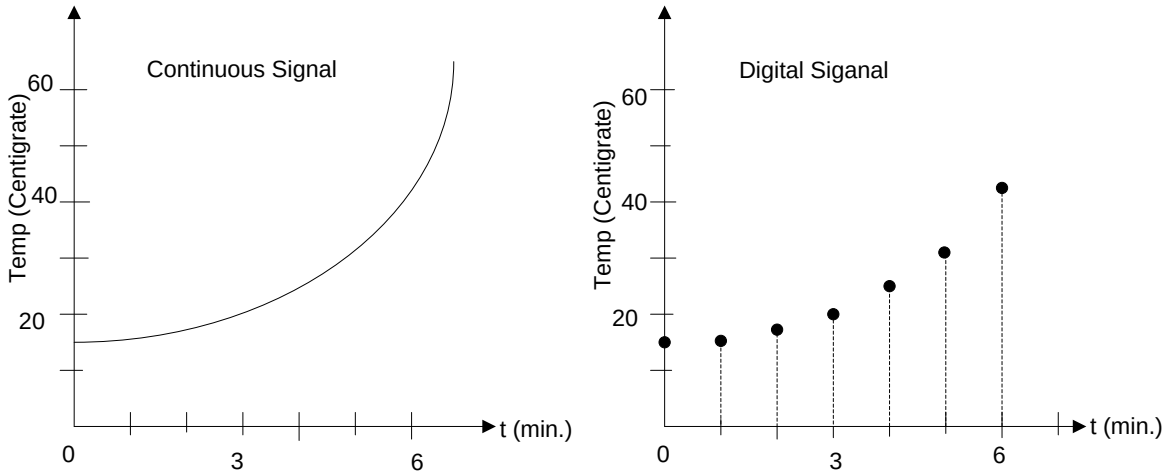
$P.Q = AB.(\overline{A} + \overline{B}) = AB.\overline{A} + AB.\overline{B} = 0 + 0 = 0$

$Therefore,\ Q = \overline{P} \Rightarrow \overline{A} + \overline{B} = \overline{AB} \Rightarrow \overline{AB} = \overline{A} + \overline{B}$

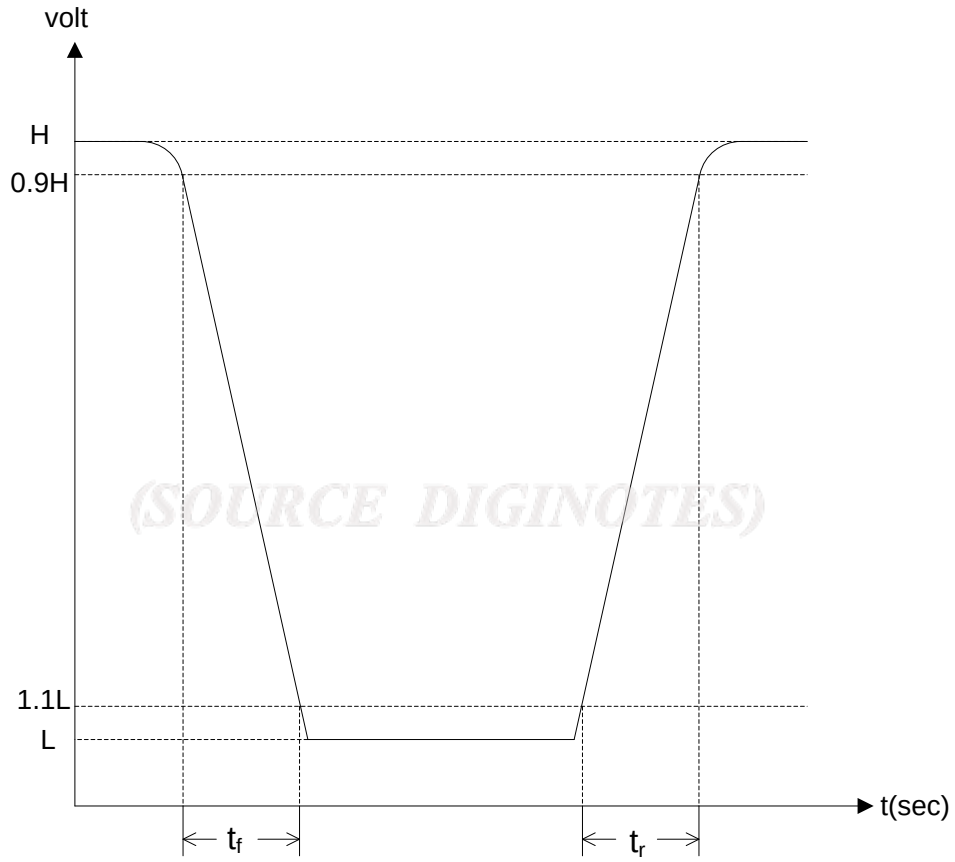
Q2. Differentiate analog and digital signals.

Answer: Analog signals are continuous and all possible values are considered. In the figure below, temperature is measured for water in a container which is heated for particular duration at all possible instant of time as a continuous signal.

Digital signal are only finite values at particular interval. In the figure below, temperature is measured for water in a container which is heated for particular duration at discrete interval of time as a digital signal.



Q3. Define (i) rise time (ii)fall time (iii)period (iv) frequency (v) duty cycle of a digital signal.
Answer: (i) Rise Time: It is defined as the time required for a signal to rise from its low level to its high level. Rise Time is measured as the time required between 1.1 L and 0.9H as shown in the figure. For example, suppose H=4V and L=2V, then 1.1L=2.2V and 0.9H=3.6V.
(ii) Fall Time: It is defined as the time required for a signal to fall from its high level to its low level. Fall Time measured is as the time required between 0.9H and 1.1L as shown in the figure. .

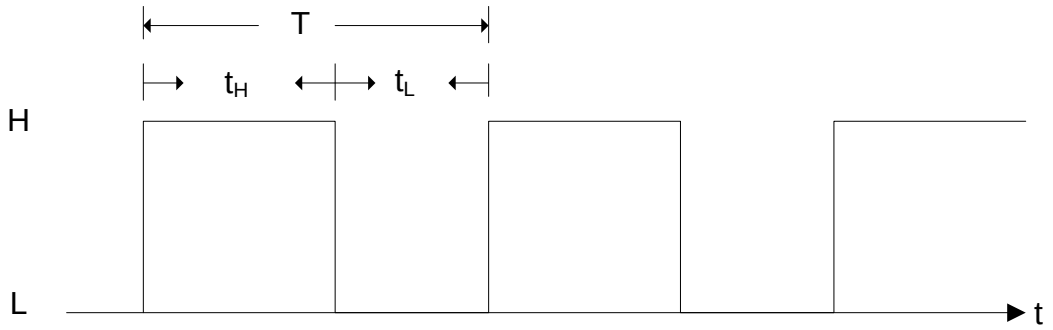


(iii) Period (T): Time required to complete one high and one low. As shown in the figure, t_H is the time required to complete one high and t_L is the time required to complete one low. $T=t_H+t_L$

(iv) Frequency (f): Frequency is the reciprocal of the time period. f=1/T

(v) Duty Cycle: Duty cycle H= $\frac{t_H}{T}$ and Duty cycle L= $\frac{t_L}{T}$

Duty cycle H is the ratio of time the signal is high to the time period. Duty cycle L is the ratio of time the signal is low to the time period.



Q4. (i) Prove that duty cycle of a symmetrical waveform is 50%. (ii) What is the value of high duty cycle (duty cycle H) if the frequency of a digital waveform is 5 MHz and the width of the positive pulse is 0.05 μs? (iii) An asymmetrical signal waveform is high for 2ms and low for 3ms. Find Frequency, Period , Duty cycle low, Duty cycle high

Answer: For a symmetrical waveform, High period is T/2 and the Low period is T/2 where T is the time period.

(i) Therefore, Duty Cycle H= $\frac{T/2}{T}\times 100\% = 50\%$ and Duty Cycle L= $\frac{T/2}{T}\times 100\% = 50\%$

(*ii*) $f = 5MHz$

$Perriod,\ T = \frac{1}{f} = \frac{1}{5\times 10^6} = 0.2\mu s$

$Width\ of\ \ the\ high\ pulse = 0.05\mu s$

$Duty\ cycle\ H = \frac{0.05}{0.2}\times 100\% = 25\%$

(*iii*) $t_H = Width\ of\ \ high\ signal = 2ms\ and\ t_L = Width\ of\ \ low\ signal = 3ms$

$Period, T = t_H + t_L = 2 + 3 = 5ms$

$Frequency,\ f = \frac{1}{T} = \frac{1}{5\times 10^{-3}} = 200Hz$

$Duty\ cycle\ low = \frac{t_L}{T} = \frac{3ms}{5ms}\times 100\% = 60\%$

$Duty\ cycle\ high = \frac{t_H}{T} = \frac{2ms}{5ms}\times 100\% = 40\%$

Q5. Describe positive logic and negative logic. List the equivalences in positive and negative logic.

Answer: If a binary 0 stands for low voltage and a binary 1 stands for high voltage, then this is called positive logic.

If a binary 1 stands for low voltage and a binary 0 stands for high voltage, then this is called negative logic.

Let us consider the table below as an example:

A	B	Y
LOW	LOW	LOW
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	HIGH

If we use positive logic, the above table is converter to:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

This is the truth table for OR Gate

If we negative logic, the same table is converted to:

A	B	Y
1	1	1
1	0	0
0	1	0
0	0	0

This is the truth table for AND Gate

Therefore, positive OR ↔ negative AND

Following are the equivalences in positive and negative logic:

Positive OR ↔ Negative AND

Positive AND ↔ Negative OR

Positive NOR ↔ Negative NAND

Positive NAND ↔ Negative NOR

Q6. Prove that (a) “Positive OR” logic is equal to “Negative AND” logic (b) “Positive AND” logic is equal to “Negative OR” logic (c) “Positive NOR” logic is equal to “Negative NAND” logic (d) “Positive NAND” logic is equal to “Negative NOR” logic

Answer: (a) Let us consider the table below:

A	B	Y
LOW	LOW	LOW
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	HIGH

If we use positive logic, the above table is converter to:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

This is the truth table for OR Gate

If we negative logic, the same table is converted to:

A	B	Y
1	1	1
1	0	0
0	1	0
0	0	0

This is the truth table for AND Gate

Therefore, “Positive OR” logic is equal to “Negative AND” logic:

(b) : (a) Let us consider the table below:

A	B	Y
LOW	LOW	LOW
LOW	HIGH	LOW
HIGH	LOW	LOW
HIGH	HIGH	HIGH

If we use positive logic, the above table is converter to:

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

This is the truth table for AND Gate

If we negative logic, the same table is converted to:

A	B	Y
1	1	1
1	0	1
0	1	1
0	0	0

This is the truth table for OR Gate

Therefore, “Positive AND” logic is equal to “Negative OR” logic

(c) (a) Let us consider the table below:

A	B	Y
LOW	LOW	HIGH
LOW	HIGH	LOW
HIGH	LOW	LOW
HIGH	HIGH	LOW

If we use positive logic, the above table is converter to:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

This is the truth table for NOR Gate

If we negative logic, the same table is converted to:

A	B	Y
1	1	0
1	0	1
0	1	1
0	0	1

This is the truth table for NAND Gate

Therefore, "Positive NOR" logic is equal to "Negative NAND"

(d)) Let us consider the table below:

A	B	Y
LOW	LOW	HIGH
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	LOW

If we use positive logic, the above table is converter to:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

This is the truth table for NAND Gate

If we negative logic, the same table is converted to:

A	B	Y
1	1	0
1	0	0
0	1	0
0	0	1

This is the truth table for NOR Gate

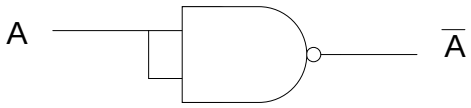
Therefore, "Positive NAND" logic is equal to "Negative NOR" logic

Q7. What is a universal gate? List the universal gates and prove their universalities.

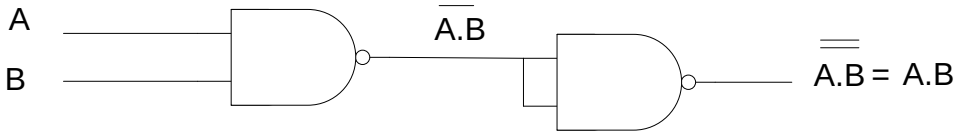
Answer: A universal gate is a gate that can be used to realize any other gate and therefore, a universal gate can be used to realize any Boolean function without using any other gate. Universal gates are NOR gate and NAND gate.

Proof of NAND gate as universal gate:
Any Boolean function can be implemented using NOT gate, AND gate and OR gate. Therefore, if NOT gate, AND gate and OR gate are implemented using NAND gate only, then it will be proved that NAND gate is a universal gate.

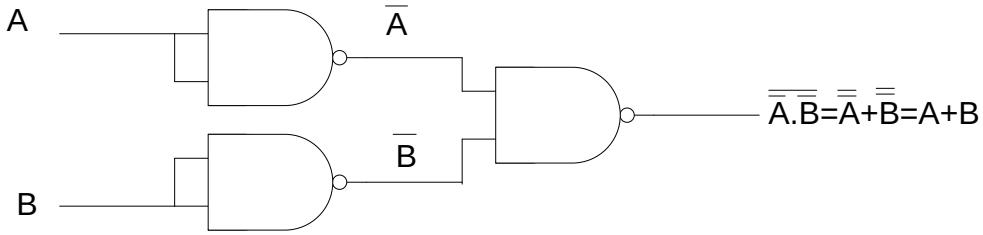
Implementing NOT using NAND gate



Implementing of AND gate using NAND gates



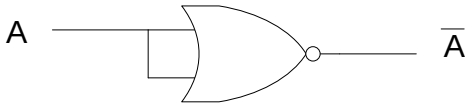
Implementing OR using NAND gate



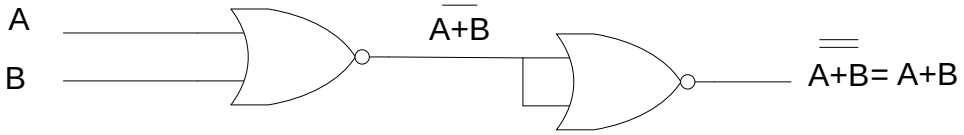
Proof of NOR gate as universal gate:

Any Boolean function can be implemented using NOT gate, AND gate and OR gate. Therefore, if NOT gate, AND gate and OR gate are implemented using NOR gate only, then it will be proved that NOR gate is a universal gate.

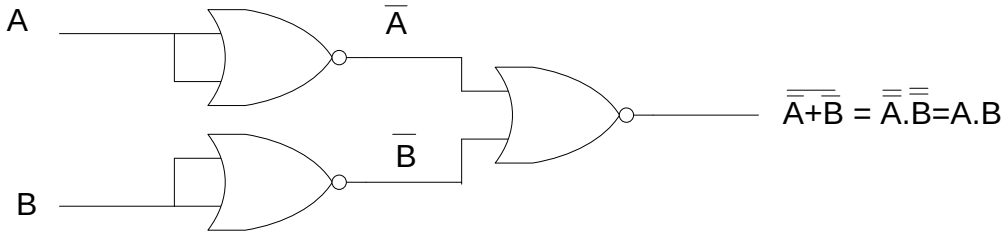
Implementing NOT using NOR gate



Implementing of OR gate using NOR gates

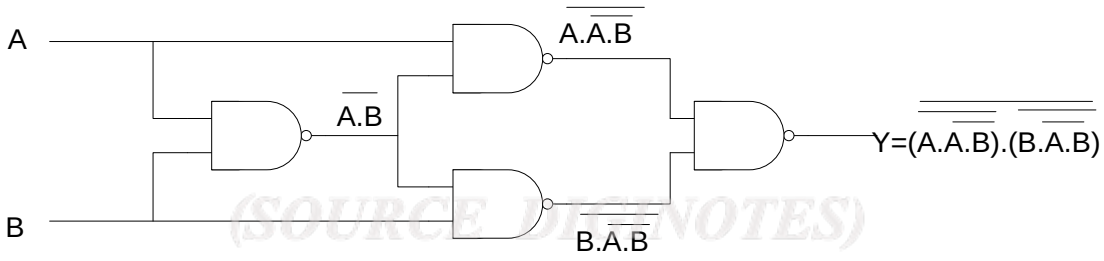


Implementing AND using NOR gates



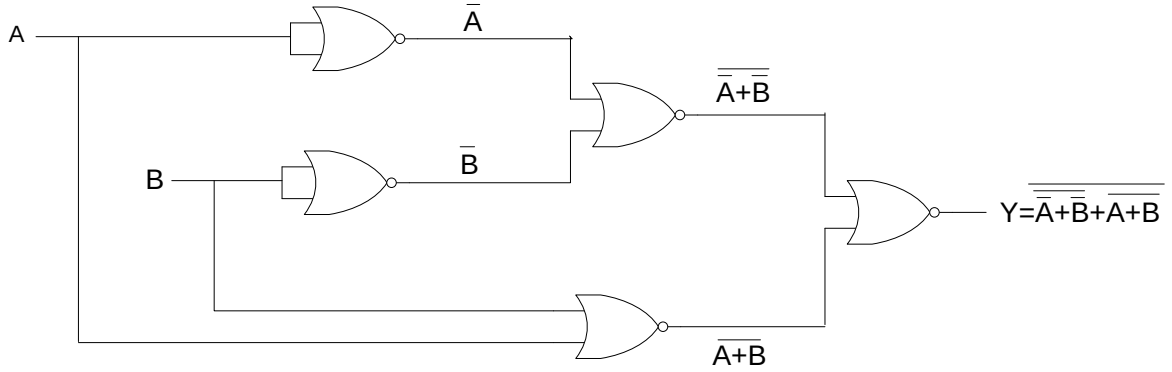
Q8. Realize the XOR gate using (i) NAND gate (ii) NOR gate.

Answer: (i) The following figure shows the realization of XOR gate with NAND gates:



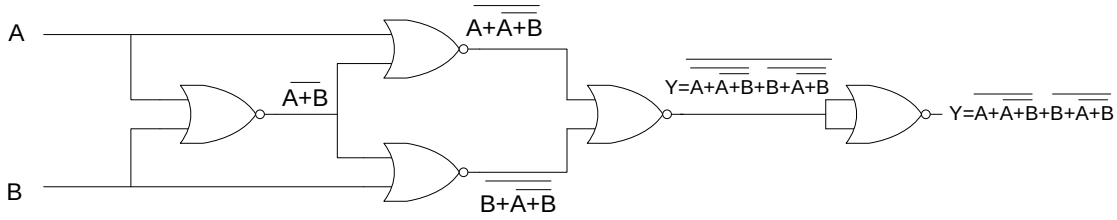
$$Y = \overline{\overline{(A.\overline{A.B})}.\overline{(B.\overline{A.B})}} = \overline{A.\overline{A.B}} + \overline{B.\overline{A.B}} = A.\overline{A.B} + B.\overline{A.B} = A.(\overline{A}+\overline{B}) + B.(\overline{A}+\overline{B}) = A.\overline{B} + \overline{A}.B = A \oplus B$$

(ii)The following figure shows the realization of XOR gate with NOR gates:



$$Y = \overline{\overline{\overline{A}+\overline{B}}+\overline{A+B}} = (\overline{\overline{\overline{A}+\overline{B}}}).(\overline{\overline{A+B}}) = (\overline{A}+\overline{B}).(A+B) = \overline{A}.A+\overline{A}.B+\overline{B}.A+\overline{B}.B = A.\overline{B}+\overline{A}.B = A\oplus B$$

Alternately,

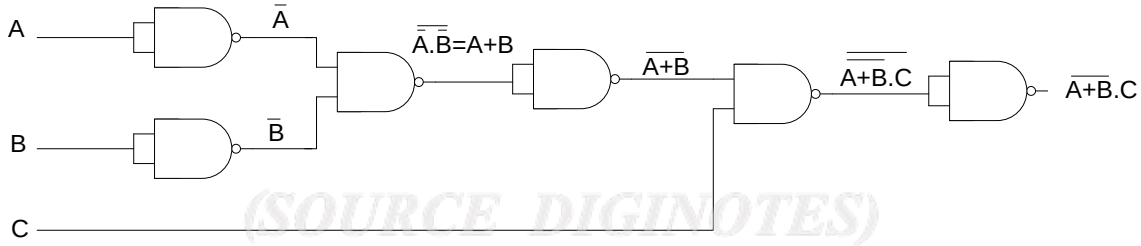


$$Y = \overline{A+\overline{A+B}}+\overline{B+\overline{A+B}} = \overline{A}.\overline{\overline{A+B}}+\overline{B}.\overline{\overline{A+B}} = \overline{A}.(A+B)+\overline{B}.(A+B) = \overline{A}.B+A.\overline{B} = A\oplus B$$

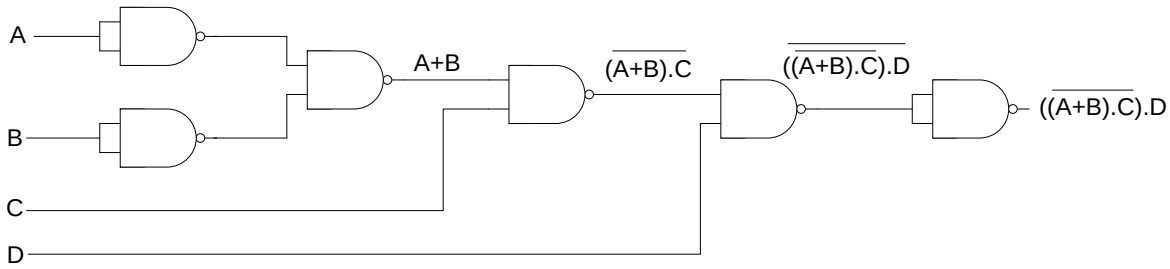
Q9. Implement the following functions using NAND gate only:

(i) $((\overline{A+B}).C)$ (ii) $Y=(\overline{(A+B).C}).D$ (iii) $\overline{((A+B).(\overline{A}+\overline{B}))}$

Answer: (i)

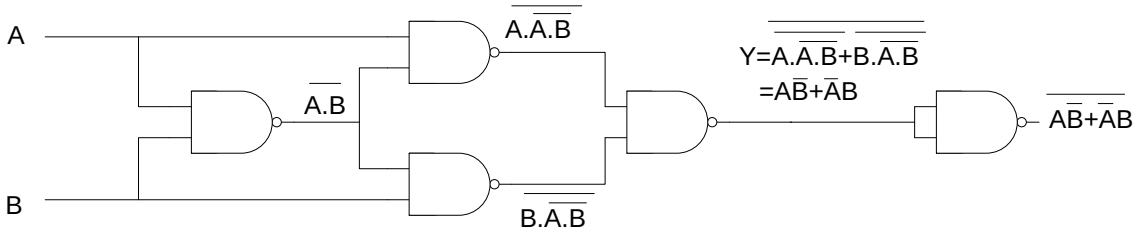


(ii)



(iii)

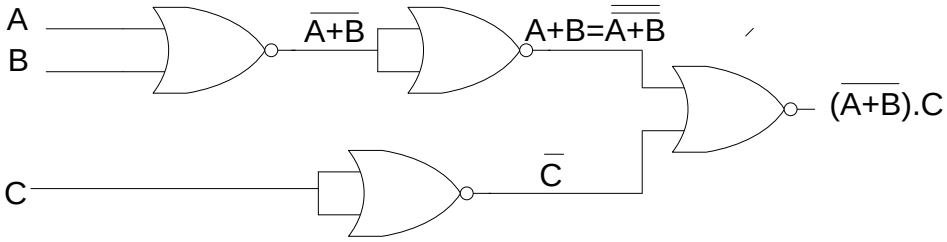
$$\overline{(A+B).(\overline{A}+\overline{B})} = \overline{A.\overline{B}+\overline{A}.B}$$



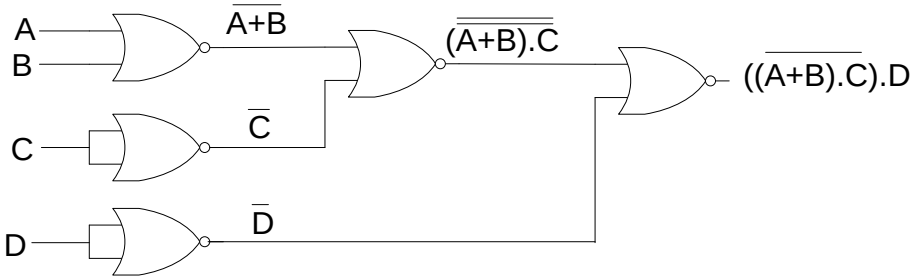
Q10. Implement the following functions using NOR gate only:

(i) $((\overline{A+B}).C)$ (ii) $Y=(\overline{(A+B).C}).D$ (iii) $\overline{((A+B).(\overline{A}+\overline{B}))}$

Answer: (i)

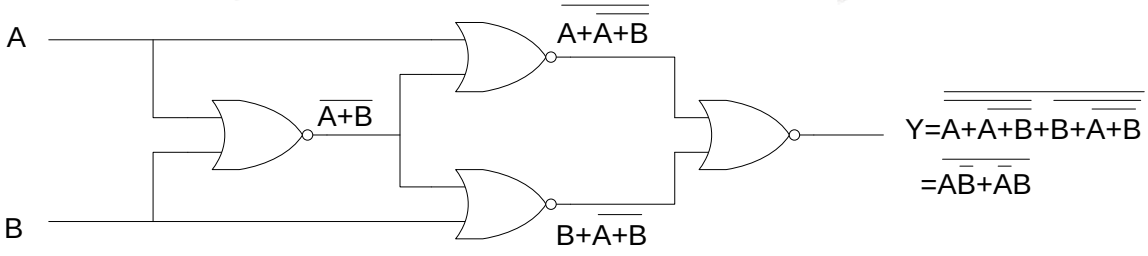


(ii)



(iii)

$$\overline{(A+B).(\overline{A}+\overline{B})} = \overline{A.\overline{B}+\overline{A}.B}$$



$$Y = \overline{A+\overline{A+B}+B+\overline{A+B}} = \overline{A}.(\overline{A+B})+\overline{B}.(\overline{A+B}) = \overline{A}.(A+B)+\overline{B}.(A+B) = A.\overline{B}+\overline{A}.B$$

Q11. Define canonical Minterm form and canonical Maxterm form.

Answer: Minterm: A minterm, denoted by m_i, $0 \le i<2^n$, is a product of n variables in which each variable is complemented if the value assigned to it is 0.

Let us consider a Boolean function $F = f(x, y, z) = x'yz + xy'z + xyz' + xyz$.

Truth table of the above function along with the minterms is shown below:

x	y	z	Minterm	F
0	0	0	m_0=x´y´z´	0
0	0	1	m_1= x´y´z	0
0	1	0	m_2= x´yz´	0
0	1	1	m_3= x´yz	1
1	0	0	m_4= xy´z´	0
1	0	1	m_5= xy´z	1
1	1	0	m_6= xyz´	1
1	1	1	m_7= xyz	1

The above function can be expressed in term of minterms as F=m_3+m_5+m_6+m_7=Σm(3,5,6,7)

The inverse of the function can be expressed as F´= Σm(0,1,2,4)

Maxterm: A maxterm, denoted by M_i, $0 \le i <2^n$, is a sum of n variables in which each variable is complemented if the value assigned to it is 1.

Let us consider a Boolean function $F = f(x, y, z) = (x + y + z)(x + y + z')(x + y' + z)(x' + y + z)$

Truth table of the above function along with maxterm is shown below:

x	y	z	Maxterm	F
0	0	0	M_0=x+y+z	0
0	0	1	M_1= x+y+z´	0
0	1	0	M_2= x+y´+z	0
0	1	1	M_3= x+y´+z´	1
1	0	0	M_4= x´+y+z	0
1	0	1	M_5= x´+y+z´	1
1	1	0	M_6= x´+y´+z	1
1	1	1	M_7= x´+y´+z´	1

The above function can be expressed in term of maxterms as F=M_0.M_1.M_2.M_4=ΠM(0,1,2,4)

The inverse of the function can be expressed as F´= ΠM(3,5,6,7)

.Q12. Express the function F=x+yz as the sum of its minterms and product of maxterms.

$$Answer: F = x + yz = x(y + y')(z + z') + yz(x + x') = xyz + xyz' + xy'z + xy'z' + xyz + x'yz$$

$$\Rightarrow F = xyz + xyz' + xy'z + xy'z' + x'yz = m_7 + m_6 + m_5 + m_4 + m_3 = \sum m(3,4,5,6,7)$$

$$Again,\ F = x + yz = (x + y)(x + z) = (x + y + zz')(x + z + yy')$$

$$\Rightarrow F = (x + y + z)(x + y + z')(x + z + y)(x + z + y') = (x + y + z)(x + y + z')(x + y' + z) = M_0.M_1.M_2 = \Pi M(0,1,2)$$

Q13. Express the function F=(x+yz) ´ as the sum of its minterms and product of maxterms.

$Answer: F = (x+yz)' = (x+(yz))' = x'.(yz)' = x'.(y'+z') = x'y' + x'z' = x'y'(z+z') + x'z'(y+y')$

$\Rightarrow F = x'y'z + x'y'z' + x'yz' + x'y'z' = x'y'z + x'y'z' + x'yz' = m_1 + m_0 + m_2 = \sum m(0,1,2)$

$Again, F = (x+yz)' = (x+(yz))' = x'.(yz)' = x'.(y'+z') = (x'+yy'+zz')(y'+z'+xx')$

$\Rightarrow F = (x'+yy'+z)(x'+yy'+z')(y'+z'+x)(y'+z'+x')$

$\Rightarrow F = (x'+y+z)(x'+y'+z)(x'+y+z')(x'+y'+z')(x+y'+z')(x'+y'+z')$

$\Rightarrow F = (x'+y+z)(x'+y'+z)(x'+y+z')(x'+y'+z')(x+y'+z')$

$\Rightarrow F = M_4.M_6.M_5.M_7.M_3 = \Pi M(3,4,5,6,7)$

Q14, Convert the following 3-variable SOP to POS form.

(i) Σm(3,5,6,7) (ii) Σm(0,2,5,6)

Answer: (i) Σm(3,5,6,7)=ΠM(0,1,2,4) (ii) Σm(0,2,5,6)=ΠM(1,3,4,7)

Q15. Convert the following 4-variable POS to SOP form.

(i) ΠM(1,3,4,7) (ii) ΠM(0,1,2,4,10,13,15)

Answer: (i)) ΠM(1,3,4,7)=Σm(0,2,5,6,8,9,10,11,12,13,14,15)

(ii) ΠM(0,1,2,4,10,13,15)=Σ(3,5,6,7,8,9,11,12,14)

Q16. Use K-Map to simplify the following functions:

$(i)\ f(A,B,C,D) = \sum m(0,2,6,10,11,12,13) + d(3,4,5,14,15)$

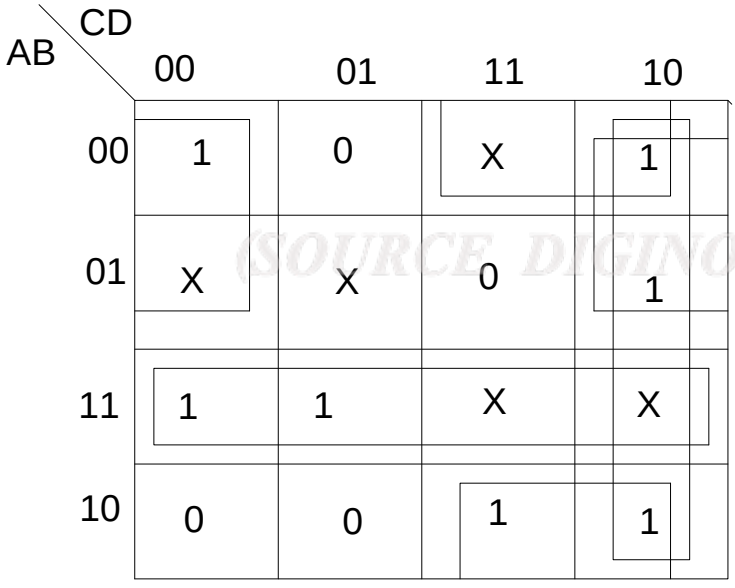
$(ii)\ f = \sum m(1,2,6,7,8,13,14,15) + d(3,5,12)$

$(iii)\ f = \sum m(1,3,4,5,13,15) + \sum d(8,9,10,11)$

$(iv)\ f(A,B,C,D) = (A+B+\overline{C})(\overline{B}+\overline{D})(\overline{A}+C)(B+C)$

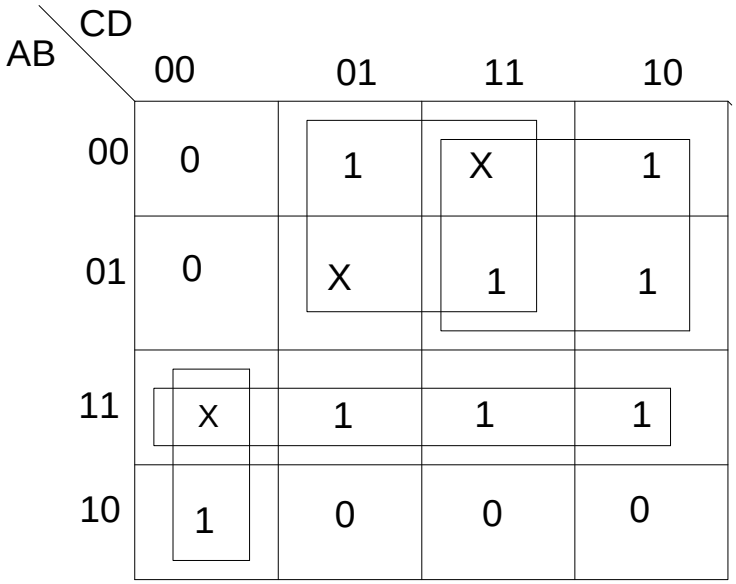
$(v)\ f(A,B,C,D) = \pi(1,2,4,5,7,8,10,11,13,14)$

Answer: (i)



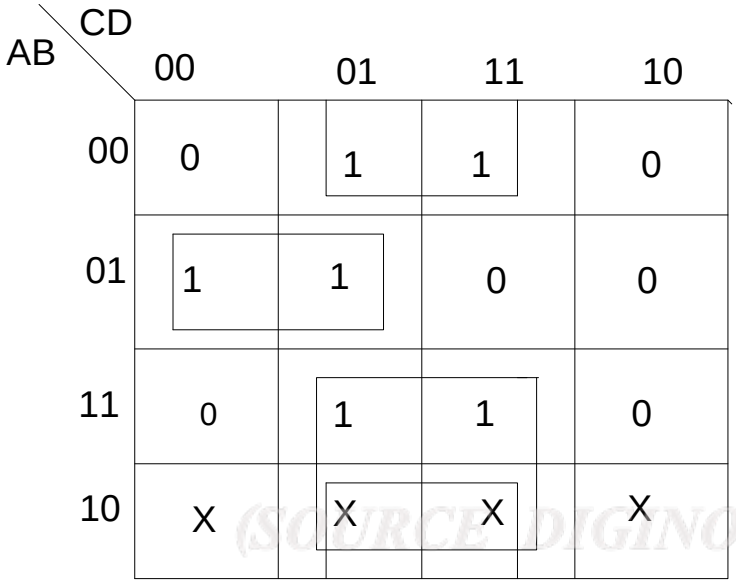
$f(A,B,C,D) = AB + C\overline{D} + \overline{B}C + \overline{A}\overline{D}$

(ii)Let us consider the variables as A, B, C and D.



$$f(A,B,C,D) = \overline{A}D + \overline{A}C + AB + A\overline{C}\,\overline{D}$$

(iii) Let us consider the variables as A, B, C and D.



$$f(A,B,C,D) = AD + \overline{B}D + \overline{A}B\overline{C}$$

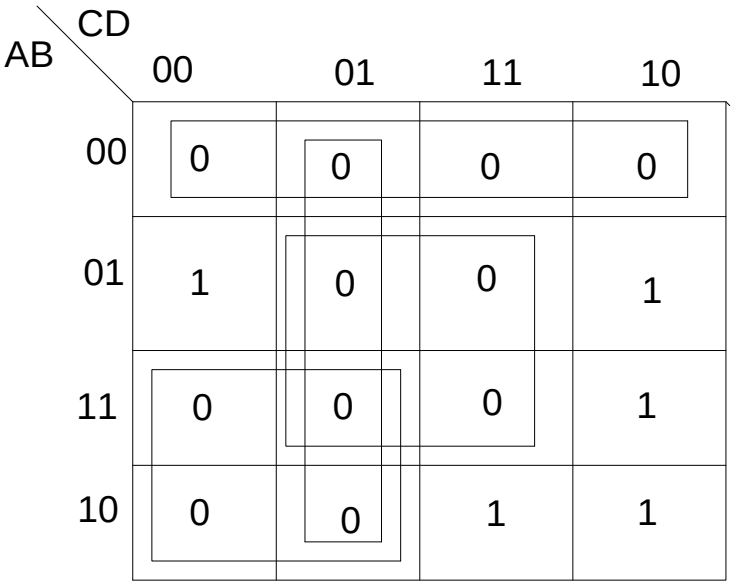
$(iv)\ f(A,B,C,D) = (A+B+\overline{C})(\overline{B}+\overline{D})(\overline{A}+C)(B+C)$

$= (A+B+\overline{C}+\overline{D})(A+B+\overline{C}+D)(\overline{A}+\overline{B}+\overline{C}+\overline{D})(\overline{A}+\overline{B}+C+\overline{D})(A+\overline{B}+\overline{C}+\overline{D})(A+\overline{B}+C+\overline{D})$

$(\overline{A}+\overline{B}+C+\overline{D})(\overline{A}+\overline{B}+C+D)(\overline{A}+B+C+\overline{D})(\overline{A}+B+C+D)(\overline{A}+B+C+\overline{D})(\overline{A}+B+C+D)$

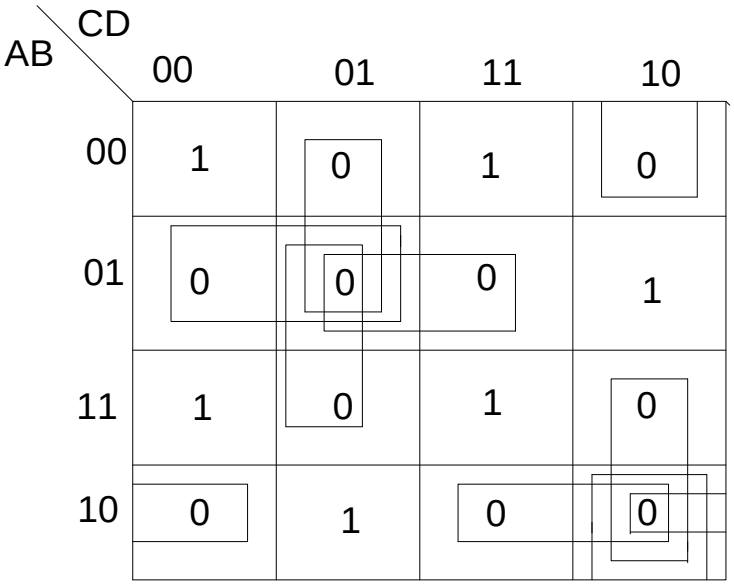
$(A+B+C+\overline{D})(A+B+C+D)$

$= M_3.M_2.M_{15}.M_{13}.M_7.M_5.M_{12}.M_9.M_8.M_1.M_0 = M_0.M_1.M_2.M_3.M_5.M_7.M_8.M_9.M_{12}.M_{13}.M_{15}$



$$f(A,B,C,D) = (A+B)(C+\overline{D})(\overline{B}+\overline{D})(\overline{A}+C)$$

(v)

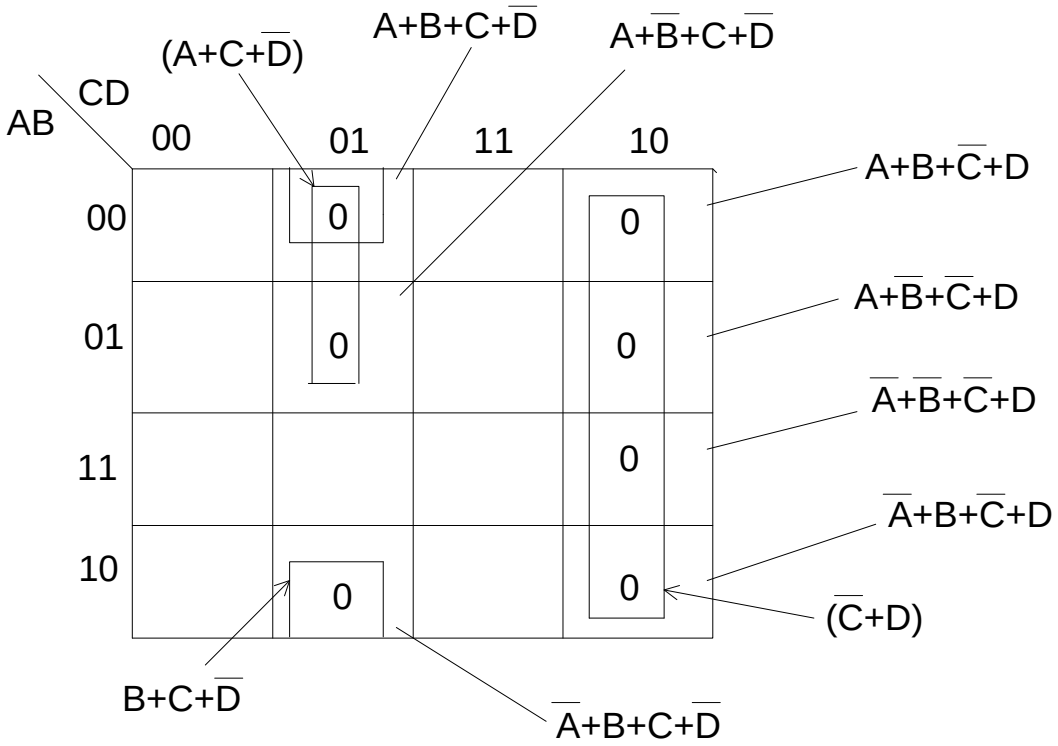


$$f = (A+\overline{B}+C)(A+\overline{B}+\overline{D})(\overline{B}+C+\overline{D})(A+C+\overline{D})(\overline{A}+B+\overline{C})(\overline{A}+\overline{C}+D)(\overline{A}+B+D)(B+\overline{C}+D)$$

Q17, Simplify the Product of Sum expression below and provide the result in POS form.

$$F(A,B,C,D) = (A+B+C+\overline{D})(A+B+\overline{C}+D)(A+\overline{B}+C+\overline{D})(A+\overline{B}+\overline{C}+D)(\overline{A}+\overline{B}+\overline{C}+D)$$
$$(\overline{A}+B+C+\overline{D})(\overline{A}+B+\overline{C}+D)$$

Answer:

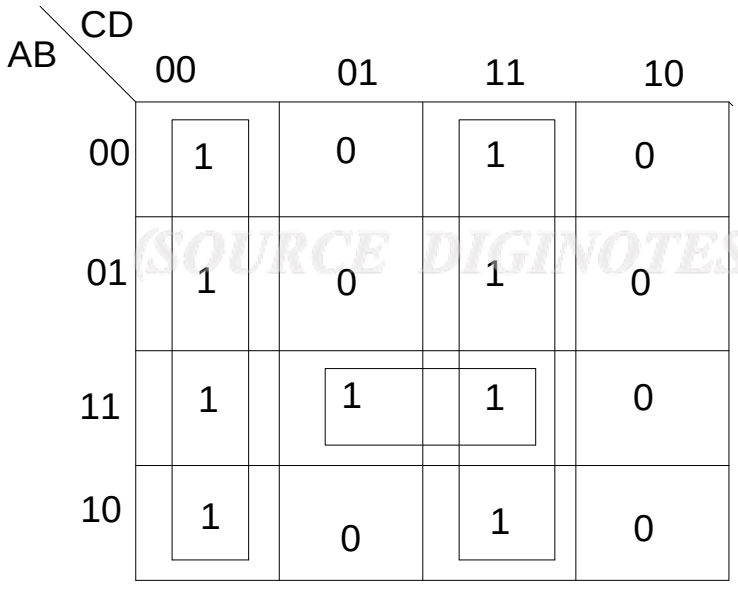


Therefore, the result in POS, $F = (\overline{C} + D)(A + C + \overline{D})(B + C + \overline{D})$

Q18. Simplify the Product Of Sum expression below and provide the result in SOP form.

$F(A, B, C, D) = (A + B + C + \overline{D})(A + B + \overline{C} + D)(A + \overline{B} + C + \overline{D})(A + \overline{B} + \overline{C} + D)(\overline{A} + \overline{B} + \overline{C} + D)$
$(\overline{A} + B + C + \overline{D})(\overline{A} + B + \overline{C} + D)$

Answer:



Therefore, the result in SOP, $F = \overline{C}\,\overline{D} + CD + ABD$

Q19. Find the minimal SOP and minimal POS of the following Boolean function using K-Map.

$f(a,b,c,d) = \sum m(6,7,9,10,13) + d(1,4,5,11)$

Answer:

ab \ cd	00	01	11	10
00	0	X	0	0
01	X	X	1	1
11	0	1	0	0
10	0	1	X	1

Minimal SOP is given by $f(a,b,c,d) = \bar{a}b + \bar{c}d + a\bar{b}c$

ab \ cd	00	01	11	10
00	0	X	0	0
01	X	X	1	1
11	0	1	0	0
10	0	1	X	1

Minimal POS is given by $f(a,b,c,d) = (a+b)(c+d)(\bar{a}+\bar{b}+\bar{c})$

Q20. Reduce the following Boolean function using K-Map and realize the simplified expression using NAND gates.

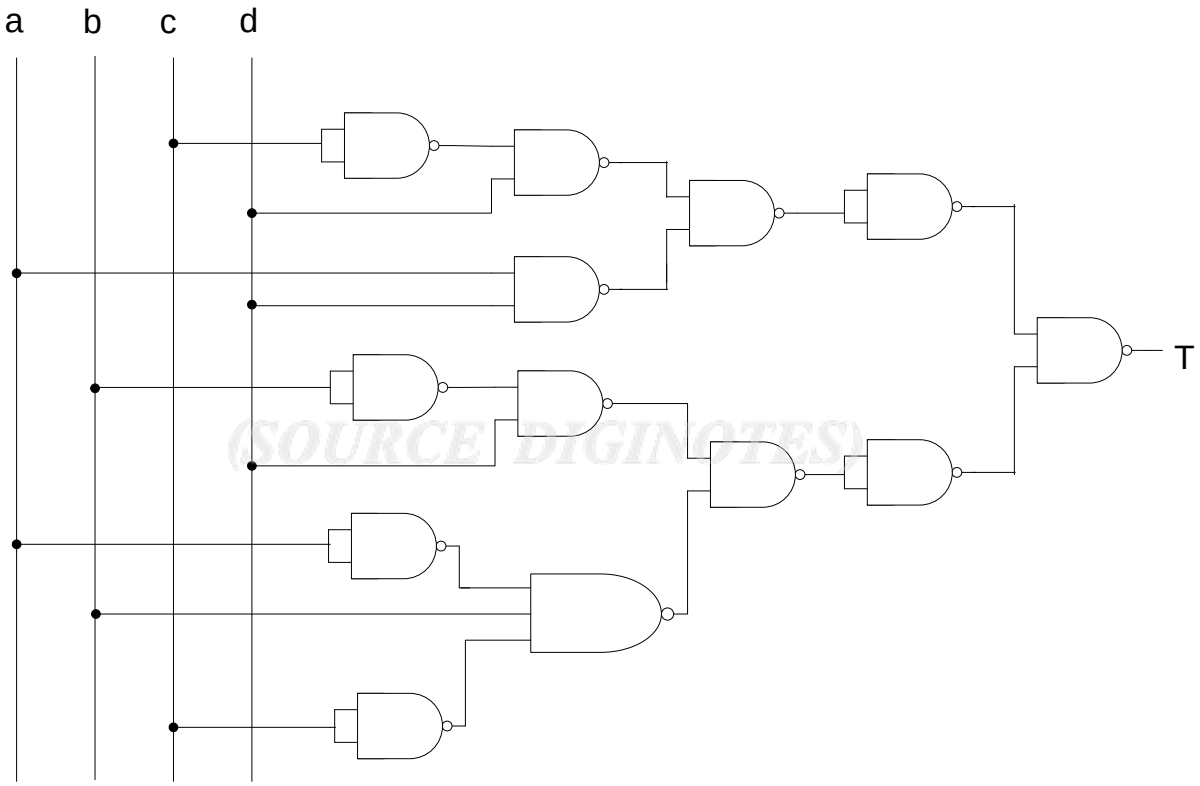
$T = f(a,b,c,d) = \sum m(1,3,4,5,13,15) + \sum d(8,9,10,11)$

Answer:

ab \ cd	00	01	11	10
00	0	1	1	0
01	1	1	0	0
11	0	1	1	0
10	X	X	X	X

$$T = f(a,b,c,d) = \bar{c}d + ad + \bar{b}d + \bar{a}\bar{b}\bar{c}$$

Following diagram shows the realization of the above expression with NAND gates

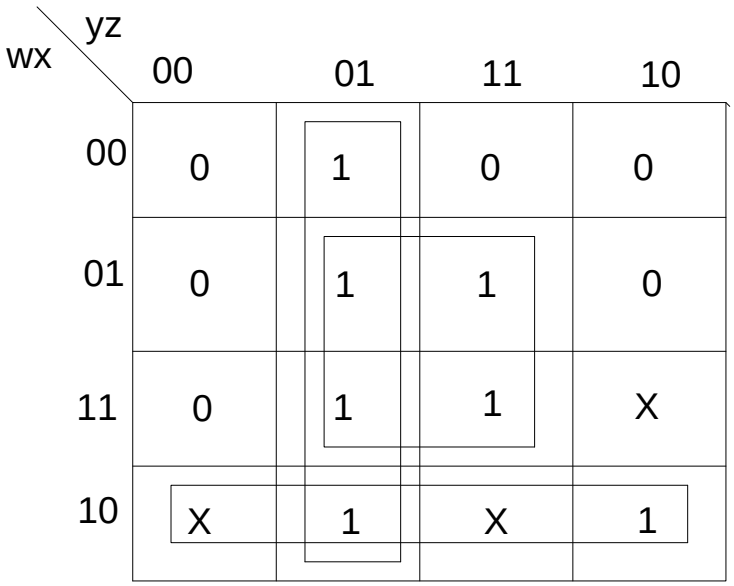


Q21. Simplify the following expressions using Karnaugh map. Implement the simplified circuit using the gates as indicated:

(*i*) $f(w,x,y,z) = \sum m(1,5,7,9,10,13,15) + d(8,11,14)$ using NAND gates.

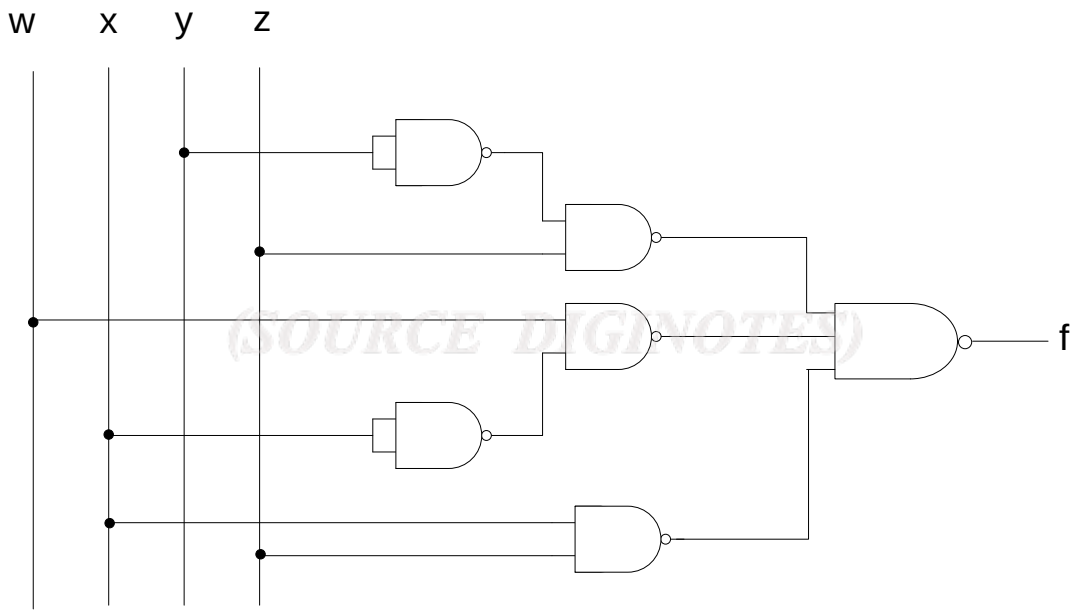
(ii) $f(A,B,C,D) = \Pi M(0,1,2,4,5,6,8,9,12,13,14)$ using NOR gates.

Answer: (i)



$f(w,x,y,z) = \bar{y}z + w\bar{x} + xz$

Following is the implementation of the simplified circuit with NAND gates.

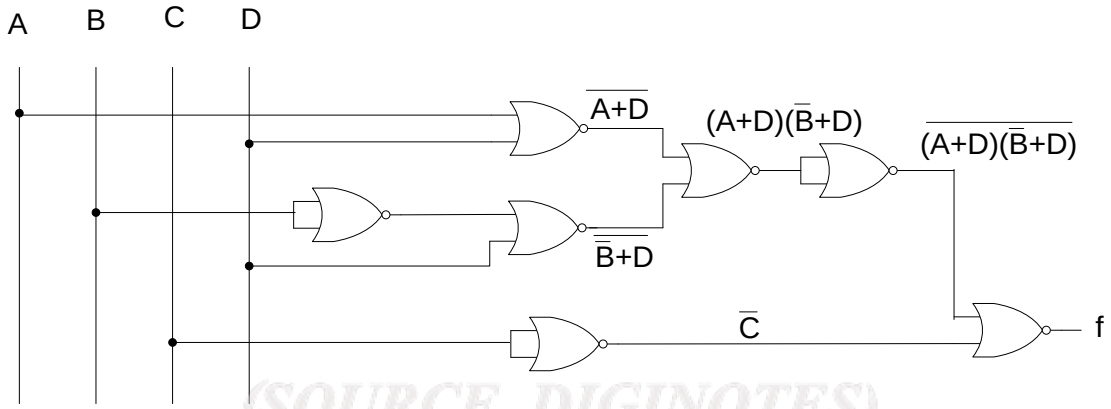


(ii)

AB \ CD	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	0	0	1	0
10	0	0	1	1

$$f(A,B,C,D) = C(A+D)(\overline{B}+D)$$

Following is the implementation of the simplified circuit with NOR gates.



Q22. Simplify the following using Quine McClusky minimization technique:

$(i) P = f(w,x,y,z) = \sum m(7,9,12,13,14,15) + \sum d(4,11)$

$(ii) Y = f(a,b,c,d) = \sum (0,1,2,6,7,9,10,12) + d(3,5)$. Verify the result using K-map.

$(iii)\ f(A,B,C,D) = \sum m(0,1,2,3,10,11,12,13,14,15)$

$(iv)\ f(W,X,Y,Z) = \sum m(1,3,6,7,8,9,10,12,13,14)$

Answer:

(i)

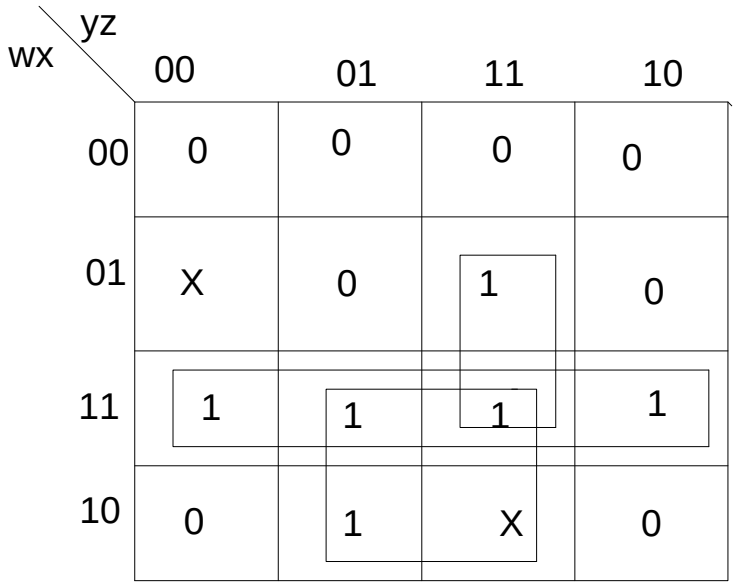
f(w,x,y,z)=Σm(7,9,12,13,14,15)+d(4,11)

Stage 1 wxyz		Stage 2 wxyz		Stage 3 wxyz	
0100	(4)√	-100	(4,12)	1- -1	(9,11,13,15)
1001	(9)√				
1100	(12)√	10-1	(9,11)√	1- -1	(9,13,11,15)
0111	(7)√	1-01	(9,13)√	11- -	(12,13,14,15)
1011	11)√	110-	(12,13)√	11- -	(12,14,13,15)
1101	(13)√	11-0	(12,14)√		
1110	1(4)√				
		-111	(7,15)		
1111	(15)√	1-11	(11,15)√		
		11-1	(13,15)√		
		111-	(14,15)√		

	7	9	12	13	14	15
wz (9,11,13,15)		√		√		√
wx (12,13,14,15)			√	√	√	√
$xy'z'$ (4,12)			√			
xyz (7,15)	√					√

$P = f(w,x,y,z) = wz + wx + xyz$

Verification:



$$P = f(w,x,y,z) = wz + wx + xyz$$

(ii)

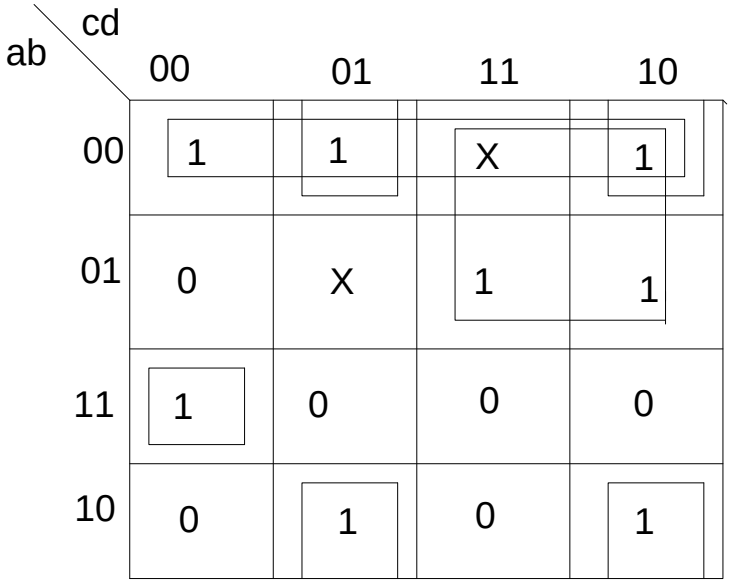
$$Y=f(a,b,c,d)=\Sigma m(0,1,2,6,7,9,10,12)+d(3,5)$$

Stage 1		Stage 2		Stage 3	
abcd		abcd		abcd	
0000	(0)√	000-	(0,1)√	00 - -	(0,1,2,3)
0001	(1)√	00-0	(0,2)√	00 - -	(0,2,1,3)
0010	(2)√	00-1	(1,3)√	0 - -1	(1,3,5,7)
0011	(3)√	0-01	(1,5)√	0 - -1	(1,5,3,7)
0101	(5)√	-001	(1,9)	0 -1-	(2,3,6,7)
0110	(6)√	001-	(2,3)√	0 -1-	(2,6,3,7)
1001	(9)√	0-10	(2,6)√		
1010	(10)√	-010	(2,10)		
1100	(12)	0-11	(3,7)√		
0111	(7)√	01-1	(5,7)√		
		011-	(6,7)√		

	0	1	2	6	7	9	10	12
$abc'd'(12)$								√
$b'c'd(1,9)$		√				√		
$b'cd'(2,10)$			√				√	
$a'b'(0,1,2,3)$	√	√	√					
$a'd(1,3,5,7)$		√			√			
$a'c(2,3,6,7)$			√	√	√			

$Y = abc'd' + b'c'd + b'cd' + a'b' + a'c$

Verification:



$Y = abc'd' + b'c'd + b'cd' + a'b' + a'c$

(iii)

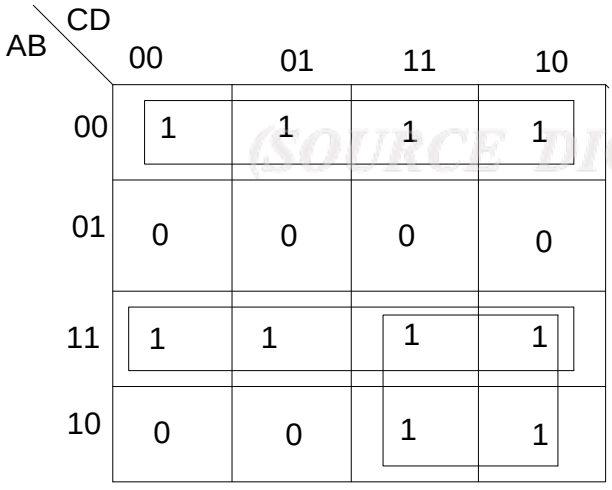
$f(A,B,C,D)=\Sigma m(0,1,2,3,10,11,12,13,14,15)$

Stage 1		Stage 2		Stage 3	
ABCD		ABCD		ABCD	
0000	(0)√	000-	(0,1)√	00 - -	(0,1,2,3)
		00-0	(0,2)√	00 - -	(0,2,1,3)
0001	(1)√				
0010	(2)√	00-1	(1,3)√	-01-	(2,3,10,11)
0011	(3)√	001-	(2,3)√	-01-	(2,10,3,11)
1010	(10)√	-010	(2,10)√		
1100	(12)√	-011	(3,11)√	1-1-	(10,11,14,15)
		101-	(10,11)√	1-1-	(10,14,11,15)
1011	(11)√	1-10	(10,14)√		
1101	(13)√	110-	(12,13)√	11- -	(12,13,14,15)
1110	(14)√	11-0	(12,14)√	11- -	(12,14,13,15)
		1-11	(11,15)√		
1111	(15)√	11-1	(13,15)√		
		111-	(14,15)√		

	0	1	2	3	10	11	12	13	14	15
$A'B'(0,1,2,3)$	√	√	√	√						
$B'C(2,3,10,11)$			√	√	√	√				
AC (10,11,14,15)					√	√			√	√
AB (12,13,14,15)							√	√	√	√

$f(A,B,C,D)=A'B'+AC+AB$ or $f(A,B,C,D)=A'B'+B'C+AB$

Verification:



$f(A,B,C,D)=A'B'+AC+AB$

(iv)

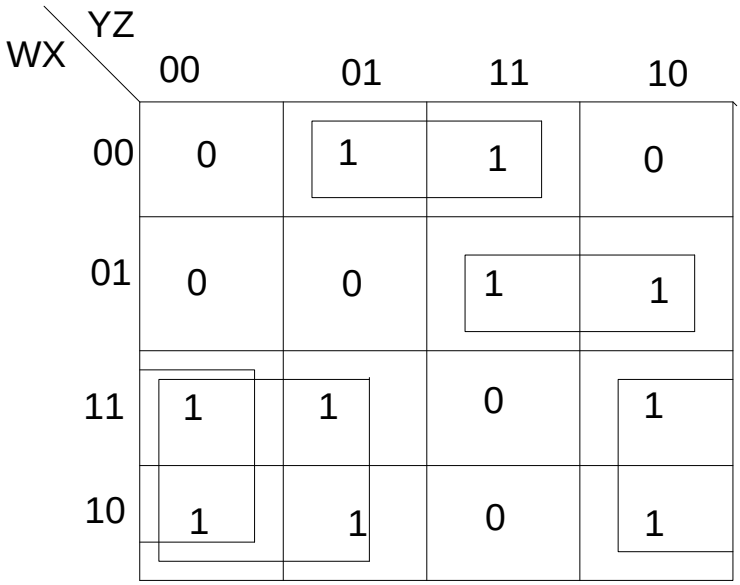
f(W,X,Y,Z)=Σm(1,3,6,7,8,9,10,12,13,14)

Stage 1		Stage 2		Stage 3	
WXYZ		WXYZ		WXYZ	
0001	(1)√	00-1	(1,3)	1-0-	(8,9,12,13)
1000	(8)√	-001	(1,9)	1- -0	(8,10,12,14)
0011	(3)√	100-	(8,9)√	1- -0	(8,12,10,14)
0110	(6)√	10-0	(8,10)√		
1001	(9)√	1-00	(8,12)√		
1010	(10)√	0-11	(3,7)		
1100	(12)√	011-	(6,7)		
0111	(7)√	-110	(6,14)		
1101	(13)√	1-01	(9,13)		
1110	(14)√	1-10	(10,14)√		
		110-	(12,13)√		
		11-0	(12,14)√		

	1	3	6	7	8	9	10	12	13	14
$W'X'Z(1,3)$	√	√								
$X'Y'Z(1,9)$	√					√				
$W'YZ(3,7)$		√		√						
$W'XY(6,7)$			√	√						
$XYZ'(6,14)$			√							√
$WY'Z(9,13)$						√			√	
$WY'(8,9,12,13)$					√	√		√	√	
$WZ'(8,10,12,14)$					√		√	√		√

$$f(W,X,Y,Z) = W'X'Z + W'XY + WY' + WZ'$$

Verification:



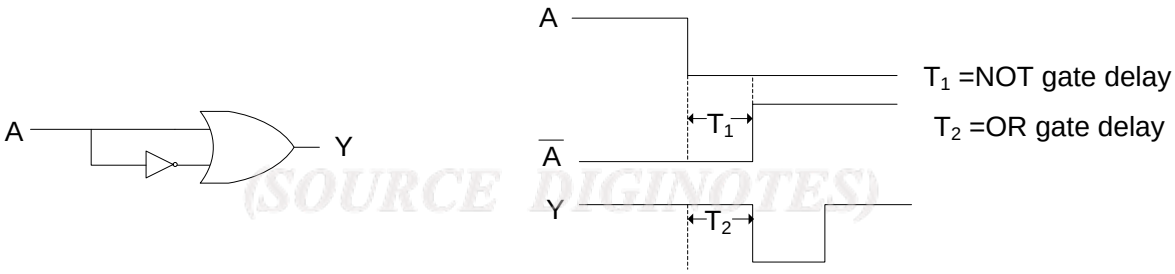
$$f(W,X,Y,Z) = W'X'Z + W'XY + WY' + WZ'$$

Q23. What are static hazards? How to design a hazard free circuit? Explain with an example.

Answer: When the input to a combinational circuit changes, unwanted switching transients may appear in the output. These transients occurs when different paths from input to output have different propagation delays.

Static-1 hazard:

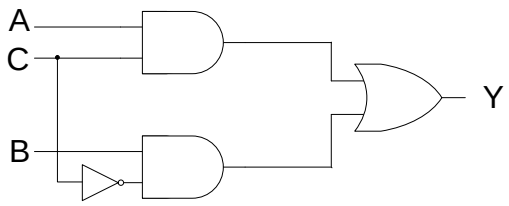
This type of hazard occurs when $Y = A + \overline{A}$ type situation appears for a logic circuit and A makes a transition $1 \rightarrow 0$.



An $A + \overline{A}$ condition should always generate 1 at the output i.e static-1. But the NOT gate output takes finite time to become 1 following $1 \rightarrow 0$ transition of A. Thus for the OR gate there are two zeros appears at the input for that small duration resulting a 0 at the output. The width of this zero is in nanosecond order and is called glitch.

Designing static-1 hazard free circuit:

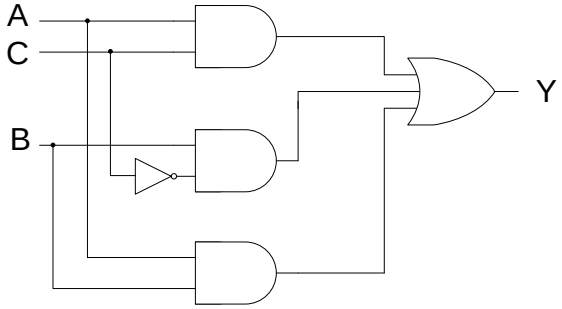
	$\overline{C}$	C
$\overline{A}\,\overline{B}$	0	0
$\overline{A}\,B$	1	0
$A\,B$	1	1
$A\,\overline{B}$	0	1



The karnaugh map shown above represented by $Y = B\overline{C} + AC$

Consider the circuit input B=1 and A=1 and then C makes transition 1→0. The output shows glitches. Now, consider the following grouping:

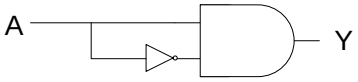
	$\overline{C}$	C
$\overline{A}\,\overline{B}$	0	0
$\overline{A}\,B$	1	0
$A\,B$	1	1
$A\,\overline{B}$	0	1

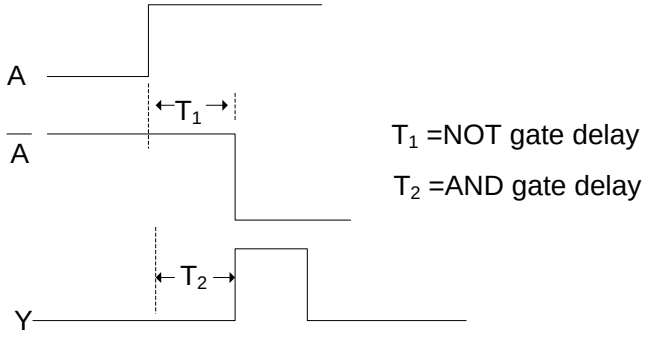


The above circuit includes one additional AB and $Y = B\overline{C} + AC + AB$. The additional ensures free from glitches.

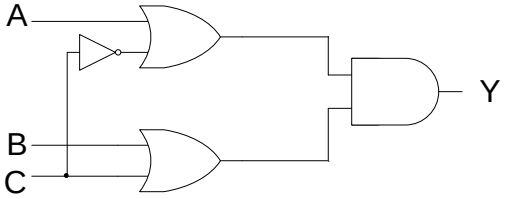
Static-0-hazard:

This type of hazard occurs when $Y = A\overline{A}$ kind of situation occurs in a logic circuit and A makes a transition 0→1. A $A\overline{A}$ condition should always generate 0 at the output i.e static-0. But the NOT gate output takes finite time to become 0 following a 0→1 transition of A. Thus for final AND gate there are two ones appearing at the inputs for small duration resulting a 1 at its output.





The circuit below is with static-0 hazard:



Consider the circuit input B=0 and A=0 and then C makes transition 0⟶1. The output shows glitches.

The circuit below is static-0 hazard free