INSTR BITS	mnemoni	15	14 13 12	11 10 9	8	7 6	5 4	3	2	1	0							
DOUBLE OPS		SZ	op code	mode		reg	mod	e		reg								
move	mov	b	1	mode 0 to 7		reg 0 to 7	mode 0	to 7		reg 0 to 7								
add	add	0	6	mode 0 to 7		reg 0 to 7	mode 0	to 7		reg 0 to 7								
subtract	sub	1	6	mode 0 to 7		reg 0 to 7	mode 0	to 7		reg 0 to 7								
compare	cmp	b	2	mode 0 to 7		reg 0 to 7	mode 0	to 7		reg 0 to 7								
bit set	bis	b	5	mode 0 to 7		reg 0 to 7	mode 0	to 7		reg 0 to 7								
bit clear	bic	b	4	mode 0 to 7		reg 0 to 7	mode 0	to 7		reg 0 to 7								
bit test	bit	b	3	mode 0 to 7		reg 0 to 7	mode 0	to 7		reg 0 to 7								
JUMPS/BRAN	NCHES	SZ	constant	typ	flg			offset										
jump	jmp	0	0	0		1	mode 0	to 7		reg 0 to 7								
jump to subr	outine jsr	0	1	0		reg 0 to 7	mode 0	to 7		reg 0 to 7		exception	n in SINGLE	OPS, to be	e treated a	s SINGLE O	P word inst	r, typ=0
return from	subrout rts	0	0	0		2	0 0	0		reg 0 to 7		exception	n in FLAG O	PS, the '2'	overlaps v	vith FLAG O	PS	
swap byte	swab	0	0	0		3	mode 0	to 7		reg 0 to 7								
branch	br	0	0	0	1			offset										
if equal	beq	0	0	1	1			offset										
if not eq	bne	0	0	1	0			offset										
if -ve	bmi	1	0	0	1			offset				For brace	hes, first c	heck [15] l	oit then co	ntinue proc	essing	
if +ve	bpl	1	0	0	0			offset					processir					
if cy	bcs	1	0	3	1			offset				1` '						
if no cy	bcc	1	0	3	0			offset										
if oflw	bvs	1	0	2	1			offset										
if no oflw	bvc	1	0	2	0			offset										
less than	blt	0	0	2	1			offset										
grt eq	bge	0	0	2	0			offset										
less eq	ble	0	0	3	1			offset										
grt than	bgt	0	0	3	0			offset										
higher	bhi	1	0	1	0			offset										
low some	blos	1	0	1	1			offset										
high some	bhis	1	0	3	0			offset										
	blo	1	0	3	1			offset										
lower																		
SINGLE OPS	DIO				1	op code	mode[:			reg[2:0]								
SINGLE OPS		SZ	constant	typ	1	op code 0	mode[a	2:0]		reg[2:0]								
SINGLE OPS clear	clr	sz b	constant 1	typ 1	1	0	mode 0	2:0] to 7		reg 0 to 7								
SINGLE OPS clear incre	clr inc	sz b b	constant 1 1	typ 1 1	1	0	mode 0 mode 0	2:0] to 7 to 7		reg 0 to 7 reg 0 to 7								
clear incre decr	clr inc dec	b b b	constant 1 1 1	typ 1 1 1 1	1	0 2 3	mode 0 mode 0 mode 0	2:0] to 7 to 7 to 7		reg 0 to 7 reg 0 to 7 reg 0 to 7								
clear incre decr negate	clr inc dec neg	b b b b	constant  1  1  1  1  1	typ 1 1 1 1 1		0 2 3 4	mode 0 mode 0 mode 0 mode 0	2:0] to 7 to 7 to 7 to 7		reg 0 to 7 reg 0 to 7 reg 0 to 7 reg 0 to 7								
clear incre decr negate test	clr inc dec neg tst	b b b b	constant  1  1  1  1  1  1  1	typ 1 1 1 1 1 1 1		0 2 3 4 7	mode 0 mode 0 mode 0 mode 0 mode 0	2:0] to 7 to 7 to 7 to 7 to 7		reg 0 to 7 reg 0 to 7 reg 0 to 7 reg 0 to 7 reg 0 to 7								
clear incre decr negate test 1s comp	clr inc dec neg tst com	b b b b b	constant  1  1  1  1  1  1  1  1	typ 1 1 1 1 1 1 1 1 1 1		0 2 3 4 7	mode 0 mode 0 mode 0 mode 0 mode 0 mode 0	2:0] to 7 to 7 to 7 to 7 to 7 to 7		reg 0 to 7 reg 0 to 7								
clear incre decr negate test 1s comp add cy	clr inc dec neg tst com	b b b b b b b	constant  1  1  1  1  1  1  1  1  1  1  1	typ 1 1 1 1 1 1 1 1 1 1 1 1 1		0 2 3 4 7 1	mode 0 mode 0 mode 0 mode 0 mode 0 mode 0 mode 0	2:0] to 7 to 7 to 7 to 7 to 7 to 7 to 7		reg 0 to 7 reg 0 to 7								
clear incre decr negate test 1s comp add cy sub cy	clr inc dec neg tst com adc sbc	b b b b b b	constant  1  1  1  1  1  1  1  1  1  1  1  1  1	typ 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		0 2 3 4 7 1 5	mode 0 mode 0 mode 0 mode 0 mode 0 mode 0 mode 0	2:0] to 7		reg 0 to 7								
clear incre decr negate test 1s comp add cy sub cy rot rt	clr inc dec neg tst com adc sbc ror	b b b b b b b b b	constant  1  1  1  1  1  1  1  1  1  1  1  1  1	typ  1  1  1  1  1  1  1  1  1  2		0 2 3 4 7 1 5 6	mode 0	2:0] to 7		reg 0 to 7								
clear incre decr negate test 1s comp add cy sub cy rot rt rot lft	clr inc dec neg tst com adc sbc ror rol	5z b b b b b b b b b b b b b	constant  1  1  1  1  1  1  1  1  1  1  1  1  1	typ  1  1  1  1  1  1  1  1  2  2		0 2 3 4 7 1 5 6 0	mode 0	2:0] to 7		reg 0 to 7								
clear incre decr negate test 1s comp add cy sub cy rot rt rot lft arith rt	clr inc dec neg tst com adc sbc ror rol asr	52	constant  1  1  1  1  1  1  1  1  1  1  1  1  1	typ  1  1  1  1  1  1  1  1  2  2  2		0 2 3 4 7 1 5 6 0 1[1]	mode 0	2:0] to 7		reg 0 to 7								
clear incre decr negate test 1s comp add cy sub cy rot rt rot lft arith rt arith lft	clr inc dec neg tst com adc sbc ror rol asr asl	5z b b b b b b b b b b b b b	constant  1  1  1  1  1  1  1  1  1  1  1  1  1	typ  1  1  1  1  1  1  1  1  2  2  2  2		0 2 3 4 7 1 5 6 0	mode 0	2:0] to 7	7	reg 0 to 7								
clear incre decr negate test 1s comp add cy sub cy rot rt rot lft arith rt arith lft Program Stat	clr inc dec neg tst com adc sbc ror rol asr asl	5z b b b b b b b b b b b b b b b b b	constant  1  1  1  1  1  1  1  1  1  1  1  1  1	typ  1  1  1  1  1  1  1  1  1  2  2  2  constant		0 2 3 4 7 1 5 6 0 1 [1] 2	mode 0	2:0] to 7	Z	reg 0 to 7	C 1							
clear incre decr negate test 1s comp add cy sub cy rot rt rot lft arith rt arith lft Program Stat clr cy	clr inc dec neg tst com adc sbc ror rol asr asl	5z b b b b b b b b b b b b b b b b c c d d d d	constant  1  1  1  1  1  1  1  1  1  1  1  1  1	typ  1  1  1  1  1  1  1  1  2  2  2  2  constant  0		0 2 3 4 7 1 5 6 0 1[1] 2 3	mode 0 filg S/C 1	2:0] to 7	0	reg 0 to 7	1							
clear incre decr negate test 1s comp add cy sub cy rot rt rot lft arith lft Program Stat clr cy clr oflw	clr inc dec neg tst com adc sbc ror rol asr asr asl tus OPS clc clv	52 b b b b b b b b b b	constant  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0	typ  1 1 1 1 1 1 1 1 1 1 2 2 2 2 2 2 0 0 0 0		0 2 3 4 7 1 5 6 0 1[1] 2 3	mode 0 fig S/C 1 0	2:0] to 7	0	reg 0 to 7	1 0							
clear incre decr negate test 1s comp add cy sub cy rot rt rot lft arith lft Program Stat clr cy clr oflw clr zero	clr inc dec neg tst com adc sbc ror rol asr asl tus OPS clc clv clz	5z b b b b b b b b b b b c c c c c c c c	constant  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0	typ  1 1 1 1 1 1 1 1 1 1 2 2 2 2 2 2 0 0 0 0		0 2 3 4 7 1 5 6 0 1[1] 2 3	mode 0 flg S/C 1 0 1 0	2:0] to 7	0 0 1	reg 0 to 7	1 0 0							
clear incre decr negate test 1s comp add cy sub cy rot rt rot lft arith rt arith rt errogram Stat clr cy clr oflw clr zero clr neg	clr inc dec neg tst com adc sbc ror rol asr asl tus OPS clc clv clz cln	5z b b b b b b b b b b b c c c c c c c c	constant  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0	typ  1 1 1 1 1 1 1 1 1 1 2 2 2 2 2 2 0 0 0 0		0 2 3 4 7 1 5 6 0 1 [1] 2 3	mode 0 1 0 1 0 1 0 0	2:0] to 7	0	reg 0 to 7	1 0							
single ops clear incre decr negate test 1s comp add cy sub cy rot rt rot lft arith rt arith lft Program Stat clr cy clr oflw clr zero clr neg set cy	clr inc dec neg tst com adc sbc ror rol asr asl tus OPS clc clv clz cln sec	5z b b b b b b b b b b b c c c c c c c c	constant  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0	typ  1  1  1  1  1  1  1  1  2  2  2  2  0  0  0  0  0  0		0 2 3 4 7 1 5 6 0 1 [1] 2 3	mode 0 1 0 1 0 1 1 1	2:0] to 7	0 0 1 0	reg 0 to 7 0 1 0 0 0	1 0 0 0							
clear incre decr negate test 1s comp add cy sub cy rot rt rot Ift arith rt arith Ift Program Stat clr cy clr zero clr neg set cy ser oflw	clr inc dec neg tst com adc sbc ror rol asr asl tus OPS clc clv clz cln sec sec	52 b b b b b b b b b b b c c c c c c c c	Constant  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0	typ  1 1 1 1 1 1 1 1 1 1 1 2 2 2 2 2 2 0 0 0 0		0 2 3 4 7 1 5 6 0 1[1] 2 3	mode 0 1 0 1 0 1 0 1 1 1 1	2:0] to 7	0 0 1 0 0	reg 0 to 7 reg 0 to 1 0 0 0 1	1 0 0 0 0							
single ops clear incre decr negate test 1s comp add cy sub cy rot rt rot lft arith rt arith lft Program Stat clr cy clr zero clr neg set cy ser oflw set zero	clr inc dec neg tst com adc sbc ror rol asr asl tus OPS clc clv clz cln sec sec sev sez	5z b b b b b b b b b b c c c c c c c c c	Constant  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	typ  1 1 1 1 1 1 1 1 1 1 1 1 2 2 2 2 2 2 0 0 0 0		0 2 3 4 7 1 5 6 0 1[1] 2 3	mode 0 1 0 1 0 1 1 1 1	2:0] to 7	0 0 1 0 0 0	reg 0 to 7 0 0 1 0 0 0 1 0 0	1 0 0 0 1 0							
single ops clear incre decr negate test 1s comp add cy sub cy rot rt rot lft arith rt arith lft Program Stat clr cy clr oflw clr zero clr neg set cy ser oflw set zero set neg	clr inc dec neg tst com adc sbc ror rol asr asl tus OPS clc clv clz cln sec sec	5z b b b b b b b b b b c c c c c c c c c	Constant  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	typ  1  1  1  1  1  1  1  1  1  1  2  2  2		0 2 3 4 7 1 5 6 0 1 [1] 2 3	mode 0 1 0 1 0 1 1 1 1 1 1	2:0] to 7	0 0 1 0 0 0 0	reg 0 to 7 0 0 1 0 0 0 0 1 0 0 0	1 0 0 0 0 1 0 0							
single ops clear incre decr negate test 1s comp add cy sub cy rot rt rot lft arith lft Program Stat clr cy clr oflw clr zero clr neg set cy set cy set oflw set zero set neg no oprn	clr inc dec neg tst com adc sbc ror rol asr asl tus OPS clc clv clz cln sec sec sev sez	5z b b b b b b b b b c c c c c c c c c c	Constant  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	typ  1 1 1 1 1 1 1 1 1 1 1 1 1 2 2 2 2 2 2		0 2 3 4 7 1 5 6 0 1 [1] 2 3 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	mode 0 1 1 0 1 1 1 1 1 1 1 0	2:0] to 7	0 0 1 0 0 0 0 0	reg 0 to 7 0 1 0 0 1 0 0 0 0 0 0 0 0 0	1 0 0 0 1 0 0 0							
single ops clear incre decr negate test 15 comp add cy sub cy rot rt rot lft arith rt arith rt arith rt clr cy clr oflw clr zero clr neg set cy set oflw set zero set neg no oprn no oprn	clr inc dec neg tst com adc sbc ror rol asr asl tus OPS clc clv clz cln sec sec sev sez	5z b b b b b b b b b b c c c c c c c c c	Constant  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	typ  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0		0 2 3 4 7 1 5 6 0 1 [1] 2 3	mode 0 1 0 1 0 1 1 1 1 1 1	2:0] to 7	0 0 1 0 0 0 0	reg 0 to 7	1 0 0 0 0 1 0 0							
SINGLE OPS clear incre decr negate test 15 comp add cy sub cy rot rt rot lft arith rt arith lft Program Stat clr cy clr oflw clr zero clr neg set cy ser oflw set zero set neg no oprn no oprn system	clr inc dec neg tst com adc sbc ror rol asr asl tus OPS clc clv clz cln sec sev sez sen	5z b b b b b b b b b c c c c c c c c c c	Constant  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	typ  1 1 1 1 1 1 1 1 1 1 1 1 1 2 2 2 2 2 2		0 2 3 4 7 1 5 6 0 1[1] 2 3 2 2 2 2 2 2 2 2 2 2 2	mode 0 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	2:0] to 7	0 0 1 0 0 0 0 0	reg 0 to 7 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 1 0 0 0							
clear incre decr negate test 1s comp add cy sub cy rot rt rot lft arith rt arith rt arith lft Program Stat clr cy clr oflw clr zero clr neg set cy ser oflw set zero set neg no oprn no oprn system rst bus	clr inc dec neg tst com adc sbc ror rol asr asl asl asl stus OPS clc clv clz cln sec sec sev sez sen	52 b b b b b b b b b b c 0 0 0 0 0	Constant  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	typ		0 2 3 4 7 1 5 6 0 1 [1] 2 3 2 2 2 2 2 2 2 2 2 2 2 2	mode 0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 0 1 0	2:0] to 7	0 0 1 0 0 0 0 0	reg 0 to 7 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 1 0 0 0							
single ops clear incre decr negate test 1s comp add cy sub cy rot rt rot lft arith rt arith lft Program Stat clr cy clr oflw clr zero clr neg set cy ser oflw set zero set neg no oprn no oprn system rst bus intr wait	clr inc dec neg tst com adc sbc ror rol asr asl tus OPS clc clr clr clr sec sec sev sez sen	52 b b b b b b b b b b b c o o o o o o o o o o o o o	Constant  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	typ  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 2 2 2 2		0 2 3 4 7 1 5 6 0 1 [1] 2 3 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	mode 0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 0 0 0	2:0] to 7	0 0 1 0 0 0 0 0	reg 0 to 7 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 1 0 0 0							
clear incre decr negate test 1s comp add cy sub cy rot rt rot lft arith rt arith rt arith lft Program Stat clr cy clr oflw clr zero clr neg set cy ser oflw set zero set neg no oprn no oprn system rst bus	clr inc dec neg tst com adc sbc ror rol asr asl asl asl stus OPS clc clv clz cln sec sec sev sez sen	52 b b b b b b b b b b c 0 0 0 0 0	Constant  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	typ		0 2 3 4 7 1 5 6 0 1 [1] 2 3 2 2 2 2 2 2 2 2 2 2 2 2	mode 0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 0 1 0	2:0] to 7	0 0 1 0 0 0 0 0	reg 0 to 7 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 1 0 0 0		FINCE			te instr wit		

INSTR BITS	mnemoni	15	14	13 12	11	10	9	8	7	6	5	4	3	2 1	0					
emult	trap	1	14	1	11		<b>9</b> )	3	4	0	,	X	3	x	U	exception SINC	GLE OP, vector - 3	4 SOP hyte inc	tr with tvn=∩	
io trap	iot	0		0			)		0			0		4		vector - 20	JEE OI , VECTOI - 3	,, JOI DYLE IIIS	a with typ-0	
ex io trap	iox	0		0			)		0			0		3		vector - 14				
intr retrn		0		0			)		0			0		2		vector - 14				
intr retrn	rti	U		U			,		U			U		2						
			1		1			-			1					1				

INSTR BITS	mnemo	ni 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0				
			-																	
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INSTR BITS		mnomoni	15	1/1	12	12	11	10	0	0	7	6		Λ	2	2	1 0				
INSTR DITS	) [	memoni	15	14	15	12	- 11	10	9	0	,	0	5	4	3	2	1 0				

INSTR BITS		mnomoni	15	1/1	12	12	11	10	0	0	7	6		Λ	2	2	1 0				
INSTR DITS	) [	memoni	15	14	15	12	- 11	10	9	0	,	0	5	4	3	2	1 0				

INSTR BITS	mnemon	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0				
			1																	

INSTR BITS		mnomoni	15	1/1	12	12	11	10	0	0	7	6		Λ	2	2	1 0				
INSTR DITS	) [	memoni	15	14	15	12	- 11	10	9	0	,	0	5	4	3	2	1 0				

INSTR BITS	mnemo	ni 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0				
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INSTR BITS		mnomoni	15	1/1	12	12	11	10	0	0	7	6		Λ	2	2	1 0				
INSTR DITS	) [	memoni	15	14	15	12	- 11	10	9	0	,	0	5	4	3	2	1 0				

INSTR BITS	mnemo	ni 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0				
			-																	
			-																	
			-																	

INSTR BITS		mnomoni	15	1/1	12	12	11	10	0	0	7	6		Λ	2	2	1 0				
INSTR DITS	) [	memoni	15	14	15	12	- 11	10	9	0	,	0	5	4	3	2	1 0				

INSTR BITS	mnemo	ni 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0				
			-																	
			-																	
			-																	
			-																	

INSTR BITS	mnomon	15	1/	12	12	11	10	0	0	7	6	-	Λ	2	2	1 0				
INSTR DITS	milemon	15	14	15	12	11	10	9	0	,	0	5	4	3	2	1 0				
			1																	
			1																	
			-																	
			1																	

INSTR BITS	mnemo	ni 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0				

INSTR BITS	mnemo	ni 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0				

INSTR BITS	mnemo	ni 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0				

INSTR BITS	mnemoni	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
																	_			

[1] shashwat: typo in specification document given as 1063 for byte rotate left