

Talaria TWO™

Ultra-Low Power Wi-Fi 802.11 b/g/n

BLE 5.0 Plus Advanced Features & Long-Range

Arm Cortex-M3 MCU

Hardware Design Guide

Release: 12-15-2021

Applicable Product Numbers:

INP1010, INP1011, INP1012, INP1013, INP1014, INP1015

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Revision History

Version	Date	Comments
1.0	09-08-2020	First version
2.0	11-19-2021	Updated PC-based Programming to include details about working with a custom application board
2.1	12-15-2021	Updated the programming pin-out details of PC-based Programming

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3 Terms & Definitions

ADC	Analog to Digital Convertor
CTS	Clear To Send
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit
I2S	Integrated Inter-IC Sound Bus
PWM	Pulse Width Modulation
RTS	Request To Send
RXD	Receive Data
SPI	Serial Peripheral Interface
TXD	Transmit Data
UART	Universal Asynchronous Receiver-Transmitter

4 Introduction

This document provides the hardware design guidelines for all Talaria TWO family of modules - INP1010/INP1011/INP1012/INP1013/INP1014/INP1015.

Module	Module Description
INP1010	Module with integrated PCB antenna
INP1011	Module with u.fl connector for external antenna
INP1012	Mini module with RF PIN for external antenna
INP1013	Module with ceramic antenna
INP1014	Mini module with integrated PCB antenna
INP1015	Mini module with u.fl connector for external antenna

Table 1: Talaria TWO modules overview

For module images, mechanical dimensions, footprint, and PIN out, refer the datasheet. The scope of this document is to provide hardware design guidelines for the modules. The design guidelines can be broadly categorized into the following sections:

1. Power supply
2. Reset
3. Peripheral interfacing
4. Production programming
5. RF/Antenna section

The Power supply, Reset & Peripheral interfacing remain same for all variations of the Talaria TWO module family.

5 Power Supply to the module

The input voltage source V_3.3V should be powered with a 3.3V +/- 10% tightly regulated power supply for the Talaria TWO module. The power supply source should be able to supply 300mA peak current, and considering other components on the board, a suitable DC-DC regulator should be chosen.

It is important to have decoupling capacitors placed close to the modules power pins VCC and GND as depicted in the Figure 1.

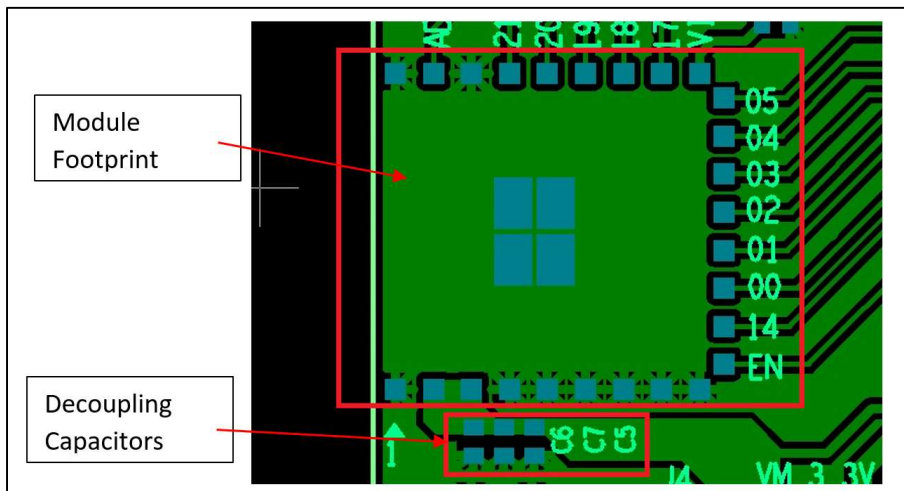


Figure 1: Decoupling Capacitors on VCC pins 2 and 3 VCC and GND pins 1 and 4

6 Reset

This pin is used to reset the module. Low on this pin puts the module in a reset stage and high on this pin releases the module from reset. During the reset stage all the GPIOs must be low or in an undriven state. EN_CHIP/RST must be held below 0.6V to reset device.

Figure 2 depicts the power up sequence for Talaria TWO.

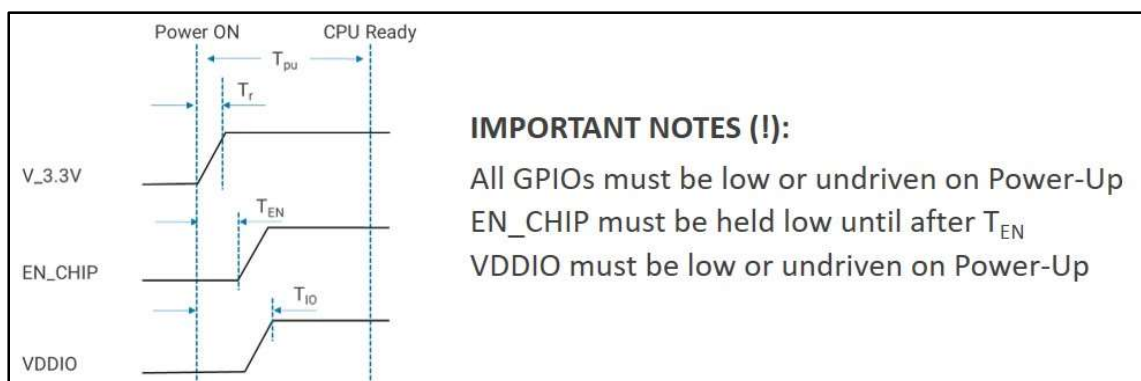


Figure 2: Power-up sequence

Figure 3 depicts the suggested reset circuit which can be used in the application boards. This reset circuit gives the module sufficient time delay to settle down after power-up or after a reset.

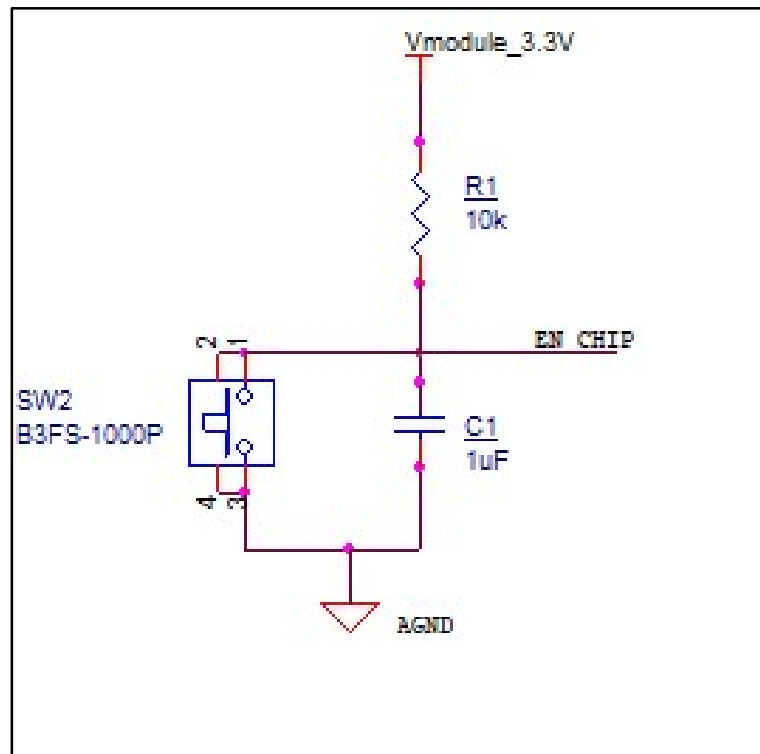


Figure 3: Reset circuit

7 Module peripherals

Talaria TWO modules have a rich set of peripherals in a compact formfactor with UART, SPI, ADC, PWM I2C, I2S and multiple GPIO's. It also has a JATG interface which can be used for extensive debugging. Peripherals are multiplexed with GPIO's, which can be selected through software.

7.1 UART Interface

There is only one UART interface available on Talaria TWO modules available on the pins GPIO1 - TXD and GPIO2 - RXD by default on power up. The other GPIOs of the module can also be configured to work as a UART. UART flow control pins RTS and CTS are optional and can be configured to any of the GPIO pins. UART interface can be used as a host interface through which a microcontroller/processor can send and receive commands from the module.

Module supports standard baudrates starting from 300 to 2560000, 921600 being the default baudrate.

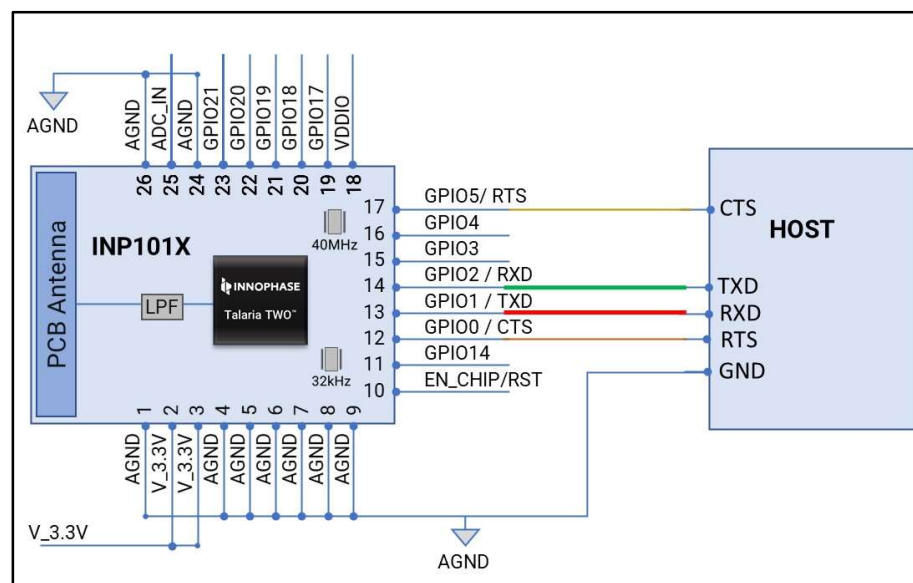


Figure 4: Host with UART Interface

Interface	Signal	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO14	GPIO17	GPIO18 ²	GPIO19	GPIO20	GPIO21
UART	RXD			●									
	TXD		●										
	CTS												
	RTS												
Console	TX								●				

Table 2: UART PINS

- : Default Power-up GPIO
- : Function Supported on GPIO
- : Required for factory production firmware loading

7.2 Console UART

Console UART TXD is a unidirectional pin available on GPIO 17 by default. Apart from the regular UART, the console UART TXD pin is only a transmit pin which can give out debug messages from the module. This pin works at a very high baudrate of 2457600. It is important to have this pin available on a header for debug purpose.

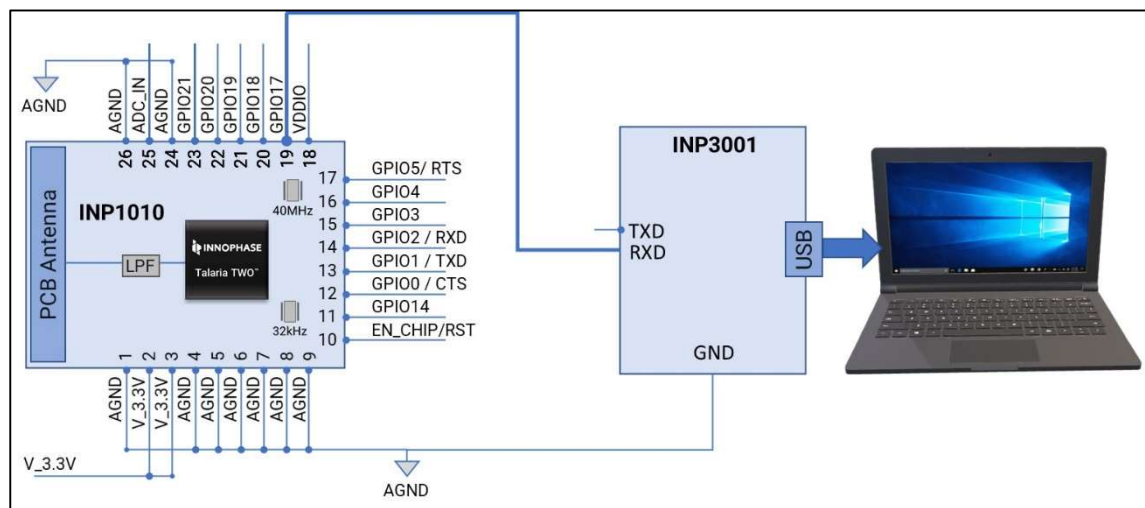


Figure 5: Console for debug messages

Layout Considerations:

1. Let the RXD and TXD pass side-by-side and make the length as short as possible.
2. Avoid routing through multiple layers.

7.3 SPI Slave Interface

There is one SPI slave available on Talaria TWO module. SPI slave pins are non-configurable, and are available only on GPIO0 - CLK, GPIO1 - MOSI, GPIO2 - MISO and GPIO5 - CS. For SPI slave, the maximum SPI CLK supported is 25Mhz.

SPI slave specifications	Details
Maximum Clock Frequency	25MHz
Clock Polarity and Phase Modes Supported	Mode 0 (CPOL=0, CPHA=0) Mode 3 (CPOL=1, CPHA=1)
Data In/Out Sequence	MSB First
Other Features	Dual SPI Mode Capable Read Status Reset

Table 3: SPI slave specifications

SPI slave is generally used to connect the module to a host microcontroller/processor. Host will act as master to send commands and receive response to control the module.

Interface	Signal	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO14	GPIO17	GPIO18 ²	GPIO19	GPIO20	GPIO21
SPI Slave	CLK	●											
	CS						●						
	MOSI		●										
	MISO			●									

Table 4: SPI slave pin-outs

- : Default power-up GPIO
- : Function supported on GPIO

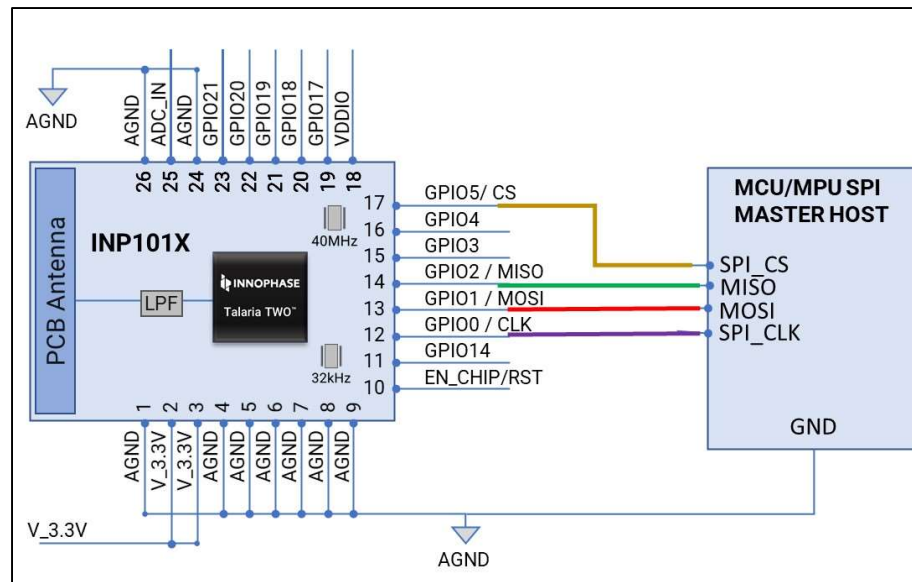


Figure 6: MCU/MPU SPI Master Host

Layout Considerations:

1. Keep all the SPI traces close to each other.
2. All the SPI lines should be length matched.
3. Have a constant impedance across the SPI traces, run a ground plane in the layers beneath the SPI lines to have consistency in impedance throughout the trace.
4. Avoid routing through multiple layers.
5. Keep the length of the SPI lines as short as possible and without vias in between.

7.4 GPIO

Talaria TWO has twelve GPIO's available. All the GPIOs are default pulled high internally with 51KΩ resistor on power-up except for GPIO 18 which is a 51KΩ pull down.

All the GPIO must be pulled low or must be undriven on power-up. Each GPIO can drive with a maximum current of 10mA and it can sink current up to 9mA. Reference voltage for all the GPIOs is established from VDDIO voltage internally.

7.5 I2C Interface

There is one I2C module available on Talaria TWO module which can act as a slave as well as a master. Any of the pins except GPIO17 and GPIO18 can be configured for I2C. There are no default GPIOs for I2C. Internally, the SCL and SDA lines have a 51K pull up.

Interface	Signal	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO14	GPIO17	GPIO18 ²	GPIO19	GPIO20	GPIO21
I2C	SCL												
	SDA												

Table 5: GPIO for I2C

I2C Specification	Details
Data Rates	100Kbps, 400Kbps, 1Mbps
Address Modes	7-bit, 10-bit
Other Features	Send STOP at End NOSTART Before Msg IGNORE NAK From Slave

Table 6: I2C Specification

7.6 ADC Interface

There is one external ADC module available on Talaria TWO module which is a 10Bit SAR ADC with dedicated PIN number 25 on the module. ADC is not multiplexed with any of the other functionalities. The voltage level it can support is a maximum of 1V. Input voltage to the pin should not exceed beyond 1V. Through software, the sampling rate can be adjusted as per the requirement.

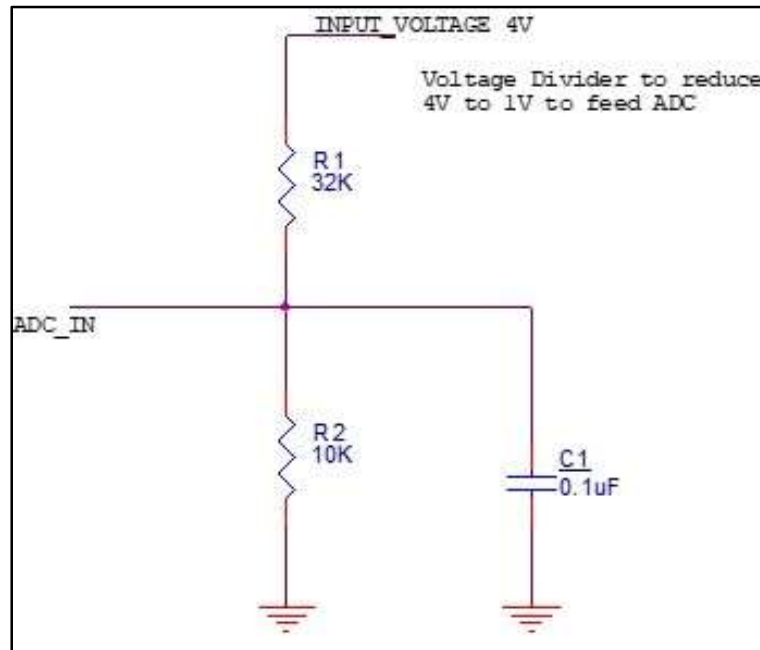


Figure 7: ADC Signal Conditioning

7.7 PWM Interface

There are four PWMs available on Talaria TWO modules which can generate a maximum frequency of 160MHz. PWM is multiplexed with other functions on GPIOs. Through software, the pin must be initialized to work as PWM. Frequency and duty cycle of the PWM can be set through software registers.

PWM Specification	Details
Base Frequency	160MHz
Duty Rate Range	0% to 100%
Pulse Alignment	Left Aligned
Other	Audio Capable

Table 7: PWM Specifications

7.8 JTAG/SWD

Compliant with ARM JTAG/SWD standards for debug purpose.

JATG pins are fixed on the pins mentioned in Table 8. They are multiplexed with other peripherals with highest priority given to the functions which are set as default on power-up.

Interface	Signal	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO14	GPIO17	GPIO18 ²	GPIO19	GPIO20	GPIO21
JTAG/SWD	TCK/ SWCLK									●			
	TMS / SWDIO										●		
	TDI											●	
	TDO / SWO												●

Table 8: JTAG/SWD pin-out

8 Production Programming

Production programming to Talaria TWO module can be done in three ways. Following are the descriptions for the same.

8.1 PC-based Programming

To perform PC-based programming, the module must connect to the PC with 6 pins listed in Table 9.

PINS	PIN DETAILS
1	GND
2	EN_CHIP/RST
3	TXD
4	RXD
5	GPIO17/CONSOLE
6	GND

Table 9: Programming Pin-out

The block diagram for the same is discussed in Figure 8 and the schematics can be extracted from the evaluation board schematics listed on our website (<https://innophaseinc.com/wp-content/uploads/modules/INP301x-EVB-A-Schematics.pdf>.)

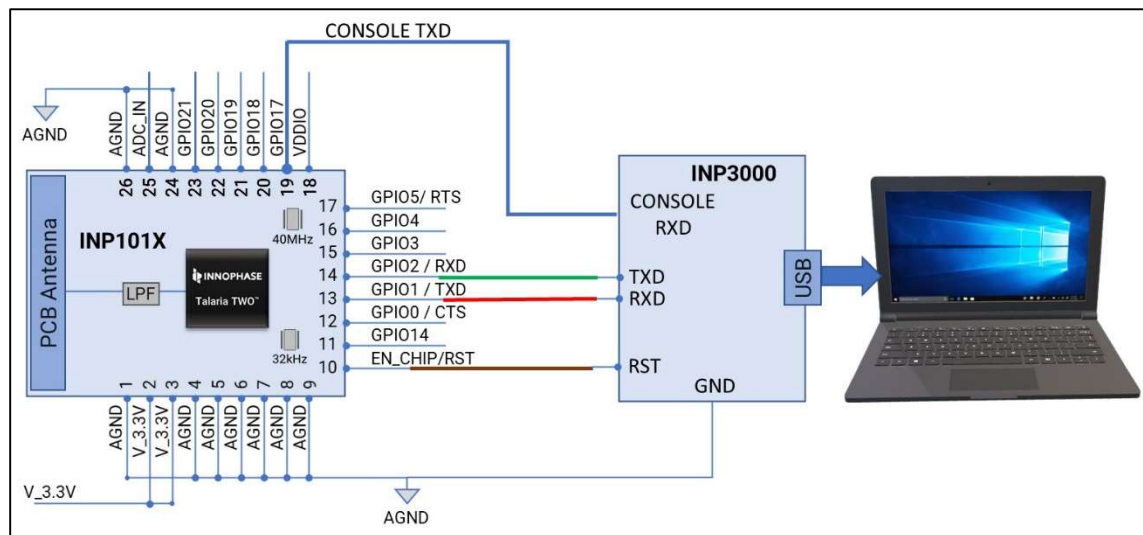


Figure 8: PC-based Programming

In case of a custom application board, it is suggested to use the INP3000 programmer board to program the module. The INP3000 comes with a Molex cable part number 151340601 (PicoBlade Female-to-PicoBlade Female Off-the-Shelf (OTS) Cable Assembly). The mating connector for it is

532610671 Pitch 1.25mm, (PicoBlade PCB Header, Single Row, Right-Angle, Surface mount, Tin (Sn) Plating, Friction Lock, 6 Circuits).

The schematics and the user guide for the programmer board INP3000 is available in the document section of the customer portal on the InnoPhase website. To get access to the customer portal, contact InnoPhase sales team: sales@innophaseinc.com.



Figure 9: Molex cable part number 151340601

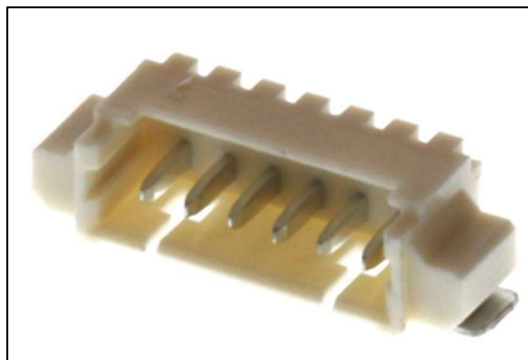


Figure 10: mating connector part number 532610671

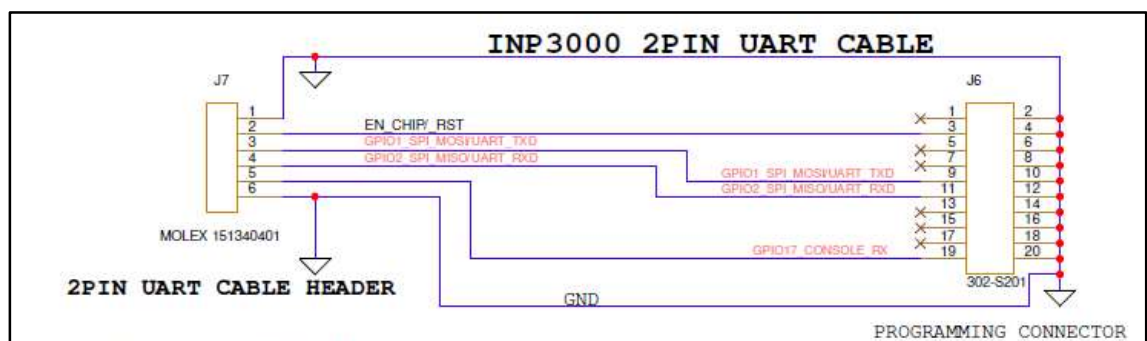


Figure 11: Programming Cable Pin outs J7

8.2 Host-based Programming

The Talaria TWO module when connected to the host microcontroller/processor can also perform firmware upgrade. Host Interface SPI/UART block diagram is as shown in Figure 12.

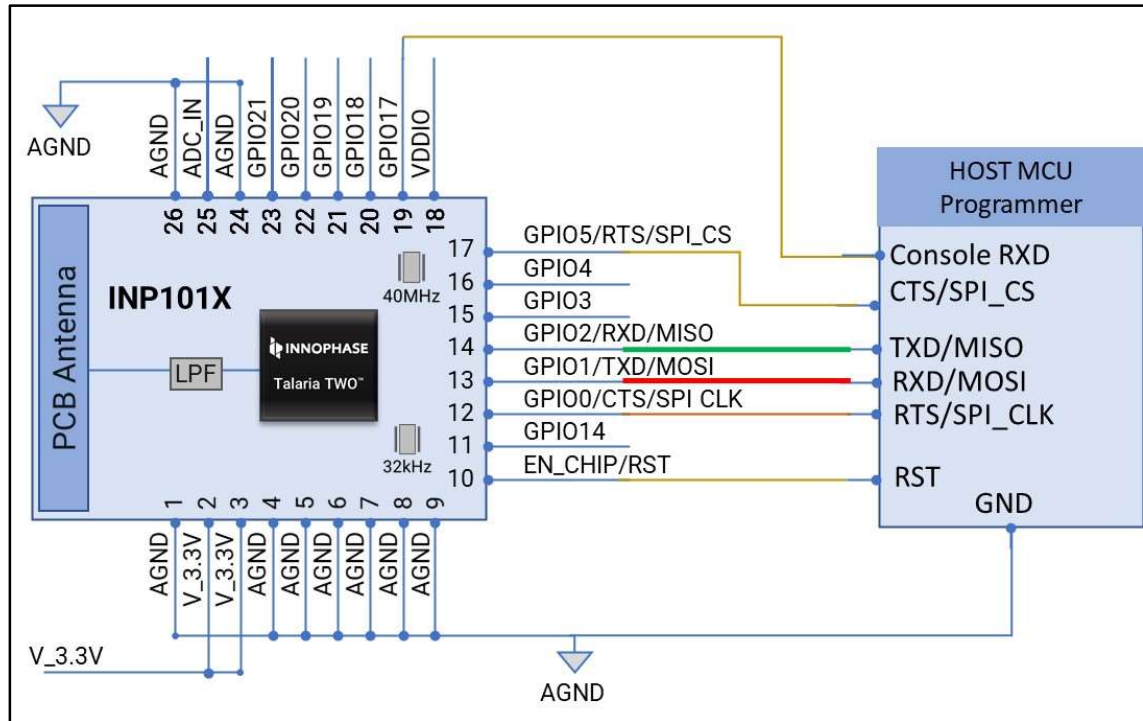


Figure 12: Host Programming UART/SPI Slave

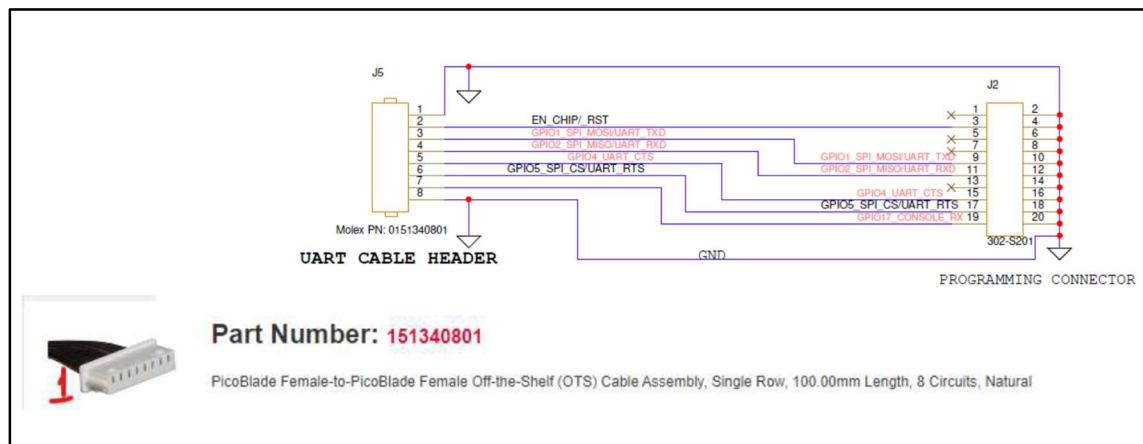


Figure 13: Evaluation board connector details

The cable part number: 161340801 as shown in Figure 13 will be provided for programming. The mating connector for the same with part number: 532610871 is as shown in Figure 14. This connector can be used on the factory setup application board along with the factory loader software application to program the modules.

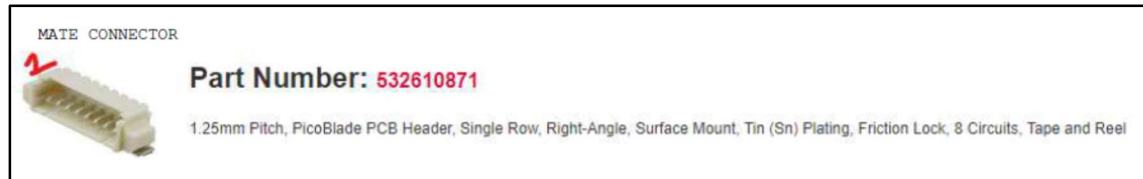


Figure 14: Programming Connector

Care must be taken to isolate the programming header from the host communication MCU/MPU header by adding jumper options on the application board.

8.3 Programming over the Air

Irrespective of the hardware interface, the host module can perform FOTA firmware upgrade over the air. The FOTA application note is available as part of the SDK release apps (sdk_x.y/apps/fota/doc/Application_for_using_Firmware_Over-The-Air-Upgrade.pdf).

Note: x.y in sdk_x.y refers to the SDK release.

9 Hibernate Mode

In the Hibernate mode, the EN_CHIP/RST pin must be held low (less than 0.6V) and the VDD must be ON (VDD 3V). In this mode, the SRAM memory is not retained and the RTC will be OFF. Host connected to this pin can put the module in Hibernate mode by a GPIO to save power. When released from Hibernate mode, the module will work with a default software application stored in the Flash. In this mode, the module consumes less than 1uA.

10 Module Placement Guidelines – INP1010/INP1013/INP1014

Talaria TWO family of modules should be placed at the edge of the application PCB for better RF performance as indicated in Figure 15. INP1010/13/14 modules have antenna on them which make it easy for integrating on application PCB.

In the above case, make sure that the antenna portion is outside of the application PCB as indicated in Figure 16.

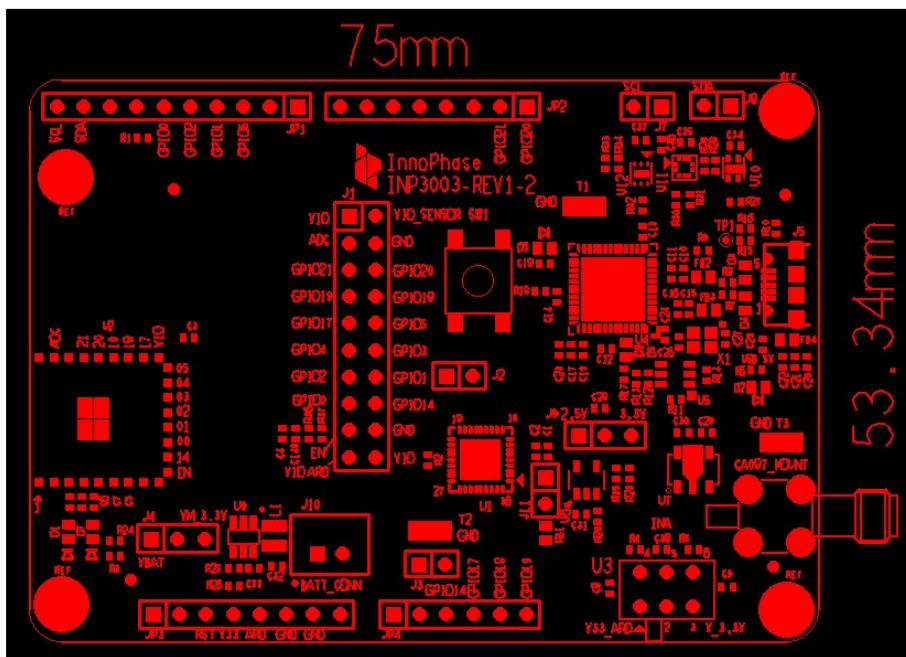


Figure 15: Module placement

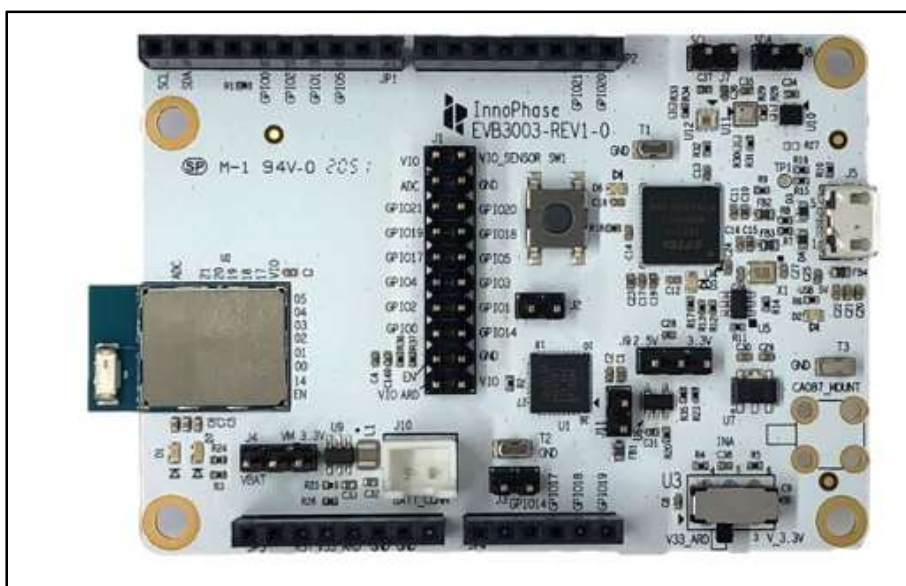


Figure 16: INP1013 Module with antenna portion outside application PCB

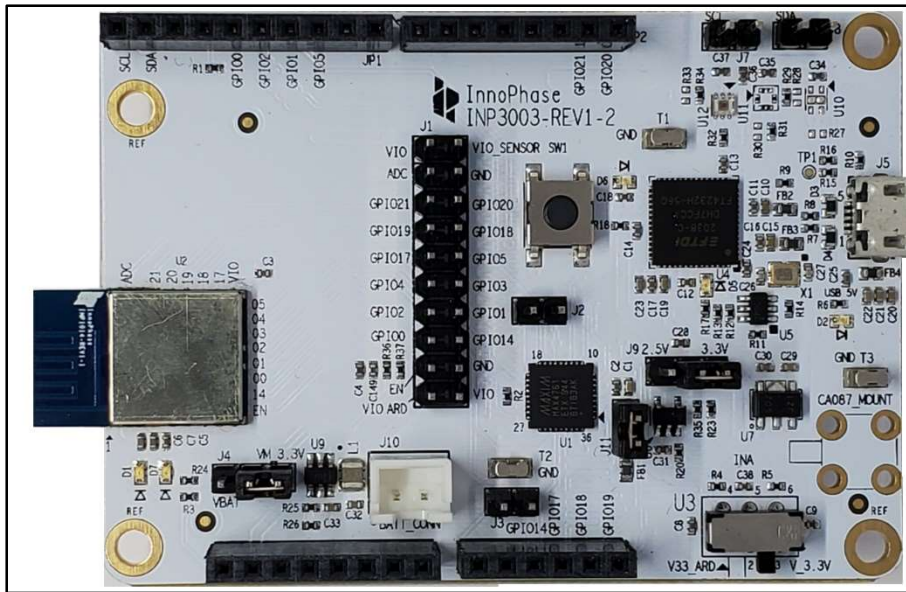


Figure 17: INP1043 Module with antenna portion outside application PCB

11 Module Placement and Antenna placement Guidelines – 1012

Talaria TWO module INP1012 does not have antenna on the module. Following are the guidelines to be followed to place the antenna on the application PCB.

1. The RFIO(Ant) pin # 30 on INP1012 has a feed point for antenna connection.
2. Feed Line coming out of the module should be 50Ω impedance matched as shown in Figure 18 and Figure 19 indicates the connector placement for the antenna.
3. Follow the clearance area specification provided by the antenna manufacturer.
4. Comply to the minimum ground plan requirement provided by the antenna manufacturer.
5. If a connector is placed on the application PCB, make sure it is 50Ω Ohm impedance connector.

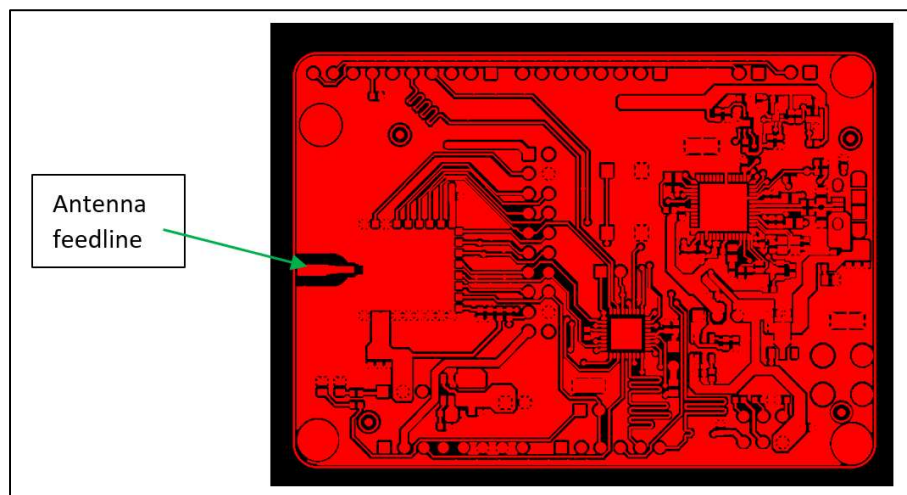


Figure 18: Antenna placement diagram

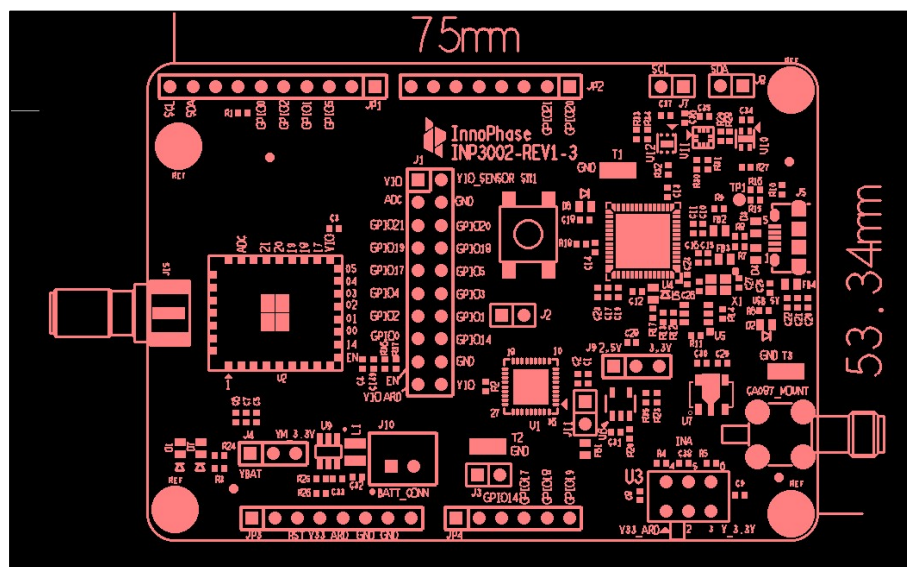


Figure 19: INP1012 module antenna connector placement

12 Module Placement Guidelines – 1011/15

INP1011 and INP1015 has u.fl RF connector on the module which makes it easy to plug in the external antenna with a mating u.fl connector. Antenna placement option indicated in the evaluation board in Figure 20. In case of u.fl select the antenna with the specifications mentioned in the datasheet to leverage the FCC certifications.

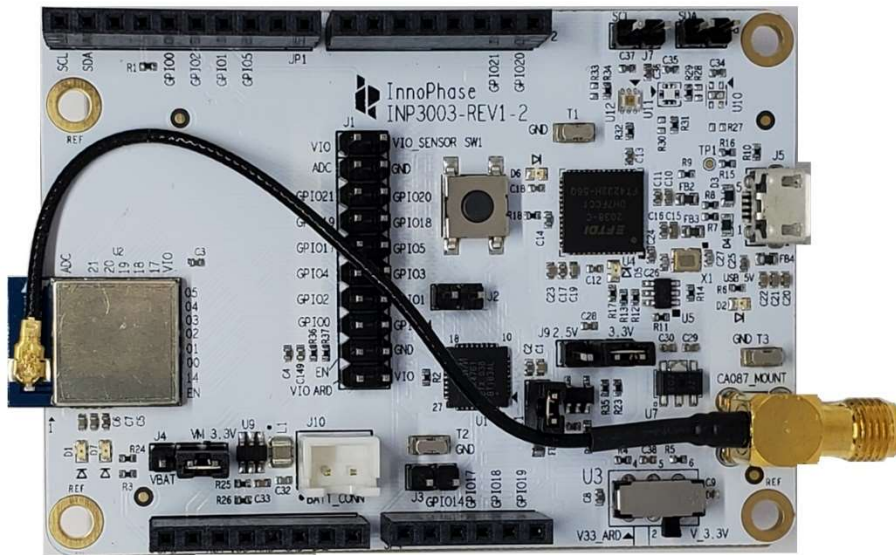


Figure 20: u.fl to SMA connector for INP1011/15

13 Thermal Ground pad

Talaria TWO modules have thermal ground pads placed in the middle of the footprint. These modules should be grounded through four vias in each PAD. The size of each pad is 1.4mm x 1.9mm. The size of the via is 12mils. Figure 21 shows the layout and via pattern for thermal conduction.

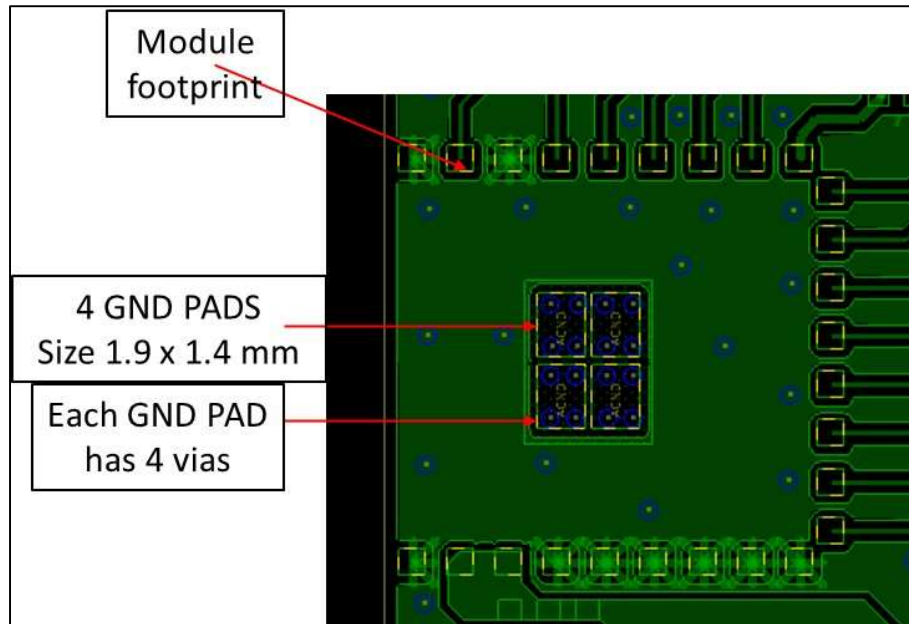


Figure 21: Thermal ground pads

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