Ex./CSE/T/213/18/2013

BCSE Examination, 2013

(2nd Year, 1st Semester)

COMPUTER ORGANISATION

Full Marks : 100 Time : Three Hours

The figures in the margin indicate full marks.

Answer *any five* questions.

1. (a) An B-bit computer has 16 bit address bus. The first 15 lines of the address bus are used to select a location within a bank of 32KBytes of memory. The high order bit of the address is used to select a register which can receive content from data bus. Detail the configuration so that memory capacity of the system would be 256K bytes using eight 32K Bytes banks.

   (b) A computer has 16 registers an ALU with 32 operations and a shifter with 8 operations, all connected to a common bus system.

   (i) Formulate a control word for a micro-operaton.

   (ii) Specify the no of bits in each field of the control word and suggest a general encoding scheme.

   (iii) Show the bits of the control word that specify the micro-operation $R_4 \rightarrow R_5 + R_6$ 8+12

[*Turn over*]

2. (a) What are the advantage of using normalised mantissa and biased exponents in floating point representation ? Discuss single precision and double precision formats for IEEE standard floating point representation.

(b) For each of the IEEE single-precision representation, explain what type of number (normalized, denormalized, infinity, zero or NaN) they represent. For normalized ones give the corresponding decimal representation.

10+10

(i) 0111 1111 1000 1111 0000 1111 0000 0000

(ii) 0000 0000 0000 0000 0000 0000 0000 0000

(iii) 0100 0010 0100 0000 0000 0000 0000 0000

(iv) 1000 0000 0100 0000 0000 0000 0000 0000

(v) 1111 1111 1000 0000 0000 0000 0000 0000

3. (a) The memory stack in a 16-bit computer contains 5A14. The stack pointer contains 3A56. A two word call subroutine instruction. is located at memory address 013E followed by the branch address 67AE at memory address 013F. What are the contents of PC, SP and the memory stack ?

(i) Before the CALL instruction is executed

(ii) After the CALL instruction is executed

(iii) After the RETURN from subroutine.

(iv) After the second RETURN from the subroutine if it be immediately called after the first RETURN.

[*Turn over*]

(b) How associative memory differ from conventional memory ? Explain the organization of associative memory with a neat diagram and describe the match logic used in such memory. 10+10

4. Consider the five stage pipelined processor specified by the following reservation table.

	1	2	3	4	5	6
S_1	×					×
S_2		×			×	
S_3			×			
S_4				×		
S_5		×				

(a) List the set of forbidden latencies and the collision vector.

(b) Draw the state transition diagram.

(c) List of simple cycles.

(d) List of greedy cycles.

(e) What is MAL

(f) Minimum allowed constant cycle.

(g) Maximum throughout of the pipeline.

(h) Is the obtained MAL is the lower bound ? 20

[*Turn over*]

5. Consider the following algorithm :

Declare registers A(8), B(8), C(8)

Start : B←data
A←00
Loop : A←A + B
B←B – 1
If B ≠ 0 go to Loop
C←A
Half : Go to Half

Design a hardware controller using D flip flops and also microprogram control memory that can implement the above algorithm. 10+10

6. (a) Draw the CSA organisation to add 8 signed nos. of 5 bit each having CLA at the last stage.

Count the minimum no. of full adders, basic adden and CLCs required for the above circuit.

Also calculate the minimum gate delay in the above addition process.

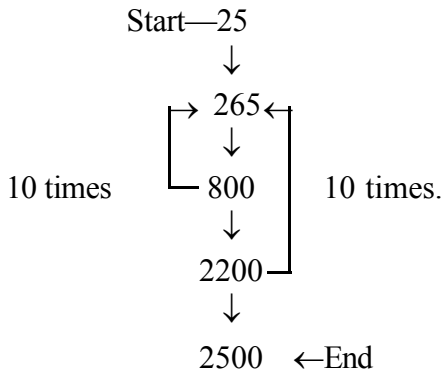
(b) Give the schematic diagram to interface two 16K byte RAM modules and four 8K bytes ROM modules with a CPU. Show the complete decoding scheme and indicate the physical address space occupied by each chip. 10+10

[*Turn over*]

7. (a) A typical computer system has 32K main memory and 2K fully associative cache memory. The cache block size is 128 bytes.

(i) How many bits are there in the TAG field ?

(ii) Find the successful hit ratio for the following program structure where LRU replacement policy in used. The program starts from address 25 and continues upto address 2500 with two embedded loops.



(b) Can there be any situation where virtual memory size is smaller than main memory size ? Justify your answer.

15+5

8. Write short notes on (***any two***) : 10×2

(i) Virtual memory

(ii) Series parallel adder.

(iii) Non-restoring type division

(iv) Nano-programming.