7. a) Consider a 20-bit floating-point number in a format with 7-bit exponent and 12-bit normalised fractional mantissa. The base of the scale factor is 4 and the exponent is represented in excess – 64 format.

Find the values of (A + B) and (A – B) where

A = 0 1000010 111111110011

and B = 0 0111110 101010101011

which are expressed in above format. Give the answers in normalised form. You are advised to use rounding method for truncation.

b) Draw the combinational circuit for paper and pencil method of multiplication for two 5-bit signed numbers.

10+10=20

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INTER COMPUTER SC. & ENGG. EXAMINATION, 2008

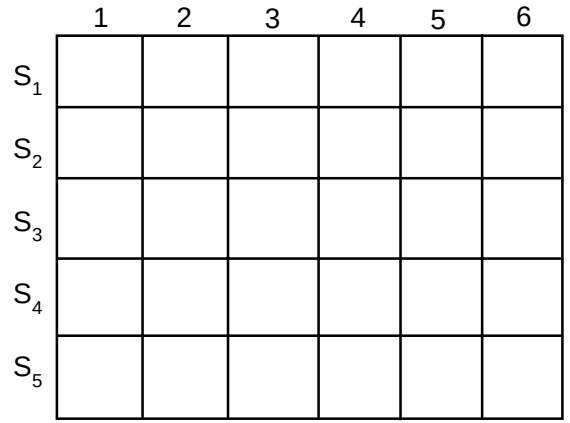
(1st Semester)

COMPUTER ORGANIZATION

Time : Three hours Full Marks : 100

*Answer any **five** questions.*

1. Consider the five stage pipelined processor specified by the following reservation table :



a) List the set of for bidden latencies and the collision vector.

b) Draw the state transition diagram.

c) List all the simple cycles from the state diagram.

d) Identify the greedy cycles among the simple cycles.

e) What is minimum average latency ?

f) What is minimum allowed constant cycle in using this pipeline.

g) What will be the maximum throughput of this pipeline ?

h) Is the MAL obtained in (e) is the lower bound ? If not how do modify the reservation table to achieve lowest MAL ? 20

2. a) Design a combinational circuit for a BCD adder showing properly the carry-in and carry-out terminals.

b) Explain Booth's Algorithm for multiplication of signed binary numbers with the help of an example

A = 0 1 0 0 1 1 0

B = 1 0 1 1 0 1 1

Also explain bit pair speed-up technique applicable to Booth's algorithm. 10+10

3. a) Draw the CSA organisation to add 8 signed numbers of 5 bit each have CLA at the last stage.

Count the minimum no. of full adder and CLC required for the circuit.

Calculate the minimum gate delay in the addition process.

Design a hardwired controller using D flop flops and also microprogram controller that will implement the above algorithm. 10+10=20

6. a) Design an ALU with three control lines C_0, C_1 and C_2 and one carry input line, two 8-bit binary input A and B are to perform the following operations (Show the first three stages and the last stage of ALU only):

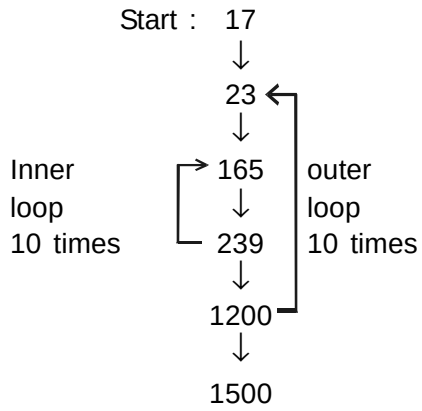
C_2	C_1	C_0	**Operations**
0	0	0	A + B
0	0	1	A – B
0	1	0	A + 1
0	1	1	A – 1
1	0	0	A AND B
1	0	1	A OR B
1	1	0	A XOR B
1	1	1	Complement A

b) Write program to evaluate the statement

X = (A + B * C) / D * E – H

Using :

(i) 3-address instruction (ii) 2-address instruction (iii) 1-address instruction (iv) 0-address instruction. 12+8=20



b) In a certain computer system with cache memory 750 μsec is the main memory access time for cache miss and 50 μsec is the access time for a cache hit. Find the percentage decrease in the effective access time if the hit ratio is increased from 80% to 90%.

15+5=20

5. Consider the following algorithm :

Declare registers A(8), B(8), C(8) :

Start : B ← data
A ← 00
Loop : A ← A + B
B ← B – I
If B ≠ 0 then goto Loop.
C ← A
Halt : Goto Halt

b) A table comprising 8 micro instructions is given below :

I_0	C_1	C_2	C_3	C_4	C_5	C_6
I_1	C_1	C_3	C_4	C_6		
I_2	C_2	C_5	C_6			
I_3	C_4	C_5	C_8			
I_4	C_7	C_8				
I_5	C_1	C_8	C_9			
I_6	C_3	C_4	C_8			
I_7	C_1	C_2	C_9			

(i) Propose an optimal hybrid micro instruction format with minimal no. of bits.

(ii) Propose nanoprogram for the above. 10+10

4. a) Main memory size is 64 k bytes.

Cache memory size is 1 k byte

Block size is 64 bytes

Block-set-associative mapping with 4-blocks per set is used.

(i) How many bits are there in each of TAG, SET and OFFSET fields?

(ii) Find successfull hit ratio for the following program structure where LRU replacement is used.