7. a) Briefly explain the two 'write' policies, write through and write back for cache design. What are the advantages and disadvantages of both the mathods?

   b) Explain the difference between full associative and direct mapped cache mapping approaches.

   c) Given the following, determine size of the sub-fields (in bits) in the address for Direct mapping, Associative mapping and Set-Associative mapping cache schemes :
   * 256 MB main memory and IMB cache memory.
   * Block size is 128 bytes.
   * There are 8 blocks in a cache set. 7+7+6

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BACHELOR OF COMPUTER Sc. ENGG. EXAMINATION, 2009

(2nd Year, 1st Semester, Supplementary)

COMPUTER ORGANIZATION

Time : Three hours Full Marks : 100

Answer any ***five*** questions.

1. a) Describe Booth's bit pair algorithm for binary multiplication and illustrate the algorithm with the example of multiplication of -23 and +29.

   b) Describe the nonrestoring type binary division algorithm and the corresponding sequential circuit for implementing it. Next verify the circuit with the example of 19 divided by 6. 10+10

2. a) Draw the CSA organisation to add 8 signed nos. of 4 bit each having ripple carry adder at the last stage. Also count the number of full adders required and calculate the gate delay in the addition process.

   b) The page reference pattern of a program is as follows:
   1, 2, 3, 4, 1, 5, 2, 3, 6, 5, 4, 1, 6, 2, 5, 4
   Which of the page replacement policies FIFO, LRU and LIFO is most suitable with cache mamory capacity 4 pages. 10+10

3. a) Consider a 16 - bit floating point number with a 6 - bit exponent (excess 31 format) and a 9 - bit normalised

mantissa. The base of the scale factor in 2. Find A + B and represent in the above format after rounding using truncation method.

A = 0	100001	111101111
B = 0	011111	011011011

(Consider that an implicit 1 is there to the left of the binary point as in IEEE format.)

b) The interface for a static memory costs Rs. 10/= compared to Rs. 50/= for a dynamic memory and if static memory costs Rs. 0.0002 per bit and dynamic memory costs Rs. 0.0001 per bit, determine how many bits must be in a memory to make dynamic memory less expensive. 15+5

4. a) Consider the following pipeline reservation table

	1	2	3	4
S_1	x			x
S_2		x		
S_3			x	

(i) What are the forbidden latencies?

(ii) Draw the state transition diagram.

(iii) List all simple cycles and greedy cycles.

(iv) Determine the optimal constant latency cycle and the minimal average latency.

(v) What will be the throughput if the clock period be 20 m sec.

b) Write short notes on ***any two*** : 10+5x2

i) Non restoring division

ii) Carry look - ahead addition

iii) Virtual memory

iv) Direct memory access

5. a) (i) How associative memory differ from conventional memory?

(ii) Explain the organization of associative memory with a neat diagram.

(iii) Describe the match logic used in associative memory.

b) Using 4 - bit parallel adder module design a single digit BCD subtractor circuit. Indicate borrow in and borrow out properly for the circuit. 10+10

6. a) In a two level virtual memory $t_{A1}=10^{-9}$ sec and $t_{A2}=10^{-2}$ sec. What must be the hit ratio H in order that access efficiency to be within 90% of its maximum possible value?

b) How are machines classified according to number of address references in instructions. Explain how a high level instruction such as

A = B + C – D * E + F / G

is incorporated in such machines. Hence in each case, comment on the number of instruction and total size of the instructions. 10+10