BACHELOR OF ENGINEERING (COMPUTER SC.) EXAMINATION, 2013

(2nd Year, 1st Semester, Supplementary)

Computer Organisation

Time : Three hours. Full Marks : 100

Answer any ***five*** questions.

1. (a) Design a combinational circuit for a BCD adder showing properly the carry-in and carry-out terminals.

   (b) Explain Booth's Algorithm for multiplication of signed binary numbers with the help of the example.

   A = 0 1 0 0 1 1 0

   B = 1 0 1 1 0 1 1

   Also explain bit-pair speed-up technique applicable to Booth's algorithm. 10+10=20

2. Consider the following algorithm

   Declare registers A(8), B(8), C(8)

   Start : B $\leftarrow$ data

   A $\leftarrow$ 00

   Loop : A $\leftarrow$ A+B

   B $\leftarrow$ B$-$1

   If B $\neq$ 0 goto Loop

   C $\leftarrow$ A

   Halt : Goto Halt

   Design a harwired controller using D flip-flops and also microprogram controller that will implement the above algorithm. 10+10=20

3. (a) Consider a 20-bit floating point number in a format with 7-bit exponent and 12 bit normalised fractional mantissa. The base has scale factor 4 and the exponent in represented in excess 64 format.

Find the values of (A+B) and (A–B) where

A = 0 1000010 111111110011

and B = 0 0111110 101010101011

which are expressed in above format. Give your answers is normalised form in the above format. Use rounding method for trancation.

(b) Draw the combinational circuit for paper and pencil method of multiplication for two 5-bit signed numbers. 10+10=20

4. (a) A computer has 16 registers an ALU with 32 operations and a shifter with 8 operations, all connected to a common bus system.

(i) Formulate a control word for a micro-operation.

(ii) Specify the no. of bits in each field of the control word and suggest a general encoding scheme.

(iii) Show the bits of the control word that specify the micro-operation $R_4 \rightarrow R_5+R_6$

(b) Write program to evaluate the statement

X=(A+B+C) / D * E –H using

(i) 3 address instruction

(ii) 2 address instruction

(iii) 1 address instruction

(iv) 0 address instruction. 10+10=20

5. (a) What are the advantage of using normalised mantissa and biased exponents in floating point representaton? Discuss single precision and double precision formats for IEEE standard floating point representation.

(b) How associative memory differe from conventional memory? Explain the organization of associative memory with a neat diagram and describe the metals logic used in such memory. 10+10=20

6. (a) Draw the CSA organisation to add 8 signed numbers of 5 bit each having CLA at the last stage. Count the minimum no. of full address and CLC required for the circuit.

Calculate the minimum gate delay in the addition process.

(b) Give the schematic diagram to interface two 16K byte RAM modules and two 8K byte ROM modules with a CPU. Show the complete decoding scheme and indicate the physical address spare occupied by each chip as per your design. 10+10=20

7. Write short notes on (any ***two***) : 10x2=20

(a) Virtual memory.

(b) Series Parallel adder.

(c) Pipe line processing.

(d) Non-restoring division.

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