(b) The interface for a static memory costs Rs. 10/- compared to Rs. 50/- for a dynamic memory and if static memory costs Rs. 0.0002 per bit and dynamic memory costs Rs. 0.0001 per bit, determine how many bits must be in a memory module to make dynamic memory less expensive.

(c) The memory stack in a 16-bit computer contains $5A14_H$. The stock pointer contains $3A56_H$. A two word call subroutine instruction is located at memory address $013E_H$. followed by the branch address of $67AE_H$ at memory address $013F_H$. What are the contents of PC, SP and the memory stack?

(i) Before the CALL instruction is executed.

(ii) After the CALL instruction is executed.

(iii) After the RETURN from subroutine

(iv) After the second RETURN from subroutine following the one in part (iii). 5+5+10

7. (a) Describe Booth's modified algorithm and show that just $\frac{N}{2}$ partial products are required to multiply two N bit binary numbers. Illustrate the algorithm with the example of multiplication of +29 and –35.

(b) Draw the schematic diagram for daisy chain polling arrangement in the case of non-vectored interrupt for three devices. 10+10

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Ex/CSE/T/213/12/2007(S)

INTER ENGG. (COMPUTER SCIENCE ENGG.) EXAMINATION, 2007

1st Semester (Supplementary)

COMPUTER ORGANISATION

Time : Three hours Full Marks : 100

Answer any *five* questions.

Different parts of a question are to be answered together.

1. (a) In a virtual memory environment using FIFO for page replacement, it is found that the successful hit ratio is unacceptably low. Comment on each of the following proposals made for increasing the hit ratio :

(i) Decrease the page size

(ii) Increase the main memory size

(iii) Replace FIFO by LRU

(iv) Go for multitasking.

(b) The page reference pattern of a program is as follows :

1, 2, 3, 4, 1, 5, 2, 3, 6, 5, 4, 1, 6, 2, 5, 4

which of the page replacement policies FIFO, LRU and LIFO is most suitable with memory capacity 4 pages?

(c) In a two level virtual memory $t_{A1} = 10^{-3}$ sec and $t_{A2} = 10^{-2}$ sec what must be the hit ratio H in order the access efficiency to be within 80% of its maximum possible value? 8+6+6

2. (a) What is the difference between a subroutine and an interrupt service routine ?

   (b) Design an ALU with three control lines C_0, C_1, and C_2 and one carry input line and two n-bit binary inputs A and B to perform the following operations (show the first two stages).

C_2	C_1	C_0	Operations
0	0	0	A+B
0	0	1	A–B
0	1	0	A+1
0	1	1	A–1
1	0	0	A and B
1	0	1	A or B
1	1	0	A XOR B
1	1	1	Complement A

5+15

3. (a) Consider a 20-bit floating point number in a format with 7-bit exponent and a 12-bit normalised fractional mantissa. The base of the scale factor in 4 and the exponents is represented in excess-64 format

   Find the values of (A+B) and (A–B) where

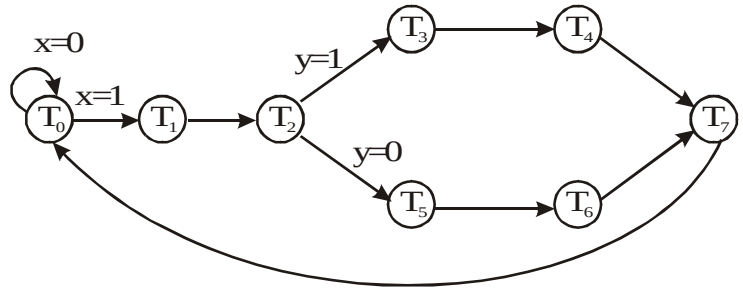
   A = 0 1 0 0 0 0 1 0 1 1 1 1 1 1 1 1 0 0 1 1

   B = 0 0 1 1 1 1 1 0 1 0 1 0 1 0 1 0 1 0 1 1

   which are represented in the above format and give the answers in normalised form. Use rounding method for truncation.

   (b) Draw the CSA organisation to add 9 signed numbers of 4-bit each having ripple carry adder at the last stage. Also calculate the number of gate delays in your addition process. 10+10

4. A control unit has two inputs X and Y and eight-states. The control state diagram is as follows :



   (a) Design the control using eight D flip flops.

   (b) Design the address sequencing part of microprogram control. 10+10

5. Write short note on any *two* of the following : 10×2

   (a) Non-restoring algorithm for binary division.

   (b) Direct memory access.

   (c) Techniques of truncation used for floating point arithmetic.

6. (a) What are the differences between asynchronous and synchronous mode of data transfer.