7. a) Suppose that a 2 KB cache has set-associative mapping. There are 16 sets, each containing 4 blocks. Main memory address size is 32 bits and smallest addressable unit in byte

   i) To what set of the cache in the address $000021BC_{16}$ assigned?

   ii) If the address $000021BC_{16}$ and $FFFF5XYZ_{16}$ are assigned to the same cache set, what values can the address digits XYZ have?

   b) A virtual memory has a block size of 1K words. There are eight secondary blocks and four primary blocks. The associative memory page table contains the following entries :

Secondary Block	Primary Block
0	3
1	1
4	2
6	0

Make a list of virtual addresses (in decimal) that will cause page fault if addressed by CPU. 10+10

Ex/CSE/T/213/18/2012(S)

BACHELOR OF ENGINEERING IN COMPUTER SCIENCE & ENGINEERING EXAMINATION, 2012

(2nd Year, 1st Semester, Supplementary)

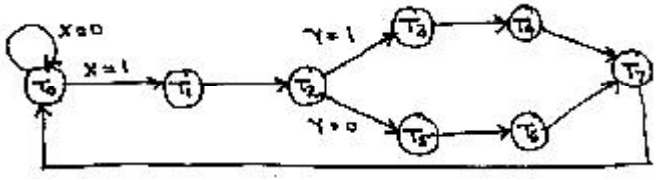
COMPUTER ORGANISATION

Time : Three Hours Full Marks - 100

Attempt any **Five** questions

Answer for a question should start from a new page and all parts of a question to be answered together

1. a) A control unit has two inputs X and Y and eight states. The control state diagram is as follows :

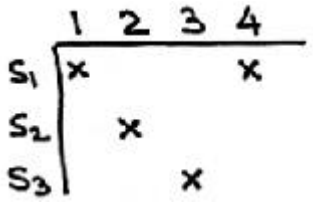


   i) Design the control using eight D flip-flops.

   ii) Design the address sequencing part of microprogram control.

   b) Assume main memory has 4 page frames and initially all page frames are empty. Consider the following order of references 1, 2, 3, 4, 5, 1, 2, 6, 1, 2, 3, 4, 5, 6, 5. Calculate the hit ratio for replacement policy (i) FIFO, (ii) LRU. 6x2+4x2

2. Consider the following pipeline reservation table



i) What are the forbidder latencies?

ii) Draw the state transition diagram.

iii) List all the simple cycles and greedy cycles.

iv) Determine the optimal constant lantenay and MAL. 20

3. a) What are the advantage of using normalised mantissa and biased exponents in the floating point representation of a binary number?

What is the IEEE standard for representing a 32-bit floating point number?

Represent + 1·125 in both single precision and double precision format.

b) For the following expression to evaluate on a stack organised machine write the pseudo machine language program 12+8

$$A * B + A * \left\{ \overline{B * D} + \left(C * E \,/\, \left(A * F \right) \right) \right\}$$

4. a) Design neatly the serial-parallel adder organisation to add 8-signed numbers of 4-bits each. Consider the delay with full adder be 100 m sec and that for shift register be 20 m sec. Find the maximum speed of addition.

b) How associative memory differs from conventional memory?

Explain the organisation of associative memory with a neat diagram.

Describe the match logic used in associative memory. 10+10

5. Write short note on any **two** :

i) Carry-look-ahead addition

ii) Virtual memory

iii) Replacement algorithms

iv) Nano programming 10x2

6. a) Describe Booth's bit pair algorithm for binary multiplication and illustrate the algorithm with the example of multiplication of –39 and +26.

b) Describe the non-restoring type binary division algorithm and the corresponding sequential circuit for implementing it. Next verify your circuit with the example of 19 divided by 5. 10+10