Ex/CSE/T/213/18/2012

BACHELOR OF COMPUTER SCIENCE ENGINEERING EXAMINATION, 2012

(2nd Year, 1st Semester)

COMPUTER ORGANISATION

Time : Three Hours Full Marks - 100

Answer any **Five** questions.

All parts of a question are to be answered collectively

1. a) Consider the five stage pipelined processor specified by the following reservation table :

	1	2	3	4	5	6
S_1	X					X
S_2		X			X	
S_3			X			
S_4				X		
S_5		X				X

i) What is the collision vector?

ii) Draw the state transition diagram.

iii) List all greedy cycles.

iv) What is minimum average latency?

v) What is minimum allowed constant cycle?

[Turn over

b) A hierarchical Cache-Main memory system has following specifications :

Cache access time of 50 nSec.

Main memory access time of 500 nSec.

80% of memory request are for read

Hit ratio of 0.9 for read access and overall hit ratio is 0.88.

Store and forward scheme is employed.

Estimate :

i) Average access time of the system considering 100% memory read cycle.

ii) Average access time of the system considering both read and write requests.

iii) Find the hit ratio for write requests. 10+10

2. a) A nonpipelined processor X has a clock rate of 250 MHz and an average CPI (cycles per instruction) of 4. Processor Y, an improved successor of X, is designed with a five stage linear instruction pipeline with clock rate 200 MHz.

i) If a program containing 1000 instructions is executed on both processors, what is the speed up of Y over X.

ii) Calculate the MIPS rate for both X and Y for this particular program.

b) Consider the following page reference sequence generated by a two-level virtual memory system that uses demand

connected by an internal processor bus. Design an efficient microinstruction format to specify various micro operations for the processor.

c) We wish to provide 8 control words for each machine instruction routine. Machine instruction op codes have 5 bits and control memory has 1024 words. Suggest a mapping from the instruction register to the control address register. 7+7+6

7. a) What are the advantage of using normalised mantissa and biased exponents in floating point representation? Discuss single precision and double precision formats for IEEE standard floating point representation.

b) Consider an 18-bit floating point number with 7-bit exponent (excess-63 format) and 10 bit normalised mantissa with scale factor -2 (with an implicit 1 at the left of mantissa as in IEEE format)

Find $A - B$ and $A * B$, represent them in the above format after rounding using truncation method. 10+10

A = 0 1100001 1100110011
B = 0 0101010 0011001100

paging and has a main memory capacity of four pages.

1, 2, 3, 4, 1, 5, 2, 3, 6, 5, 4, 1, 6, 2, 5, 4.

which of the page replacement policies FIFO or LRU is more suitable for use with this system? 10+10

3. a) A virtual memory has a block size of 1K words. There are eight secondary blocks and four primary blocks. The associative memory page table contains the following entries :

Secondary block	Primary block
0	3
1	1
4	2
6	0

Make a list of virtual addresses (in decimal) that will cause a page fault if addressed by CPU.

b) Suppose that a 2 KB cache has set-associative mapping. There are 16 sets, each containing 4 blocks. Main memory address size is 32 bits and smallest addressable unit is byte (i) To what set of the cache is the address $000021BC_{16}$ assigned? (ii) If the addresses $000021BC_{16}$ and $FFFFF5XYZ_{16}$ are assigned to the same cache set, what values can the address digits XYZ have? 10+10

[Turn over

4. a) Calculate the relative speeds of a 16-bit adder using (i) ripple carry only, (ii) 4-bit ripple carry blocks with carry look ahead in between, (iii) two level carry look-ahead scheme. Derive all necessry expression related to your answers.

b) Draw the combinational circuit for paper pencil method of multiplication for two signed numbers −29 and +29. Also find the total delay in multiplication. 10+10

5. Write short note on (any **two**) 10x2=20

i) Restoring type division

ii) Associative memory

iii) Micro programming

iv) Carry save addition

6. a) An 8-bit computer has 16-bit address bus. The first 15 lines of the address bus are used to select a location within a bank of 32 KPs of memory. The high order bit of the address is used to select a register which receives the contents of the data bus. Explain has this configuration can be used to extend the memory capacity of the system to eight banks of 32 KB each for a total of 256 KB of memory.

b) A processor has 16 registers, an ALU with 16 logical and 16 arithmetic functions and a shifter with 8 operations, all