7. a) In a certain computer system with cache memory 750 μsec is the main memory access time for cache miss and 50 μsec is the access time for cache hit. Find the percentage decrease in the effective access time if the hit ratio is increased from 75% to 95%.

   b) The page reference pattern of a program is as follows :

   1, 2, 3, 4, 1, 5, 2, 3, 6, 5, 4, 1, 6, 2, 5, 4

   Which of the page replacement policies FIFO, LRU and LIFO is most suitable with cache memory capacity 4 pages.

10+10

Ex/CSE/T/213/18/2011(S)

BACHELOR OF COMPUTER SC. ENGG. EXAMINATION, 2011

(2nd Year, 1st Semester, Supplementary)

COMPUTER ORGANISATION

Time : Three hours Full Marks : 100

Answer ***any five*** questions.

(Answer for any question should start from a new page and all parts of a question should be answered together.)

1. a) Write a program to evaluate the statement

$$X = \frac{(A + B) * C}{(B - C) * D}$$

   i) Using general register computer with 3-address instructions.

   ii) Using general register computer with 2-address instructions.

   iii) Using general register computer with 1-address instructions.

   iv) Using stack organised computer with 0-address instructions.

   b) The memory unit of a computer has 256 words of 32 bit each. The computer has an instruction format with four fields; opcode, mode to specify one of seven addressing modes, register address field to specify one of 25 processor registers and memory address.

Specify the instruction format and the no. of bits in each field if each instruction is one memory word long. Also find the total no. of operations that can be performed by the ALU. 3×4+8

2. Consider the following algorithm :

Declare registers A(8), B(8), C(8)

Start : A ← 0
B ← 00001010
Loop : A ← A + B
B ← B – 1
If B < > 0 then go to loop
C ← A
Halt : Goto Halt

Design a hardwired controller using D-flipflop and microprogram controller that will implement this algorithm. 20

3. Write short notes on (***any two***) : 10×2

i) Non-restoring division.

ii) Carry-look-ahead adder.

iii) Virtual Memory.

4. a) Draw the CSA organisation to add 8 signed numbers of 4-bit each having ripple carry adder at the last stage. Also count the number of full adders required and calculate the gate delay in the addition process.

b) How associative memory differs from conventional memory? Explain the organisation of associative memory with a neat diagram. Describe the match logic used in associative memory. 10+10

5. a) Draw the combinational circuit for paper pencil method of multiplication for two signed numbers — 29 and +23. Find also the total delay in multiplication.

b) Draw the block diagram for implementing bit pair multiplication algorithm (sequential logic). Next verify step by step with the example of –29 and +23. 10+10

6. 16 K byte of main memory is implemented using 8 nos. of 2 K byte modules used in interleaved fashion. Following three organisations are proposed.

i) Eight way interleaved.

ii) Two groups of four way interleaved.

iii) Four groups of two way interleaved.

For each of the organization

a) Show address decoding scheme and address assignment pattern.

b) Maximum unusable space when one module fails.

c) Comment on the relative merits of the three organizations. 20