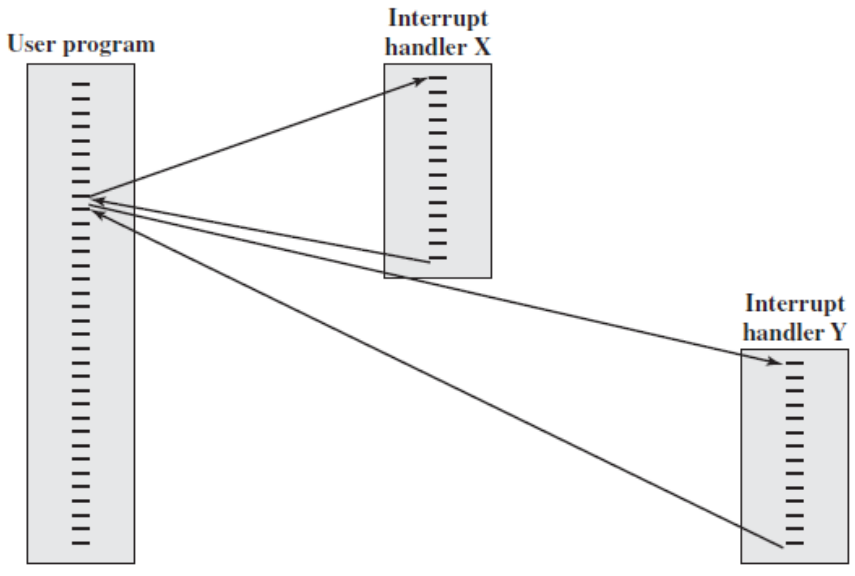
Multiple Interrupts

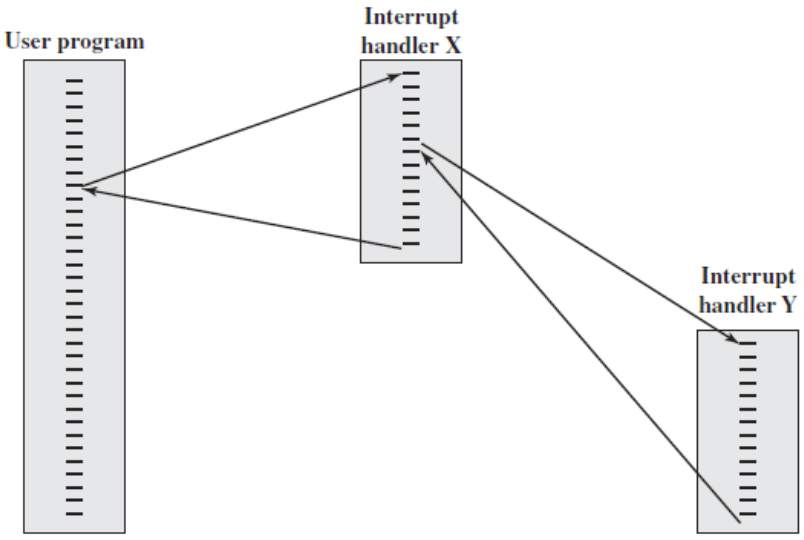
- Disable interrupts
  - Processor will ignore further interrupts whilst processing one interrupt
  - Interrupts remain pending and are checked after first interrupt has been processed
  - Interrupts handled in sequence as they occur
- Define priorities
  - Low priority interrupts can be interrupted by higher priority interrupts
  - When higher priority interrupt has been processed, processor returns to previous interrupt

Multiple Interrupts - Sequential



(a) Sequential interrupt processing

Multiple Interrupts – Nested



(b) Nested interrupt processing

Time Sequence of Multiple Interrupts

Communications priority > Disk > Printer

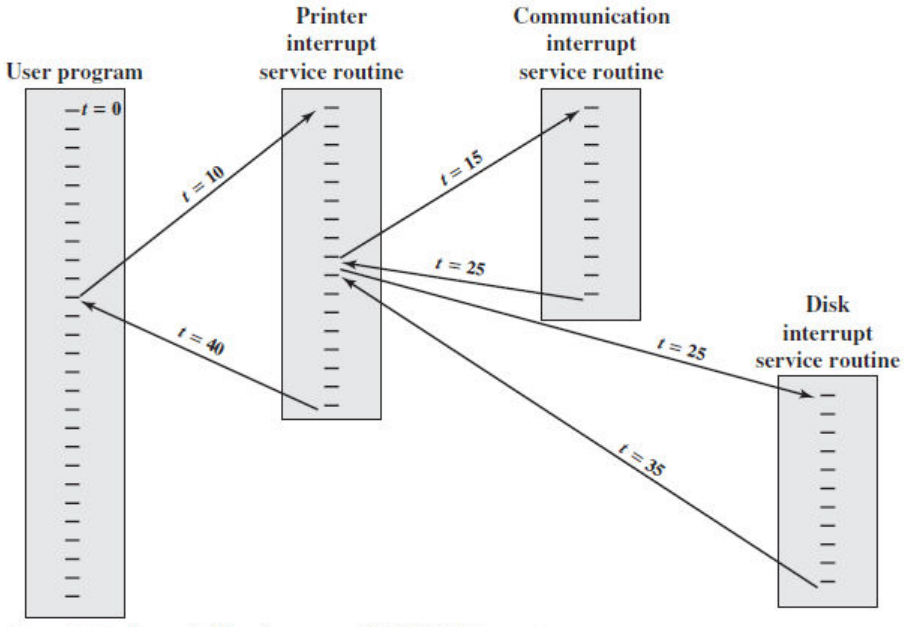
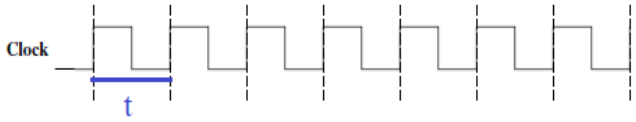


Figure 3.14 Example Time Sequence of Multiple Interrupts

Clock speed and instructions per second

- Quarts crystal generates high frequency signal → frequency is f
- 1GHz processor receives 1 billion pulse every second --- clock rate
- One pulse is clock cycle
- The time between pulses is the cycle time : t =1/f
- One instruction takes several cycles



Instruction execution rate

- I_c is instruction count in one program
- CPI_i cycle per instruction for instruction type i
- Different instructions require different cycles

- Overall CPI is

$$CPI = \frac{\sum_{i=1}^{n}(CPI_i \times I_i)}{I_c}$$

Program time

The processor time T needed to execute a given program can be expressed as

$$T = I_c \times CPI \times \tau$$

A common measure of performance for a processor is the rate at which instructions are executed, expressed as millions of instructions per second (MIPS), referred to as the **MIPS rate**. We can express the MIPS rate in terms of the clock rate and CPI as follows:

$$\text{MIPS rate} = \frac{I_c}{T \times 10^6} = \frac{f}{CPI \times 10^6}$$

Example

- F= 2.5 GHz
- 30 add operation with CPI=5
- 15 multi operation with CPI=11
- 7 load operation with CPI=9
- 6 divide operation with CPI=13

Ic= 30+ 15 + 7 + 6 = 58

CPI= (30x5 + 15x11 + 7x9 + 6x13)/ 58

CPI=7.86

t= 1/f = 1/(2.5x10^9)=0.4 x 10^-9 sec

T = 58 x 7.86 x 0.4 x 10^-9 = 182.4 x 10^-9

example

F=400 MHz

Instruction Type	CPI	Instruction Mix
Arithmetic and logic	1	60%
Load/store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	8	10%

The average CPI when the program is executed on a uniprocessor with the above trace results is $CPI = 0.6 + (2 \times 0.18) + (4 \times 0.12) + (8 \times 0.1) = 2.24$. The corresponding MIPS rate is $(400 \times 10^6)/(2.24 \times 10^6) \approx 178$.

Example

- For the multi-cycle MIPS
  - Load 5 cycles
  - Store 4 cycles
  - R-type 4 cycles
  - Branch 3 cycles
  - Jump 3 cycles
- If a program has
  - 10% load instructions
  - 20% store instructions
  - 50% R-type instructions
  - 8% branch instructions
  - 2% jump instructions
- what is the CPI?

  CPI = 5x0.10 + 4x0.20 + 4x0.50 + 3x0.08 + 3x0.02 = 3.6