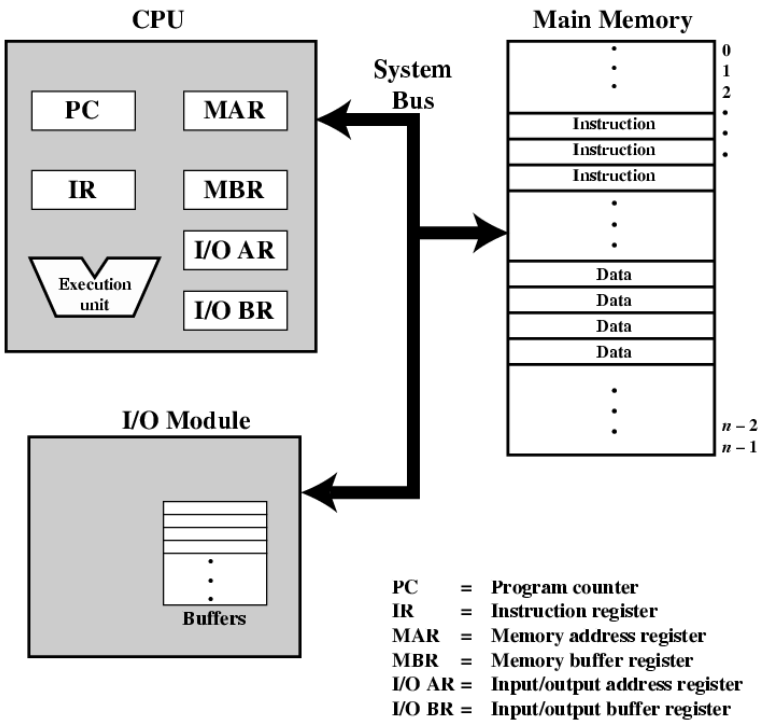
William Stallings
Computer Organization and Architecture 8th Edition

Chapter 3

Top Level view of Computer Functions and Interconnections

Computer Components: Top Level View

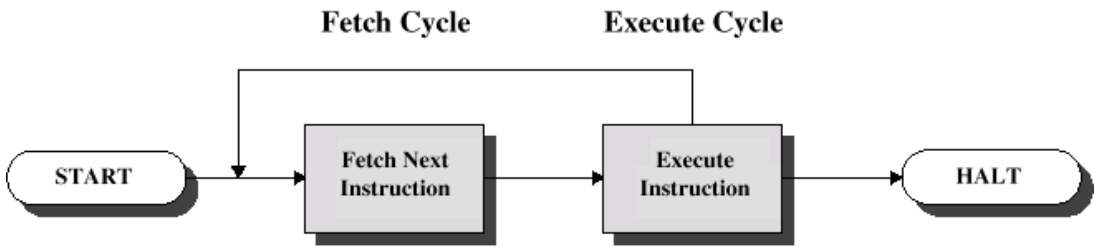


What is a program?

- A sequence of steps
- For each step, an arithmetic or logical operation is done
- For each operation, a different set of control signals is needed

Instruction Cycle

- Two steps:
  - Fetch
  - Execute



Fetch Cycle

- Program Counter (PC) holds address of next instruction to fetch
- Processor fetches instruction from memory location pointed to by PC
- Increment PC
  - Unless told otherwise
- Instruction loaded into Instruction Register (IR)
- Processor interprets instruction and performs required actions

Execute Cycle

- Processor-memory
  - data transfer between CPU and main memory
- Processor- I/O
  - Data transfer between CPU and I/O module
- Data processing
  - Some arithmetic or logical operation on data
- Control
  - Alteration of sequence of operations
  - e.g. jump
- Combination of above

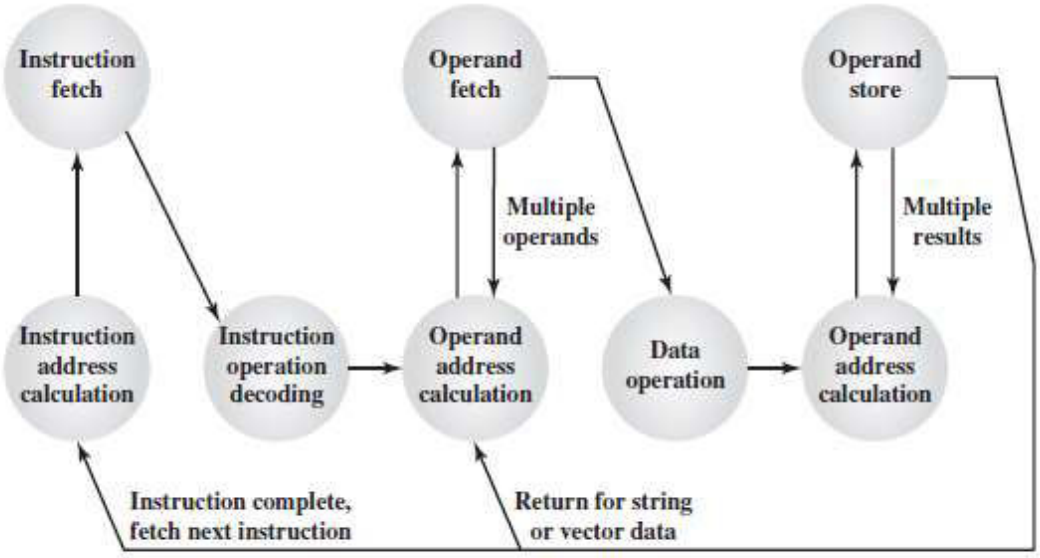


Figure 3.6 Instruction Cycle State Diagram

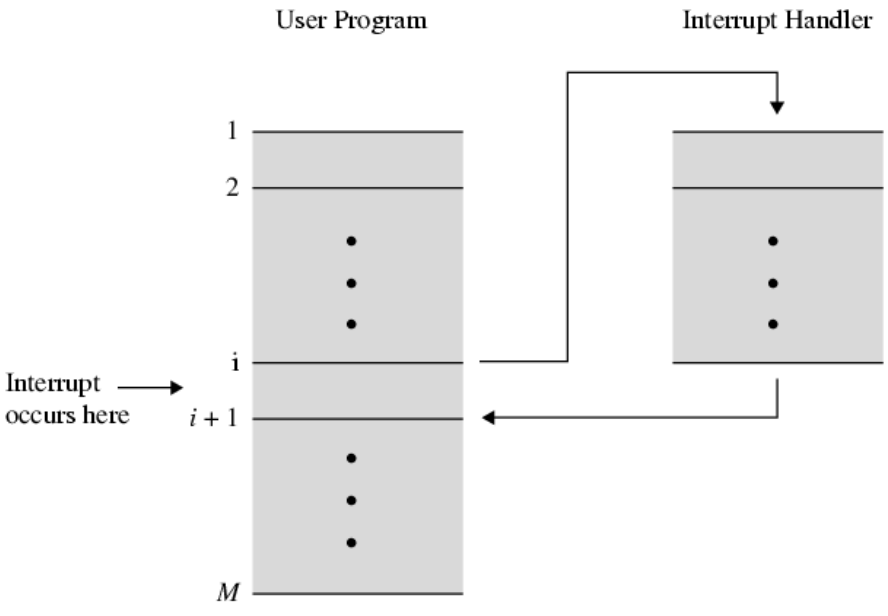
Interrupts

- Mechanism by which other modules (e.g. I/O) may interrupt normal sequence of processing
- Most Common Classes of interrupts:
  - Program
    - e.g. overflow, division by zero
  - Timer
    - Generated by internal processor timer
    - Used in pre-emptive multi-tasking
  - I/O
    - from I/O controller to signal completion of an operation or an error
  - Hardware failure
    - e.g. memory parity error, or power failure

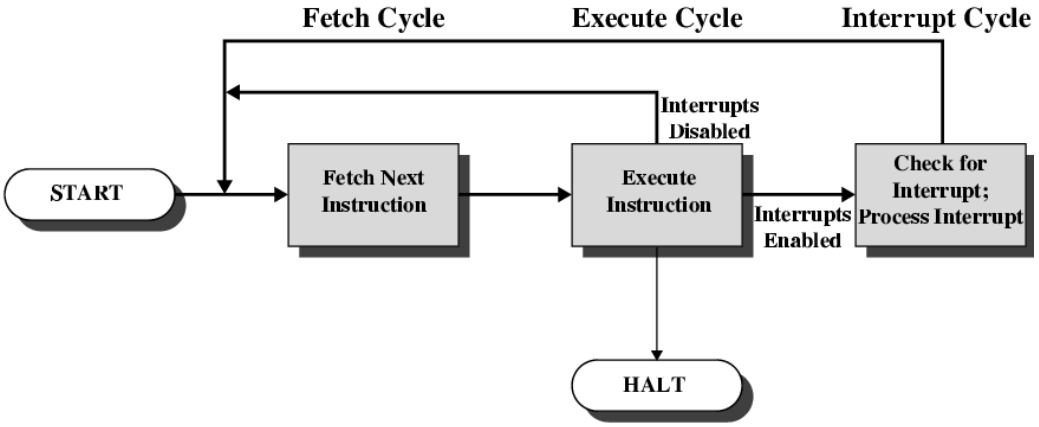
Interrupt Cycle

- Added to instruction cycle
- Processor checks for interrupt
  - Indicated by an interrupt signal
- If no interrupt, fetch next instruction
- If interrupt pending:
  - Suspend execution of current program
  - Save context
  - Set PC to start address of interrupt handler routine
  - Process interrupt
  - Restore context and continue interrupted program

Transfer of Control via Interrupts



Instruction Cycle with Interrupts



Instruction Cycle (with Interrupts) - State Diagram

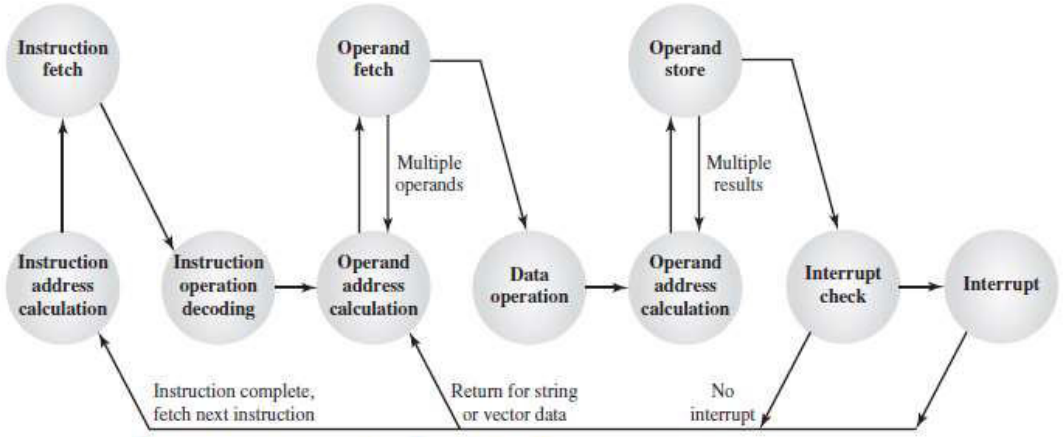


Figure 3.12 Instruction Cycle State Diagram, with Interrupts