Buses Structures

- Several interconnection systems can be used in computers.
- The most common are single and multiple bus structures.
- e.g. Control/Address/Data bus (PC)
- **Bus** : a communication pathway connecting two or more devices.
- Usually broadcast, often grouped into several lines.
- Example: a 32-bit data bus has 32 single-bit channels.
- Power lines may not be shown in diagrams.

Data Bus

- Carries data: “data” and “instruction”.
- Width is a key determinant of performance.
  - 8, 16, 32, 64 bit

Address bus

- Identify the source or destination of data.
- e.g. CPU needs to read an instruction (data) from a given location in memory.
- Bus width determines maximum memory capacity of system
  - e.g. 8080 has 16 bit address bus giving 64k address space

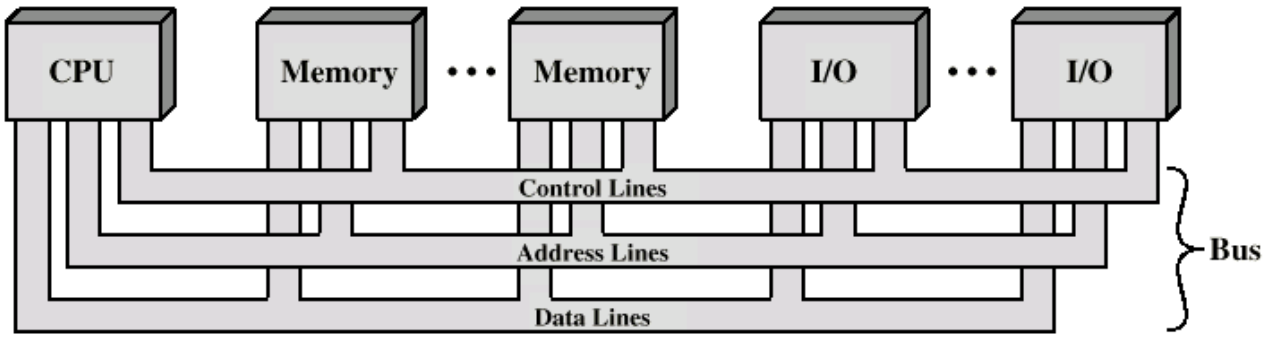
$$2^{10} = 1\,KB$$

$$2^{16} = 2^{10} \times 2^{6} = 64\,KB$$

Control Bus

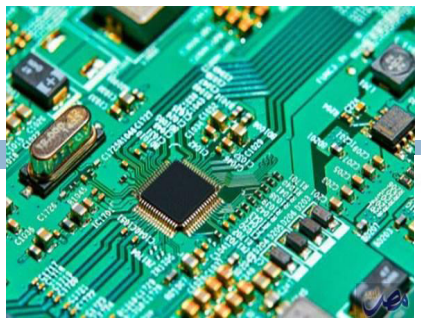
- Control and timing information
  - Memory read/write signal
  - Interrupt request
  - Clock signals

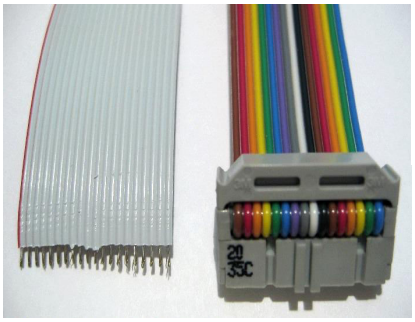
Bus Interconnection Scheme



What Do Buses Look Like?

- Parallel lines on circuit boards
- Ribbon cables
- Strip connectors on motherboard
  - e.g. PCI
- Sets of wires





Single Bus Problems

Lots of devices on one bus leads to:

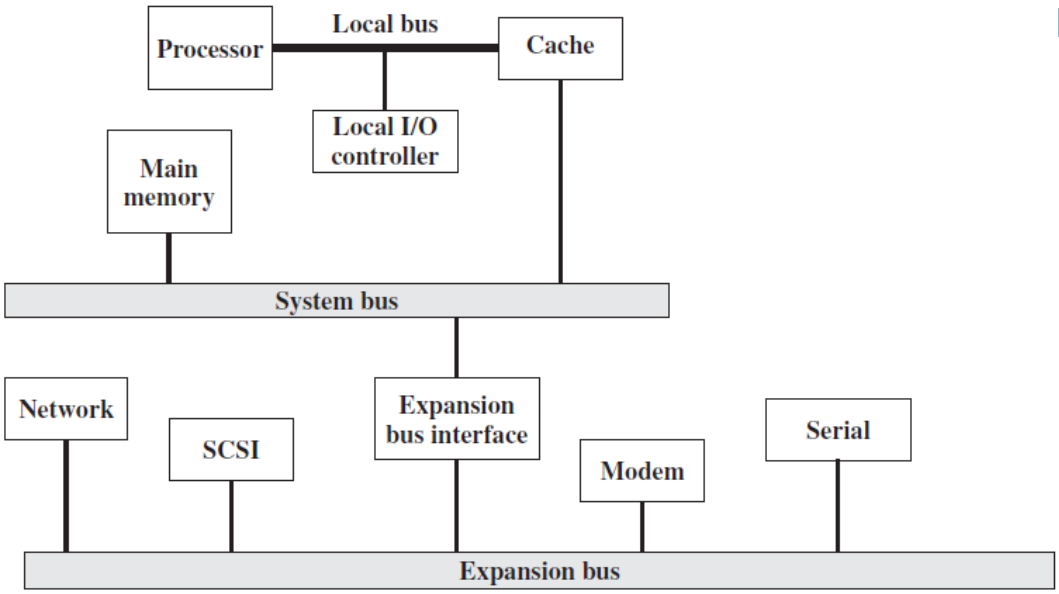
- Propagation delays: signals take longer to travel along the bus.
- Long data paths mean coordination of bus usage becomes slower, which can affect overall performance.
- If aggregate data transfer approaches bus capacity, the system slows down.

Solution: Most systems use multiple buses to overcome these problems.

Bus Types

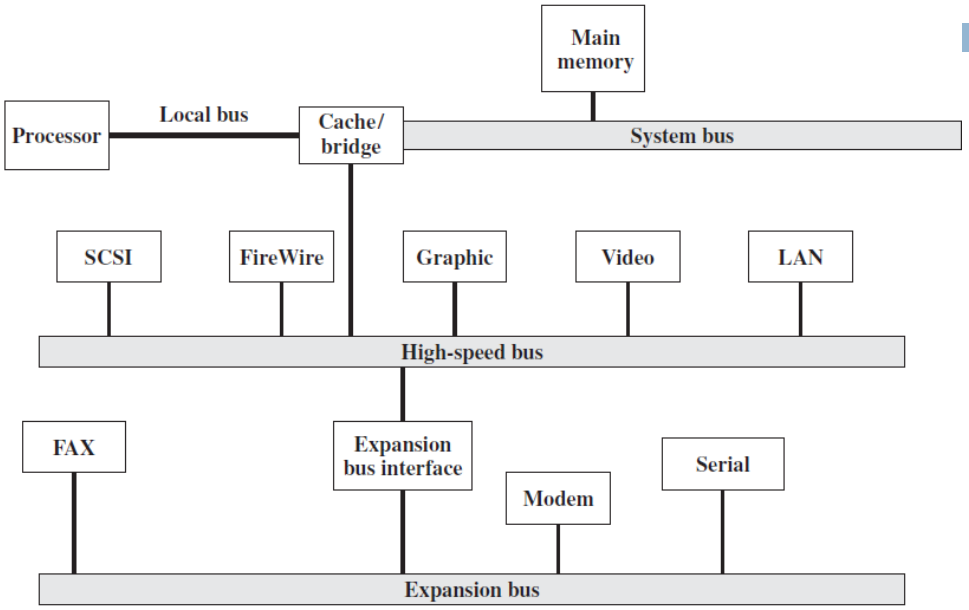
- Dedicated: Separate data & address lines
  - Advantages:
    * Higher speed (data and address can be sent at the same time)
    * Simpler control
  - Disadvantages: Requires more lines.
- Multiplexed: Shared lines for both data and address
  - A control line indicates whether the signal is Address valid or Data valid
  - Advantage - fewer lines
  - Disadvantages
    * More complex control
    * Lower overall performance

Traditional Bus Architecture (ISA)



(a) Traditional bus architecture

High Performance Architecture



(b) High-performance architecture

PCI Bus

- Peripheral Component Interconnection
- Developed by Intel and released into the public domain
- Bus Width: Supports 32-bit or 64-bit data transfers.
- Around 50 lines, divided into several groups:

PCI Bus Lines (required)

- Systems lines
  - Including clock and reset
- Address & Data lines
  - 32 lines used for time-multiplexed address/data transfers
- Interface Control lines
- Arbitration lines
  - Not shared
  - Direct connection to PCI bus arbiter
- Error lines

PCI Bus Lines (Optional)

- Interrupt lines
  - Not shared
- Cache support
- 64-bit Bus Extension
  - Additional 32 lines
  - Time multiplexed
  - 2 lines to enable devices to agree to use 64-bit transfer
- JTAG/Boundary Scan
  - For testing procedures

PCI Commands

Transaction between initiator (master) and target :

- Master claims the bus: Initiator device requests control of the PCI bus.
- Determine type of transaction
  - e.g. I/O read/write
- Address phase: Master sends the target address.
- Data Phase(s): One or more cycles for transferring data.