pixhawk®

DS-010 Pixhawk Autopilot Bus Standard

Revision: 0.3.0
Revision date: Apr 14, 2020

Abstract

This document is the formal version of the Pixhawk industry standard that includes all aspects of the hardware standard required to build compatible autopilots.

Table of contents

Document Revisions

Revision	Editor	Reviewer	Comments
0.1.0	Lorenz Meier	David Sidrane	Initial specification
0.2.0	Lorenz Meier	David Sidrane	Addition of FMUv6X draft
0.3.0	Lorenz Meier	David Sidrane	Split up into focused documents

Contact and Public Developer Call

This standard is being developed on a public developer call.
For further questions, please contact the maintainer of the standard, lorenz@px4.io.

Trademark Guideline

Pixhawk is a registered trademark and is used to mark and protect the consistent use of this standard. The requirements for this are covered in this document: Trademark Guideline

License and Disclaimer

Flight Management Unit Standards

- FMUv1: No product name (2012, 168 MHz M4)
- FMUv2: Pixhawk 1 (2013, 168 MHz M4)
- FMUv3: Pixhawk 2 (2015, 168 MHz M4, redundant sensors)
- FMUv4: Pixracer (2015, 168 MHz M4)
- FMUv4X: Pixhawk 3 Pro (2017, 168 MHz M4, redundant sensors)
- FMUv5: Pixhawk 4 (2018, 200 MHz M7)
- FMUv5X: Pixhawk 5X (2019, 200 MHz M7, temp-calibrated, redund. sensors)
- FMUv6: Pixhawk 6 (2019, 400-600 MHz H7)
- FMUv6X: Pixhawk 6X (2020, 400-600 MHz H7, calibrated, redund. sensors)

Interface Standards

- **OBSOLETE**: Pixhawk connector standards v1 (2011-2015)
  - Connector: Hirose DF13
  - Pinout: Obsolete
- Pixhawk connector standards v2 (2015-)
  - Connector: JST GH
  - Pinout: Pixhawk connector pinout
- Pixhawk Autopilot Bus (PAB)
  - Connector: 100-pos Hirose DF40
  - Connector: 50-pos Hirose DF40

Common External Interfaces

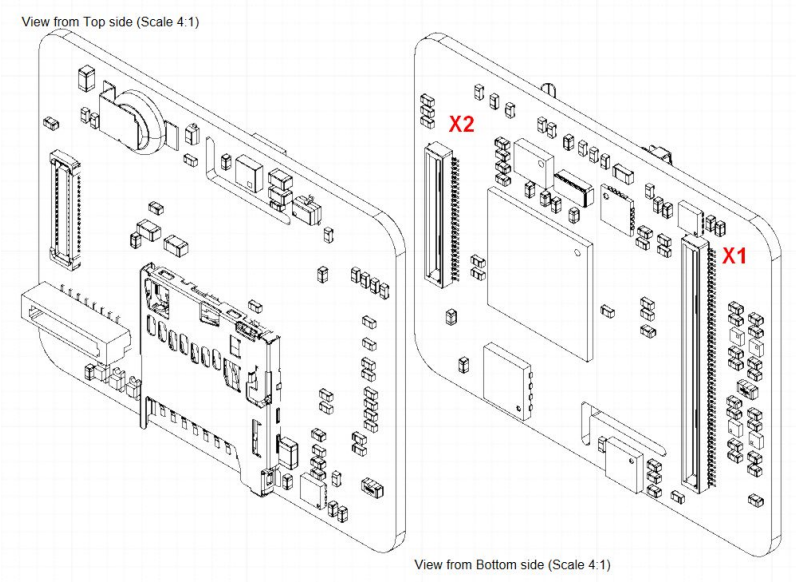
This list describes the mandatory external interfaces.

Standard	FMUv5	FMUv5X	FMUv6	FMUv6X
Stable	06/2018	06/2019	12/2019	02/2020
Clock	200 MHz	200 MHz	480 MHz	480 MHz
RAM	512 KB	512 KB	1 MB	1 MB
PAB / SoM		✔	x	✔
UART (RTS/CTS)	2	3	3	3
UART	2	4	2	4
Debug	6-pos	10-pos	10-pos	10-pos
Ethernet	x	✔	✔	✔
CAN	2	2	3	3
I2C	2	3 (+NFC)	2	3 (+NFC)
Power input	analog	digital	digital	digital
PWM out	6 + 8 (IO)	8 + 8 (IO)	8	8

Pixhawk Autopilot Bus (PAB) and Module Standard

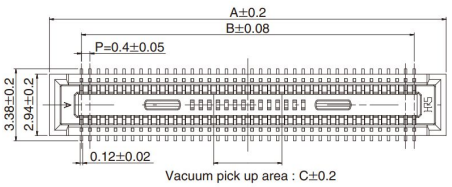
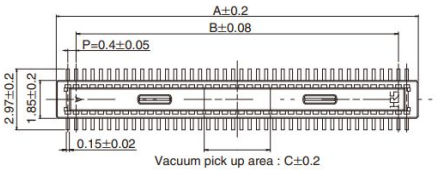
The usage of this bus is mandatory for all System-on-Module designs (SOM). However, if autopilot and baseboard are integrated into one unit, this connector pair (PAB X1 and PAB X2) can be omitted. See the mechanical section for dimensions.

TIP: Leverage the Altium footprint available in the support files folder



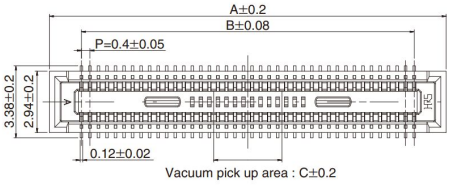
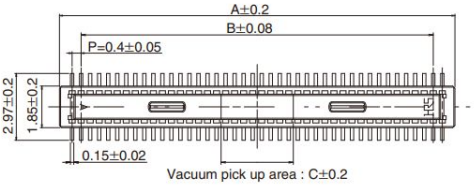
Connector X1 (PAB X1)

The 100-pin connector is automotive grade, low-cost, vibration resilient and allows very high density assemblies.

Side	Baseboard side (bottom)	Autopilot side (top)
Part Number	Hirose DF40HC(3.0)-100DS-0.4V(58)	Hirose DF40C-100DP-0.4V(51)
Distributors	DigiKey	DigiKey
Dimensions	 A = 22.6mm B = 19.6mm	 A = 21.52mm B = 19.6mm

Connector X2 (PAB X2)

The 50-pin connector is automotive grade, low-cost, vibration resilient and allows very high density assemblies.

Side	Baseboard side (bottom)	Autopilot side (top)
Part Number	Hirose DF40HC(3.0)-50DS-0.4V(51)	Hirose DF40C-50DP-0.4V(51)
Distributors	Digikey	Digikey
Dimensions	 A = 12.6mm B = 9.6mm	 A = 11.52mm B = 9.6mm

X1 Pinout

Mandatory main bus with the critical Pixhawk interfaces.

2	1	2	GND (Pin 2)
FMU_CH7	3	4	BUZZER_1
FMU_CH6	5	6	GND
FMU_CH5	7	8	I2C3_SDA_BASE_MS5611_BARBED_EXTERNAL1
GND	9	10	I2C3_SCL_BASE_MS5611_BARBED_EXTERNAL1
FMU_CH4	11	12	I2C2_SDA_BASE_GPS2_MAG_LED_PM2
FMU_CH3	13	14	I2C2_SCL_BASE_GPS2_MAG_LED_PM2
FMU_CH2	15	16	I2C1_SDA_BASE_GPS1_MAG_LED_PM1
FMU_CH1	17	18	I2C1_SCL_BASE_GPS1_MAG_LED_PM1
GND	19	20	GND
FMU_SAFETY_SWITCH_IN	21	22	UART7_RTS_TELEM1
FMU_nSAFETY_SWITCH_LED_OUT	23	24	UART7_CTS_TELEM1
HW_VER_REV_DRIVE	25	26	GND
HW_VER_SENSE	27	28	UART8_TX_GPS2
V_RTC_BAT	29	30	UART8_RX_GPS2
GND	31	32	GND
VDD_3V3_SPEKTRUM_POWER_EN	33	34	USART1_RX_GPS1
VDD_5V_PERIPH_nEN	35	36	USART1_TX_GPS1
VDD_5V_PERIPH_nOC	37	38	GND
FMU_PPM_INPUT	39	40	USART2_TX_TELEM3
GND	41	42	USART2_RX_TELEM3

GND	43	44	GND
GND	45	46	USART2_RTS_TELEM3
GND	47	48	USART2_CTS_TELEM3
VDD_5V_IN	49	50	GND
VDD_5V_IN	51	52	UART5_TX_TELEM2
VDD_5V_IN	53	54	UART5_RX_TELEM2
VDD_5V_IN	55	56	GND
CAN2_TX	57	58	UART5_RTS_TELEM2
CAN2_RX	59	60	UART5_CTS_TELEM2
GND	61	62	GND
CAN1_TX	63	64	UART7_TX_TELEM1
CAN1_RX	65	66	UART7_RX_TELEM1
GND	67	68	GND
USART3_TX_DEBUG	69	70	USART6_RX_FROM_IO__RC_INPUT
USART3_RX_DEBUG	71	72	USART6_TX_TO_IO__NC
GND	73	74	GND
FMU_SWDIO	75	76	USB_D_P
FMU_SWCLK	77	78	USB_D_N
GND	79	80	VBUS_SENSE
VDD_5V_HIPOWER_nEN	81	82	GND
VDD_5V_HIPOWER_nOC	83	84	FMU_VDD_3V3
nARMED	85	86	FMU_VDD_3V3
FMU_nRST	87	88	GND
nPOWER_IN_A	89	90	ADC1_6V6
nPOWER_IN_B	91	92	ADC1_3V3
nPOWER_IN_C	93	94	GND
GND	95	96	UART4_RX
FMU_CAP1	97	98	UART4_TX
GND	99	100	GND

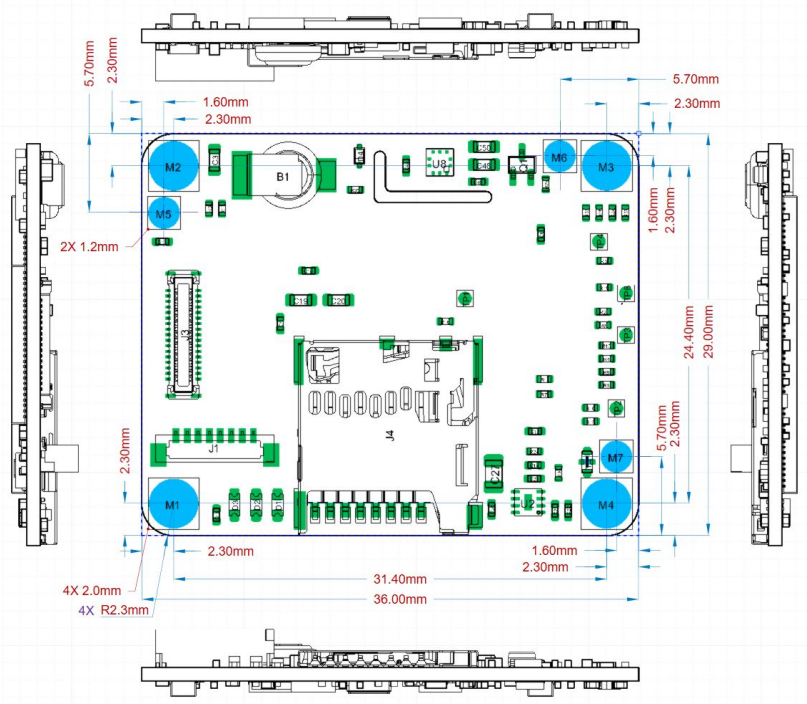
X2 Pinout

Advanced bus (optional) containing ethernet and external SPI port.

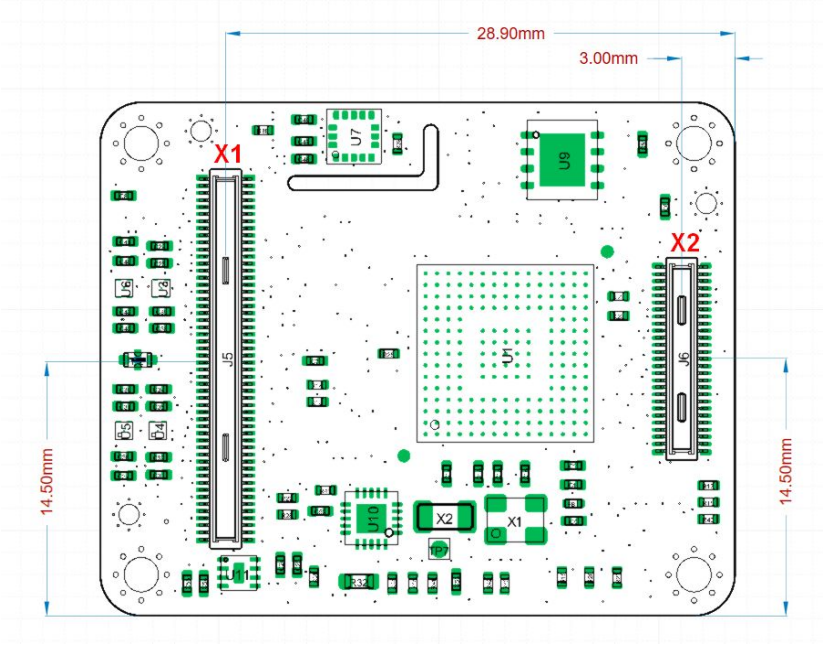
GND (Pin 1)	1	2	ETH_MDIO
ETH_REF_CLK	3	4	ETH_MDC
GND	5	6	ETH_POWER_EN
ETH_CRS_DV	7	8	GND
GND	9	10	SPARE01
ETH_RXD0	11	12	SPARE02
GND	13	14	SPARE03
ETH_RXD1	15	16	SPARE04
GND	17	18	SPARE05
ETH_TXD0	19	20	SPARE06
GND	21	22	SPARE07
ETH_TXD1	23	24	SPARE08
GND	25	26	SPARE09
ETH_TX_EN	27	28	SPARE10
GND	29	30	SPARE11
SPI6_MISO_EXTERNAL1	31	32	SPARE12
SPI6_MOSI_EXTERNAL1	33	34	SPARE13
SPI6_SCK_EXTERNAL1 (SWO)	35	36	SPARE14
GND	37	38	SPARE15
SPI6_nRESET_EXTERNAL1	39	40	SPARE16
SPI6_nCS1_EXTERNAL1	41	42	SPARE17
SPI6_nCS2_EXTERNAL1	43	44	PG6
SPI6_DRDY2_EXTERNAL1	45	46	GND
SPI6_DRDY1_EXTERNAL1	47	48	NFC_GPIO
SPIX_SYNC	49	50	PH11

Mechanical Design

Top view of FMU SOM



Bottom view of FMU SOM



PCB Layout Guidelines

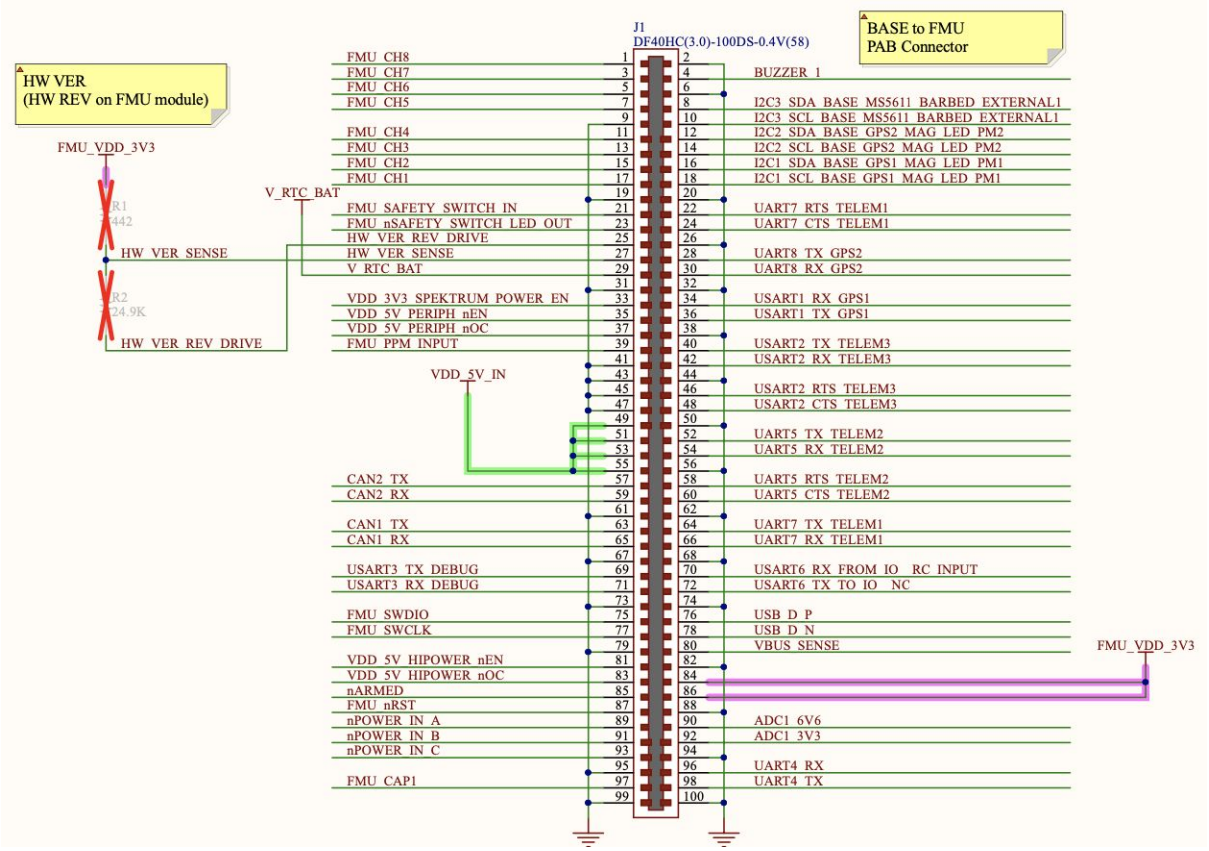
- The base board should be impedance controlled with 50 ohms single ended, 90 ohms differential for USB, and 100 ohms differential for Ethernet.
- Impedance controlled signal traces should not be routed such that they cross a split in their respective reference planes. A signal crossing a plane split may cause unpredictable return path currents impacting signal quality and potentially creating EMI problems.
- Provide 3x the gap separation between adjacent ground fill copper and both USB and Ethernet differential signal traces.
- Ethernet RMII interface signals ETH_TX_EN, ETH_TXD1, ETH_TXD0, ETH_CRS_DV, ETH_RXD1, ETH_RXD0 should each be kept under 6" in length with length matching to each other within 2". ETH_TXD0 is ~1" on the FMUM board and ~0.5" longer than the rest of the RMII interface signals. Therefore on the base board ETH_TXD0 should be less than 5" in length and the remainder of RMII signals should match (ETH_TXD0 - 0.5") to with 2".
- While it is possible to mount low profile components under the FMU SOM, it is recommended that some form of heatsinking provision be employed to remove heat from bottom side M7 processor U1, such as a metal housing that is thermally connected to U1. Use of such a metal housing may require a keepout area under the SOM.
- The four 2.0 mm mounting holes with 3.6 mm pads are connected to ground and are intended to provide electrical grounding to the base board through metal standoffs.
- The DF40 connectors establish a 3mm board to board spacing between the SOM and base board.
- Port protection diodes and series resistors should be placed close to the connectors they are providing protection for.
- Ethernet common mode chokes specify removing copper planes and traces from beneath the parts for best performance.
- The impedance from input connector, through power path selector, to VDD_5V_IN should be given special attention to reduce voltage drops. Keep traces wide (at least 1mm) and use multiple vias when changing layers (at least 2).

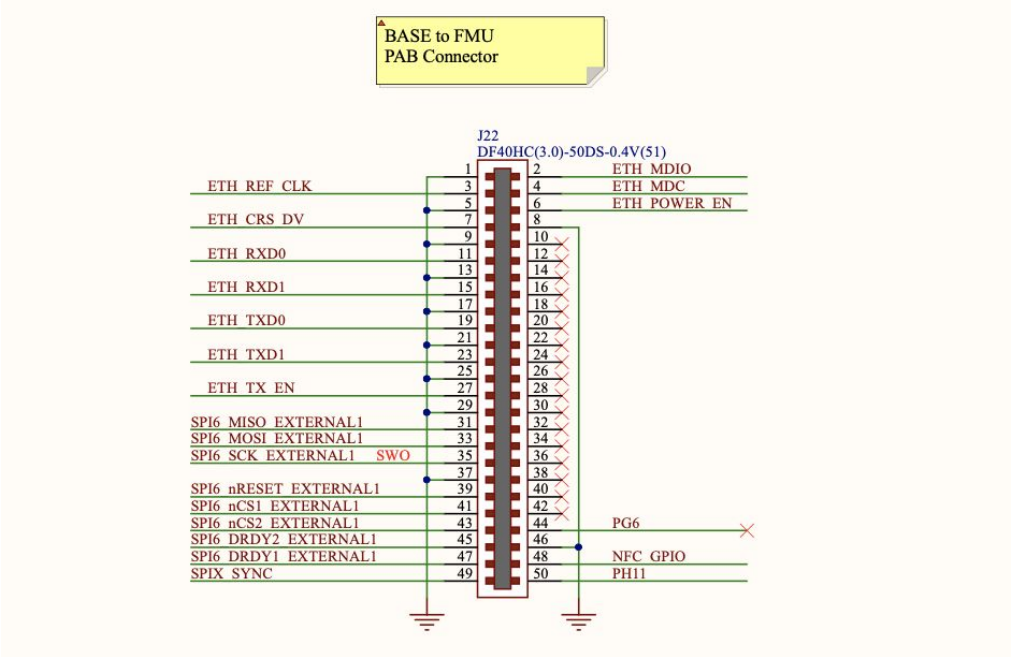
Baseboard Design Examples (FMUv5X, FMUv6X)

The design examples in this section have been proven as part of a reference design and are offered for convenience.

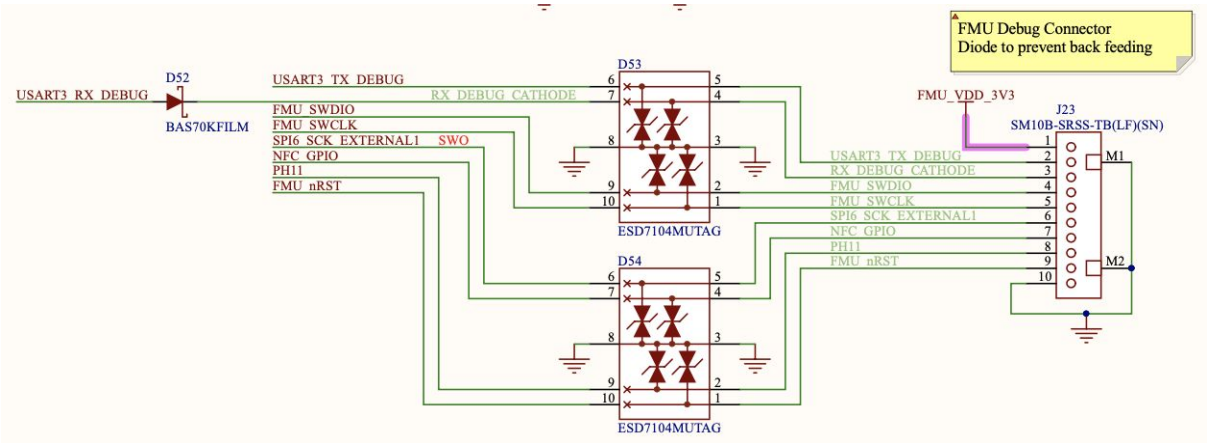
The design examples are not part of the formal specification and implementing the board differently is permitted. They serve as a baseline to ensure successful adoption of the standard.

Base to FMU Connectors (X1, X2)

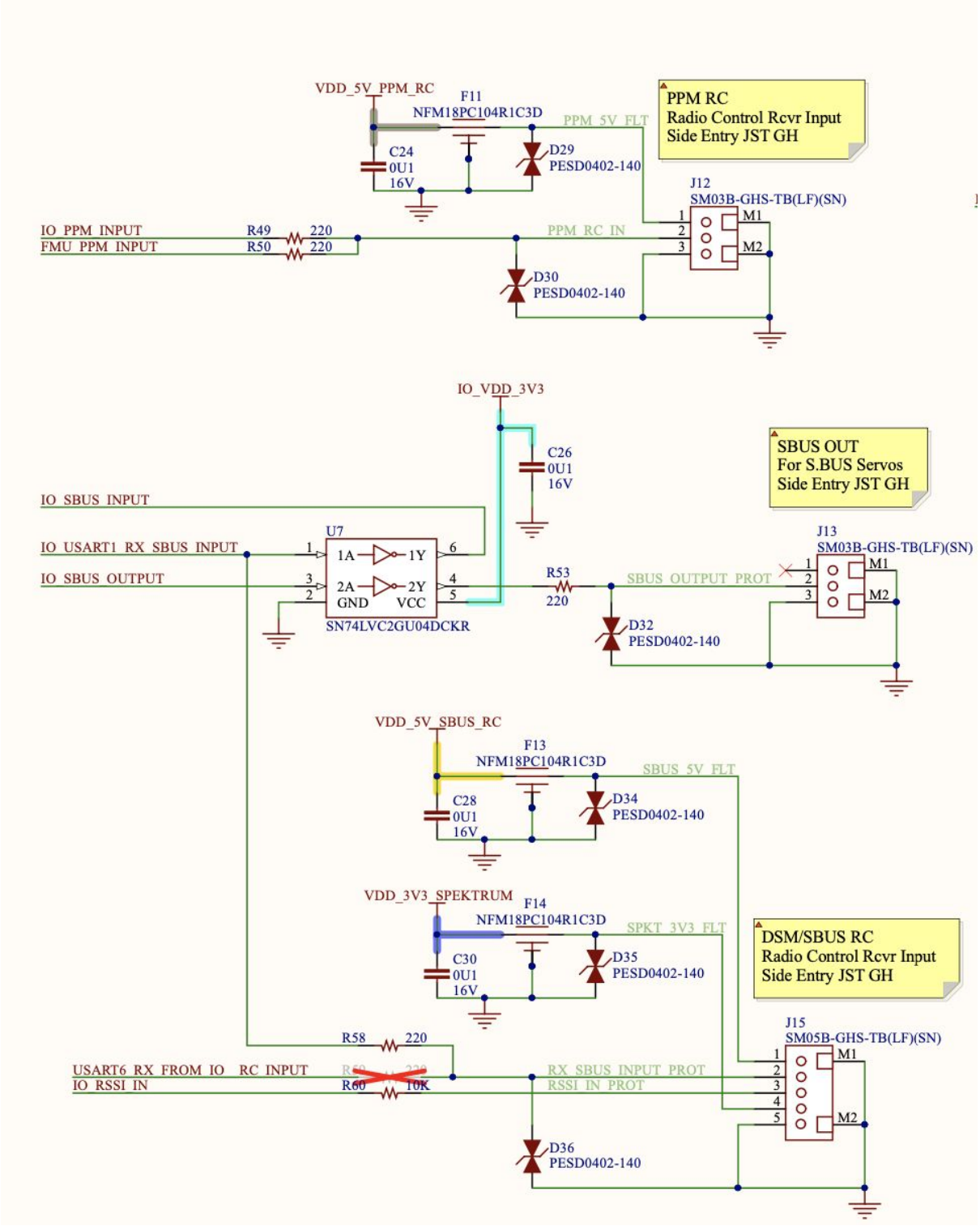




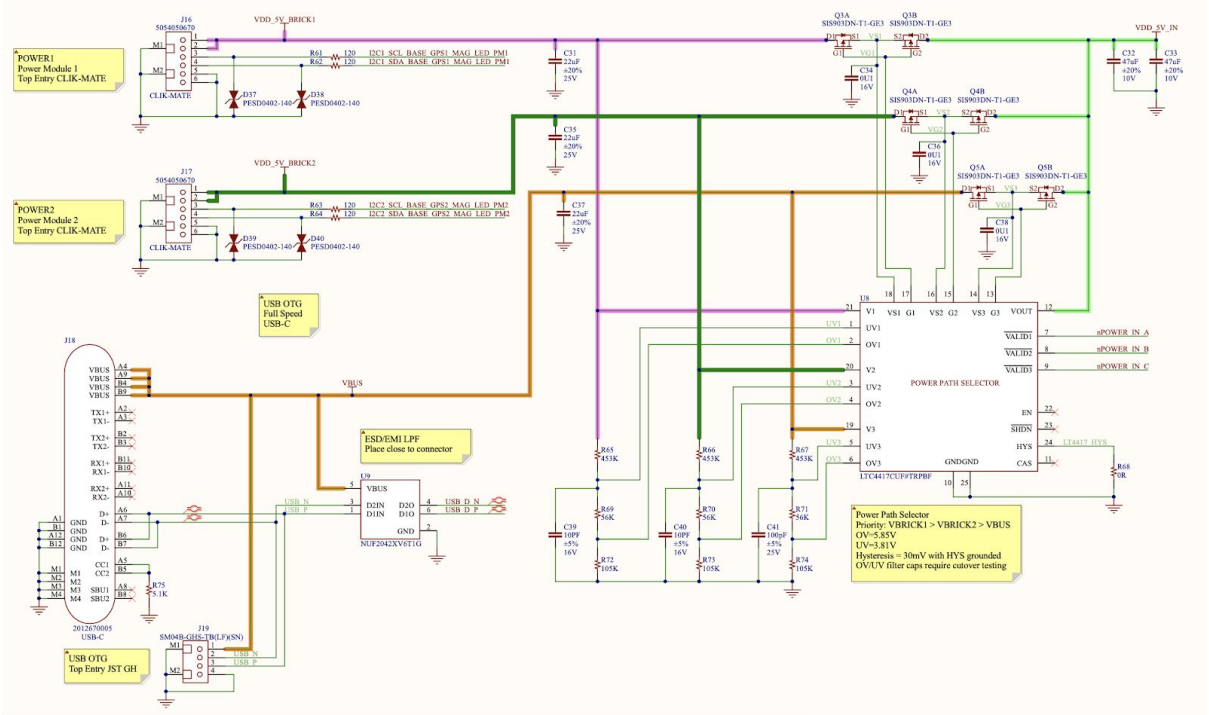
FMU Debug Connector



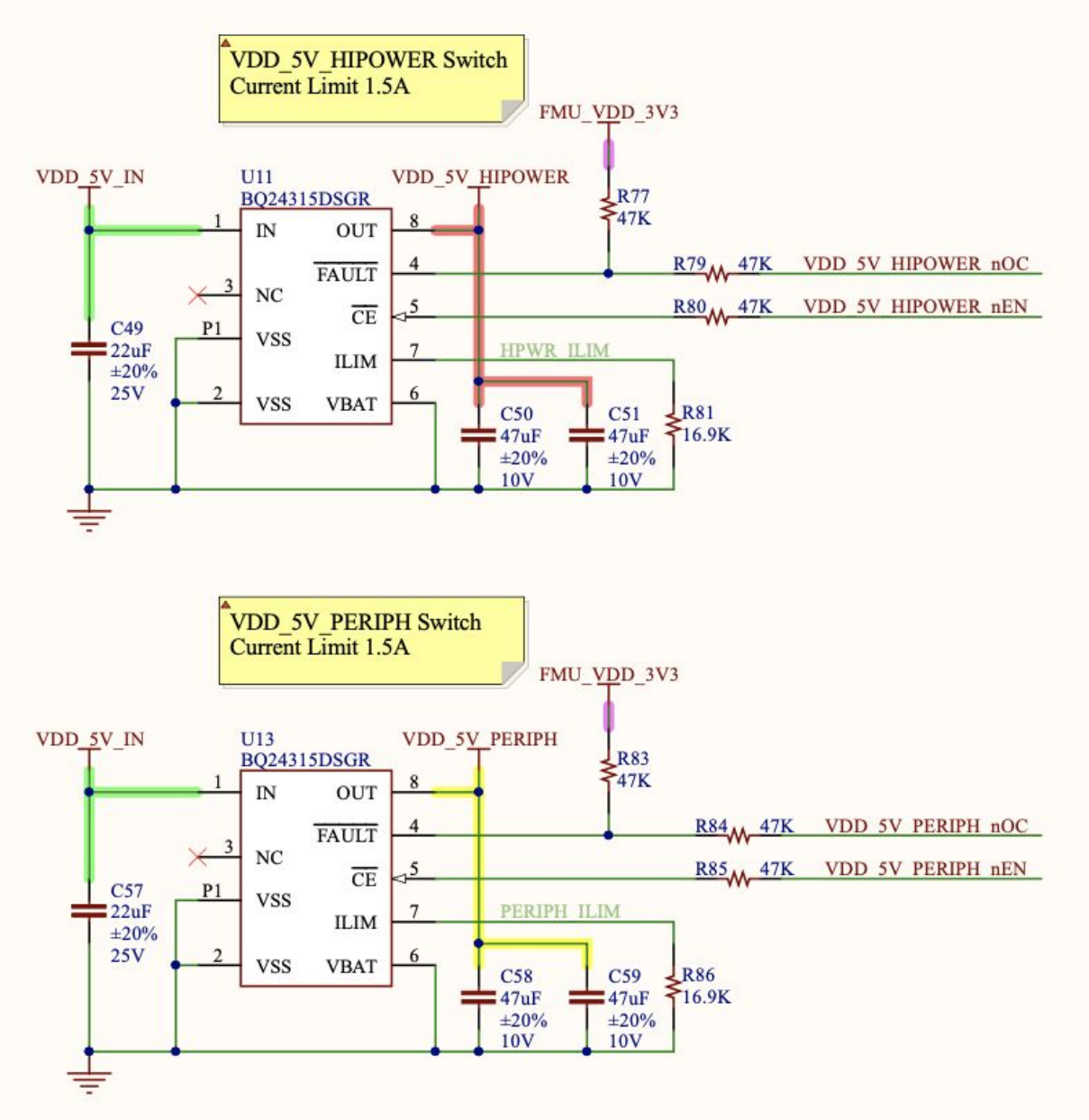
RC Inputs


VDD_5V_PPM_RC
F11
NFM18PC104R1C3D
PPM_5V_FLT
C24
0U1
16V
D29
PESD0402-140
PPM RC
Radio Control Rcvr Input
Side Entry JST GH
J12
SM03B-GHS-TB(LF)(SN)
M1
M2
IO_PPM_INPUT
FMU_PPM_INPUT
R49 220
R50 220
PPM_RC_IN
D30
PESD0402-140
IO_VDD_3V3
C26
0U1
16V
SBUS OUT
For S.BUS Servos
Side Entry JST GH
IO_SBUS_INPUT
IO_USART1_RX_SBUS_INPUT
IO_SBUS_OUTPUT
U7
1A
1Y
2A
2Y
GND
VCC
SN74LVC2GU04DCKR
R53
220
SBUS_OUTPUT_PROT
J13
SM03B-GHS-TB(LF)(SN)
D32
PESD0402-140
VDD_5V_SBUS_RC
F13
NFM18PC104R1C3D
SBUS_5V_FLT
C28
0U1
16V
D34
PESD0402-140
VDD_3V3_SPEKTRUM
F14
NFM18PC104R1C3D
SPKT_3V3_FLT
C30
0U1
16V
D35
PESD0402-140
DSM/SBUS RC
Radio Control Rcvr Input
Side Entry JST GH
J15
SM05B-GHS-TB(LF)(SN)
R58 220
USART6_RX_FROM_IO_RC_INPUT
IO_RSSI_IN
R60 10K
RX_SBUS_INPUT_PROT
RSSI_IN_PROT
D36
PESD0402-140

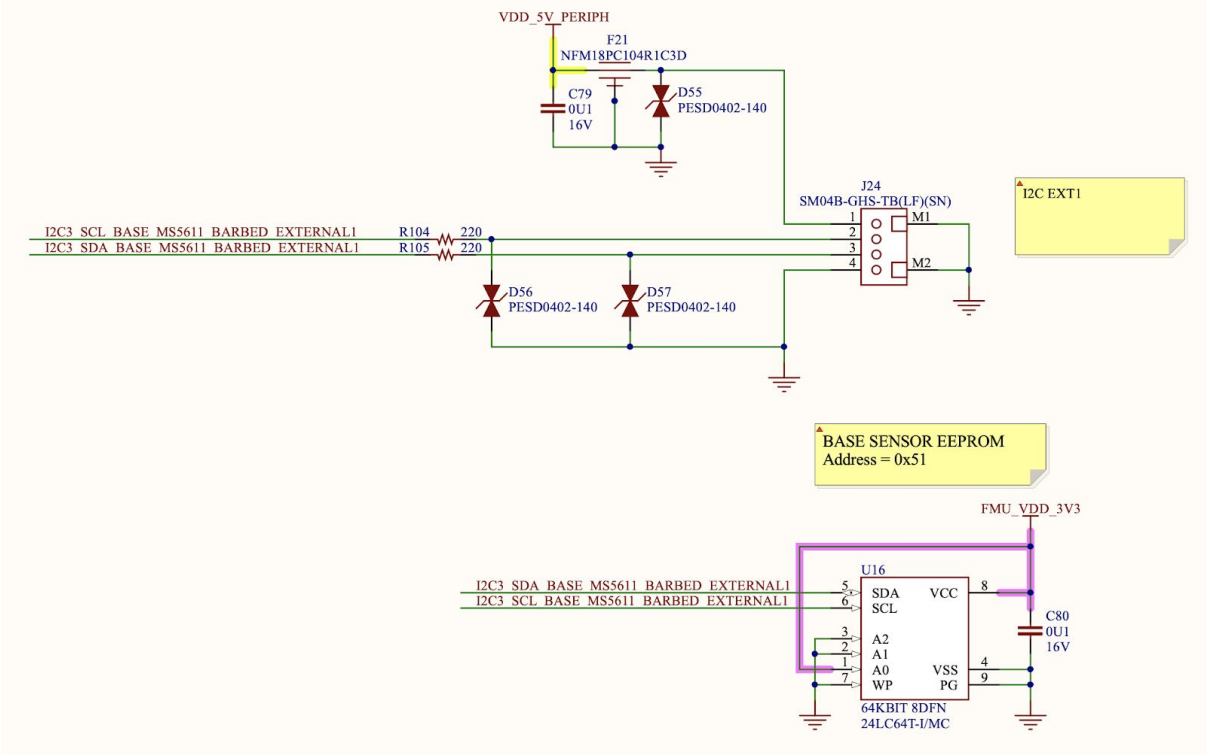
Powerpath Selector



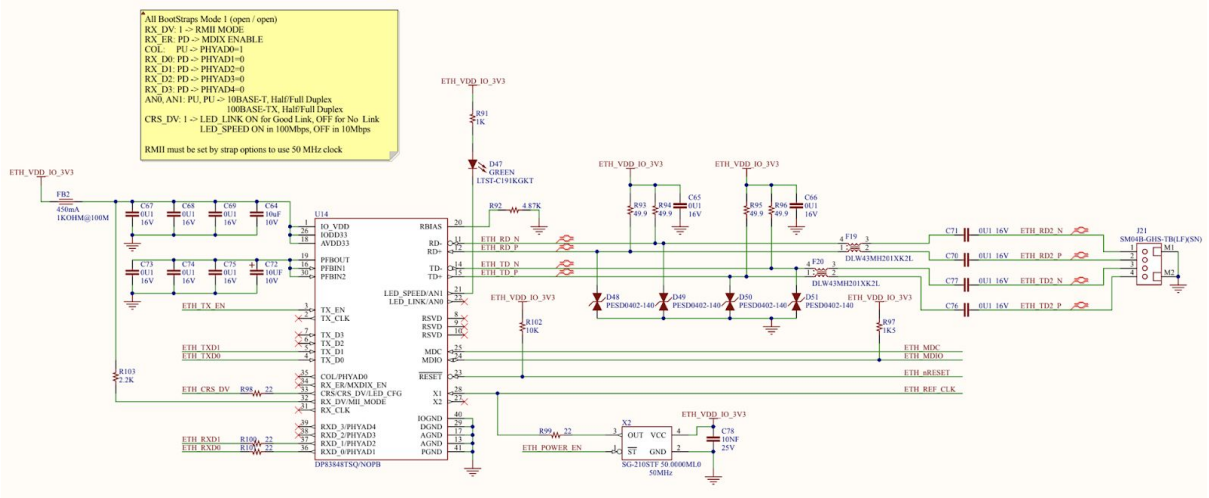
Peripheral Power Protection



Baseboard EEPROM and Sensor Connections



Ethernet Transceiver



GPS / Audio Interface