Design Assignment on Building an IC TESTER

Prepared for

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CS F241 - Microprocessor Programming and Interfacing

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Problem Statement

Design a Microprocessor based Tester to test the logical functioning of the following chips:

- 7400
- 7408
- 7432
- 7486
- 747266

The IC to be tested will be inserted in a 14 pin ZIF socket.
The IC number is to be entered via a keyboard. The keyboard has keys 0-9, backspace, enter and test.
The user places the IC in the ZIF socket closes it – then enters the IC No, followed by enter key.
The IC No. is displayed on the 7-segment display.
The testing will start once the user presses “TEST” key.
After Test the result PASS/FAIL must be displayed on the 7-segment display.

Assumptions

The following assumptions have been considered in the designing of the IC Tester:

- Only “TEST” key will be pressed after “ENTER” key.
- If IC is not entered properly, or ZIF Socket is not closed, then “FAIL” will be displayed.
- First key pressed is always a digit.

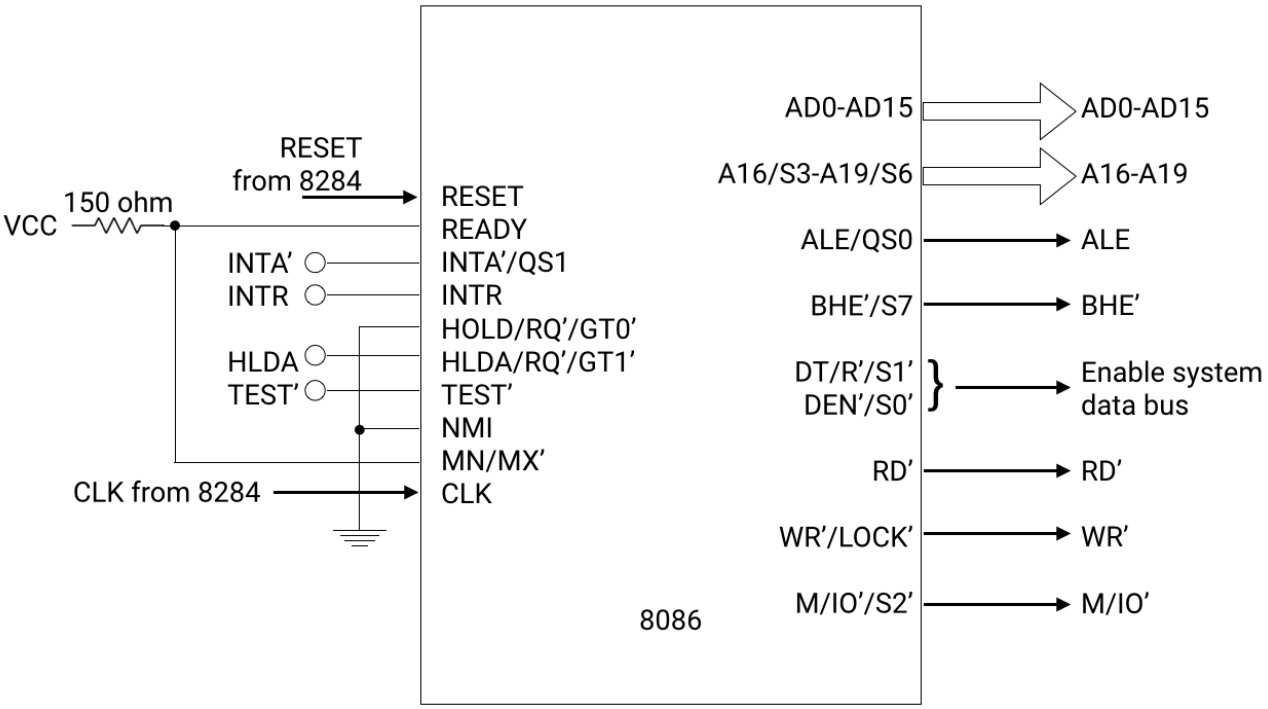
User Guide

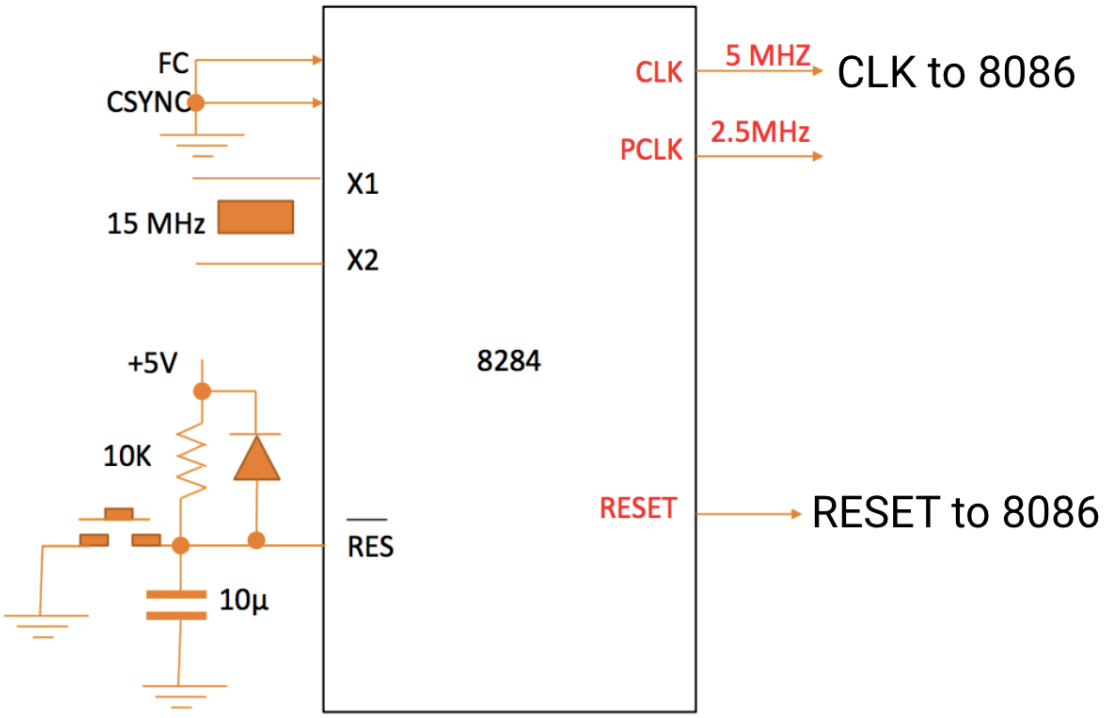
1. Enter the IC in the ZIF Socket and lock it.
2. Enter the IC number by pressing the keys on the keypad.
3. Press “ENTER” key on the keypad.
4. IC number will be displayed.
5. Press “TEST” key on the keypad.
6. If the IC is valid, “PASS” will be displayed.
7. Else, “FAIL” will be displayed.
8. In case a wrong digit is typed, use “BACKSPACE” key to erase that digit.

List of ICs and Components Used

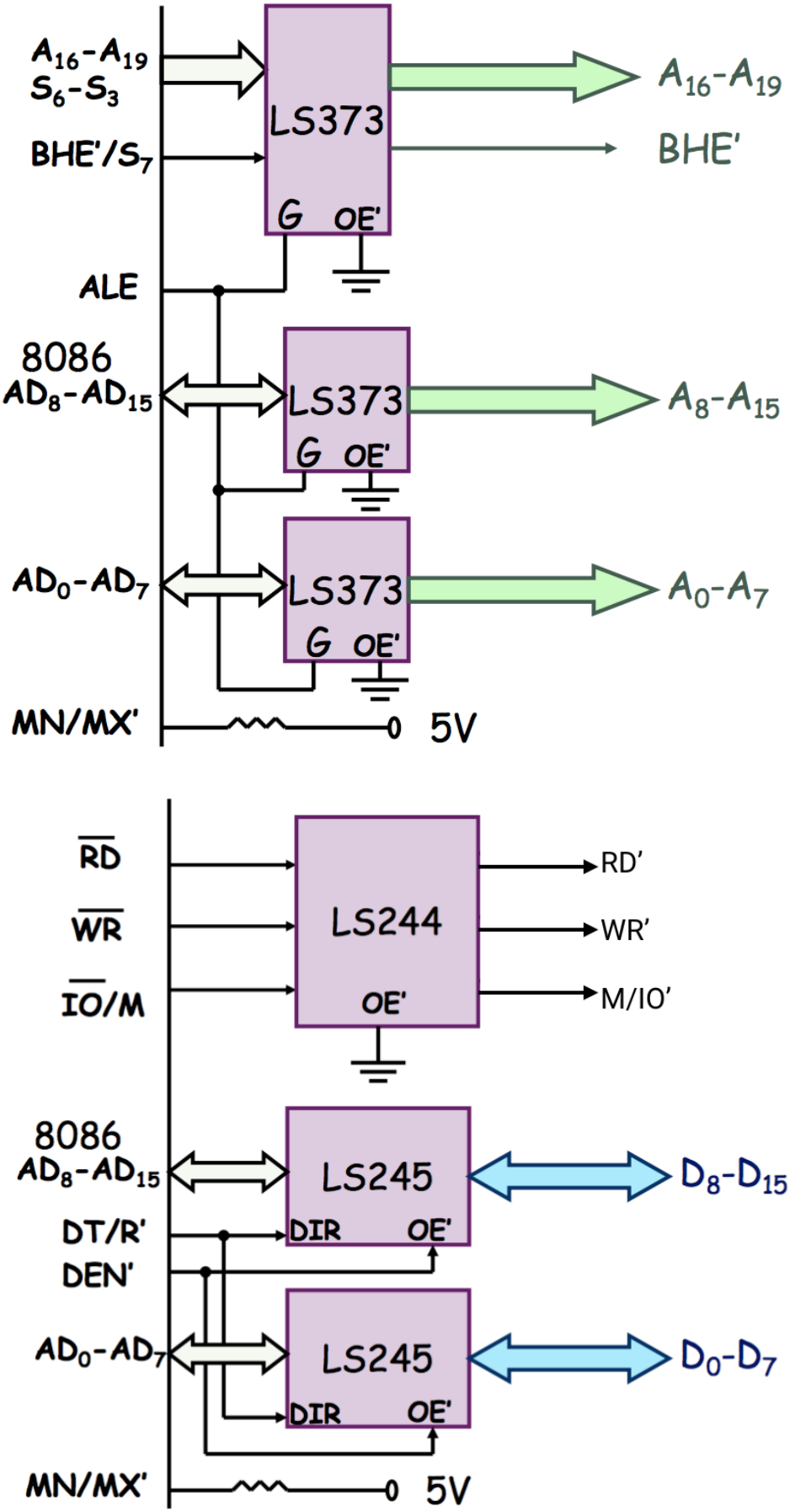
Component	Quantity
8086 (Microprocessor)	1
8284A	1
8255A	2
74LS138 (3:8 Decoder)	2
NL7SZ19 (2:4 Decoder)	2
LS373	3
LS244	1
LS245	2
6116 (2KB RAM)	2
2716 (2KB ROM)	4
7-Segment Anode Display	6
Switch	17
14 pin ZIF Socket	1
10K ohm Resistor	4
150 ohm Resistor	10
690 ohm Resistor	6
2N2905 (BJT)	10

Connections





System Bus of 8086



Memory Interfacing

4K ROM starting at 00000H
4K RAM starting at 01000H
4K ROM starting at FF000H

Number of Chips

2K ROM Chips (chip number) = 4
2K RAM Chips (chip number) = 2

Memory Allocation

ROM1 (even):	00000H,	00002H,	00004H,	. . . ,	00FFEH
ROM1 (odd):	00001H,	00003H,	00005H,	. . . ,	00FFFH
RAM1 (even):	01000H,	01002H,	01004H,	. . . ,	01FFEH
RAM1 (odd):	01001H,	01003H,	01005H,	. . . ,	01FFFH
ROM2 (even):	FF000H,	FF002H,	FF004H,	. . . ,	FFFFEH
ROM2 (odd):	FF001H,	FF003H,	FF005H,	. . . ,	FFFFFH

ROM1: 00000H - 00FFFH

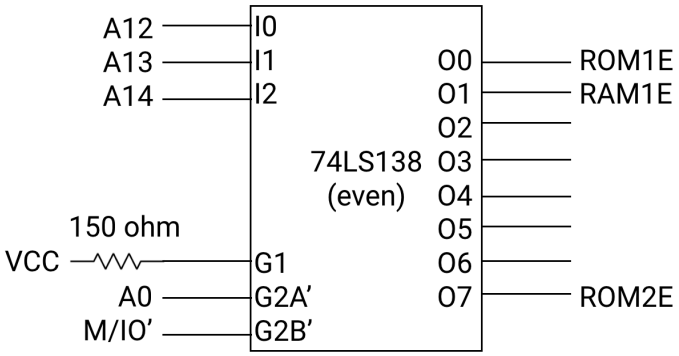
A19	A18	A17	A16	A15	A14	A13	A12	A11	. . .	A0
0	0	0	0	0	0	0	0	0	. . .	0
0	0	0	0	0	0	0	0	1	. . .	1

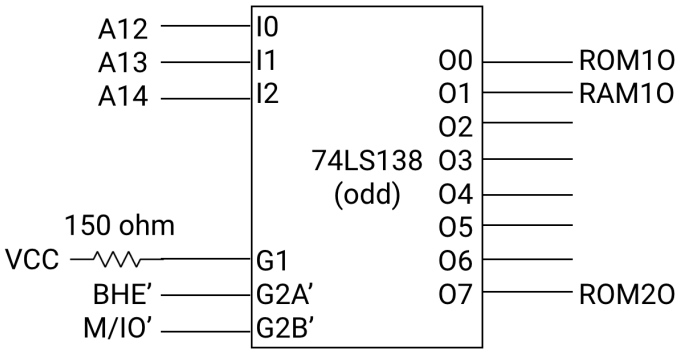
RAM1: 01000H - 01FFFH

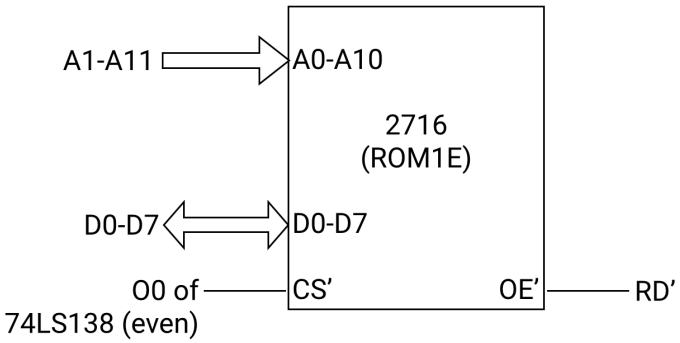
A19	A18	A17	A16	A15	A14	A13	A12	A11	. . .	A0
0	0	0	0	0	0	0	1	0	. . .	0
0	0	0	0	0	0	0	1	1	. . .	1

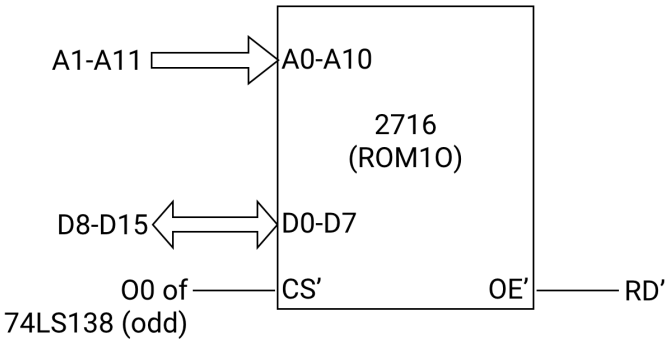
ROM2: FF000H- FFFFFH

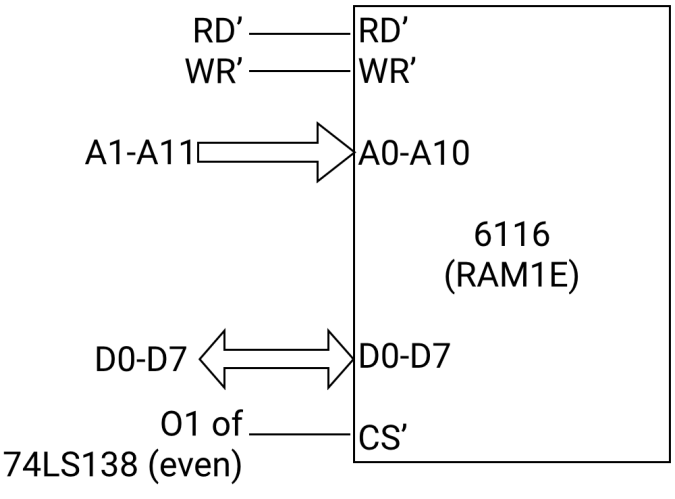
A19	A18	A17	A16	A15	A14	A13	A12	A11	. . .	A0
1	1	1	1	1	1	1	1	0	. . .	0
1	1	1	1	1	1	1	1	1	. . .	1

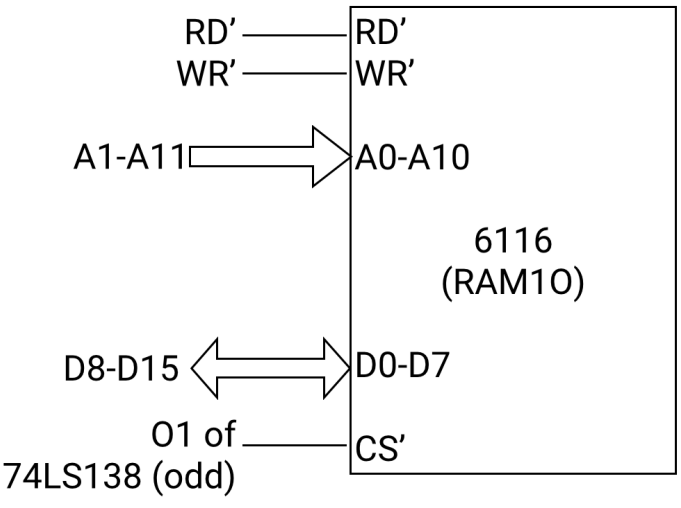


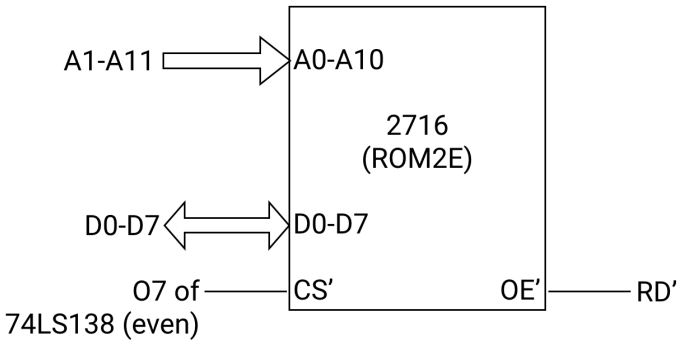


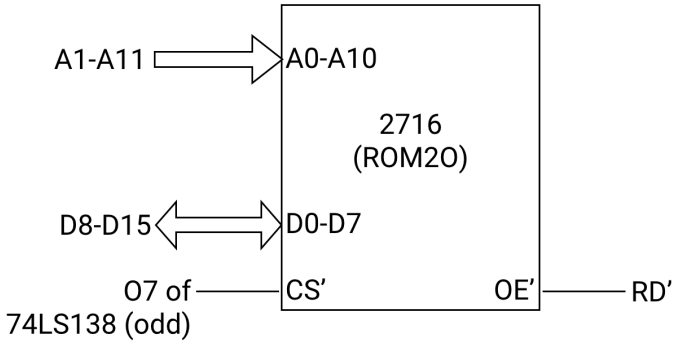









A1-A11
A0-A10
2716
(ROM2E)
D0-D7
D0-D7
O7 of
74LS138 (even)
CS'
OE'
RD'


A1-A11
A0-A10
2716
(ROM2O)
D8-D15
D0-D7
O7 of
74LS138 (odd)
CS'
OE'
RD'

Input-Output Interfacing

I/O Allocation

8255A(1):	00000H,	00002H,	00004H,	00006H
8255A(2):	00008H	0000AH	0000CH	0000EH

8255A(1): 00000H - 00007H

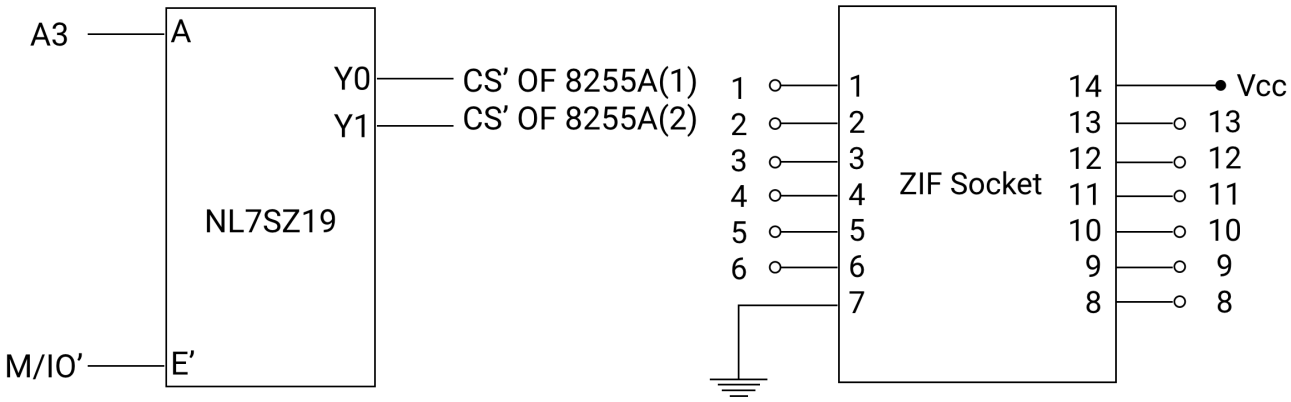
A19	A18	A17	. . .	A6	A5	A4	A3	A2	A1	A0
0	0	0	. . .	0	0	0	0	0	0	0
0	0	0	. . .	0	0	0	0	1	1	1

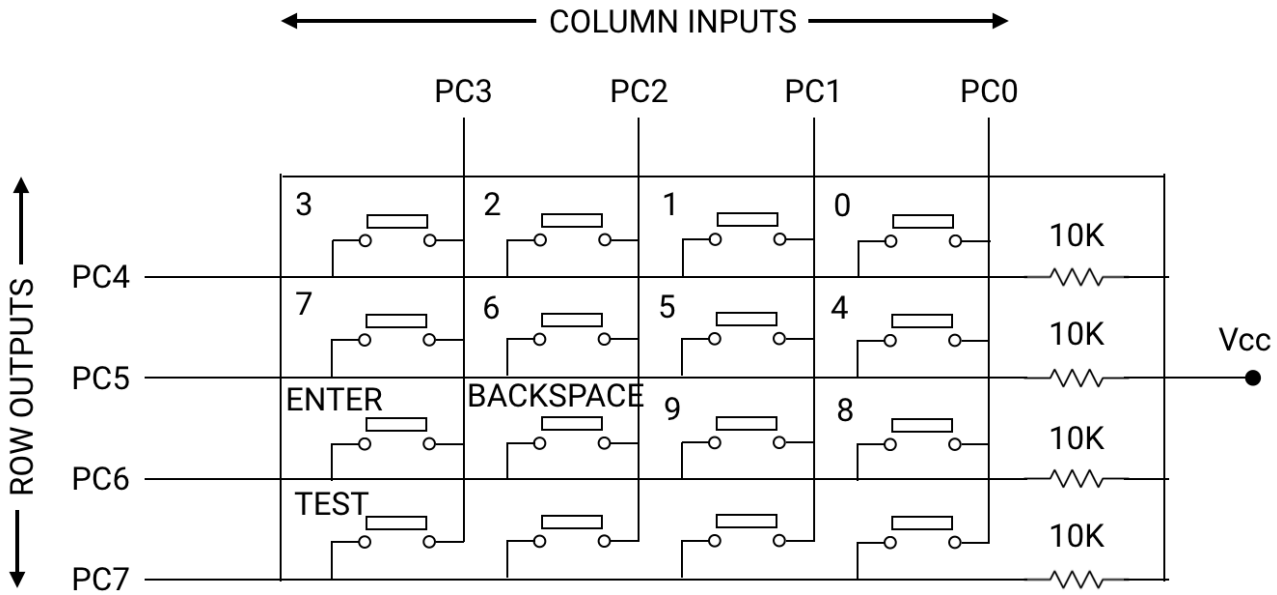
8255A(2): 00008H - 0000FH

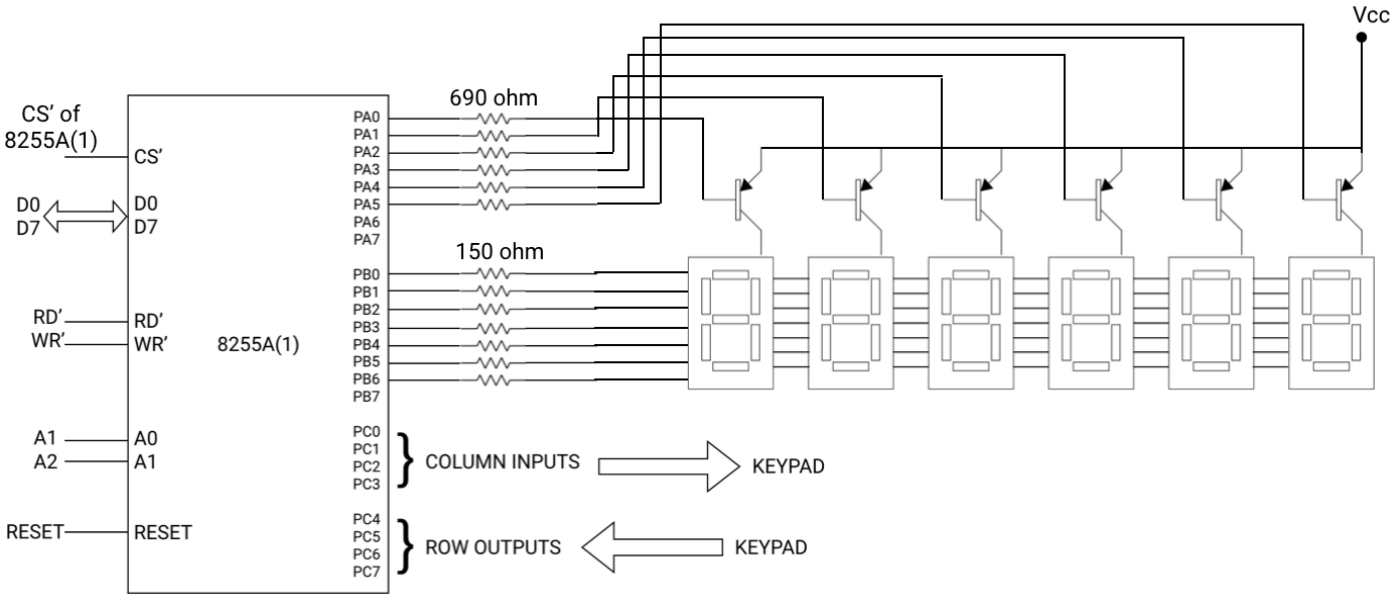
A19	A18	A17	. . .	A6	A5	A4	A3	A2	A1	A0
0	0	0	. . .	0	0	0	1	0	0	0
0	0	0	. . .	0	0	0	1	1	1	1

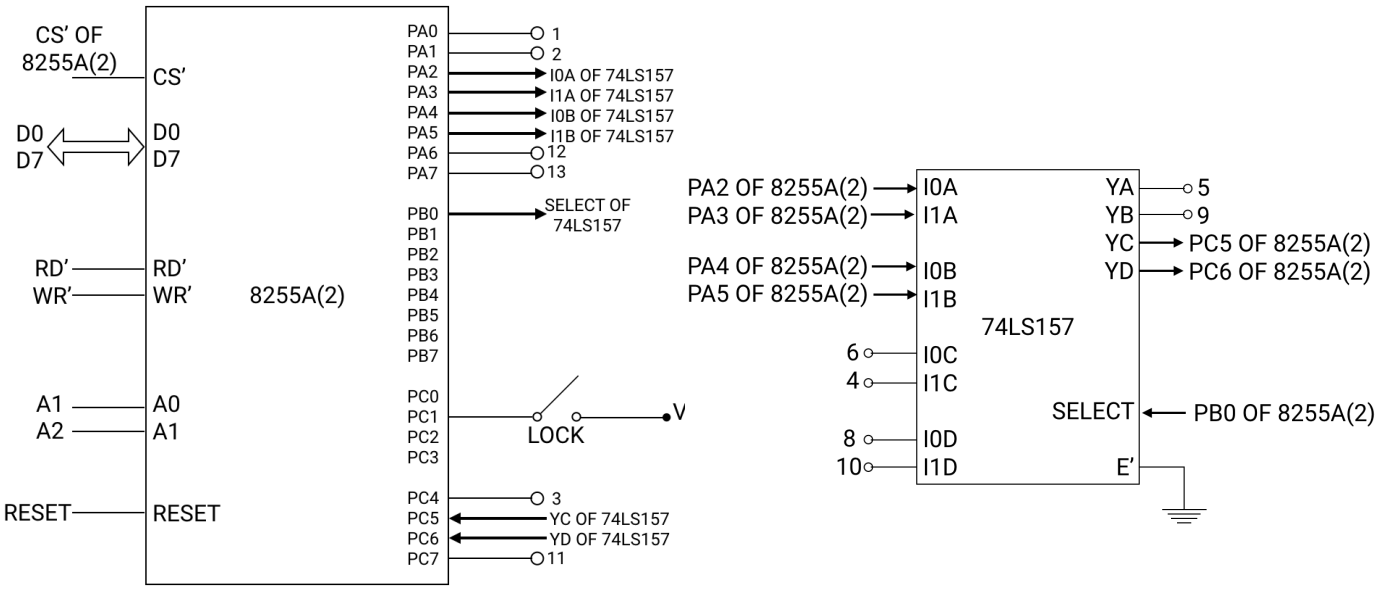
I/O Pins of ICs to be tested

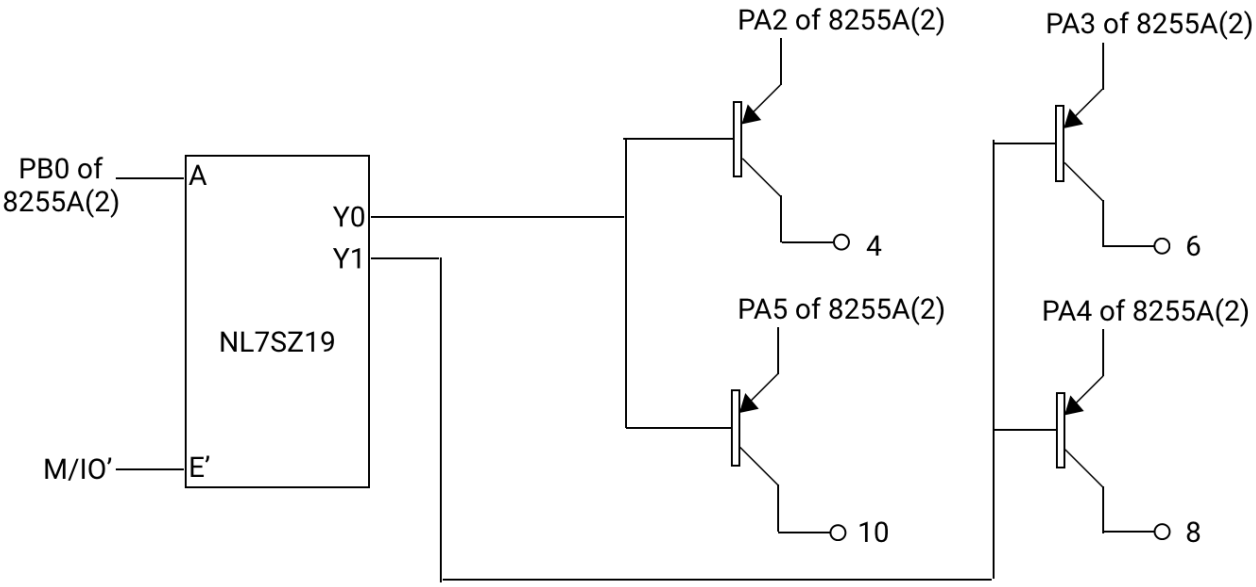
IC	1	2	3	4	5	6	7	8	9	10	11	12	13	14
7400	1A	1B	1Y	2A	2B	2Y	GND	3Y	3A	3B	4Y	4A	4B	VCC
7408	1A	1B	1Y	2A	2B	2Y	GND	3Y	3A	3B	4Y	4A	4B	VCC
7432	1A	1B	1Y	2A	2B	2Y	GND	3Y	3A	3B	4Y	4A	4B	VCC
7486	1A	1B	1Y	2A	2B	2Y	GND	3Y	3A	3B	4Y	4A	4B	VCC
747266	1A	1B	1Y	2Y	2A	2B	GND	3A	3B	3Y	4Y	4A	4B	VCC


A3
A
Y0
CS' OF 8255A(1)
Y1
CS' OF 8255A(2)
NL7SZ19
M/IO'
E'
1
2
3
4
5
6
7
ZIF Socket
14
13
12
11
10
9
8
Vcc

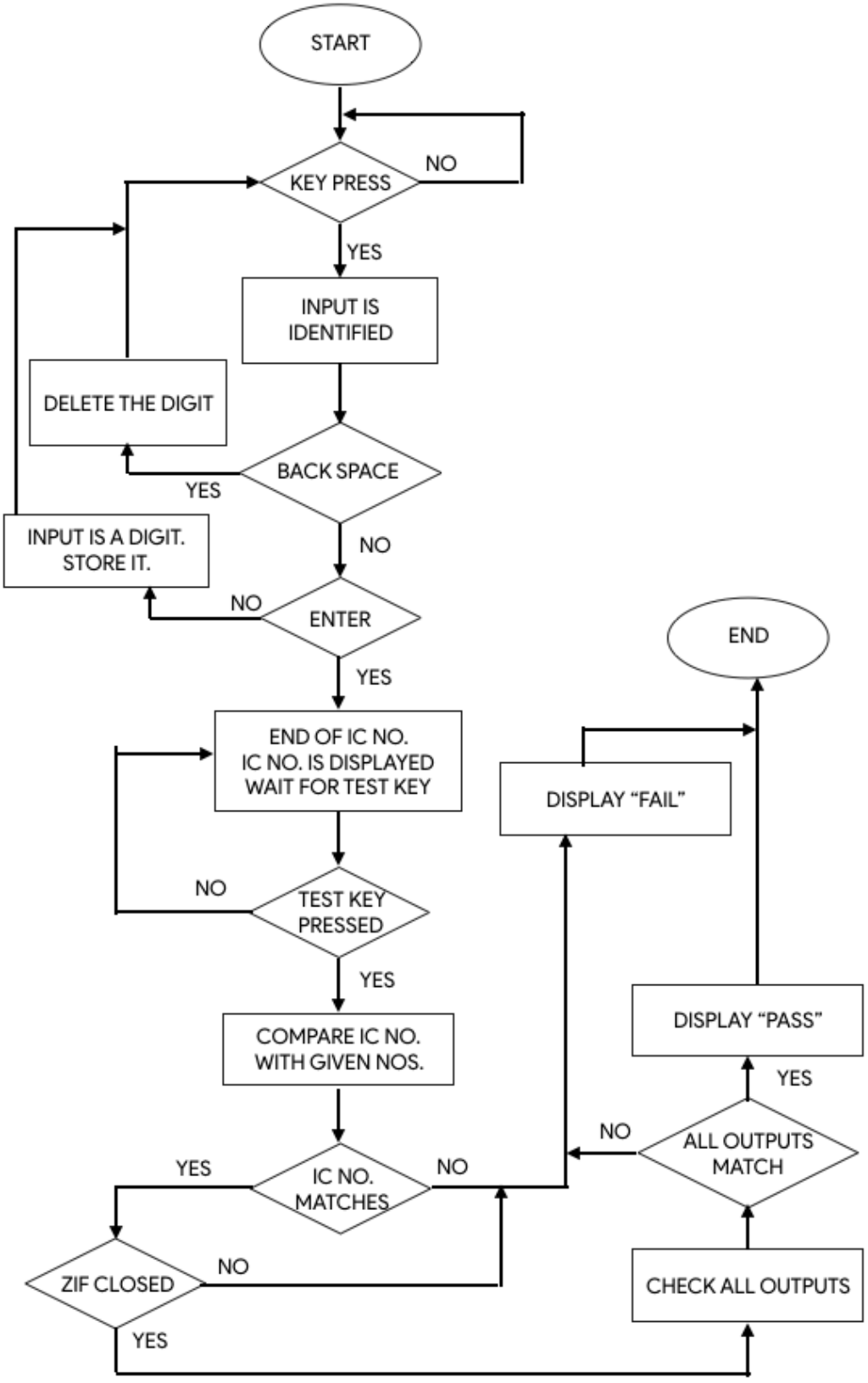

COLUMN INPUTS
PC3
PC2
PC1
PC0
ROW OUTPUTS
PC4
PC5
PC6
PC7
3
2
1
0
7
6
5
4
ENTER
BACKSPACE
9
8
TEST
10K
Vcc


Vcc
CS' of
8255A(1)
CS'
D0
D7
RD'
WR'
8255A(1)
A1
A2
A0
A1
RESET
690 ohm
150 ohm
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
COLUMN INPUTS
KEYPAD
PC4
PC5
PC6
PC7
ROW OUTPUTS
KEYPAD


CS' OF 8255A(2)
CS'
D0
D7
D0
D7
RD'
WR'
RD'
WR'
8255A(2)
A1
A2
A0
A1
RESET
RESET
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
1
2
I0A OF 74LS157
I1A OF 74LS157
I0B OF 74LS157
I1B OF 74LS157
12
13
SELECT OF 74LS157
LOCK
V
3
YC OF 74LS157
YD OF 74LS157
11
PA2 OF 8255A(2)
PA3 OF 8255A(2)
PA4 OF 8255A(2)
PA5 OF 8255A(2)
I0A
I1A
I0B
I1B
74LS157
6
4
8
10
I0C
I1C
I0D
I1D
YA
YB
YC
YD
SELECT
E'
5
9
PC5 OF 8255A(2)
PC6 OF 8255A(2)
PB0 OF 8255A(2)


PB0 of 8255A(2)
A
Y0
Y1
NL7SZ19
M/IO'
E'
PA2 of 8255A(2)
4
PA3 of 8255A(2)
6
PA5 of 8255A(2)
10
PA4 of 8255A(2)
8

Flow Chart


START
KEY PRESS
NO
YES
INPUT IS IDENTIFIED
DELETE THE DIGIT
BACK SPACE
YES
NO
INPUT IS A DIGIT. STORE IT.
NO
ENTER
YES
END
END OF IC NO. IC NO. IS DISPLAYED WAIT FOR TEST KEY
DISPLAY "FAIL"
NO
TEST KEY PRESSED
YES
DISPLAY "PASS"
COMPARE IC NO. WITH GIVEN NOS.
YES
NO
ALL OUTPUTS MATCH
YES
IC NO. MATCHES
NO
ZIF CLOSED
NO
CHECK ALL OUTPUTS
YES