EE577B HW2 Part C: Testbench Analysis and Verification

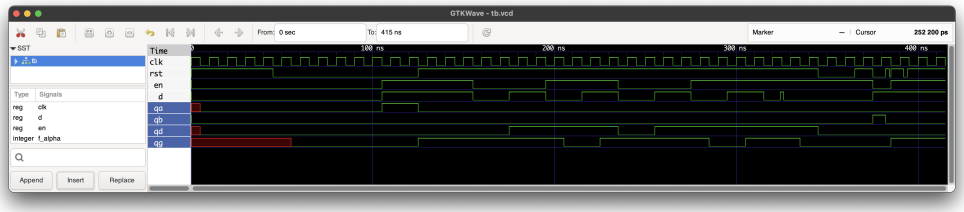
Testbench configuration

Clock frequency is 100 MHz with period 10 ns. Sampling occurs on every negative edge at times 5 ns, 15 ns, 25 ns, and so on. The shared reset signal `rst` is used by all four DFFs which internally interpret polarity and synchrony as required by the specification:

Module	Reset mechanism	Reset polarity	Data enable polarity
`dff_alpha`	Synchronous	Active HIGH	Active HIGH
`dff_beta`	Asynchronous	Active HIGH	Active LOW
`dff_gamma`	Synchronous	Active LOW	Active HIGH
`dff_delta`	Asynchronous	Active LOW	Active LOW

The testbench asserts reset for five clock cycles at the beginning as follows. From 0 ns to 50 ns `rst` is `1` which asserts alpha and beta. From 50 ns to 100 ns `rst` is `0` which asserts gamma and delta. After 100 ns the stimulus drives explicit scenarios for functional coverage. Console timestamps provided in picoseconds have been interpreted in nanoseconds for readability.

Waveforms



Phase 1: initial assertion for alpha and beta

Times from 0 ns to 50 ns with `rst` equal to `1`, `en` equal to `0`, `d` equal to `0`.

- At 0 ns: `qa` is unknown then becomes `0` at the first negative edge 5 ns due to synchronous active HIGH reset. `qb` is `0` immediately due to asynchronous active HIGH reset. `qg` remains unknown because gamma is not asserted in this phase and enable is low. `qd` becomes `0` at negative edges since delta has active LOW enable and captures `d` = 0.
- Observed lines at 5 ns, 15 ns, 25 ns, 35 ns, 45 ns match the above.

Phase 2: initial assertion for gamma and delta

Times from 50 ns to 100 ns with `rst` equal to `0`.

- `qg` becomes `0` at the next negative edge 55 ns due to synchronous active LOW reset. `qd` is held at `0` by asynchronous active LOW reset. `qa` and `qb` remain `0`. All outputs are `0` by 55 ns and remain `0` through 100 ns.

Alpha sanity capture

Times 105 ns to 120 ns with `rst` deasserted for alpha by setting `rst` equal to `0`, and with `en` equal to `1`, `d` equal to `1` prior to a negative edge.

- At 105 ns `qa` becomes `1`. This proves correct operation of alpha with synchronous active HIGH reset and active HIGH enable.

Gamma sanity capture

Times 125 ns to 140 ns with `rst` deasserted for gamma by setting `rst` equal to `1`, and with `en` equal to `1`, `d` equal to `1` prior to a negative edge.

- At 125 ns `qg` becomes `1`. This proves correct operation of gamma with synchronous active LOW reset and active HIGH enable. In the same window alpha is returned to reset because `rst` is `1` which is the active level for alpha.

Exhaustive enable and data combinations

A neutral region is maintained by holding `rst` at the deasserted level for all four modules and cycling through all (`en`, `d`) pairs.

- When `en` equals `1`, alpha and gamma capture `d` on negative edges while beta and delta hold their previous values. This behavior is visible at 205 ns to 235 ns and again later.
- When `en` equals `0`, beta and delta capture `d` on negative edges while alpha and gamma hold. This behavior is visible at 175 ns, 205 ns, 235 ns, and subsequent repetitions.

Data timing relative to the sampling edge

- At 324 ns and 325 ns the stimulus changes `d` just before a negative edge then just after a negative edge. Values are captured only at the negative edge as expected. The capture one nanosecond before the edge is effective at the next negative edge. The change one nanosecond after the edge is not visible until the following negative edge.

Synchronous reset demonstrations

- For alpha with synchronous active HIGH reset, asserting `rst` equal to `1` across a negative edge returns `qa` to `0` at that edge. This is observed in the region around 345 ns to 370 ns.
- For gamma with synchronous active LOW reset, asserting `rst` equal to `0` across a negative edge returns `qg` to `0` at that edge. This is observed in the same region when `rst` is driven low.

Asynchronous reset demonstrations

- For beta with asynchronous active HIGH reset, a mid cycle assertion of `rst` equal to `1` forces `qb` to `0` immediately without waiting for a clock edge. The console shows `qb` equal to `1` at 375 ns followed by `qb` equal to `0` when `rst` is pulsed at 382 ns.
- For delta with asynchronous active LOW reset, a mid cycle assertion of `rst` equal to `0` forces `qd` to `0` immediately. This is visible in the region around 392 ns.

Verification summary

- Initial five cycle assertions verify both reset polarities at the beginning of simulation.
- Alpha and gamma captures with `en` equal to `1` and `d` equal to `1` confirm synchronous operation and correct polarity handling.
- Exhaustive (`en`, `d`) combinations demonstrate enable polarity for all modules.
- Timing checks around the negative edge confirm edge aligned sampling.
- Synchronous resets take effect only on the next negative edge. Asynchronous resets take effect immediately.