MAKERERE  UNIVERSITY

COLLEGE OF ENGINEERING, DESIGN, ART AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

SCHOOL OF ENGINEERING

BACHELOR OF SCIENCE IN ELECTRICAL ENGINEERING

YEAR THREE

ELE3103: APPLIED DIGITAL ELECTRONICS

GROUP ASSIGNMENT 2

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Question One

The following figure shows the intersection of a main highway with a secondary access road. Vehicle-detection sensors are placed along lanes C and D (main road) and lanes A and B (access road). These sensor outputs are LOW (0) when no vehicle is present and HIGH (1) when a vehicle is present. The intersection traffic light is to be controlled according to the following logic:

1. The East-West (E-W) traffic light is green when both lanes C and D are occupied.
2. The E-W light is green when either C or D is occupied but lanes A and B are both not occupied.
3. The North-South (N-S) light is green whenever both lanes A and B are occupied but C and D are not both occupied.
4. The N-S light is also green when either A or B is occupied while C and D are both vacant.
5. The E-W light is green when no vehicles are present. There should be two outputs, N-S and E-W, that go HIGH when the corresponding light is to be green.

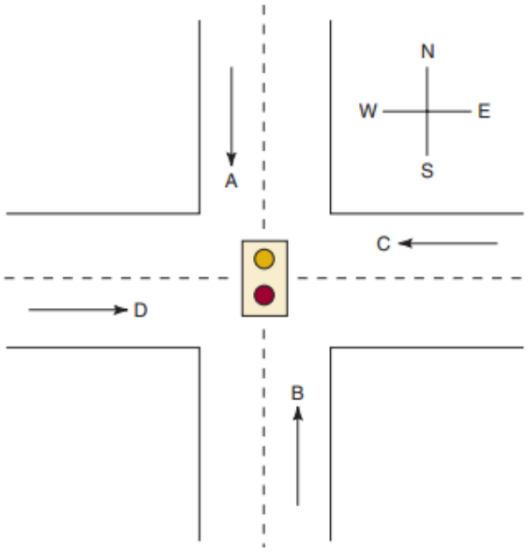


Figure 1: The intersection of a main highway with a secondary access road

(a)

Using the sensor outputs A, B, C, and D as inputs, design a logic circuit to control the traffic light.

truth table for the logic

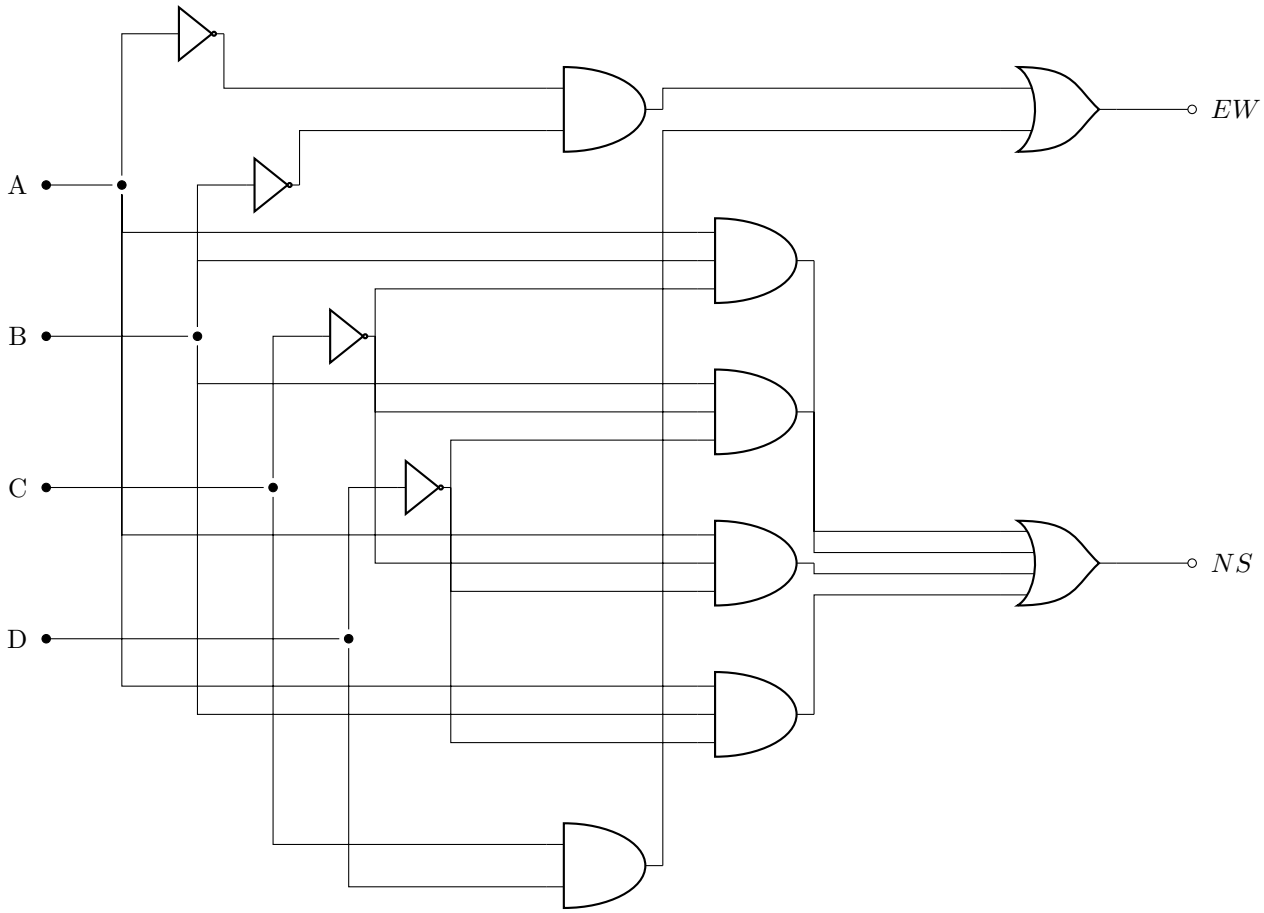
A	B	C	D	E-W	N-S	
0	0	0	0	1	0	$\overline{A}\overline{B}\overline{C}\overline{D}$
0	0	0	1	1	0	$\overline{A}\overline{B}\overline{C}D$
0	0	1	0	1	0	$\overline{A}\overline{B}C\overline{D}$
0	0	1	1	1	0	$\overline{A}\overline{B}CD$
0	1	0	0	0	1	$\overline{A}B\overline{C}\overline{D}$
0	1	0	1	0	0	
0	1	1	0	0	0	
0	1	1	1	1	0	$\overline{A}BCD$
1	0	0	0	0	1	$A\overline{B}\overline{C}\overline{D}$
1	0	0	1	0	0	
1	0	1	0	0	0	
1	0	1	1	1	0	$A\overline{B}CD$
1	1	0	0	0	1	$AB\overline{C}\overline{D}$
1	1	0	1	0	1	$AB\overline{C}D$
1	1	1	0	0	1	$ABC\overline{D}$
1	1	1	1	1	0	$ABCD$

AB \ CD	00	01	11	10
00	1	1	1	1
01	0	0	1	0
11	0	0	1	0
10	0	0	1	0

$$E - W = \overline{A}\overline{B} + CD$$

AB \ CD	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	1	0	1
10	1	0	0	0

$$N - S = B\overline{C}\overline{D} + AB\overline{C} + A\overline{C}\overline{D} + AB\overline{D}$$



(b)

Use Quartus software to implement the circuit in (a). Show the code, RTL viewer schematic, and timing diagram of the circuit performance.

```
SUBDESIGN GROUPASSIGNMENT1
(
    A,B,C,D      : INPUT;
    E_W, N_S     : OUTPUT;
)
VARIABLE
    E,F,Y,H,G,T : NODE;
BEGIN
    E = !A&!B;
    F = C&D;
    Y = !D&B&A;
    H= !C&B&A;
    G = B&!C&!D;
    T = A&!C&!D;
    N_S = T#G#H#Y;
    E_W = E#F;
END;
```

Figure 2: The AHDL code for the circuit in question 1

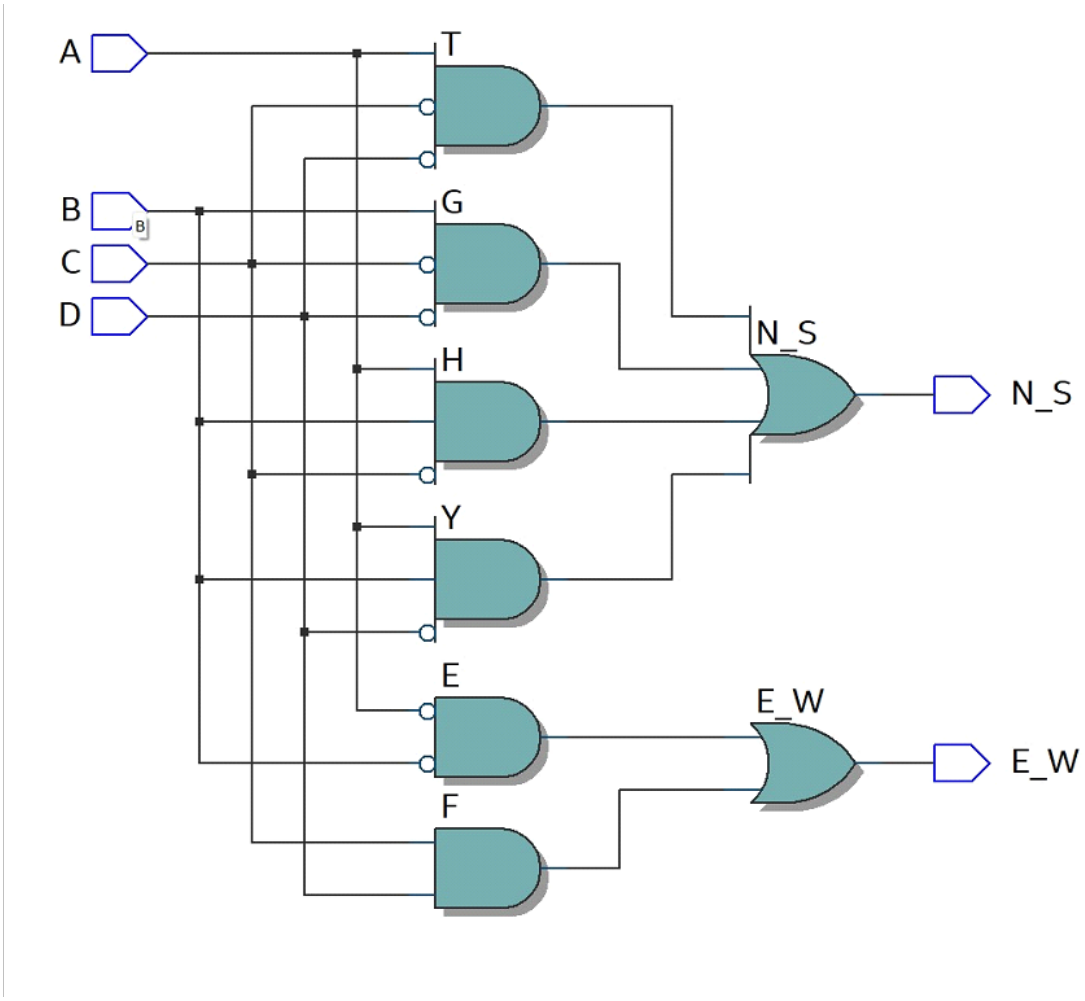


Figure 3: The Quartus generated schematic for the circuit in question 1

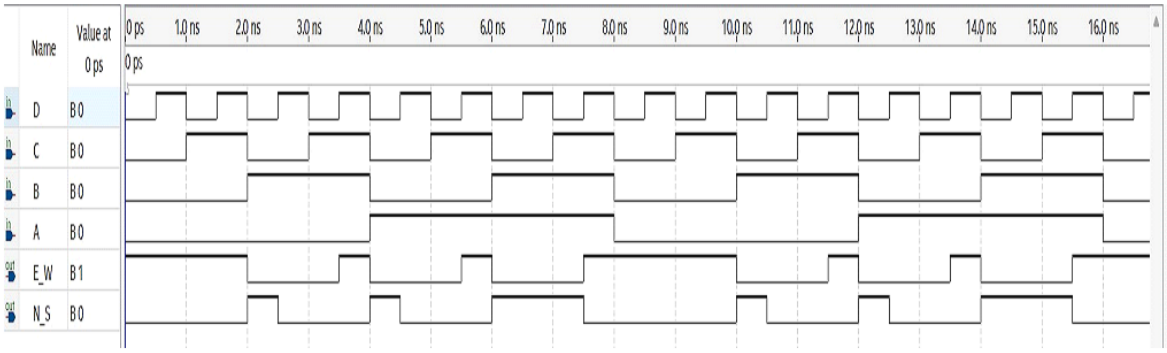


Figure 4: Timing diagram for the circuit in question 1

Question 2

The following figure shows an automobile alarm circuit used to detect certain undesirable conditions. The three switches are used to indicate the status of the door by the driver‘s seat, the ignition, and the headlights, respectively.

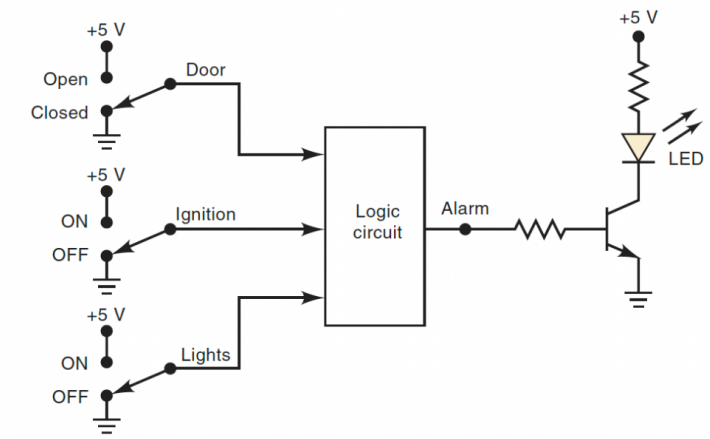


Figure 5: An automobile alarm circuit used to detect certain undesirable conditions

(a)

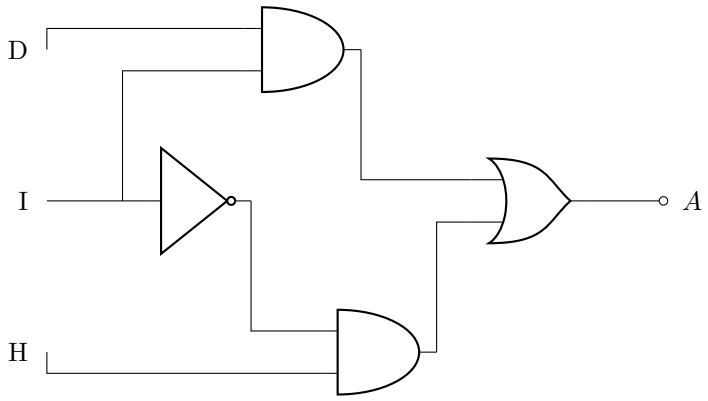
Design the logic circuit with these three switches as inputs so that the alarm is activated whenever either of the following conditions exists: i. The headlights are on while the ignition is off. ii. The door is open while the ignition is on

let D = door I = ignition H= lights A = alarm

H	I	D	A	
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	$\bar{H}ID$
1	0	0	1	$H\bar{I}\bar{D}$
1	0	1	1	$H\bar{I}D$
1	1	0	0	
1	1	1	1	HID

H \ ID	00	01	11	10
0	0	0	1	0
1	1	1	1	0

$$A = H\bar{I} + ID$$



(b)

Use Quartus software to implement the circuit in (a). Show the code, RTL viewer schematic, and timing diagram of the circuit performance.

```
1   SUBDESIGN GROUPASSIGNMENT2
2   (
3       H,I,D : INPUT;
4       A     : OUTPUT;
5   )
6   VARIABLE
7       M,N   : NODE;
8   BEGIN
9       M = D&I;
10      N = H&!I;
11      A = M#N;
12  END;
13
```

Figure 6: The AHDL code for the circuit in question 2

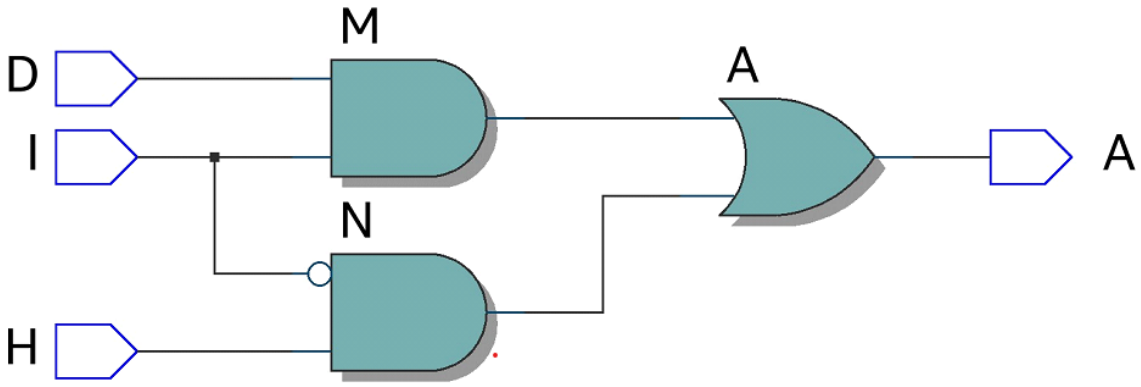


Figure 7: The Quartus generated schematic for the circuit in question 2

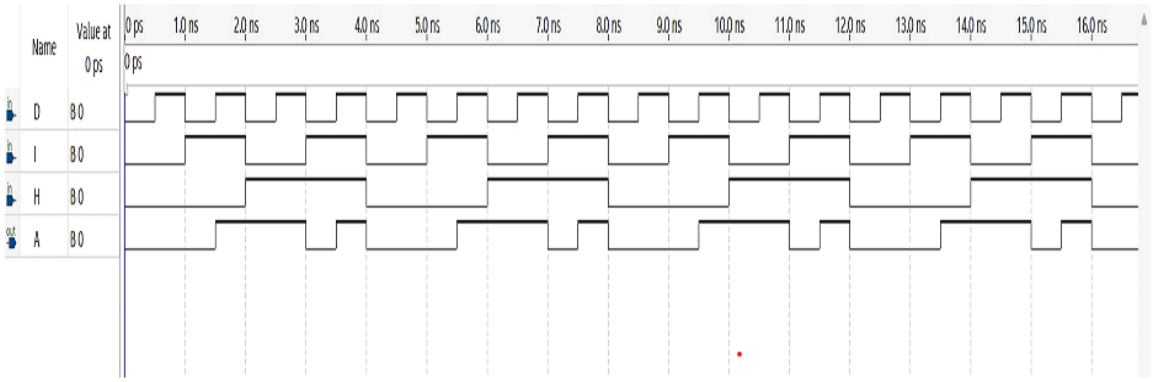


Figure 8: Timing diagram for the circuit in question 2

Question 3

The following figure shows four switches that are part of the control circuitry in a copy machine. The switches are at various points along the path of the copy paper as the paper passes through the machine. Each switch is normally open, and as the paper passes over a switch, the switch closes. It is impossible for switches SW1 and SW4 to be closed at the same time.

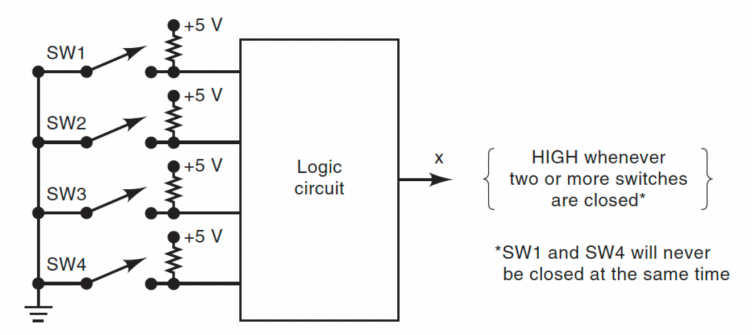


Figure 9: Four switches that are part of the control circuitry in a copy machine

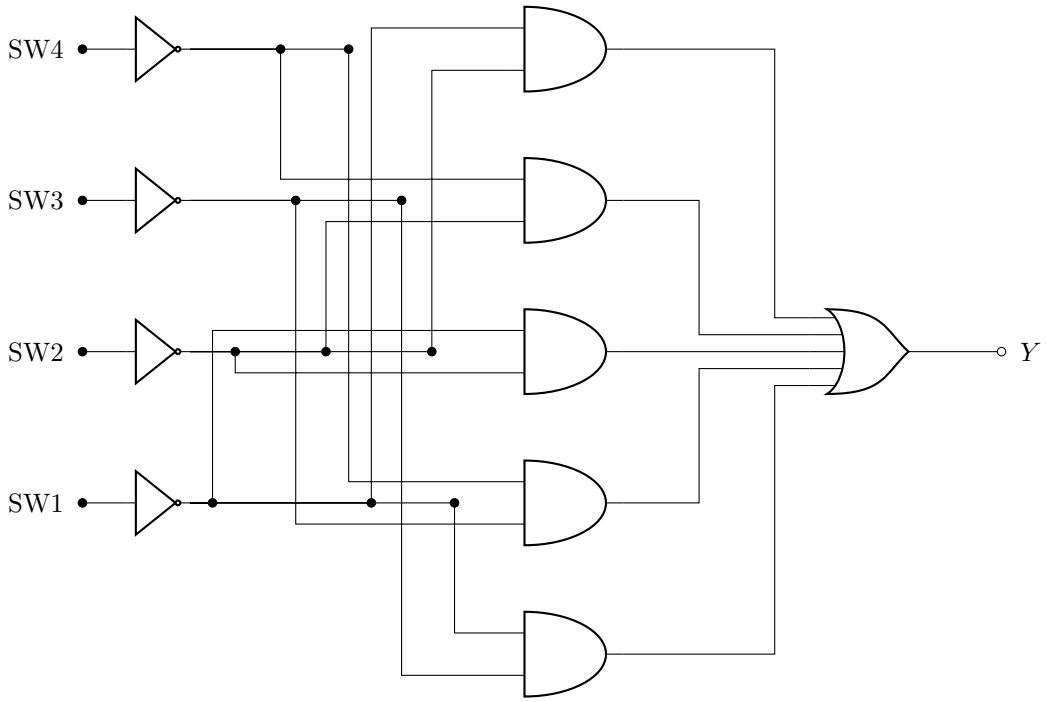
(a)

Design the logic circuit to produce a HIGH output whenever two or more switches are closed at the same time. Use K mapping and take advantage of the don‘t-care conditions.

SW4	SW3	SW2	SW1	Y	
0	0	0	0	x	
0	0	0	1	1	$\overline{SW4}\overline{SW3}\overline{SW2}SW1$
0	0	1	0	x	
0	0	1	1	1	$\overline{SW4}\overline{SW3}SW2SW1$
0	1	0	0	x	
0	1	0	1	1	$\overline{SW4}SW3\overline{SW2}SW1$
0	1	1	0	x	
0	1	1	1	0	
1	0	0	0	1	$SW4\overline{SW3}\overline{SW2}\overline{SW1}$
1	0	0	1	1	$SW4\overline{SW3}\overline{SW2}SW1$
1	0	1	0	1	$SW4\overline{SW3}SW2\overline{SW1}$
1	0	1	1	0	
1	1	0	0	1	$SW4SW3\overline{SW2}\overline{SW1}$
1	1	0	1	0	
1	1	1	0	0	
1	1	1	1	0	

SW4SW3 \ SW2SW1	00	01	11	10
00	x	1	1	x
01	x	1	0	x
11	1	0	0	0
10	1	1	0	1

$$Y = \overline{SW4}\,\overline{SW3} + \overline{SW4}\,\overline{SW2} + \overline{SW2}\,\overline{SW1} + \overline{SW3}\,\overline{SW2} + \overline{SW3}\,\overline{SW1}$$



(b)

Use Quartus software to implement the circuit in (a). Show the code, RTL viewer schematic, and timing diagram of the circuit performance

```
SUBDESIGN GROUPASSIGNMENT3
(
    SW1,SW2,SW3,SW4    : INPUT;
    Y                  : OUTPUT;
)
VARIABLE
    A,B,C,D,E              : NODE;
BEGIN
    A = !SW2&!SW1;
    B = !SW3&!SW1;
    C = !SW4&!SW3;
    D = !SW2&!SW3;
    E = !SW2&!SW4;
    Y = A#B#C#D#E;
END;
```

Figure 10: The AHDL code for the circuit in question 3

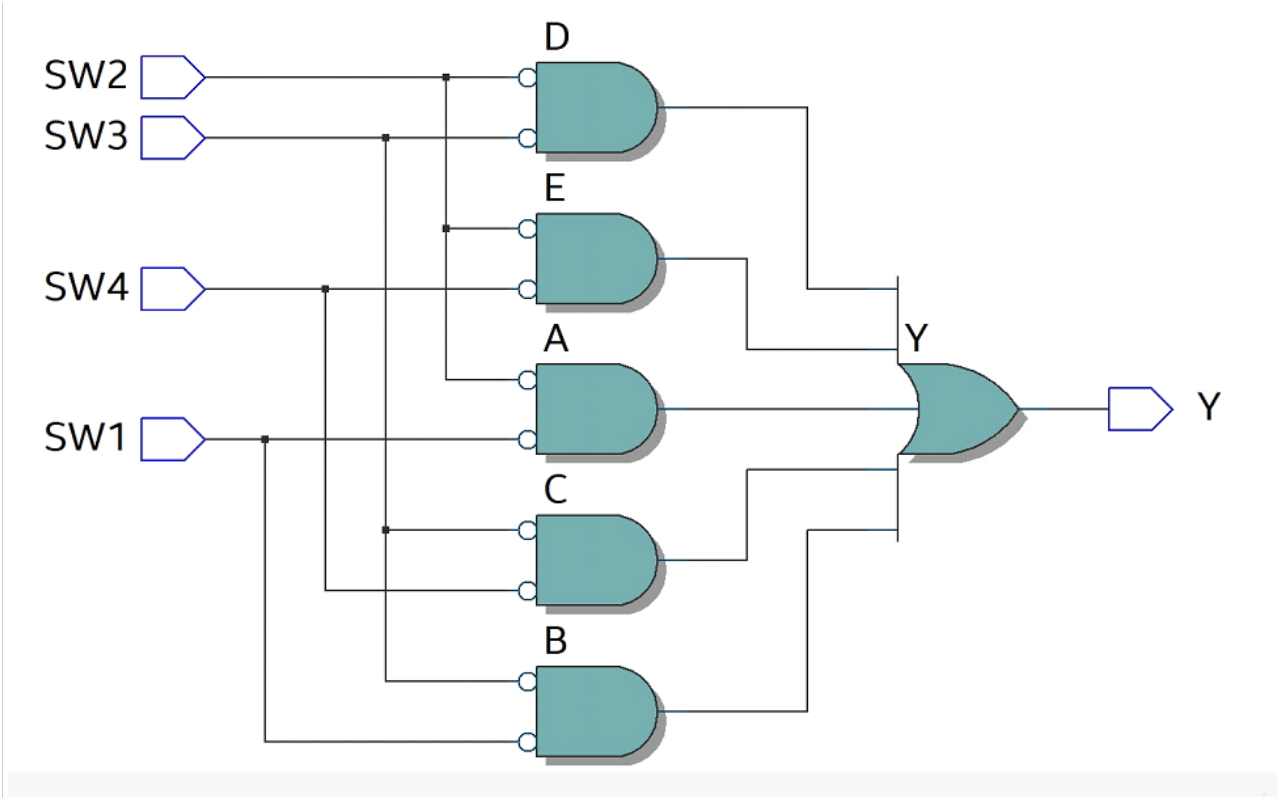


Figure 11: The Quartus generated schematic for the circuit in question 3

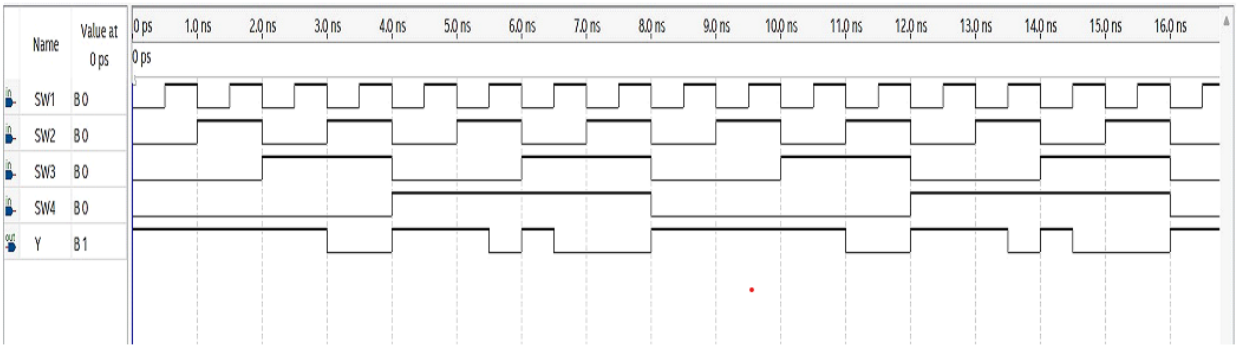


Figure 12: Timing diagram for the circuit in question 3