ESC0830

Flash Macro Datasheet

Version 0.1

Contents

1 Overview

This document is for Flash Macro (FM) at ESC0830.

Features

- HV pumps are embedded as parts of FM to support erase/program operation
- Page size is 512 Bytes
- Sector size is 4K Bytes
- 8K Bytes special area for trimming code and special data storage
- Synchronous read/write operations
- 32 bits data-in and 32 bits data-out
- Less than 1μA leakage current
- 50 ns read access time
- **8.2 ms page write time (0.2 ms pre-program + 6.0 ms page erase + 2.0 ms page program)**
- More than 100K cycles' endurance @85℃
- More than 10 years' data retention @85℃
- The macro must be placed with the x-axis vertical to the wafer notch.

2 Flash Macro Symbol

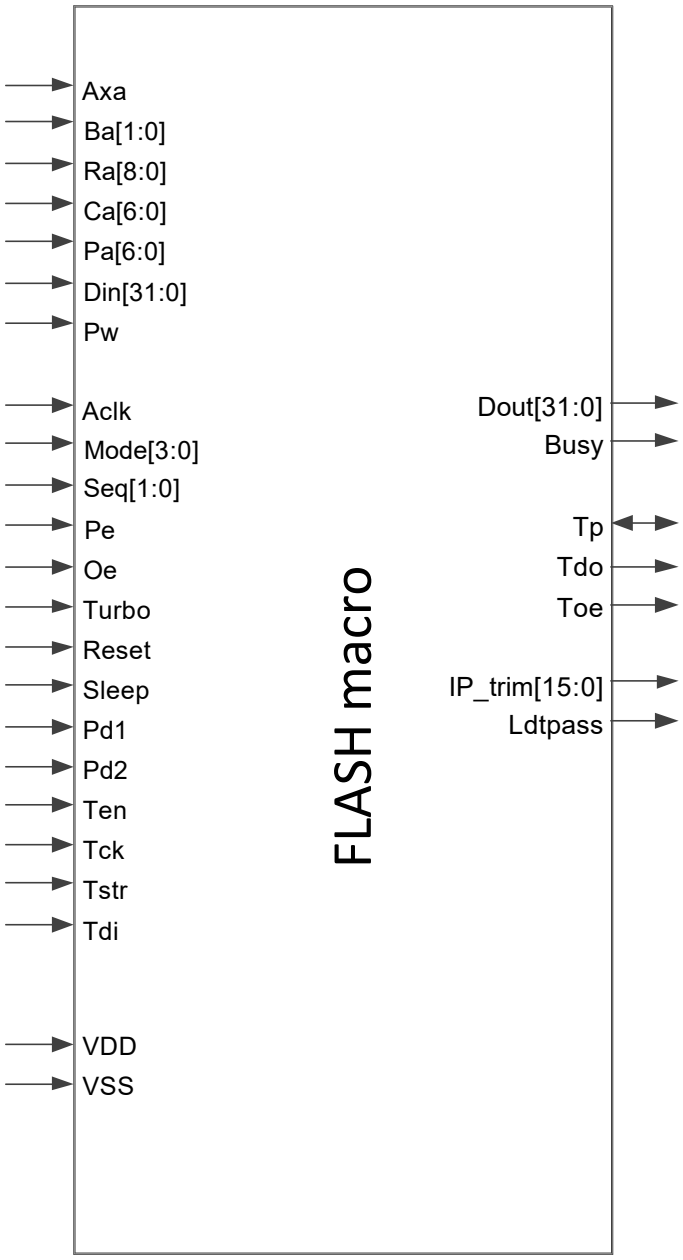


Figure 2-1 Flash macro symbol

3 PIN Description

Table 3-1 Flash macro PIN list and description

PIN Name	In/Out	Signal Type	Description
Axa	In	CMOS	Supervisory memory select address
Ba[1:0]	In	CMOS	Bank address
Ra[8:0]	In	CMOS	Row address
Ca[6:0]	In	CMOS	Column address
Pa[6:0]	In	CMOS	Page latch address
Din[31:0]	In	CMOS	Data in
Pw	In	CMOS	Write page latch clock
Aclk	In	CMOS	Synchronous clock for read and write operation
Mode[3:0]	In	CMOS	Operation mode select
Seq[1:0]	In	CMOS	**N**on-**V**olatile (**NV**) operation sequence control
Pe	In	CMOS	Pump enable
Oe	In	CMOS	Output enable
Turbo	in	CMOS	High to accelerate read reference setup
Reset	In	CMOS	Macro reset
Sleep	In	CMOS	Standby mode enable
Pd1	In	CMOS	Power down switch for trimming register circuitry
Pd2	In	CMOS	Power down switch for FM except trimming register circuitry
Ten	In	CMOS	Test mode input, set to ‘0, when normal operation
Tck	In	CMOS	Test mode input, set to ‘0, when normal operation
Tstr	In	CMOS	Test mode input, set to ‘0, when normal operation
Tdi	In	CMOS	Test mode input, set to ‘0, when normal operation
Ldtpass	Out	CMOS	Trimming data reload mode calibration flag bit
IP_trim[15:0]	Out	CMOS	Trimming bits to other IPs
Dout[31:0]	Out	CMOS	Data out
Busy	Out	CMOS	Signal to indicate macro busy in trimming data reload or NV operations
Tp	Inout	Analog	Analog input/output when test mode, for wafer sorting use
Tdo	Out	CMOS	Test mode output, outputs ‘0, when normal operation
Toe	Out	CMOS	Test mode output, outputs ‘0, when normal operation
VDD	In	Power	Power
VSS	In	Ground	Ground

4 Memory Configuration

The definition of the FM memory area is presented inFigure 4-1.
NM – **N**ormal **M**emory, for customer data/code storage
SM – **S**upervisory **M**emory, for trimming code and special data storage

Axa	Ba[1:0]	Ra[8:0]	Row	Sector	Bank	Bulk
1,b1	-	9,h00F	SM row 0~15	-	-	-
		...				
		9,h000				
1,b0	2,b11	9,h1FF	NM row 2047	Sector 255	Bank 3	Bulk
		...	...			
		9,h1F8	NM row 2040			
		...	...	...		
		9,h007	NM row 1543	Sector 192		
		...	...			
		9,h000	NM row 1536			
	2,b10	9,h1FF	NM row 1535	Sector 191	Bank 2	
		...	...			
		9,h1F8	NM row 1528			
		...	...	...		
		9,h007	NM row 1031	Sector 128		
		...	...			
		9,h000	NM row 1024			
	2,b01	9,h1FF	NM row 1023	Sector 127	Bank 1	
		...	...			
		9,h1F8	NM row 1016			
		...	...	...		
		9,h007	NM row 519	Sector 64		
		...	...			
		9,h000	NM row 512			
	2,b00	9,h1FF	NM row 511	Sector 63	Bank 0	
		...	...			
		9,h1F8	NM row 504			
		...	...	...		
		9,h007	NM row 7	Sector 0		
		...	...			
		9,h000	NM row 0			

Figure 4-1 Address mapping

The normal memory bits are divided into several banks. According to different memory demands, there are **up to** 512 rows per bank and 512 Bytes on a row. A sector is defined as 8 NM rows, which enables erase/program of a group of rows. The internal FM addresses are divided into bank addresses Ba, row addresses Ra, column addresses Ca, and page latch addresses Pa.

There are **up to** 16 rows in the supervisory memory. A special address Axa is used to enable SM rows while the Ra[3:0] address is used to select one of 16 special rows. They are not affected by any sector, bank operations.

When the memory capacity of Flash Macro is between 1MB and 512KB, **the memory address will be equally distributed in each Bank.**

5 Operation Mode

Several operation modes of FM can be accessible by setting Mode[3:0] inputs and other signals as shown in various timing diagrams. The mode control truth table is presented below

Table 5-1 FM operation mode

Mode[3:0]	Description
0000	Normal mode, normal read(or margin read) operation enabled
0001	Clear page latches
0010	Set page-write-all bit for filling all page buffers with a single Byte write, will be cleared after any other mode.
0011	Unused
0100	Trimming data reload
0101	Unused
0110	Reserved for test mode operation
0111	Set PEP (pre-program) bit for soft pre-program of all selected memory cells, will be cleared after any program cycle automatically.
1000	Erase page (or row)
1001	Erase all pages in a sector
1010	Erase all pages in a bank except in SM
1011	Erase bulk all pages except in SM
1100	Program page (or row)
1101	Program all pages in a sector
1110	Program **bank** all even/odd pages, Ra[0] to select even or odd pages
1111	Program **bank** all pages

5.1 Read Operation

The synchronous read operation at certain addresses is entered when a read mode of '0000' is set on the Mode inputs, with proper address on the address inputs at the rising edge of Aclk. Seq[1:0] input should be "00" for read operation. Data would be available on the output Dout after an access time of 'Taa'. Please refer toFigure 10-1for the timing diagram of "Read Operation".

5.2 Trimming Data Reload

Trimming Data Reload is active when mode of '0100' is set on the Mode inputs. When FM starts to load trimming value to internal setting registers, Busy signal would be set to '1' .

IP_trim pins are the output trimming bits to other IPs. The default value of **IP_trim** would be set to '0' after Flash Macro **reset** signal is completed. **Ldtpass** pin is the calibration flag bit, **Ldtpass** signal would be set to default value '0' after Flash Macro **reset** signal is completed.

If the trimming data reload calibration is **passed**, the **Ldtpass** signal would be set to '1' and all of **IP_trim** output bits would be set to a trimming value to other IPs.

If the trimming data reload calibration is **failed**, the **Ldtpass** signal would be hold at default value '0' and all of **IP_trim** output bits hold at default value '0'.

After the trimming data loading procedure is finished, the **Busy** signal would be set to '0'. Please refer toFigure 10-2for the timing diagram of "Load trimming data".

Trimming data reload is needed after reset. Trimming data reload only can be executed one time after reset. Trimming data are stored in 1st row of SM area (Axa=1, Ra=0), It is prohibited to be erased or programmed during normal operation.

Table 5-3 SM area address assignment

Axa	Ra	Ca	Dout[31:0]	
			[31:16]	[15:0]
1	0	4	~IP_trim[15:0]	IP_trim[15:0]

5.3 Write Operation

Write operation in a non-volatile (NV) memory includes 4 required steps.

1. Pre-Program the selected memory location to all pseudo ‘1’.
2. Erase the selected memory location to all ‘0’.
3. Clear page latches.
4. Write data into the corresponding page latch/latches.
5. Program page latch contents into memory location.
6. Repeat 3~5 if program unit is smaller than erase unit.

When a memory location is erased, the data would be ‘0’. When the location is programmed, the data would be ‘1’. An erased location (‘0’) can be changed to ‘1’ using program operation. But a programmed location (‘1’) cannot be changed to ‘0’ using program operation. Therefore, the erase step is always needed for a new write to occur.

5.3.1 Writing Page Latches

Page latches can be imagined as one page of SRAM that temporarily hold data before they are programmed into the non-volatile memory. Writing into page latches is an operation that is not controlled by Aclk. It is controlled by an input signal Pw. Though there will be as many page latches as there are Bytes/columns in a page, page addresses (Pa) that are different from Ca are used for addressing page latches. Please refer toFigure 10-4 for the timing diagram of “Writing Page Latches”.

Besides write page latches one by one, one write page latch cycle, to fill all page latches with the same data, is available after setting mode “0010”.

Page write operation occurs independent of the Aclk controlled modes, especially read operation. The FM can be considered to have independent read and page write ports.

Clear page latches should be executed before this mode. In one write page latch cycle, besides write page latches one by one, when mode set as “0000” by Aclk. Also it’s available that filling all page latches with the same data after setting mode “0010” by Aclk.

5.3.2 Clear Page Latches

Different with writing page latches, clear page latches is controlled by Aclk. This mode is entered by setting mode “0001”. Seq[1:0] input should be “00”. Page latch data will be cleared in one Aclk cycle. Please refer toFigure 10-5 for the timing diagram of “Clear Page Latches”.

5.3.3 Non-Volatile Modes

The non-volatile operations are the program and erase operations. Each operation has to go through Seq sequence 1 → 2→ 3 → 0. When FM is doing NV operation, Busy signal would be set to "1" at seq sequence "1". When operation is done, Busy signal will set "0" at seq sequence "0". These are long operations where the time required to complete them is in the order of milliseconds. This sequencing takes the device through the required high voltage cycles that will erase or program a memory location. Pe signal is used in one of the step, which also switches on the positive and negative pump to provide the high voltages to the macro. Please refer to Figure 10-3 for the timing diagrams of "High Voltage Cycles".

Erase Page (or Row):

Erase all data of the selected page.

Erase Sector:

Erase all data of the selected sector except for the SM.

Erase Bank:

Erase all data of the selected bank except for the SM.

Erase Bulk:

Erase data of the entire bulk except for the SM.

Program Page:

Program the selected page with page latch data.

Program Sector:

Program the selected sector except for the SM with page latch data.

Program Bank Even/Odd Pages:

Program bank all even (Ra[0]=0)/odd (Ra[0]=1) pages except for the SM with page latch data.

Program Bank:

Program one bank except for the SM with page latch data.

Pre-program:

Program all selected locations to pseudo '1' status from previously erase or program mode. To execute pre-program operation, the following two steps are required:

1) Set PEP bit (mode "0111");
2) Program (mode "11xx") selected locations with HV duration in time of hundreds of micro seconds.

Note: It is prohibited to program the same page once more after erase followed by the first program.

6 Power Mode

The FM supports multiple power modes as follows:

Hibernate-1 Mode: This is an ultra-low power mode, which tuning off the power of entire FM. The leakage current during this mode is denoted by Ilkg-1. The startup timing from Hibernate-1 mode is shown inFigure 10-6.

Hibernate-2 Mode: In this mode, FM is powered off except trimming register circuitry. Trimming codes are retained and no further trimming data reload operations are needed. The leakage current during this mode is denoted by Ilkg-2. The startup timing from hibernate-2 mode is shown in Figure 10-6.

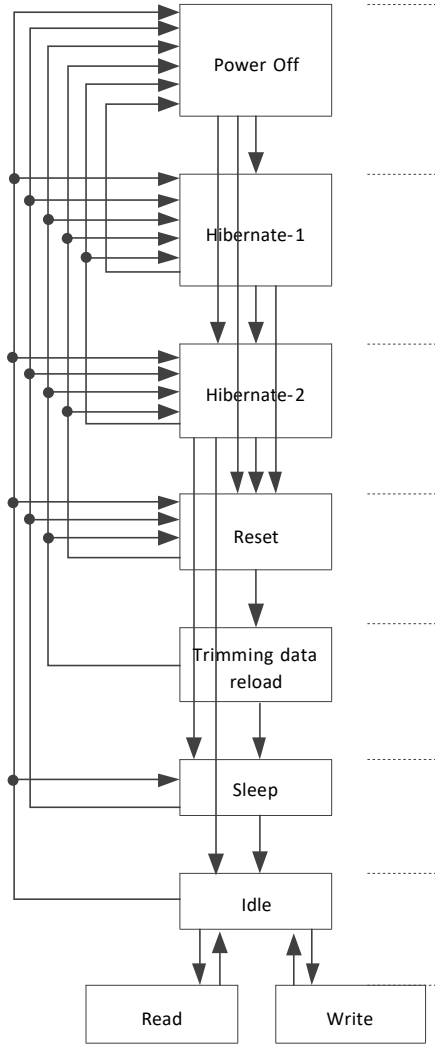
Reset Mode: This mode is to initialize FM. Reset operation is needed after power up, or after exiting from Hibernate-1, or exiting from Hibernate-2 with Hibernate-1 or Power off prior to it.

Trimming data reload mode: Trimming data reload is needed after chip reset. Refer to Figure 10-2 for the timing diagram.

Sleep Mode: This is a low power mode, FM is powered ON but no circuitry active. The sleep current is denoted by Isb. The wakeup from sleep timing is shown inFigure 10-6.

Idle Mode: In this mode, the macro is ready to do a read or NV operation immediately while the Aclk is not toggling. The current in this mode is denoted by Icc0. Turbo=1 in this mode is to accelerate the time read reference setup from sleep mode. The current in this mode is denoted by Icc1.

Active Mode: Active Read mode is the mode in which the macro is doing active read operations. The current is denoted by Icc2. Active Page Write mode is the mode in which the macro is doing page write operations. The current is denoted by Icc3. Active NV operation mode is the mode in which the macro is doing program/erase operations. The current is denoted by Icc4.



	VDD	Pd1	Pd2	Reset	Sleep	Dout	Busy	Ldtpass	Tdo	Toe	Tp
Power Off	OFF	X	X	X	X	-[1]	-[1]	-[1]	-[1]	-[1]	-[1]
Hibernate-1	ON	1[2]	1	X	X	Hi-Z/ 0[5]	0	0	0	0	Hi-Z
Hibernate-2	ON	0	1	0	X	Hi-Z/ 0[5]	0	0	0	0	Hi-Z
Reset	ON	0	0	1	X	Dout[3]	0[4]	0[6]	0[4]	0[4]	Hi-Z[4]
Trimming data reload	ON	0	0	0	X	Dout[3]	1	1[6]	0[4]	0[4]	Hi-Z[4]
Sleep	ON	0	0	0	1	Dout[3]	0[4]	1[6]	0[4]	0[4]	Hi-Z[4]
Idle	ON	0	0	0	0	Dout[3]	0[4]	1[6]	0[4]	0[4]	Hi-Z[4]
Read / Write	ON	0	0	0	0	Dout[3]	0/1[4]	1[6]	0[4]	0[4]	Hi-Z[4]

Figure 6-1 Power mode transition

Note [1]: In power off mode, its value is uncertainty.

Note [2]: '0' stands for logic '0' in VDD power domain, '1' stands for logic '1' in VDD power domain, 'Hi-Z' stands for Hi-Z status in VDD power domain.

Note [3]: Dout=0/1 when OE=1, or Dout=Hi-Z when OE=0.

Note [4]: Under user mode.

Note [5]: Dout=0 when OE=1, or Dout=Hi-Z when OE=0.

Note [6]: Ldtpass=0 after Reset signal is completed. Ldtpass='1' when Trimming data reload calibration is passed,Ldtpass=0 when Trimming data reload calibration is failed.

7 Test Mode

Various test modes are supported and accessible through Ten, Tck, Tstr, Tdi, Tdo and Toe pins. When Ten is high, FM test mode is activated. Tester can interface with FM through Tck, Tstr, Tdi, Tdo, Toe and Tp in test mode.

Tck is test mode clock. Tstr is test command strobe enable signal. Tdi is test mode data input. Tdo is test mode data output. Toe indicates test data output valid or not. Besides these, Tp is an analog input/output pin to pass through several of analog signals.

Test mode operation is to be used for flash test only. Customer need to ensure the accessible of these pins through **C**hip **P**robing (**CP**) test. Section 8 introduces the guideline of how connecting these pins the IO and/or user logic.

8 Circuit Integration Guideline

Figure 8-2is showing the general integration guideline of the FM. It is to be noticed that the output drive capability of Tdio IO has high relationship to CP test time. We would recommend the drive capability of Tdio IO output speed no less than 20MHz. Regarding the TP IO, the requirement of ESD protection capability is not too high since PAD bounding is not necessary.

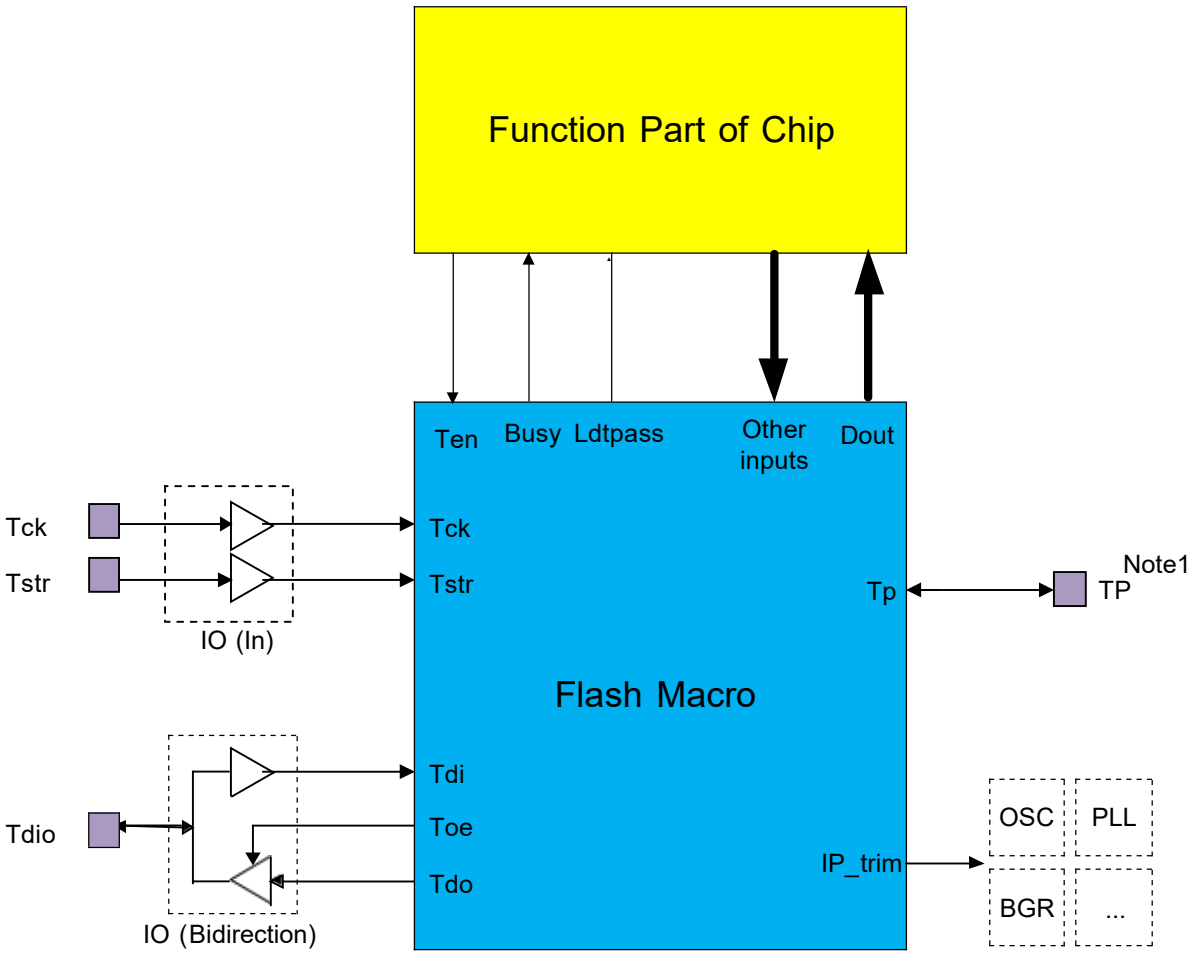


Figure 8-2 Circuit integration guideline

Note1:

Tp is the test pin of FM which is used to monitor Flash characters during testing. It can be negative voltage during test, antenne diode is not allowed on it. Basic ESD protection capability has been implemented in it. There is no necessary to have ESD protection circuit outside of the IP.

9 DC Specification

Table 9-2 Recommended operation condition

Symbol	Description	Spec			Units
		Min	Typ	Max	
Ta	Operation ambient temperature range	-40	25	85	ºC
Tj	Operation junction temperature range	-40	25	100	ºC
VDD	External power supply	1.08	1.2	1.32	V

Table 9-3 FM DC specification

Symbol	Description	Spec			Units
		Min	Typ	Max	
Ilkg_1	Leakage Current Pd1 = 1, Pd2 = 1 All other inputs are stable CMOS levels.			1	μA
Ilkg_2	Leakage Current Pd1 = 0, Pd2 = 1 All other inputs are stable CMOS levels.			30	μA
Isb	Standby Current Pd1=0, Pd2=0, Sleep=1, Aclk=0 All other inputs are stable CMOS levels.			10	μA Tj=25°C
				120	μA Tj=100°C
Icc0	Idle Current Sleep=0, Turbo=0, Aclk=0, Pclk active All other inputs not toggling and at CMOS levels.			500	uA
Icc1	Idle Current Sleep=0, Turbo=1, Aclk=0, Pclk active All other inputs not toggling and at CMOS levels.			700	uA
Icc2	Read Current @ tcy=50ns			3	mA
Icc3	Page Write Current (exclude page-write-all mode)			2	mA
Icc4	Page Program/Erase Current			3	mA

10 AC Specification

Table 10-4 FM AC specifications

Symbol	Description	Specification			Units
		Min	Typ	Max	
Taa	Access time Aclk to Dout valid			50	ns
Tcy	Aclk cycle time when read	>Taa			ns
	Aclk cycle time when Trimming data reload	100			ns
Tdoh	Dout hold time after Aclk rise	0			ns
Taw	Aclk clock high pulse time	10			ns
Tawl	Aclk clock low pulse time	10			ns
Tas	Address/Mode/Seq Setup to Aclk rising	2.0			ns
Tah	Address/Mode/Seq Hold to Aclk rising	2.0			ns
Toz	Oe falling to Dout Hi-Z			2.0	ns
Toe	Oe rising to Dout valid			2.0	ns
Twcy	Write Cycle time Pw to Pw	40			ns
Tpw	Pw clock high pulse width	16			ns
Tpwl	Pw clock low pulse time (32bit)	16			ns
Tpas	Page buffer address setup to Pw rising	3.0			ns
Tpah	Page buffer address hold from Pw falling (32bit)	3.0			ns
Tds	Data setup to Pw falling	16			ns
Tdh	Data hold from Pw falling (32bit)	3.0			ns
Ts1	Sequence 1 cycle time	15			μs
Ts2p	Aclk rising to Pe rising setup time	5			μs
Tbw	Busy time when Mode=4,b0100			100*Tcy	-
Tpe[1]	Pe high pulse width when Mode=4,b1000	5.7	6.0	6.3	ms
	Pe high pulse width when Mode=4,b1100	1.9	2.0	2.1	ms
	Pe high pulse width when pre-program	190	200	210	μs
Tps3	Pe falling to Aclk rising setup time	60			μs
Ts3	Sequence 3 cycle time	5			μs
Ts0	Sequence 0 cycle time	6			μs
Tpd12	Pd1 falling to Pd2 falling time	0			μs
Tpd1f	Pd1 falling to Reset falling time	3			μs
Tpd2f	Pd2 falling to Reset falling time	3			μs
Tpd2s	Pd2 falling to Sleep falling time	6			μs
Trw	Reset high pulse width time	100			ns
Trcs[2]	Reset falling to Aclk rising time	Tps3			-
	Reset falling to Aclk rising time	1			μs
Tactv	Sleep falling to Aclk rising time (Turbo=0)	6.0			μs
	Sleep falling to Aclk rising time (Turbo=1)	3.0			μs

Turbs	Turbo falling to Aclk rising time	3			μs

Note [1]: Erase/Program time for sector/bank/bulk need to increase 200 us.

Note [2]: Minimum Tps3 is required to discharge internal high voltage if reset from NV operation.

10.1 Read Cycles

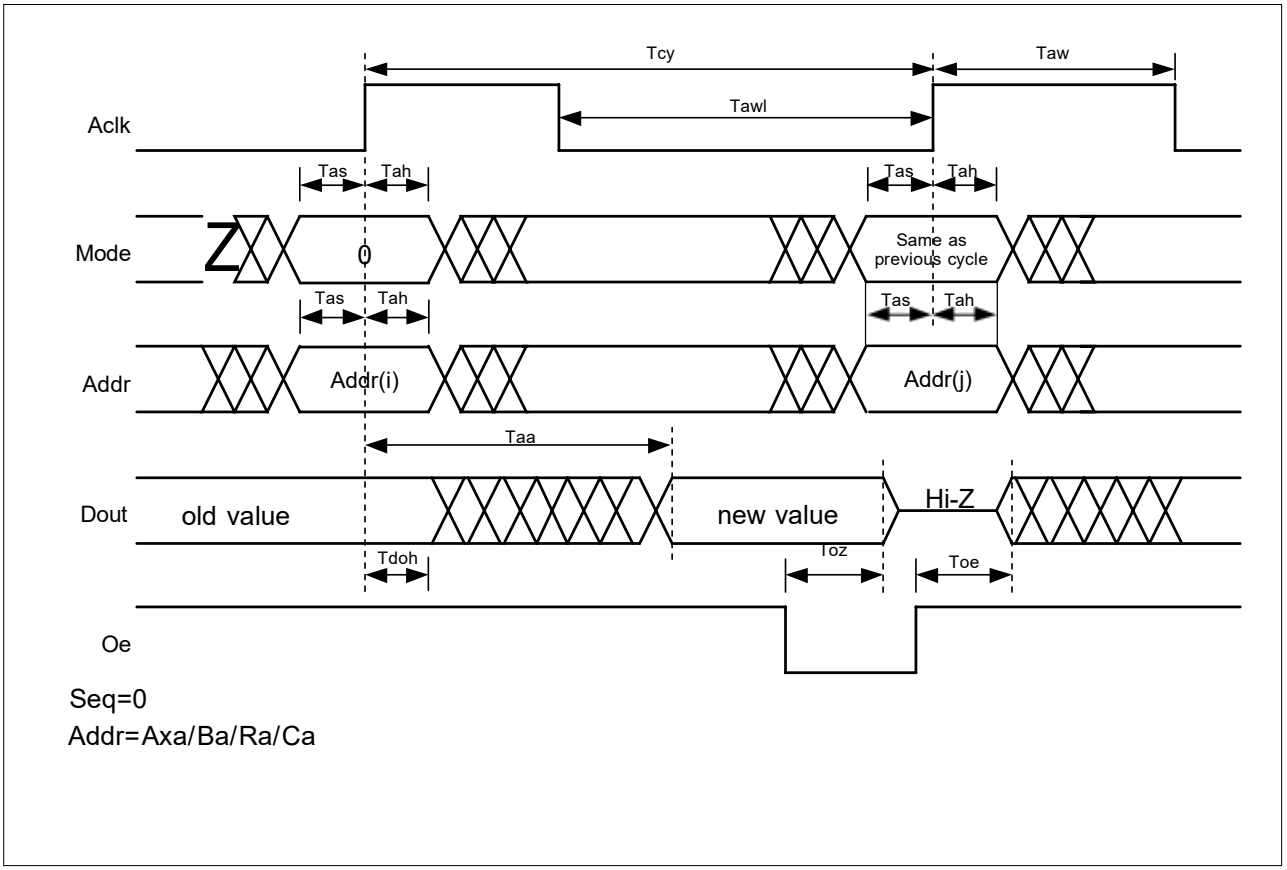


Figure 10-1 Read cycles

10.2 Trimming Data Reload

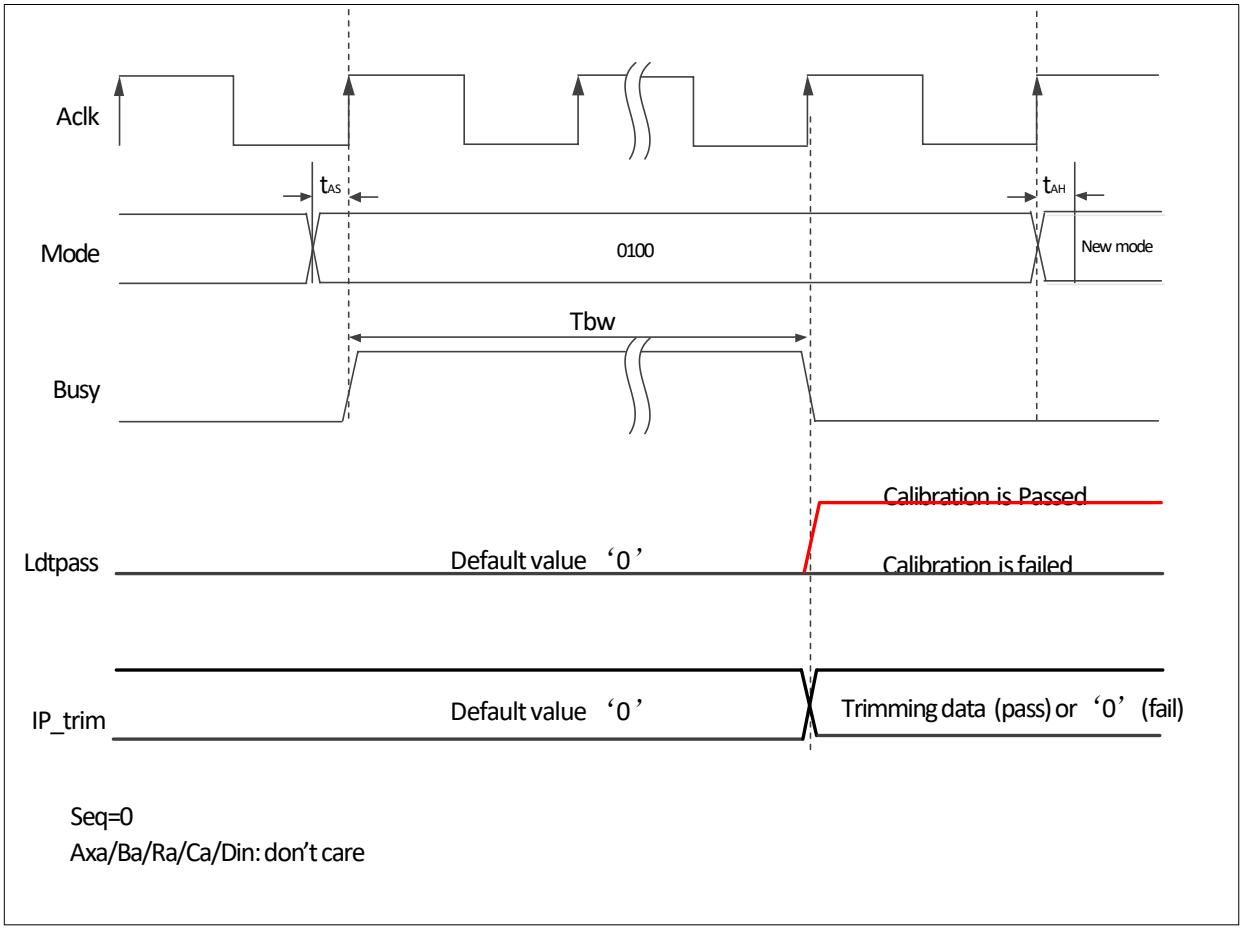


Figure 10-2 Trimming Data Reload

10.3 High Voltage Cycles

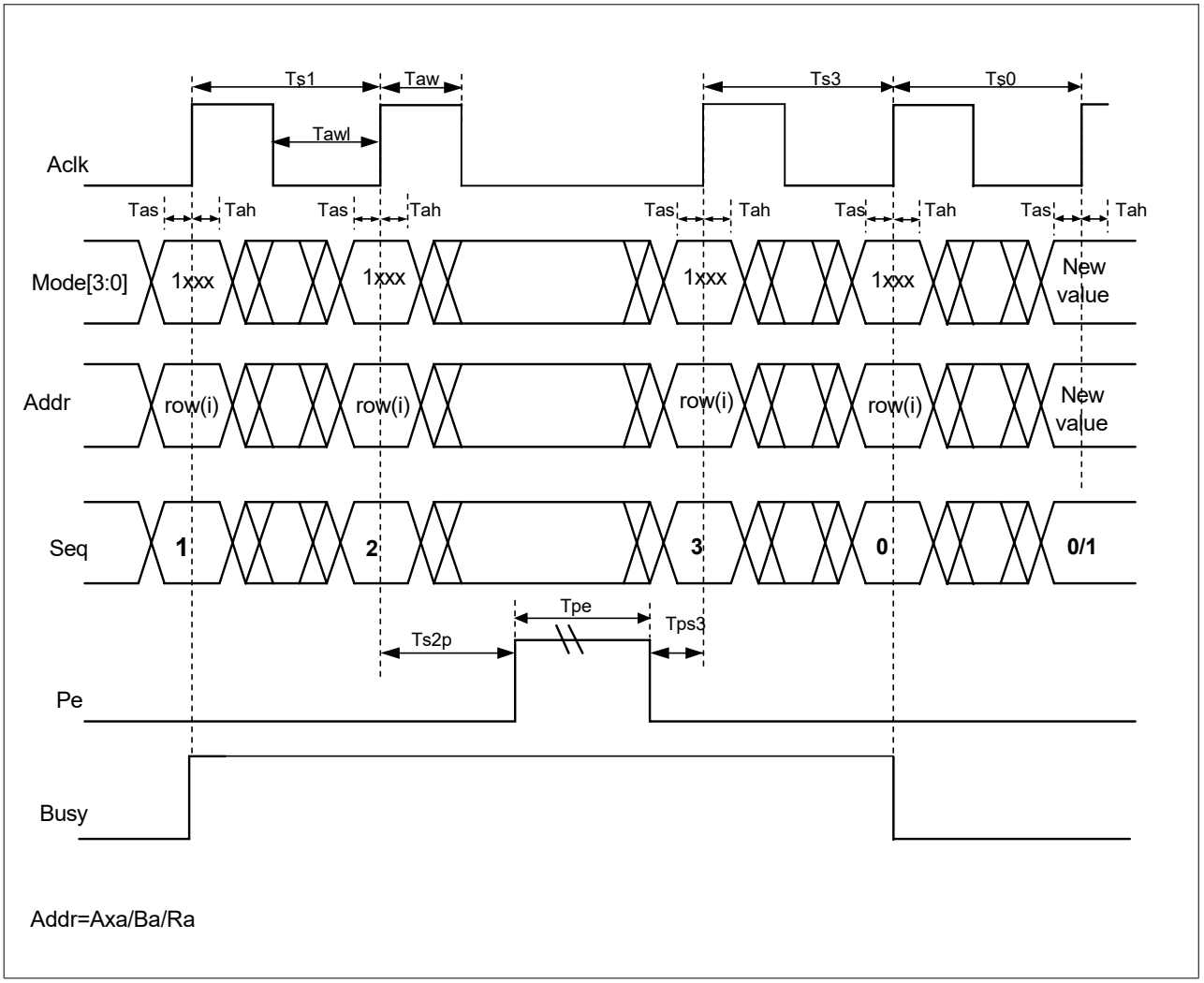


Figure 10-3 HV cycles

10.4 Write Page Latch Cycles and write all page latches

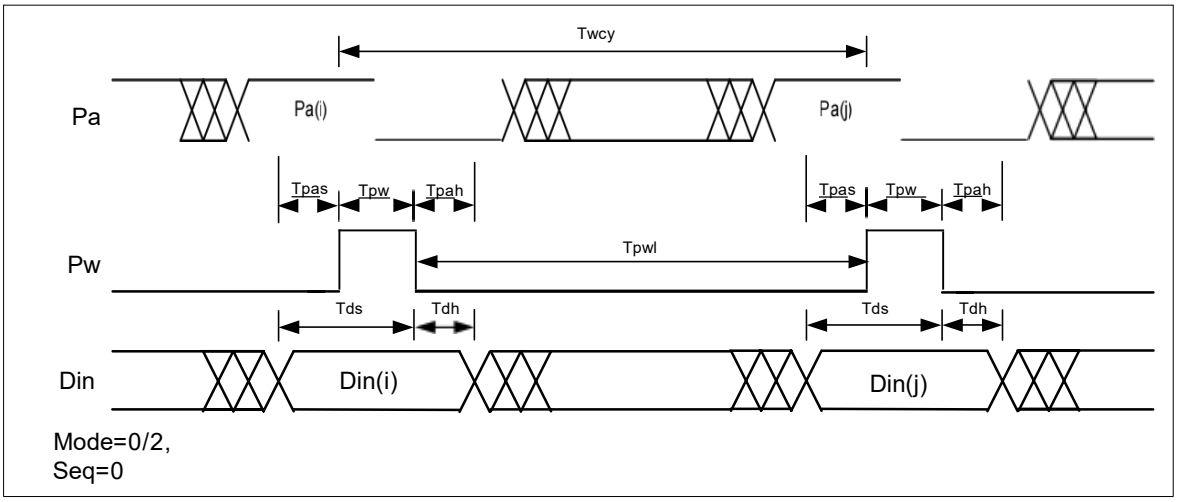


Figure 10-4 Write page latch cycles or Write all page latches

10.5 Set PEP bit or Clear Page Latch Cycles

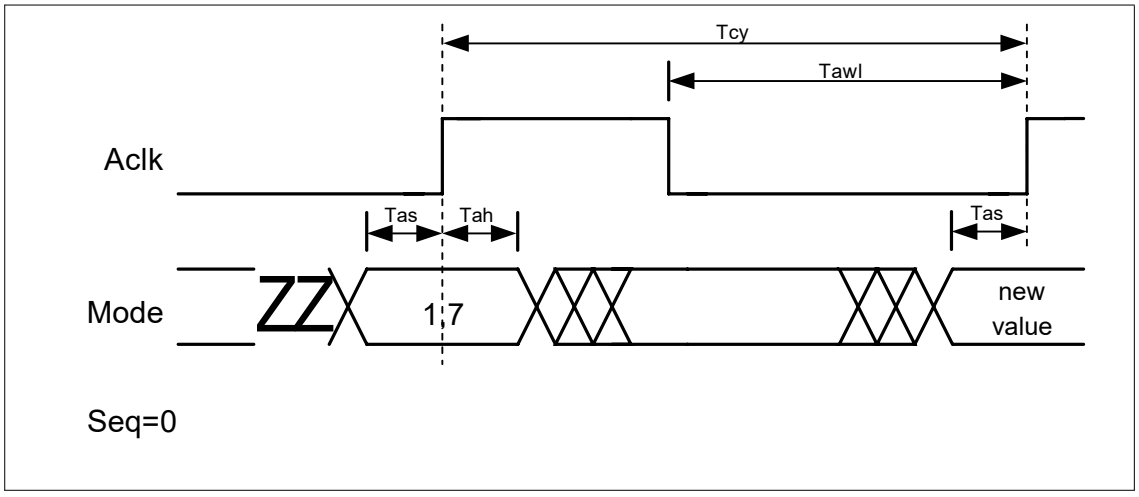


Figure 10-5 Set PEP bit or Clear page latch cycles

10.6 Power Up or Sleep to Active

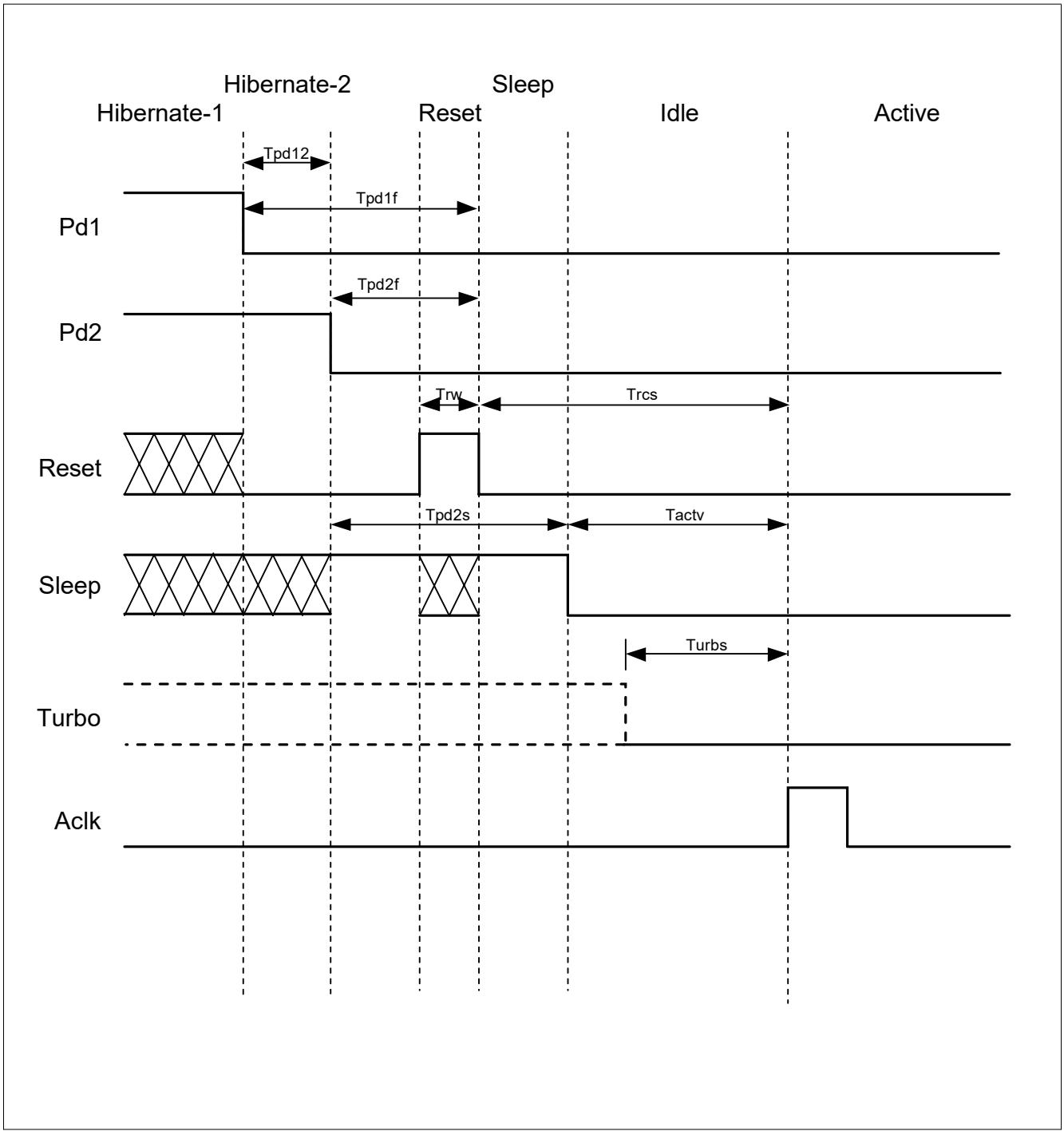


Figure 10-6 Power up or sleep to active

11 Layout Notes

1) The FM is laid out with four inner metal layers.
2) It is recommended to route power ring around FM.
3) Please pay attention to all the pins which should be connected to power. Considering IR drops, **the metal routing of these pins is required to be wider than the pin width and near the power ring as possible.** Power and ground resistance to PAD should less than 10ohm respectively.
4) Metal routing between TP PIN and IO PAD is recommended as: width > 10um, space >0.5um.
5) Since the DNWELL layer is used inside FM, it is not allowed to place any other devices within 6.5um apart from the FM.
6) Metal-5 routing over the FM can only be used for dummy metal or power & ground purpose.

12 Revision History

Version	Description	Date	Author
0.1	Initial release.	2025/12/08	