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| **Course No.: CCE413 Credit : 3 Contact Hours: 3** | **Total Marks: 100** |

* 1. **Rationale:**

To be a successful computer engineer one need to know the architecture and design concepts underlying modern complex VLSIs and system-on-chips.

**11.2 Objectives:**

1. To learn about top-down design hierarchy and technology trends.
2. Be able to use mathematical methods and circuit analysis models in analysis of CMOS digital electronics circuits.
3. Be able to apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.
4. To design complex CMOS gate and circuits like adder, subtractor, multiplier, memory cell.
5. To know about Hardware modeling, Architectural Synthesis, ASIC design.

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| **11.3**  **Learning Outcomes** | **11.4**  **Course Content** | **11.5**  **Teaching Strategy/ Learning Experience** | **11.6 Assessment Strategy** |
| a)Explain top to down design approach,  b)Define automation algorithms | VLSI design methodology: top-down design approach, technology trends and design, automation algorithms | Lecture | Short Question |
| a) Draw the inverters and basic gate using CMOS technology  b) Analyze the Ids versus Vds for CMOS inverter circuit. | Introduction to CMOS inverters and basic gates | Lecture  Exercise | Spot Test  Quiz  Short Question  Analytical |
| 1. Analyze the inversion channel for CMOS. 2. List the layout and design rules | Brief overview of CMOS fabrication process: layout and design rules | Lecture  Exercise | Spot Test  Quiz  Short Question  Analytical |
| 1. Illustrate buffer circuit design, 2. Explain complex CMOS gates | Basic CMOS circuit characteristics and performance estimation; Buffer circuit design; Complex CMOS gates | Lecture  Exercise | Spot Test  Quiz  Short Question  Analytical |
| 1. Implement adder, multiplier using design rules 2. Draw the different memory structures cell and data path | CMOS building blocks: adder, multiplier; data path and memory structures | Lecture  Exercise | Spot Test  Quiz  Short Question  Analytical |
| 1. Analyze hardware modeling 2. Explain logic networks 3. Apply the state diagrams 4. Show the data flow diagram and sequencing graphs | Hardware modeling: hardware modeling languages, logic networks, state diagrams, data-flow and sequencing graphs, behavioral optimization. | Lecture  Exercise | Spot Test  Quiz  Short Question  Analytical |
| 1. Explain the different architectural synthesis. 2. Apply the pipelined circuit for synthesis | Architectural Synthesis: circuit specification, strategies for architectural optimization, data-path synthesis, control unit synthesis and synthesis of pipelined circuits. | Lecture  Exercise | Spot Test  Quiz  Short Question  Analytical |
| 1. Design ASIC using FPGA and PLDs technology | ASIC design using FPGA and PLDs. | Lecture  Exercise | Spot Test  Quiz  Short Question  Analytical |

**RECOMMENDED BOOKS AND PERIODICALS**

**Text Books**: