



North South University
Department of Electrical & Computer Engineering
Project

Course Code: CSE231

Course Title: Digital Logic Design

Section: 07

Project Name: Display the first 7 digit of the ID using 7 segment display

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1. Combinational Part

First 7 digits of ID: 1912374

Binary Inputs	Outputs	7 segment Display output								
A	B	C	a	b	c	d	e	f	g	
0	0	0	0	1	1	0	0	0	0	1
0	0	1	1	1	1	1	0	1	1	9
0	1	0	0	1	1	0	0	0	0	1
0	1	1	1	1	0	1	1	0	1	2
1	0	0	1	1	1	1	0	0	1	3
1	0	1	1	1	1	1	0	0	0	7
1	1	0	0	1	1	0	0	1	1	4
1	1	1	1	1	1	1	1	1	0	0

Kmap:

for 'a':

		\bar{B}		B	
		\bar{A}	A	\bar{C}	C
0	1	1	0		
1	1	1	0		

$$a = C + \bar{A}\bar{B}$$

for 'b':

		\bar{B}		B	
		\bar{A}	A	\bar{C}	C
1	1	1	1	1	1
1	1	1	1	1	1

$$b = 1$$

for 'c':

	\bar{B}	B	
\bar{A}	1 1	0	1
A	1 1	1 1	
	\bar{C}	C	\bar{C}

$$c = \bar{B} + \bar{C} + A$$

for 'd':

	\bar{B}	B	
\bar{A}	0	1 1	0
A	1	0 1	0
	\bar{C}	C	\bar{C}

$$d = \bar{A}C + \bar{B}C + A\bar{B}\bar{C}$$

for 'e':

	\bar{B}	B	
\bar{A}	0 0 1	0	
A	0 0 1	0	
	\bar{C}	C	\bar{C}

$$e = BC$$

for 'f':

	\bar{B}	B	
\bar{A}	0 1 0 0		
A	0 0 1 1		
	\bar{C}	C	\bar{C}

$$f = \bar{A}\bar{B}\bar{C} + AB$$

for 'g':

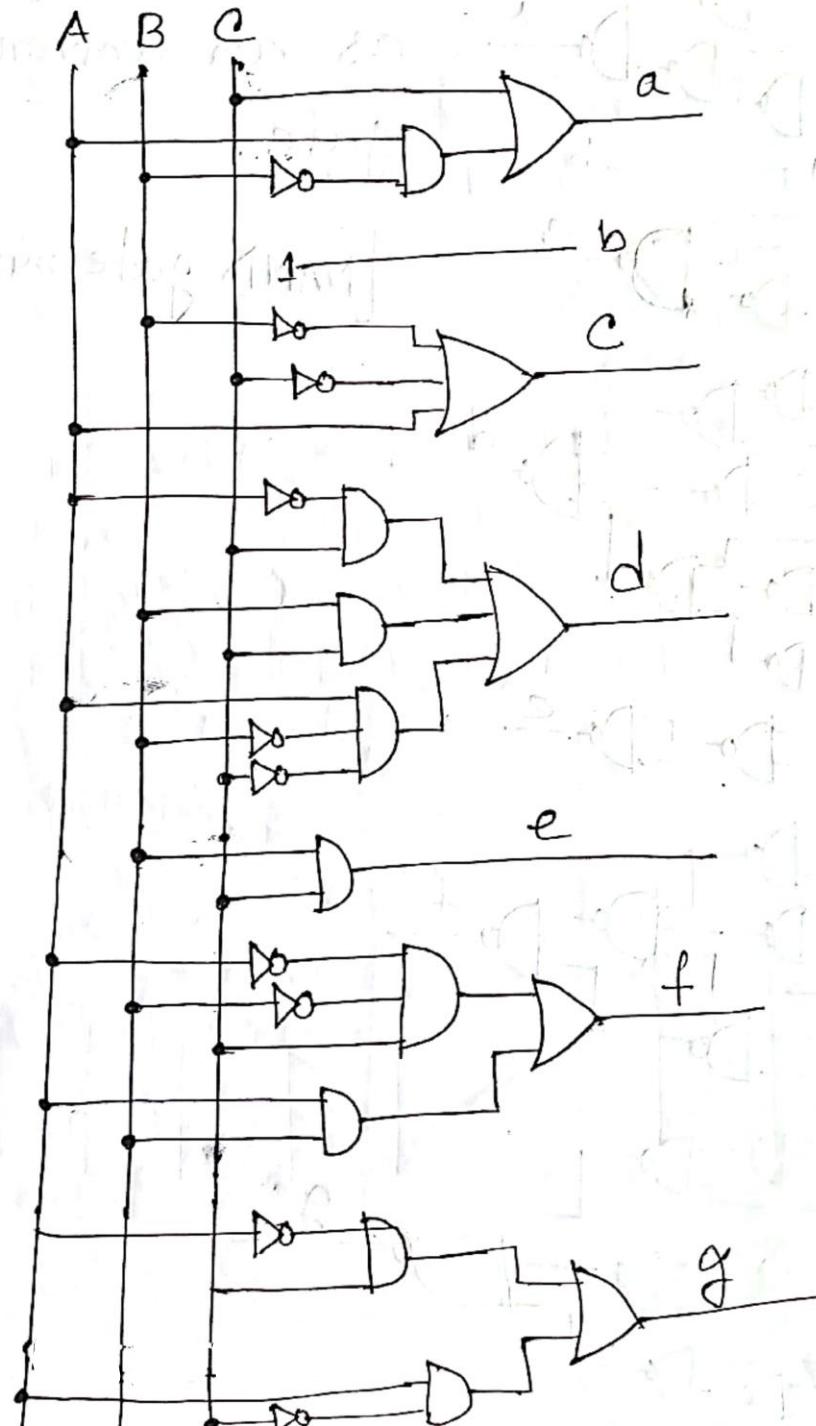
	\bar{B}	B	
\bar{A}	1 1		
A	1		
	\bar{C}	C	\bar{C}

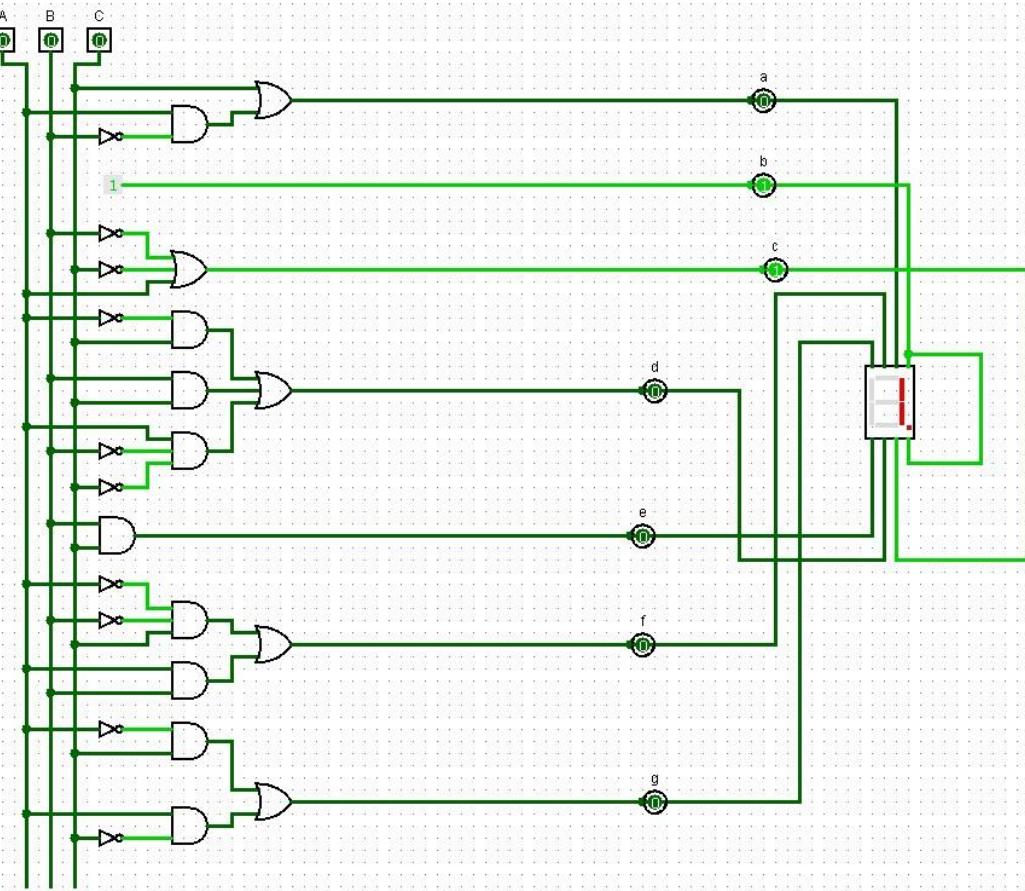
$$g = \bar{A}C + A\bar{C}$$

@ Normal gates

@

Basic gates / Normal gates:



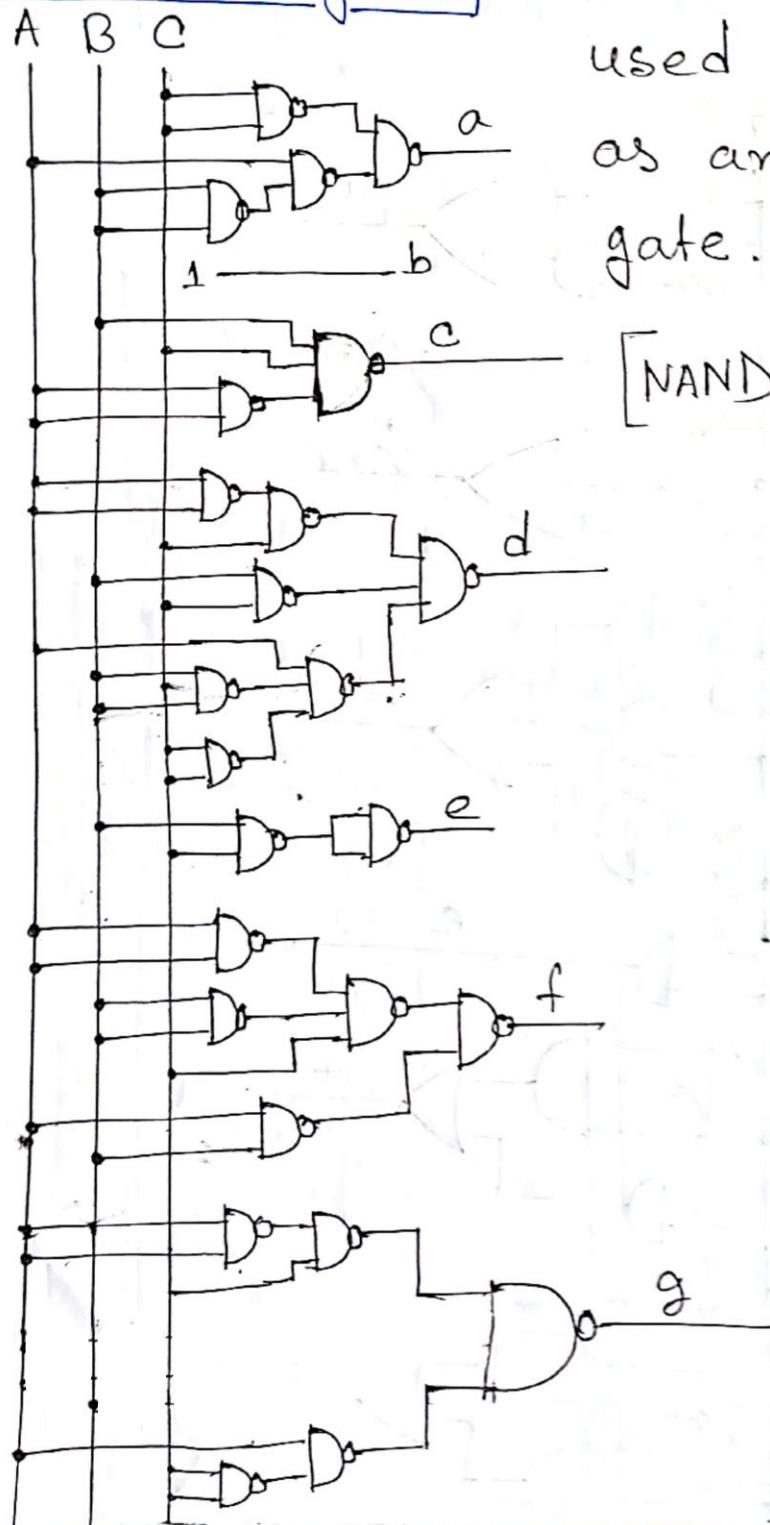


⑥ Universal gate

$$\begin{array}{l|l} \therefore a = c + AB & \therefore c = \overline{\overline{B} + \overline{C} + A} \\ \Rightarrow \overline{\overline{a}} = \overline{\overline{c} + A\overline{B}} & \Rightarrow \overline{\overline{c}} = \overline{\overline{B} + \overline{C} + A} \\ \Rightarrow a = \overline{\overline{c} \cdot A\overline{B}} & \Rightarrow c = \overline{\overline{B} \cdot \overline{C} \cdot \overline{A}} = \overline{B \cdot C \cdot \overline{A}} \end{array}$$

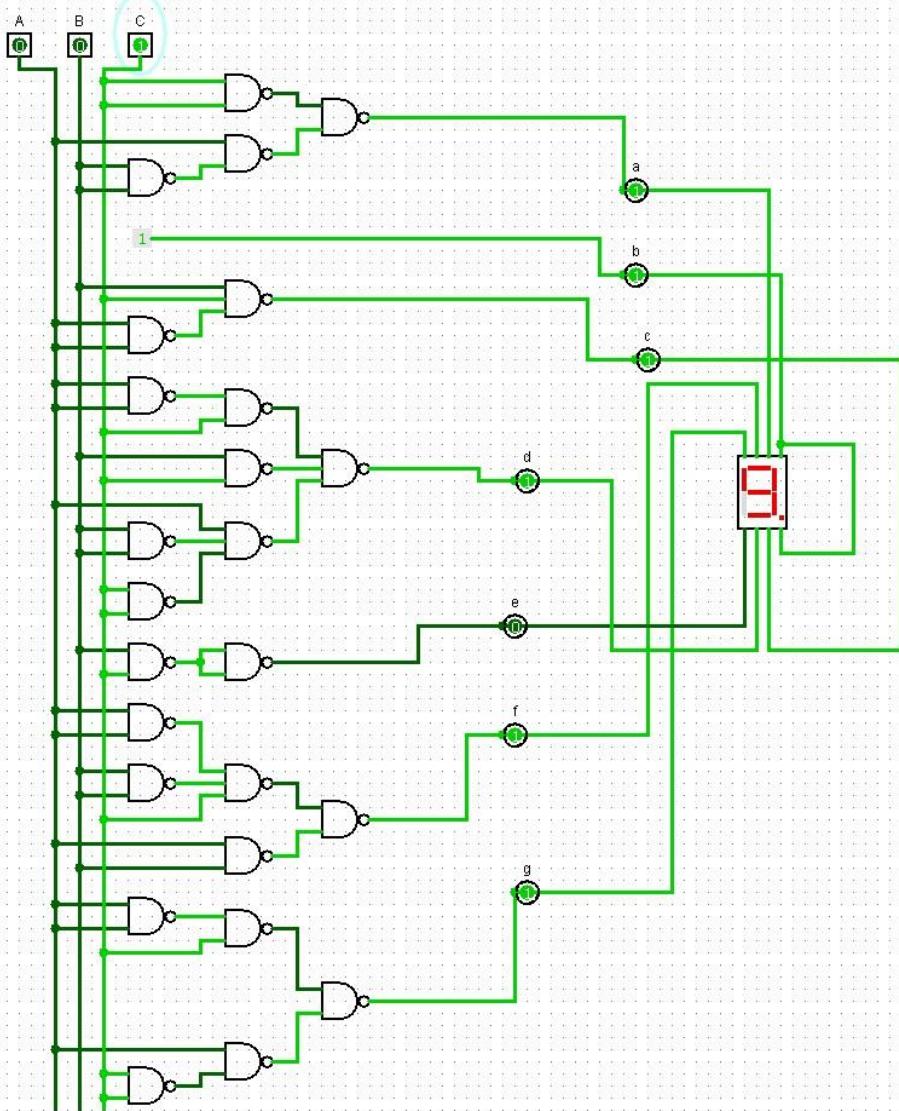
$$\begin{array}{l|l} \therefore d = \overline{Ac} + Bc + A\overline{B}\overline{C} & \therefore e = \overline{Bc} \\ \Rightarrow \overline{\overline{d}} = \overline{\overline{Ac} + Bc + A\overline{B}\overline{C}} & \Rightarrow \overline{\overline{e}} = \overline{\overline{Bc}} \\ \Rightarrow d = \overline{\overline{Ac} \cdot \overline{Bc} \cdot \overline{A\overline{B}\overline{C}}} & \Rightarrow e = \overline{Bc} \end{array}$$

$$\begin{array}{l|l} \therefore f = \overline{ABC} + AB & \therefore g = \overline{Ac} + A\overline{C} \\ \Rightarrow \overline{\overline{f}} = \overline{\overline{\overline{ABC} + AB}} & \Rightarrow \overline{\overline{g}} = \overline{\overline{\overline{Ac} + A\overline{C}}} \\ \Rightarrow f = \overline{\overline{\overline{ABC}} \cdot \overline{AB}} & \Rightarrow g = \overline{\overline{Ac} \cdot \overline{A\overline{C}}} \end{array}$$

(b) Universal gates:

Here we have used NAND gate as an universal gate.

[NAND gate minimized]



① Decoder

② Decoder:

$$\text{Here, } a = \sum (1, 3, 4, 5, 7)$$

$$b = \sum (2, 3, 4, 6, 7)$$

$$c = \sum (0, 1, 2, 4, 5, 6, 7)$$

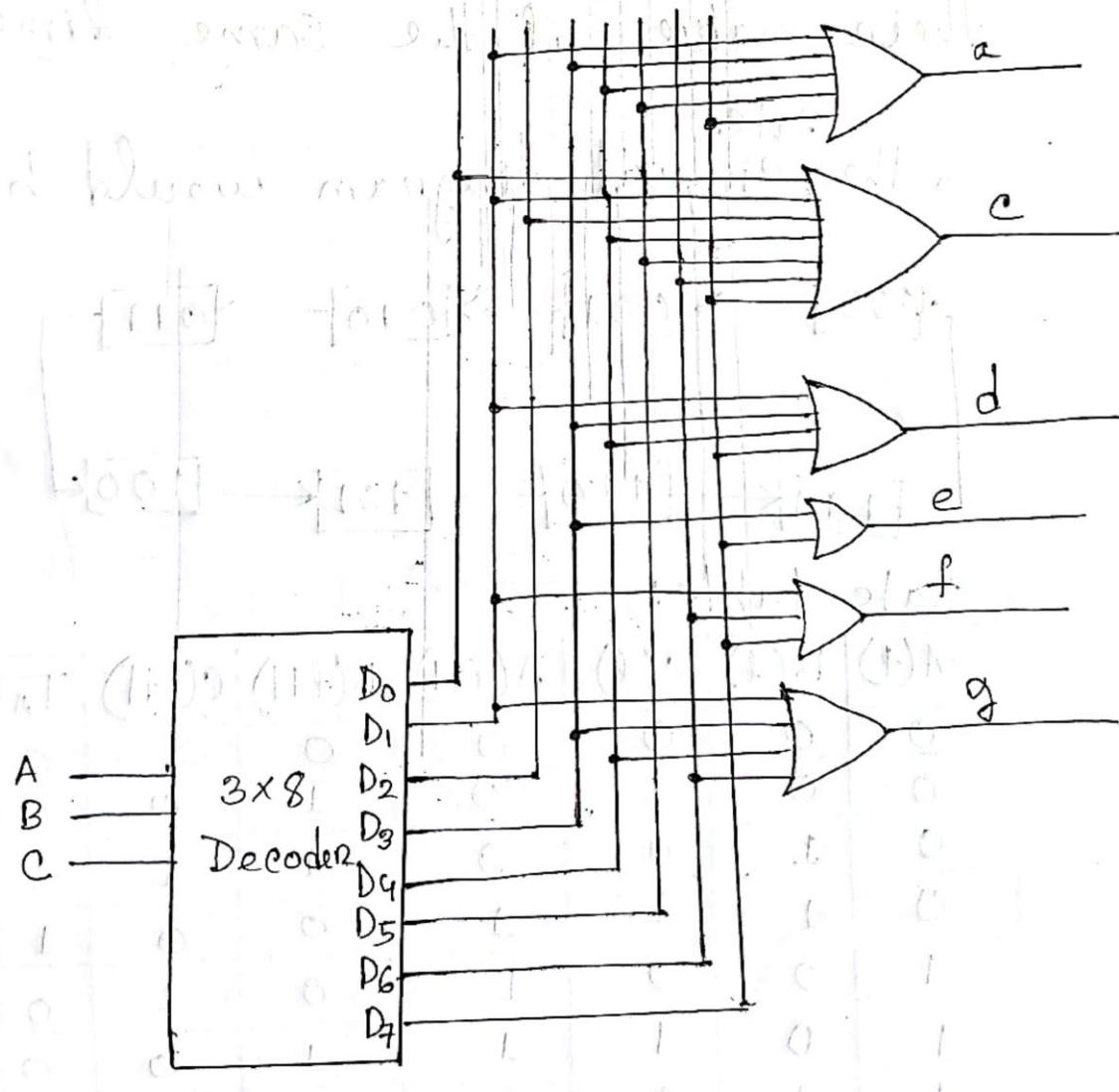
$$d = \sum (1, 3, 4, 7)$$

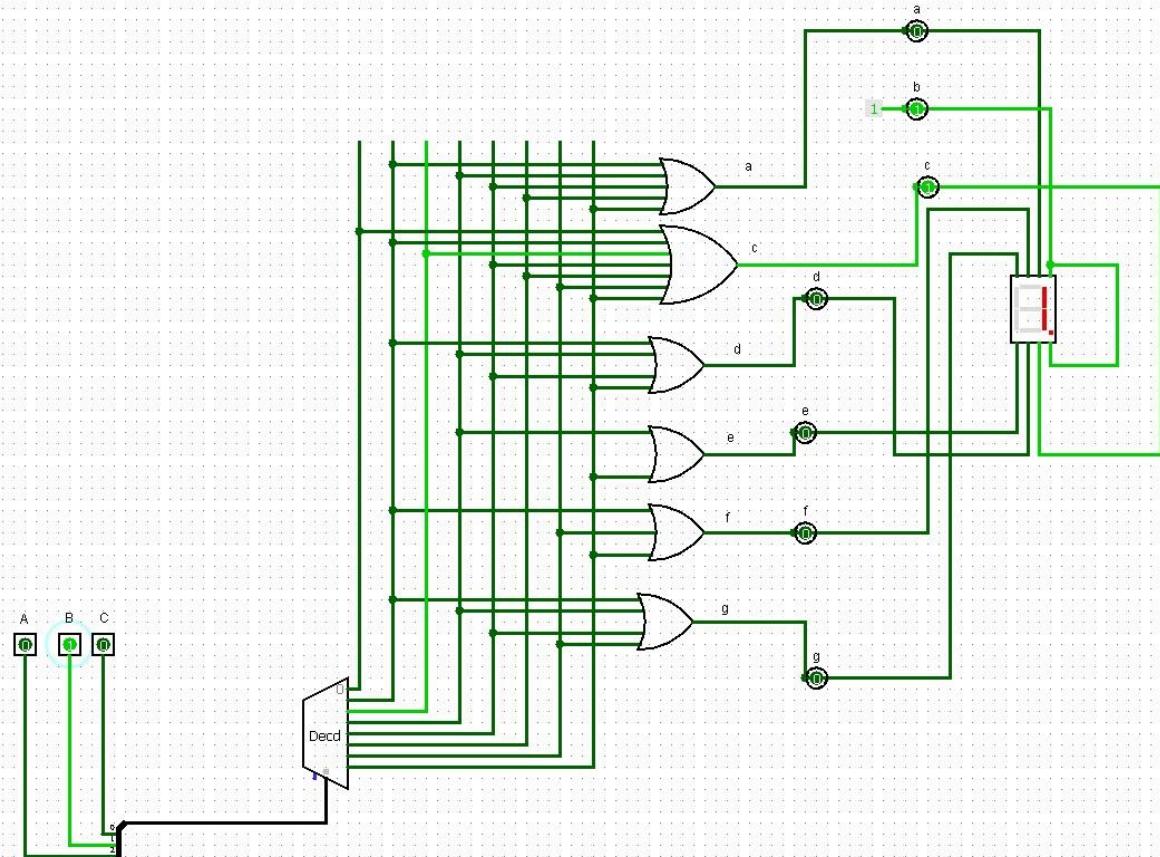
$$e = \sum (3, 7)$$

$$f = \sum (1, 6, 7) ; g = \sum (1, 3, 4, 6)$$

[I have used Truth table to find the minterms of a, c, d, e, f]

Implementation of the Decoder





d) Mux

(d)

Mux:

Let A and B be select bits,

$$\therefore a = \sum(1, 3, 4, 5, 7)$$

	I ₀	I ₁	I ₂	I ₃
\bar{C}	m ₀	m ₂	m ₄	m ₆
C	m ₁	m ₃	m ₅	m ₇
	C	C	1	C

$$\therefore b = 1$$

$$\therefore d = \sum(1, 3, 4, 7)$$

	I ₀	I ₁	I ₂	I ₃
\bar{C}	m ₀	m ₂	m ₄	m ₆
C	m ₁	m ₃	m ₅	m ₇
	C	C	\bar{C}	C

$$\therefore e = \sum(3, 7)$$

	I ₀	I ₁	I ₂	I ₃
\bar{C}	m ₀	m ₂	m ₄	m ₆
C	m ₁	m ₃	m ₅	m ₇
	0	C	0	C

	I ₀	I ₁	I ₂	I ₃
\bar{C}	m ₀	m ₂	m ₄	m ₆
C	m ₁	m ₃	m ₅	m ₇
	1	\bar{C}	1	1

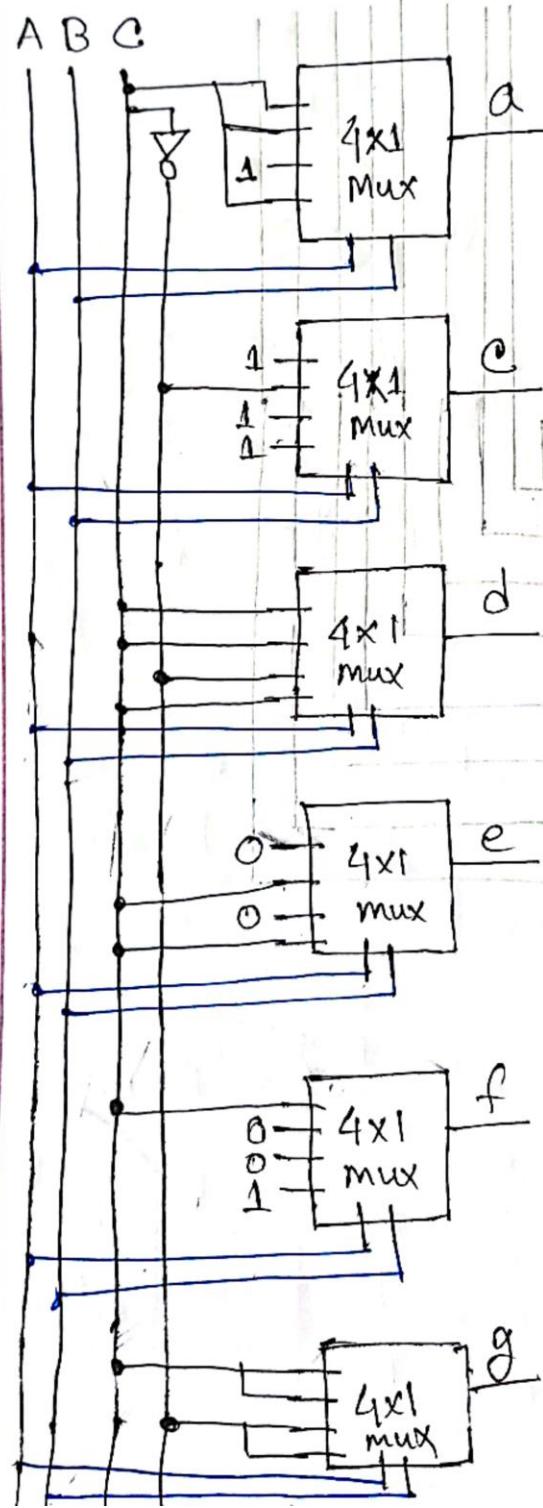
$$\therefore f = \sum(1, 6, 7)$$

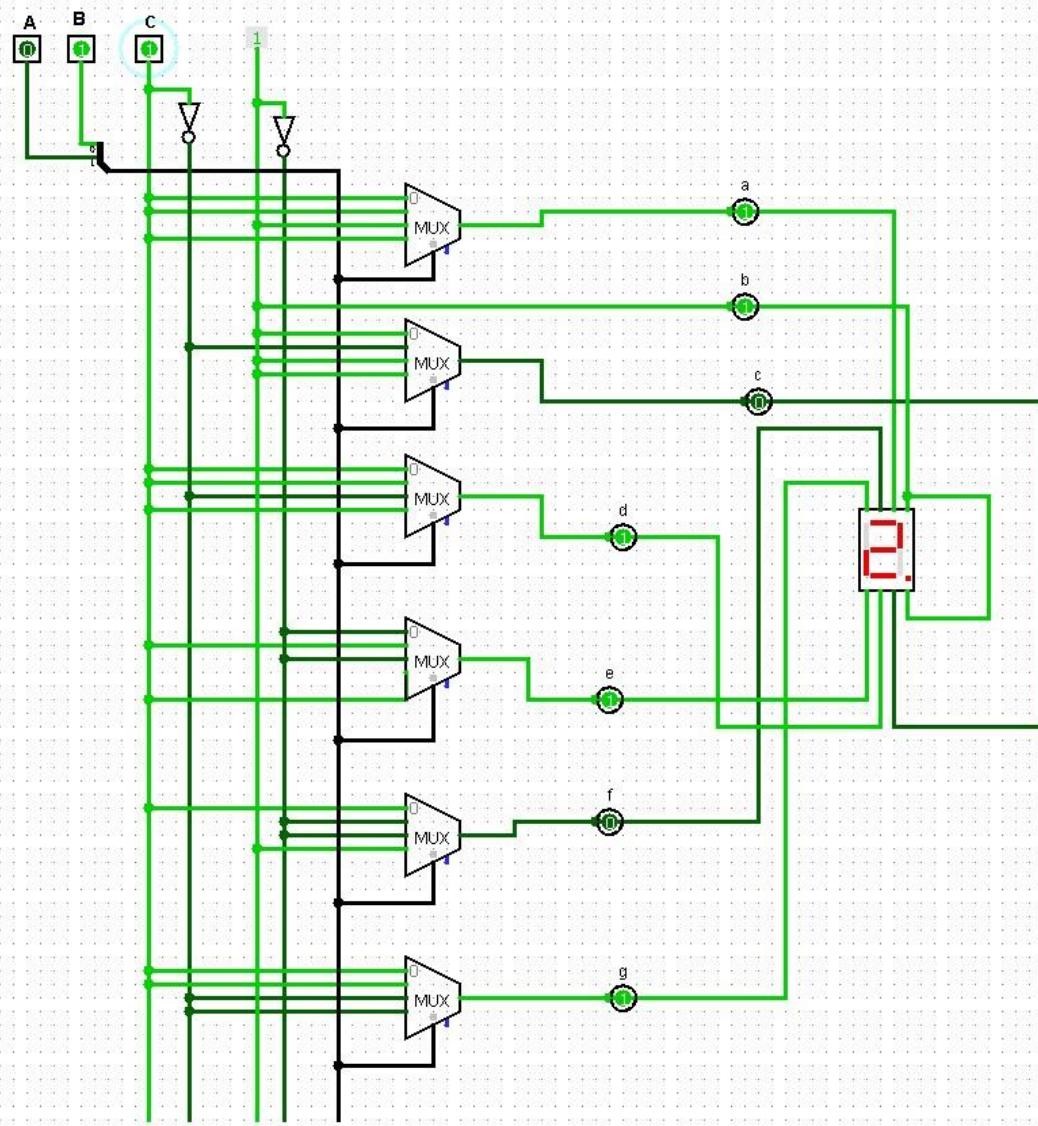
	I ₀	I ₁	I ₂	I ₃
\bar{C}	m ₀	m ₂	m ₄	m ₆
C	m ₁	m ₃	m ₅	m ₇
	C	0	0	1

$$\therefore g = \sum(1, 3, 4, 6)$$

	I ₀	I ₁	I ₂	I ₃
\bar{C}	m ₀	m ₂	m ₄	m ₆
C	m ₁	m ₃	m ₅	m ₇
	C	C	\bar{C}	C

Implementation of the Mux:

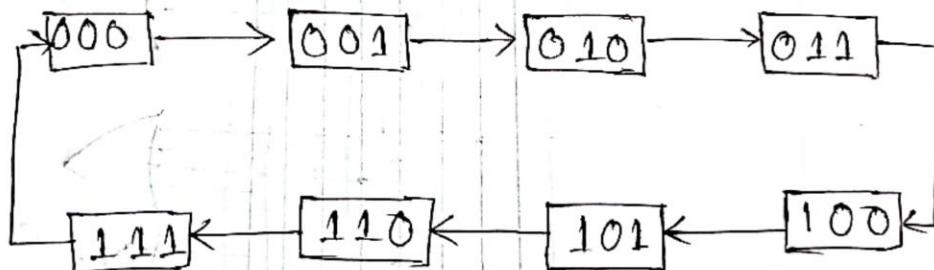




2. Sequential Part

Here, I have used ^{sequential} synchronous counter because in synchronous counter all the flip flop will change their value at the same time.

So the circuit diagram would be



state table:

A(t)	B(t)	C(t)	A(t+1)	B(t+1)	C(t+1)	T _A	T _B	T _C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	0	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

Kmapfor T_A

		1	
		1	

for T_B

	1	1	
	1	1	

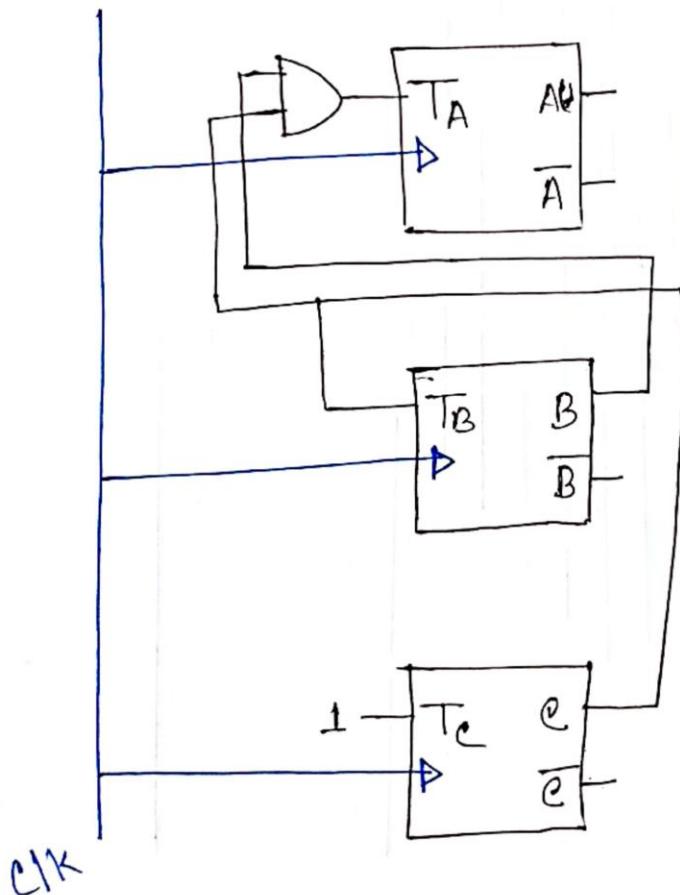
for T_C

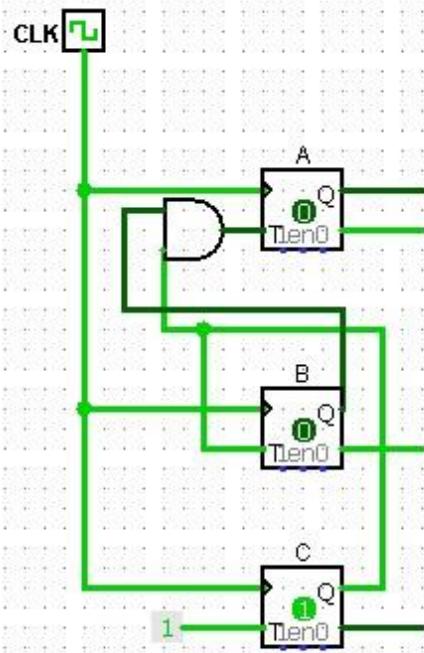
1	1	1	1
1	1	1	1

$$\therefore T_A = B(t) \bar{c}(t)$$

$$\therefore T_B = c(t)$$

$$\therefore T_C = 1$$





A Synchronous Counter Using T Flip-Flop

