Computer Architecture

Fall, 2019

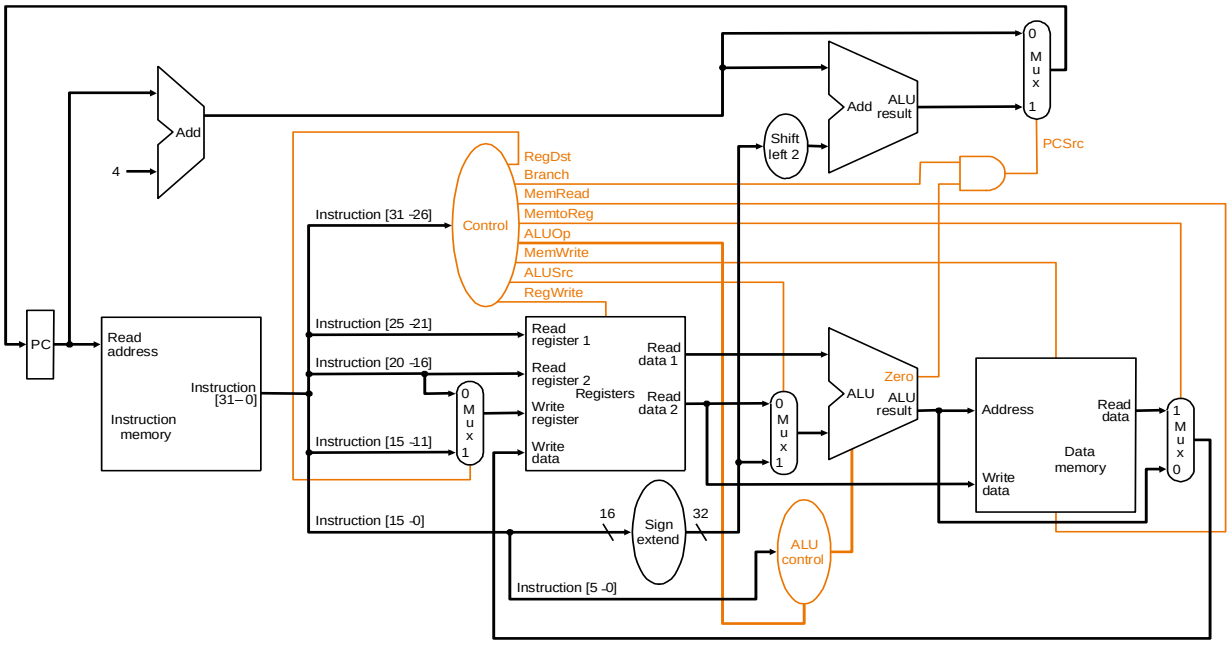
Week 10

2019.11.11

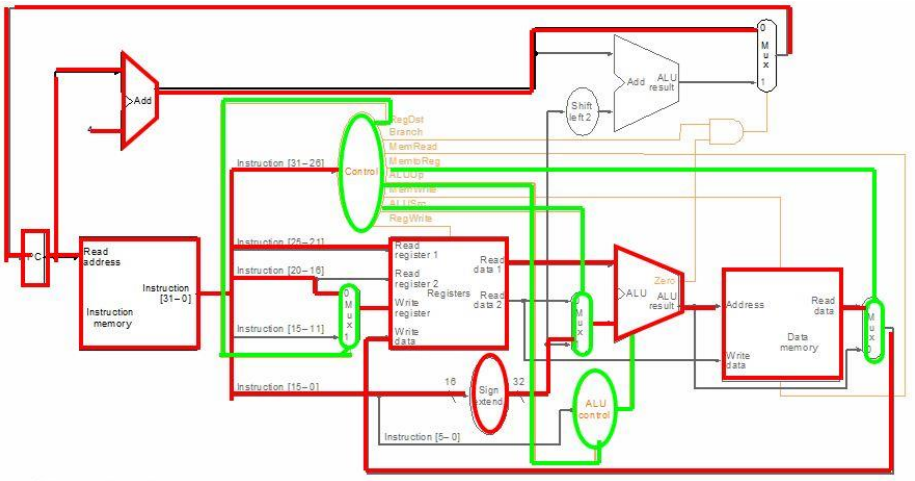
組別：_____ 簽名：_____

[group2]

1. 請畫出 datapath operation for lw



Ans：

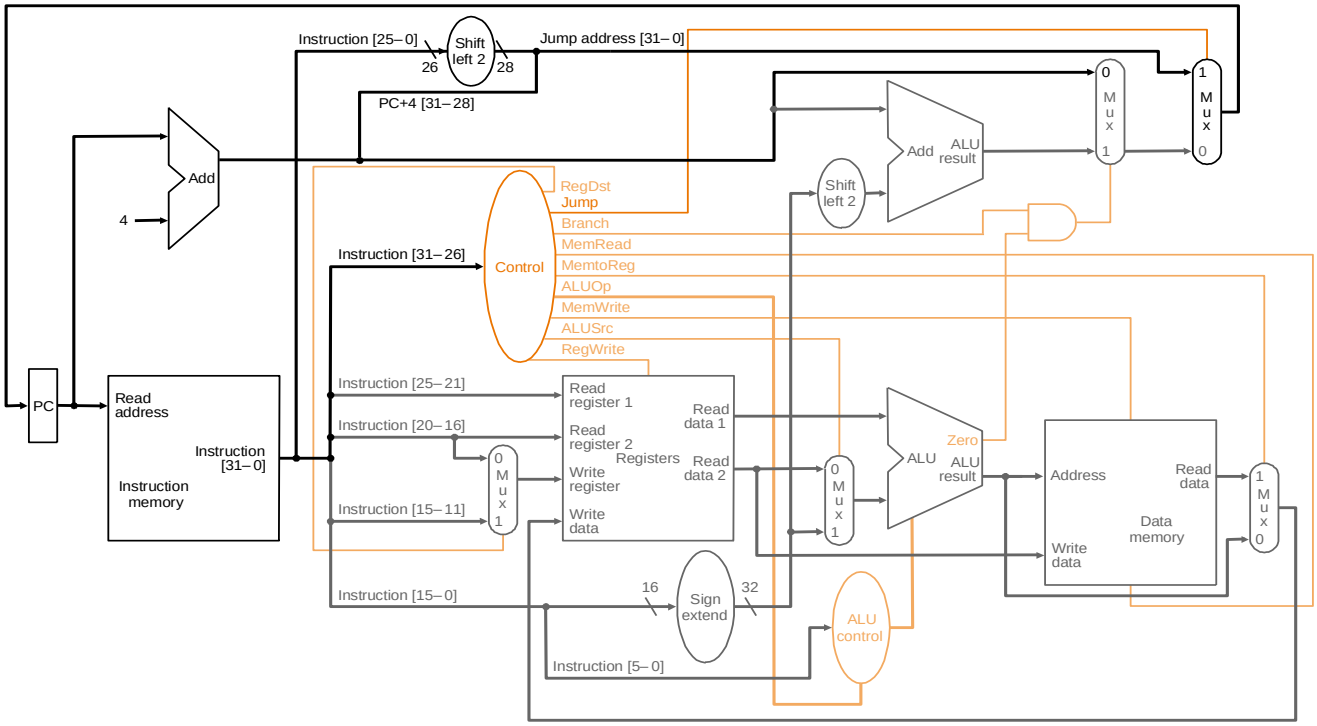


[group3] (對抗賽)

2.

Q: Following problems assume that logic blocks needed to implement a processor's data path have the following latencies:

Operation	Instruction-Memory	Add	Mux	ALU	Register	Data-Memory	Sign-Extend	Shift-Left-2
Latency (ps)	250	60	20	80	100	300	10	5



For the processor shows above, that only has one type of instruction: unconditional PC-relative branch. What would the cycle time be for this datapath? And What's for conditional PC-relative branches ?

A:

Unconditional PC-Relative branch:

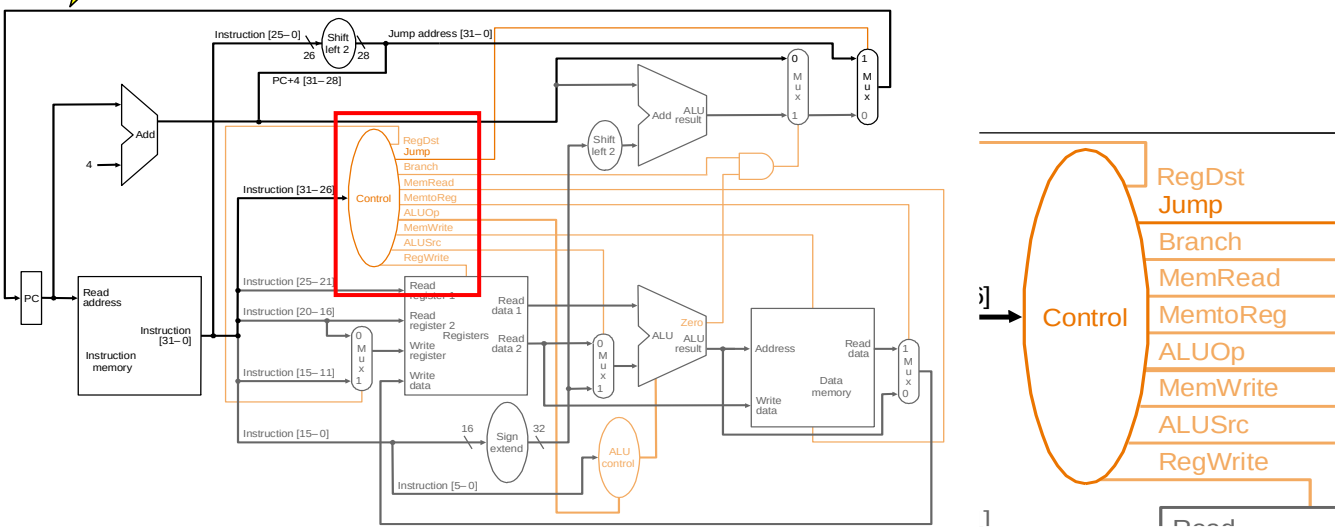
250(Instruction-Memory) + 5(Shift-Left-2) + 20(Mux) = 275 ps

Conditional PC-Relative branch:

250(Instruction-Memory) + 100(Register) + 20(Mux) + 80(ALU) + 20(Mux) + 20(Mux) = 490ps

[group4]

3.



What is each control signals for instruction “beq” and “sw” ? (reference p.66)

Ans：

beq：RegDst：x
ALUSrc：0
MemtoReg：x
RegWrite：0
MemRead：0
MemWrite：0
Branch：1
ALUop：01
jump：0

sw：RegDst：x
ALUSrc：1
MemtoReg：x
RegWrite：0
MemRead：0
MemWrite：1
Branch：0
ALUop：00
jump：0

[group5] (對抗賽)

4. 請問在 controller 解碼 opcode 以後，有哪兩個 control signal 不一定能立刻決定以及其原因？

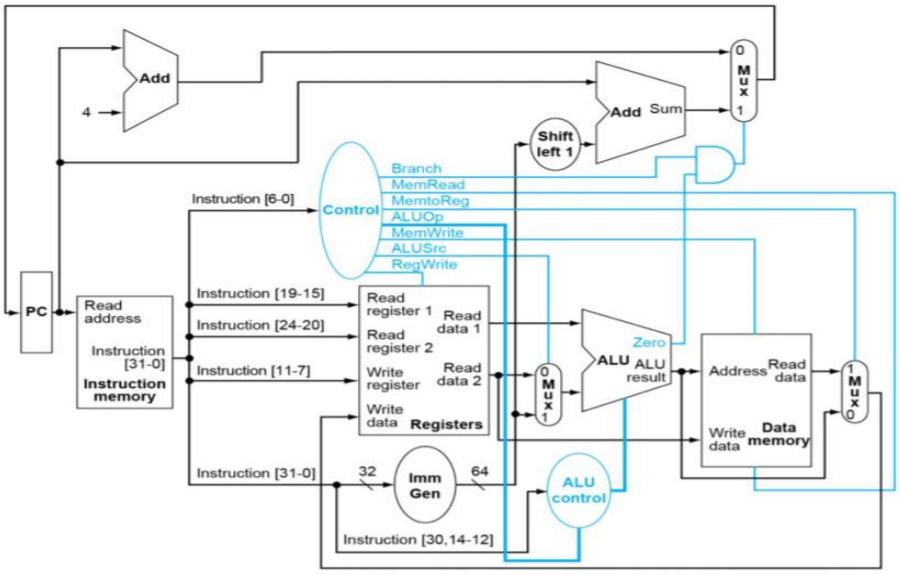
A1.

PCsrc, 因為要等 branch 中兩個比較用的暫存器裡面的值相減完確定是否為零，其結果再跟 Branch 做 and，才有結果

ALU control, 如果是 Rtype 指令，必須要等解完 function code 才能知道是要做什麼樣的 ALU 計算

[group6] (對抗賽)

5.



(a) Consider the single-cycle processor shown above. Which instruction(s) among add, sd, ld, and beq may fail if the signal RegWrite is stuck at 0?

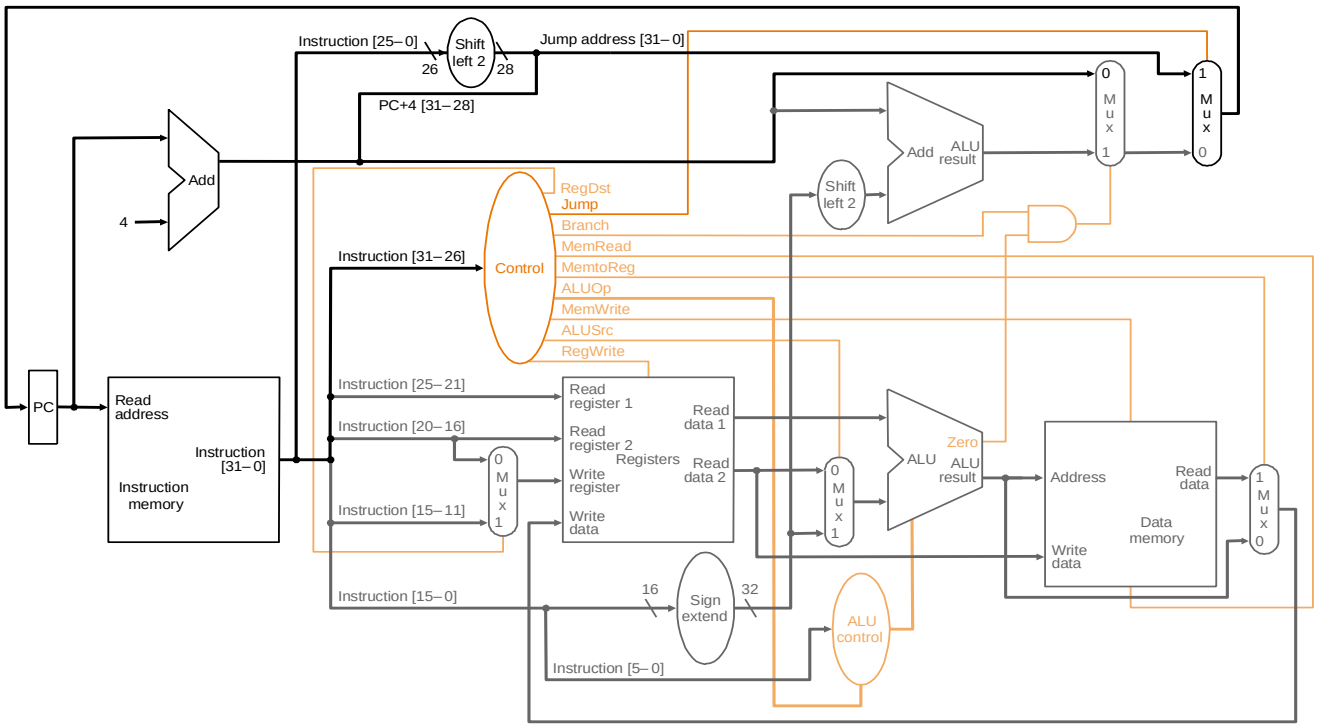
(b) Which instruction(s) among add, sd, ld, and beq may fail if the signal ALUSrc is stuck at 1?

Ans (a): add, ld

Ans (b): add, beq

[group9] (對抗賽)

6. 請請參考以下的 processor 設計圖，完成下列表格的 Mux 控制訊號。(若為 don't care condition，請在該空格中畫 X)



	add	sub	addi	lw	sw	beq	bne
RegDst							
MemtoReg							
ALUSrc							
Branch							

Ans.

	add	sub	addi	lw	sw	beq	bne
RegDst	**1**	**1**	**0**	**0**	**X**	**X**	**X**
MemtoReg	**0**	**0**	**0**	**1**	**X**	**X**	**X**
ALUSrc	**0**	**0**	**1**	**1**	**1**	**0**	**0**
Branch	**0**	**0**	**0**	**0**	**0**	**1**	**1**

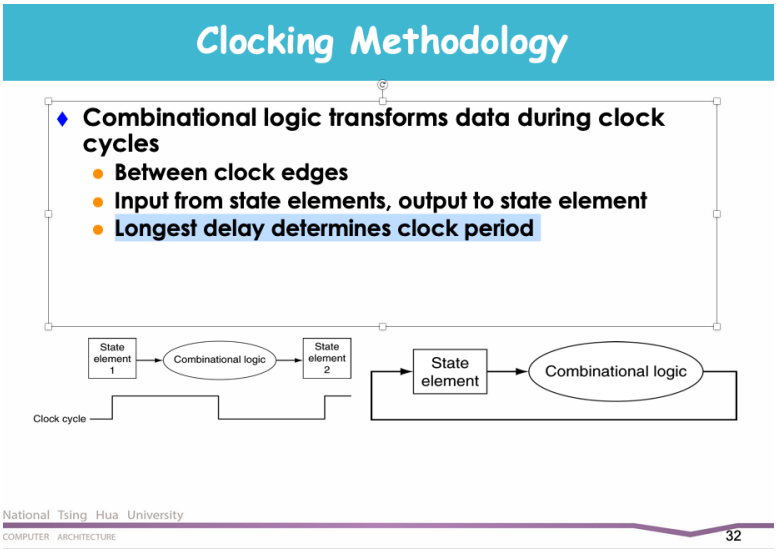
[group10] (對抗賽)

7. 關於 single cycle MIPS CPU 回答以下問題

(1) 請問為什麼要找出 MIPS 設計中的 Critical Path?

(2) Single cycle design 的缺點為？（Hint:請舉例指令，以除了 critical path 的指令所需的 cycle time 和其他指令所需 cycle time 作為比較解釋，或是從 ）

ANS1： 因為 **Longest delay determines clock period**

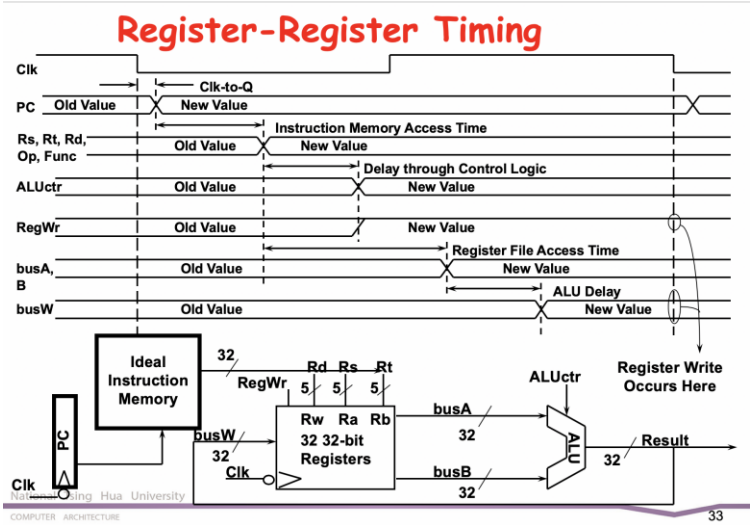


ANS2:

(1)因為 Cycle time 必須設為 critical path 所需的 cycle time，

例如 add 指令不需要那麼長的 cycle time 就可以完成，但執行 add 時還是需要用到 critical path 所需的 cycle time，才可以在執行下一個指令。

(2)在同一 cycle 中大部分 Functional Unit 為 idle 狀態.



[group11] (對抗賽)

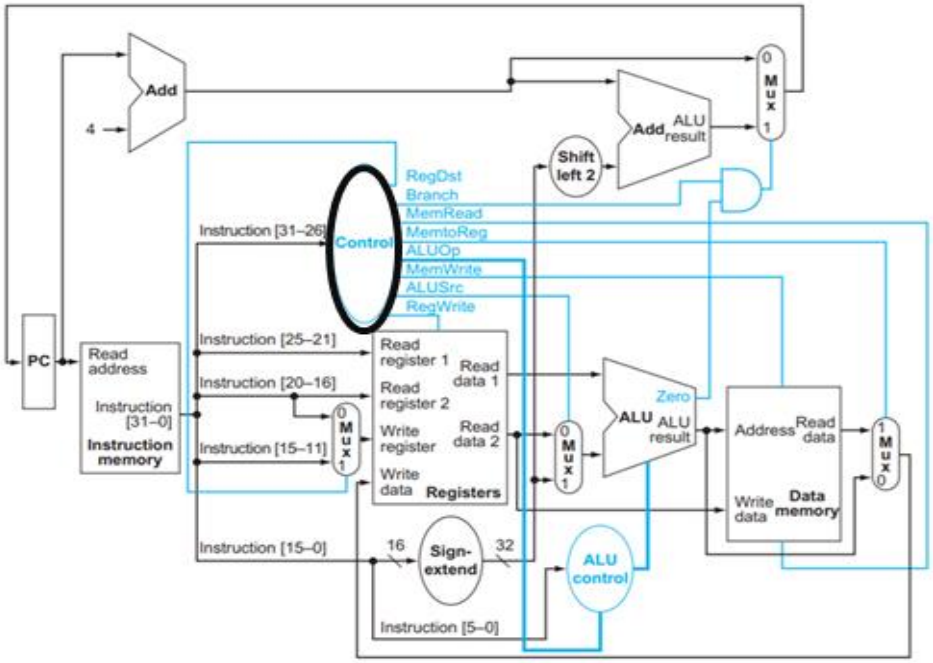
8. Which of the following statement is true?

(A) all of the Mux in this processor can be determined by control.

(B) In R-type, ALU function is defined by ALUop.

(C) Worst case timing in this processor is Load.

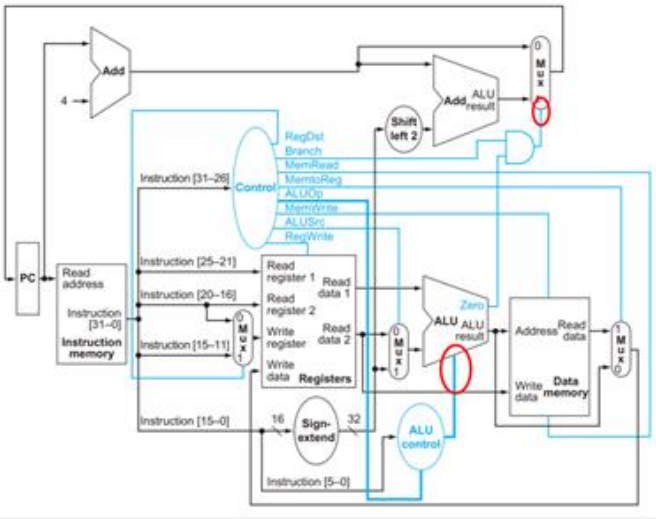
(D) PC always become PC+4 in next cycle.



Ans:

(C) true

(A)



(B) In R-type, ALU function is defined by instruction[5-0]. (ALUop =00)

(D) beq, bne may add PC + 4 + immediate||00

jump will add PC + 4 + PC[31-28]||immediate||00