# NT3H1101/NT3H1201

## NTAG I²C - Energy harvesting NFC Forum Type 2 Tag with field detection pin and I²C interface

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Product data sheet
COMPANY PUBLIC

## 1. General description

NTAG I²C - The entry to the NFC world: simple and lowest cost.

The NTAG I²C is the first product of NXP's NTAG family offering both contactless and contact interfaces (see Figure 1). In addition to the passive NFC Forum compliant contactless interface, the IC features an I²C contact interface, which can communicate with a microcontroller if the NTAG I²C is powered from an external power supply. An additional externally powered SRAM mapped into the memory allows a fast data transfer between the RF and I²C interfaces and vice versa, without the write cycle limitations of the EEPROM memory.

The NTAG I²C product features a configurable field detection pin, which provides a trigger to an external device depending on the activities at the RF interface.

The NTAG I²C product can also supply power to external (low power) devices (e.g. a microcontroller) via the embedded energy harvesting circuitry.

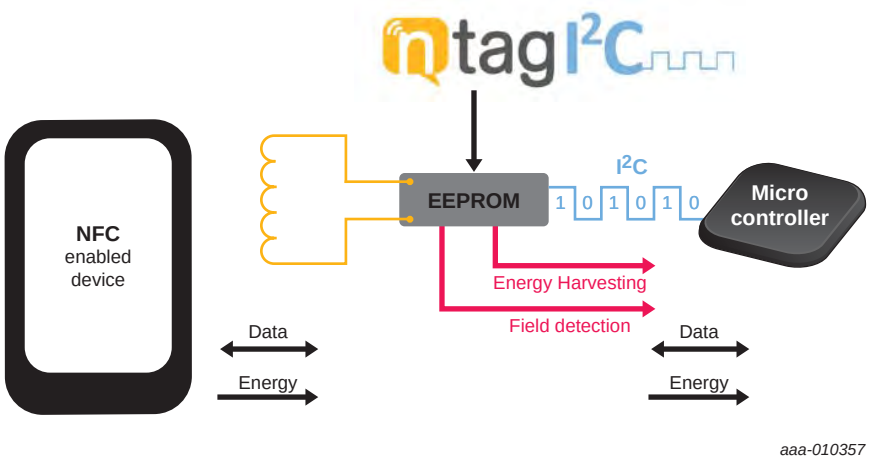



**Fig 1. Contactless and contact system**

# 2. Features and benefits

## 2.1 Key features

- RF interface NFC Forum Type 2 Tag compliant
- I²C interface
- Configurable field detection pin based on open drain implementation that can be triggered upon the following events:
  - RF field presence
  - First start of communication
  - Selection of the tag only
- 64 byte SRAM buffer for fast transfer of data (Pass-through mode) between the RF and the I²C interfaces located outside the User Memory
- Wake up signal at the field detect pin when:
  - New data has arrived from one interface
  - Data has been read by the receiving interface
- Clear arbitration between RF and I²C interfaces:
  - First come, first serve strategy
  - Status flag bits to signal if one interface is busy writing to or reading data from the EEPROM
- Energy harvesting functionality to power external devices (e.g. microcontroller)
- FAST READ command for faster data reading

## 2.2 RF interface

- Contactless transmission of data
- NFC Forum Type 2 Tag compliant (see Ref. 1)
- Operating frequency of 13.56 MHz
- Data transfer of 106 kbit/s
- 4 bytes (one page) written including all overhead in 4.8 ms via EEPROM or 0.8 ms via SRAM (Pass-through mode)
- Data integrity of 16-bit CRC, parity, bit coding, bit counting
- Operating distance of up to 100 mm (depending on various parameters, such as field strength and antenna geometry)
- True anticollision
- Unique 7 byte serial number (cascade level 2 according to ISO/IEC 14443-3 (see Ref. 2)

## 2.3 Memory

- 1904 bytes freely available with User Read/Write area (476 pages with 4 bytes per pages) for the NTAG I²C 2k version
- 888 bytes freely available with User Read/Write area (222 pages with 4 bytes per pages) for the NTAG I²C 1k version
- Field programmable RF read-only locking function with static and dynamic lock bits configurable from both I²C and NFC interfaces
- 64 bytes SRAM volatile memory without write endurance limitation

- Data retention time of 20 years
- Write endurance 500,000 cycles

### 2.4 I²C interface

- I²C slave interface supports Standard (100 kHz) and Fast (up to 400 kHz) mode (see Ref. 3)
- 16 bytes (one block) written in 4.5 ms (EEPROM) or 0.4 ms (SRAM - Pass-through mode) including all overhead
- RFID chip can be used as standard I²C EEPROM

### 2.5 Security

- Manufacturer-programmed 7-byte UID for each device
- Capability container with one time programmable bits
- Field programmable read-only locking function per page for first 12 pages and per 16 (1k version) or 32 (2k version) pages for the extended memory section

### 2.6 Key benefits

- The Pass-through mode allows fast download and upload of data from RF to I²C and vice versa without the cycling limitation of EEPROM
- NDEF message storage up to 1904 bytes (2k version) or up to 888 bytes (1k version)
- The mapping of the SRAM inside the User Memory buffer allows dynamic update of NDEF message content

## 3. Applications

With all its integrated features and functions the NTAG I²C is the ideal solution to enable a contactless communication via an NFC device (e.g., NFC enabled mobile phone) to an electronic device for:

- Zero power configuration (late customization)
- Smart customer interaction (e.g., easier after sales service, such as firmware update)
- Advanced pairing (for e.g., WiFi or Blue tooth) for dynamic generation of sessions keys

Easier product customization and customer experience for the following applications:

- Home automation
- Home appliances
- Consumer electronics
- Healthcare
- Printers
- Smart meters

# 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| NT3H1101W0FUG | FFC bumped | 8 inch wafer, 150um thickness, on film frame carrier, electronic fail die marking according to SECS-II format), Au bumps, 1k Bytes memory, 50pF input capacitance | - |
| NT3H1201W0FUG | FFC bumped | 8 inch wafer, 150um thickness, on film frame carrier, electronic fail die marking according to SECS-II format), Au bumps, 2k Bytes memory, 50pF input capacitance | - |
| NT3H1101W0FHK | XQFN8 | Plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.6mm; 1k bytes memory, 50pF input capacitance | SOT902-3 |
| NT3H1201W0FHK | XQFN8 | Plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.6mm; 2k bytes memory, 50pF input capacitance | SOT902-3 |
| NT3H1101W0FTT | TSSOP8 | Plastic thin shrink small outline package; 8 leads; body width 3 mm; 1k bytes memory; 50pF input capacitance | SOT505-1 |
| NT3H1201W0FTT | TSSOP8 | Plastic thin shrink small outline package; 8 leads; body width 3 mm; 2k bytes memory; 50pF input capacitance | SOT505-1 |

# 5. Marking

**Table 2. Marking codes**

| Type number | Marking code |
|---|---|
| NT3H1201FHK | N12 |
| NT3H1101FHK | N11 |
| NT3H1101W0FFT | 31101 |
| NT3H1201W0FFT | 31201 |

## 6. Block diagram

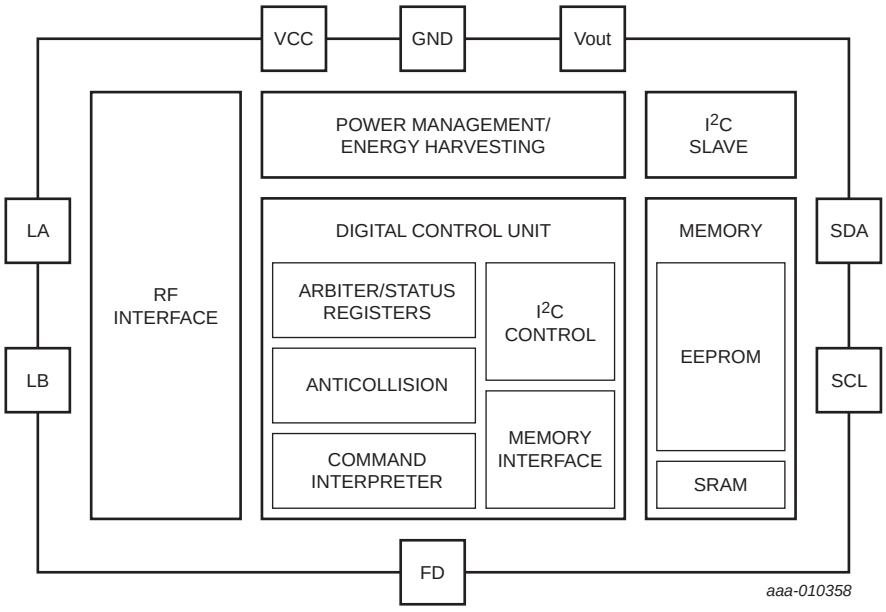
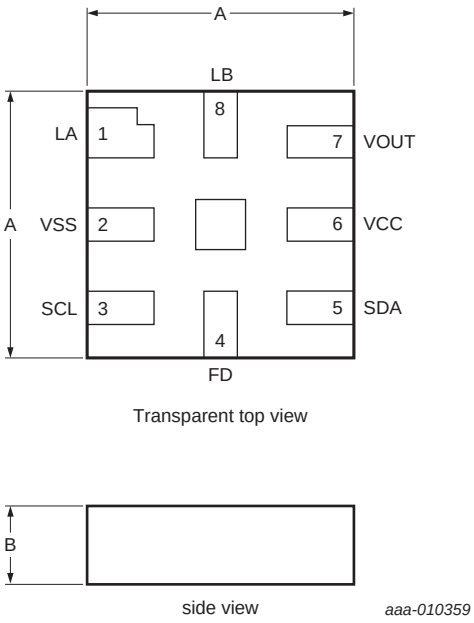



**Fig 2. Block diagram**

# 7. Pinning information

## 7.1 Pinning

### 7.1.1 XQFN8

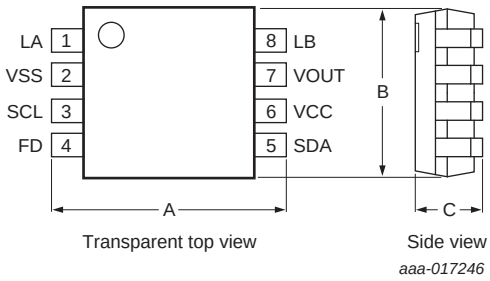



(1) Dimension A: 1.6 mm

(2) Dimension B: 0.5 mm

**Fig 3. Pin configuration for XQFN8**

### 7.1.2 TSSOP8




(1) Dimension A: 5.1 mm

(2) Dimension B: 3.1 mm

(3) Dimension C: 1.1 mm

**Fig 4. Pin configuration for TSSOP8**

## 7.2 Pin description

**Table 3. Pin description for XQFN8 and TSSOP8**

| Pin | Symbol | Description |
|---|---|---|
| 1 | LA | Antenna connection LA |
| 2 | VSS | GND |
| 3 | SCL | Serial Clock I²C |
| 4 | FD | Field detection |
| 5 | SDA | Serial data I²C |
| 6 | VCC | VCC in connection (external power supply) |
| 7 | VOUT | Voltage out (energy harvesting) |
| 8 | LB | Antenna connection LB |

NXP recommends leaving the central pad of the XQFN8 package unconnected.

# 8. Functional description

## 8.1 Block description

NTAG I²C ICs consist of (see details below): 2016 bytes of EEPROM memory, 64 Bytes of SRAM, a RF interface, Digital Control Unit (DCU), Power Management Unit (PMU) and an I²C interface. Energy and data are transferred via an antenna consisting of a coil with a few turns, which is directly connected to NTAG I²C IC.

- RF interface:
  - modulator/demodulator
  - rectifier
  - clock regenerator
  - Power-On Reset (POR)
  - voltage regulator
- Anticollision: multiple cards may be selected and managed in sequence
- Command interpreter: processes memory access commands supported by the NTAG I²C
- EEPROM interface

## 8.2 RF interface

The RF-interface is based on the ISO/IEC 14443 Type A standard.

This RF interface is passive and therefore requires to be supplied by an RF field (e.g. NFC enabled device) at all times to be able to operate. It is not operating even if the NTAG I²C is powered via its contact interface (Vcc).

Data transmission from the RF interface is only happening if RF field from an NFC enabled device is available and adequate commands are sent to retrieve data from the NTAG I²C.

For both directions of data communication, there is one start bit (start of communication) at the beginning of each frame. Each byte is transmitted with an odd parity bit at the end. The LSB of the byte with the lowest address of the selected block is transmitted first.

The maximum length of an NFC device to tag frame used in this product is 82 bits (7 data bytes + 2 CRC bytes = 7×9 + 2×9 + 1 start bit).

The maximum length of a tag to NFC device frame (response to READ command) is 163 bits (16 data bytes + 2 CRC bytes = 16 × 9 + 2 × 9 + 1 start bit).

In addition the proprietary FAST_READ command has a variable response frame length, which depends on the start and end address parameters. E.g. when reading the SRAM at once the length of the response is 595 bits (64 data bytes + 2 CRC bytes = 64 × 9 + 2 × 9 + 1 start bit). The overall maximum supported response frame length for FAST READ is up to 9235 bits (1024 data bytes + 2 CRC bytes = 1024 × 9 + 2 × 9 + 1 start bit), but here the maximum frame length supported by the NFC device must be taken into account when issuing this command.

For a multi-byte parameter, the least significant byte is always transmitted first. For example, when reading from the memory using the READ command, byte 0 from the addressed block is transmitted first, followed by bytes 1 to byte 3 out of this block. The same sequence continues for the next block and all subsequent blocks.

### 8.2.1 Data integrity

The following mechanisms are implemented in the contactless communication link between the NFC device and the NTAG I²C IC to ensure very reliable data transmission:

- 16 bits CRC per block
- Parity bits for each byte
- Bit count checking
- Bit coding to distinguish between “1”, “0” and “no information”
- Channel monitoring (protocol sequence and bit stream analysis)

The commands are initiated by the NFC device and controlled by the Digital Control Unit of the NTAG I²C IC. The command response depends on the state of the IC, and for memory operations, also on the access conditions valid for the corresponding page.

### 8.2.2 RF communication principle

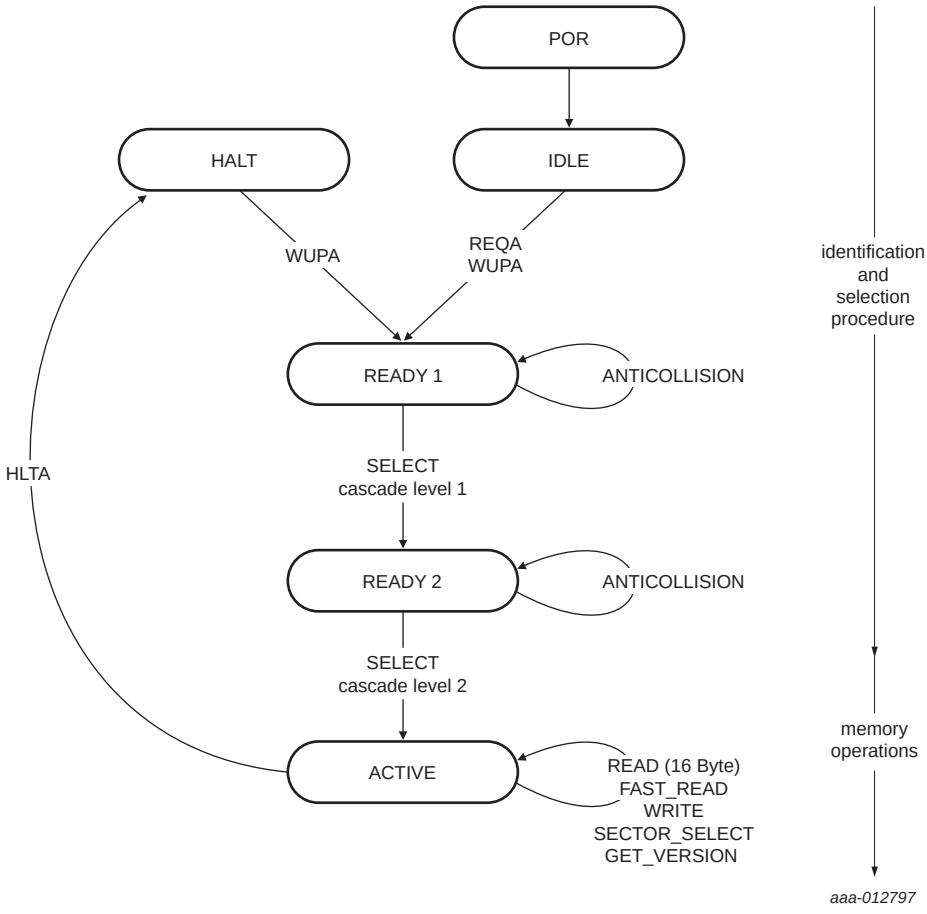



**Fig 5. RF communication principle of NTAG I²C**

The overall RF communication principle is summarized in Figure 5.

#### 8.2.2.1 IDLE state

After a power-on reset (POR), the NTAG I²C switches to the IDLE state. It only exits this state when a REQA or a WUPA command is received from the NFC device. Any other data received while in this state is interpreted as an error, and the NTAG I²C remains in the IDLE state.

After a correctly executed HLTA command e.g., out of the ACTIVE state, the default waiting state changes from the IDLE state to the HALT state. This state can then only be exited with a WUPA command.

#### 8.2.2.2 READY 1 state

In the READY 1 state, the NFC device resolves the first part of the UID (3 bytes) using the ANTICOLLISION or SELECT commands in cascade level 1. This state is correctly exited after execution of the following command:

- SELECT command from cascade level 1: the NFC device switches the NTAG I²C into READY2 state where the second part of the UID is resolved.

#### 8.2.2.3 READY 2 state

In the READY 2 state, the NTAG I²C supports the NFC device in resolving the second part of its UID (4 bytes) with the cascade level 2 ANTICOLLISION command. This state is usually exited using the cascade level 2 SELECT command.

**Remark:** The response of the NTAG I²C to the SELECT command is the Select AcKnowledge (SAK) byte. In accordance with ISO/IEC 14443, this byte indicates if the anticollision cascade procedure has finished. If finished, the NTAG I²C is now uniquely selected and only this device will communicate with the NFC device even when other contactless devices are present in the NFC device field.

#### 8.2.2.4 ACTIVE state

All memory operations are operated in the ACTIVE state.

The ACTIVE state is exited with the HLTA command and upon reception, the NTAG I²C transits to the HALT state. Any other data received when the device is in this state is interpreted as an error. Depending on its previous state, the NTAG I²C returns to either to the IDLE state or HALT state.

#### 8.2.2.5 HALT state

HALT and IDLE states constitute the two wait states implemented in the NTAG I²C. An already processed NTAG I²C can be set into the HALT state using the HLTA command. In the anticollision phase, this state helps the NFC device distinguish between processed tags and tags yet to be selected. The NTAG I²C can only exit this state upon execution of the WUPA command. Any other data received when the device is in this state is interpreted as an error, and NTAG I²C state remains unchanged.

## 8.3 Memory organization

The memory map is detailed in Table 4 (1k memory) and Table 5 (2k memory) from the RF interface and in Table 6 (1k memory) and Table 7 (2k memory) from the I²C interface. The SRAM memory is not mapped from the RF interface, because in the default settings of the NTAG I²C the Pass-through mode is not enabled. Please refer to Section 11 for examples of memory map from the RF interface with SRAM mapping.

The structure of manufacturing data, static lock bytes, capability container and user memory pages (except of the user memory length) are compatible with other NTAG products.

Any memory access which starts at a valid address and extends into an invalid access region will return 00h value in the invalid region.

### 8.3.1 Memory map from RF interface

Memory access from the RF interface is organized in pages of 4 bytes each.

**Table 4. NTAG I²C 1k memory organization from the RF interface**

| Sector address | Page address | | Byte number within a page | | | | Access conditions |
|---|---|---|---|---|---|---|---|
| | Dec. | Hex. | 0 | 1 | 2 | 3 | |
| 0 | 0 | 00h | Serial number | | | | READ |
| | 1 | 01h | Serial number | | | Internal | READ |
| | 2 | 02h | Internal | | Static lock bytes | | READ/R&W |
| | 3 | 03h | Capability Container (CC) | | | | READ&WRITE |
| | 4 | 04h | User memory | | | | READ&WRITE |
| | ... | ... | | | | | |
| | 15 | 0Fh | | | | | |
| | ... | ... | | | | | |
| | 225 | E1h | | | | | |
| | 226 | E2h | Dynamic lock bytes | | | 00h | R&W/READ |
| | 227 | E3h | Invalid access - returns NAK | | | | n.a. |
| | 228 | E4h | | | | | |
| | 229 | E5h | | | | | |
| | 230 | E6h | | | | | |
| | 231 | E7h | | | | | |
| | 232 | E8h | Configuration registers | | | | see 8.3.11 |
| | 233 | E9h | | | | | |
| | 234 | EAh | Invalid access - returns NAK | | | | n.a. |
| | ... | ... | | | | | |
| | 255 | FFh | | | | | |
| 1 | ... | ... | Invalid access - returns NAK | | | | n.a. |
| 2 | ... | ... | Invalid access - returns NAK | | | | n.a. |
| 3 | 0 | 00h | Invalid access - returns NAK | | | | n.a. |
| | ... | ... | | | | | |
| | 248 | F8h | Session registers | | | | see 8.3.11 |
| | 249 | F9h | | | | | |
| | ... | ... | Invalid access - returns NAK | | | | n.a. |
| | 255 | FFh | | | | | |

**Table 5. NTAG I²C 2k memory organization from the RF interface**

| Sector address | Page address | | Byte number within a page | | | | Access conditions |
|---|---|---|---|---|---|---|---|
| | Dec. | Hex. | 0 | 1 | 2 | 3 | |
| 0 | 0 | 00h | Serial number | | | | READ |
| | 1 | 01h | Serial number | | | Internal | READ |
| | 2 | 02h | Internal | | Static lock bytes | | READ/R&W |
| | 3 | 03h | Capability Container (CC) | | | | READ&WRITE |
| | 4 | 04h | User memory | | | | READ&WRITE |
| | ... | ... | | | | | |
| | 15 | 0Fh | | | | | |
| | ... | ... | | | | | |
| | ... | ... | | | | | |
| | 255 | FFh | | | | | |
| 1 | 0 | ... | | | | | |
| | 1 | ... | | | | | |
| | ... | ... | | | | | |
| | ... | ... | | | | | |
| | 223 | DFh | | | | | |
| | 224 | E0h | Dynamic lock bytes | | | 00h | R&W/READ |
| | 225 | E1h | Invalid access - returns NAK | | | | n.a. |
| | 226 | E2h | | | | | |
| | 227 | E3h | | | | | |
| | 228 | E4h | | | | | |
| | 229 | E5h | | | | | |
| | 230 | E6h | | | | | |
| | 231 | E7h | | | | | |
| | 232 | E8h | Configuration registers | | | | see 8.3.11 |
| | 233 | E9h | | | | | |
| | 234 | EAh | Invalid access - returns NAK | | | | n.a. |
| | ... | ... | | | | | |
| | 255 | FFh | | | | | |
| 2 | ... | ... | Invalid access - returns NAK | | | | n.a. |
| 3 | 0 | 00h | Invalid access - returns NAK | | | | n.a. |
| | ... | ... | | | | | |
| | 248 | F8h | Session registers | | | | see 8.3.11 |
| | 249 | F9h | | | | | |
| | ... | ... | Invalid access - returns NAK | | | | n.a. |
| | 255 | FFh | | | | | |

### 8.3.2 Memory map from I²C interface

The memory access of NTAG I²C from the I²C interface is organized in blocks of 16 bytes each.

**Table 6. NTAG I²C 1k memory organization from the I²C interface**

| I²C block address | | Byte number within a block | | | | Access conditions |
|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | |
| | | 4 | 5 | 6 | 7 | |
| | | 8 | 9 | 10 | 11 | |
| Dec. | Hex. | 12 | 13 | 14 | 15 | |
| 0 | 00h | I²C addr.* | Serial number | | | R&W/READ |
| | | Serial number | | | Internal | READ |
| | | Internal | | Static lock bytes | | READ/R&W |
| | | Capability Container (CC) | | | | READ&WRITE |
| 1 | 01h | User memory | | | | READ&WRITE |
| ... | ... | | | | | |
| 55 | 37h | | | | | |
| 56 | 38h | User memory | | | | READ&WRITE |
| | | User memory | | | | READ&WRITE |
| | | Dynamic lock bytes | | | 00h | READ&WRITE |
| | | 00h | 00h | 00h | 00h | READ |
| 57 | 39h | Invalid access - returns NAK | | | | n.a. |
| 58 | 3Ah | Configuration registers | | | | see 8.3.11 |
| | | 00h | 00h | 00h | 00h | READ |
| | | 00h | 00h | 00h | 00h | |
| 59 | 3Bh | Invalid access - returns NAK | | | | n.a. |
| ... | ... | | | | | |
| 247 | F7h | | | | | |
| 248 | F8h | SRAM memory (64 bytes) | | | | READ&WRITE |
| ... | ... | | | | | |
| 251 | FBh | | | | | |
| ... | ... | Invalid access - returns NAK | | | | n.a. |
| 254 | FEh | Session registers (requires READ register command) | | | | see 8.3.11 |
| | | 00h | 00h | 00h | 00h | READ |
| | | 00h | 00h | 00h | 00h | |
| ... | ... | Invalid access - returns NAK | | | | n.a. |

**Remark: *** The byte 0 of block 0 is always read as 04h. Writing to this byte modifies the I²C address.

**Table 7. NTAG I²C 2k memory organization from the I²C interface**

| I²C block address | | Byte number within a block | | | | Access conditions |
|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | |
| | | 4 | 5 | 6 | 7 | |
| | | 8 | 9 | 10 | 11 | |
| Dec. | Hex. | 12 | 13 | 14 | 15 | |
| 0 | 00h | I²C addr.* | Serial number | | | R&W/READ |
| | | Serial number | | | Internal | READ |
| | | Internal | | Static lock bytes | | READ/R&W |
| | | Capability Container (CC) | | | | READ&WRITE |
| 1 | 01h | User memory | | | | READ&WRITE |
| ... | ... | | | | | |
| 119 | 77h | | | | | |
| 120 | 78h | Dynamic lock bytes | | | 00h | READ&WRITE |
| | | 00h | 00h | 00h | 00h | READ |
| | | 00h | 00h | 00h | 00h | |
| | | 00h | 00h | 00h | 00h | |
| 121 | 79h | Invalid access - returns NAK | | | | n.a. |
| 122 | 7Ah | Configuration registers | | | | see 8.3.11 |
| | | 00h | 00h | 00h | 00h | READ |
| | | 00h | 00h | 00h | 00h | |
| 127 | 7Bh | Invalid access - returns NAK | | | | n.a. |
| ... | ... | | | | | |
| 247 | F7h | | | | | |
| 248 | F8h | SRAM memory (64 bytes) | | | | READ&WRITE |
| ... | ... | | | | | |
| 251 | FBh | | | | | |
| ... | ... | Invalid access - returns NAK | | | | n.a. |
| 254 | FEh | Session registers (requires READ register command) | | | | see 8.3.11 |
| | | 00h | 00h | 00h | 00h | READ |
| | | 00h | 00h | 00h | 00h | |
| ... | ... | Invalid access - returns NAK | | | | n.a. |

**Remark: *** The byte 0 of block 0 is always read as 04h. Writing to this byte modifies the I²C address.

### 8.3.3 EEPROM

The EEPROM is a non volatile memory that stores the 7 byte UID, the memory lock conditions, IC configuration information and the 1904 bytes user data (888 byte user data in case of the NTAG I²C 1k version).

### 8.3.4 SRAM

For frequently changing data, a volatile memory of 64 bytes with unlimited endurance is built in. The 64 bytes are mapped in a similar way as done in the EEPROM, i.e., 64 bytes are seen as 16 pages of 4 bytes.

The SRAM is only available if the tag is powered via the VCC pin.

The SRAM is located at the end of the memory space and it is always directly accessible by the I²C host (addresses F8h to FBh). An RF reader cannot access the SRAM memory in normal mode (i.e., outside the Pass-through mode). The SRAM is only accessible by the RF reader if the SRAM is mirrored onto the EEPROM memory space.

With Memory Mirror enabled (SRAM_MIRROR_ON_OFF = 1b - see Section 11.2), the SRAM can be mirrored in the User Memory (page 1 to page 116 - see Section 11.2) for access from the RF side.

The Memory mirror must be enabled once both interfaces are ON as this feature is disabled after each POR.

The register SRAM_MIRROR_BLOCK (see Table 14) indicates the address of the first page of the SRAM buffer. In the case where the SRAM mirror is enabled and the READ command is addressing blocks where the SRAM mirror is located, the SRAM mirror byte values will be returned instead of the EEPROM byte values. Similarly, if the tag is not VCC powered, the SRAM mirror is disabled and reading out the bytes related to the SRAM mirror position would return the values from the EEPROM.

In the Pass-through mode (PTHRU_ON_OFF = 1b - see Section 8.3.11), the SRAM is mirrored to the fixed address 240 - 255 for RF access (see Section 11) in the first memory sector for NTAG I²C 1k and in the second memory sector for NTAG I²C 2k.

### 8.3.5 UID/serial number

The unique 7-byte serial number (UID) is programmed into the first 7 bytes of memory covering page addresses 00h and 01h - see Figure 6. These bytes are programmed and write protected in the production test.

SN0 holds the Manufacturer ID for NXP Semiconductors (04h) in accordance with ISO/IEC 14443-3.

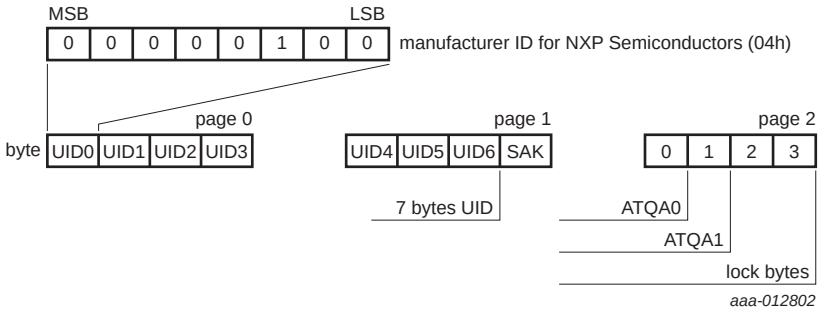



**Fig 6. UID/serial number**

### 8.3.6 Static lock bytes

The bits of byte 2 and byte 3 of page 02h (via RF) or byte 10 and 11 address 0h (via I²C) represent the field programmable, read-only locking mechanism (see Figure 7). Each page from 03h (CC) to 0Fh can be individually locked by setting the corresponding locking bit Lx to logic 1 to prevent further write access. After locking, the corresponding page becomes read-only memory.

The three least significant bits of lock byte 0 are the block-locking bits. Bit 2 controls pages 0Ah to 0Fh (via RF), bit 1 controls pages 04h to 09h (via RF) and bit 0 controls page 03h (CC). Once the block-locking bits are set, the locking configuration for the corresponding memory area is frozen.

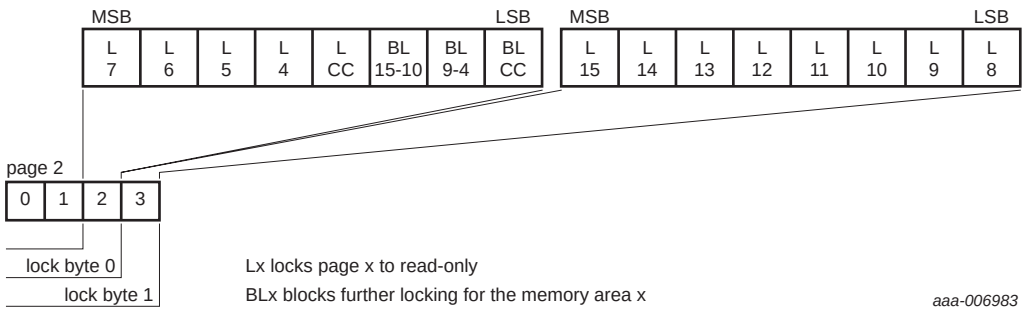



**Fig 7. Static lock bytes 0 and 1**

For example, if BL15-10 is set to logic 1, then bits L15 to L10 (lock byte 1, bit[7:2]) can no longer be changed. The static locking and block-locking bits are set by the bytes 2 and 3 of the WRITE command to page 02h. The contents of the lock bytes are bit-wise OR'ed and the result then becomes the new content of the lock bytes.

This process is irreversible from RF perspective. If a bit is set to logic 1, it cannot be changed back to logic 0. From I²C perspective, the bits can be reset to 0b by writing bytes 10 and 11 of block 0. I²C address is coded in byte 0 of block 0 and may be changed unintentionally.

The contents of bytes 0 and 1 of page 02h are unaffected by the corresponding data bytes of the WRITE.

The default value of the static lock bytes is 00 00h.

### 8.3.7 Dynamic Lock Bytes

To lock the pages of NTAG I²C starting at page address 10h and onwards, the dynamic lock bytes are used. The dynamic lock bytes are located at page E2h sector 0 (NTAG I2C 1k) or address E0h sector 1 (NTAG I2C 2k). The three lock bytes cover the memory area of 830 data bytes (NTAG I2C 1k) or 1846 data bytes (NTAG I2C 2k). The granularity is 16 pages for NTAG I2C 1k (see Figure 8) and 32 pages for NTAG I2C 2k (see Figure 9) compared to a single page for the first 48 bytes (see Figure 7).

**Remark:** Set all bits marked with RFUI to 0 when writing to the dynamic lock bytes.

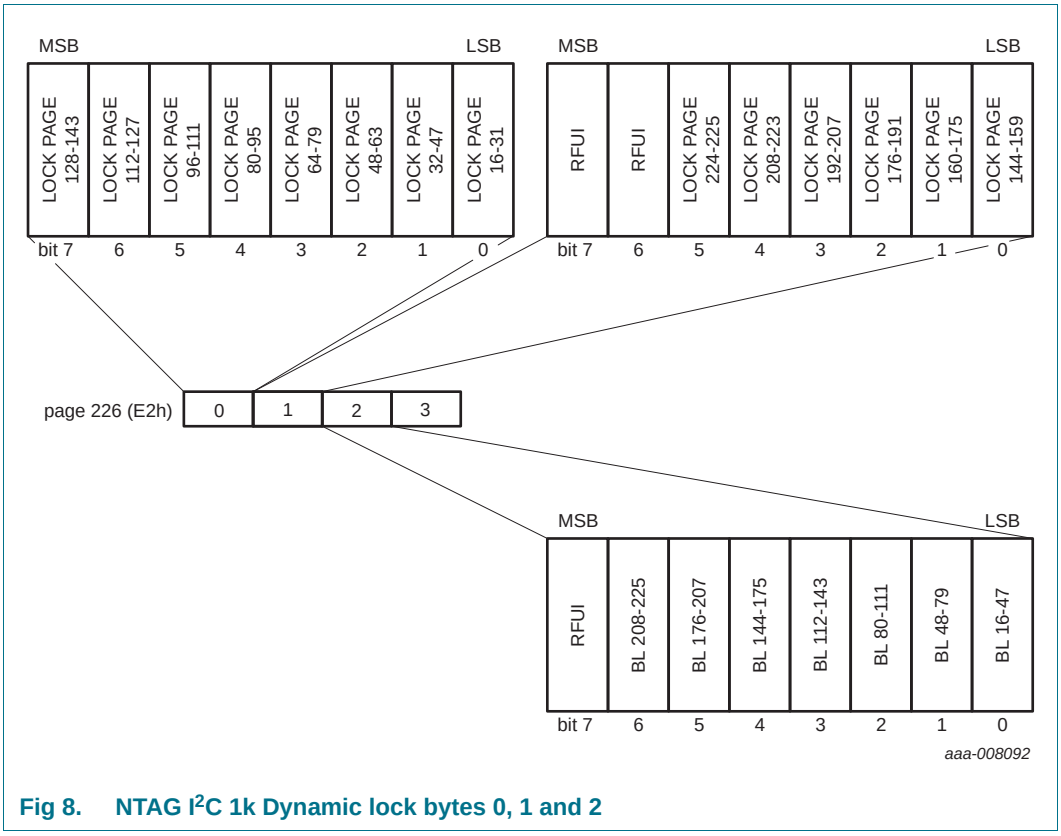



**Fig 8. NTAG I²C 1k Dynamic lock bytes 0, 1 and 2**

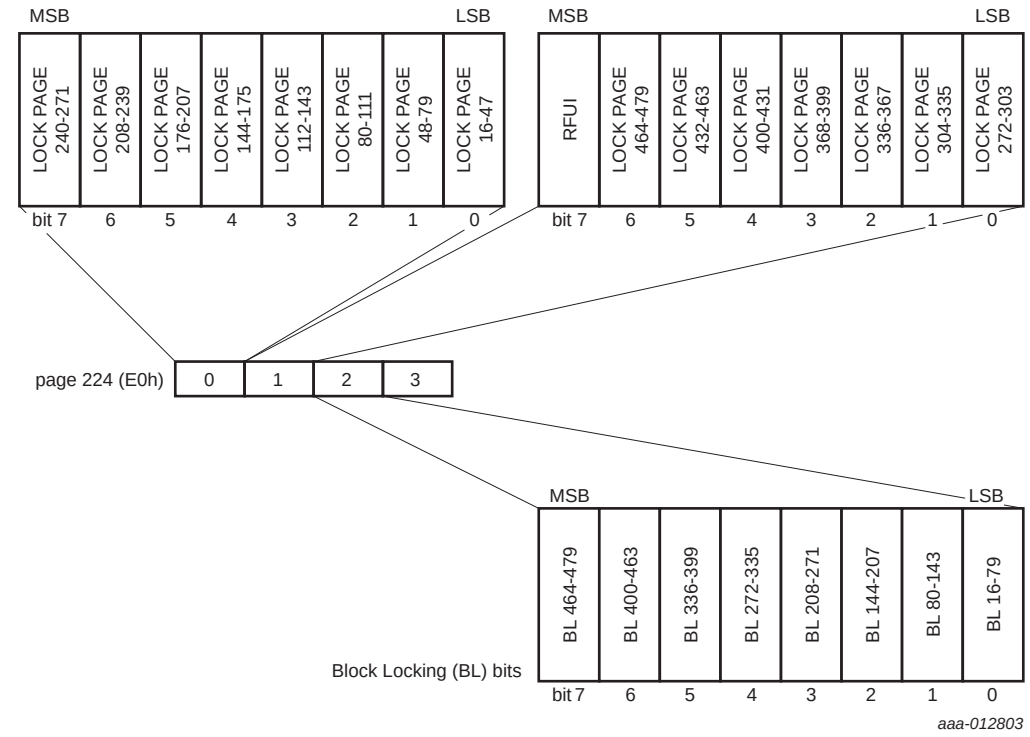



**Fig 9. NTAG I²C 2k Dynamic lock bytes 0, 1 and 2**

The default value of the dynamic lock bytes is 00 00 00h. The value of Byte 3 is always 00h when read.

Reading the 3 bytes for the dynamic lock bytes and the Byte 3 (00h) from RF interface (address E2h sector 0 (NTAG I²C 1k) or E0h sector 1 (NTAG I²C 2k) or from I²C (address 38h (NTAG I²C 1k) or 78h (NTAG I²C 2k)) will also return a fixed value for the next 12 bytes of 00h.

Like for the static lock bytes, this process of modifying the dynamic lock bytes is irreversible from RF perspective. If a bit is set to logic 1, it cannot be changed back to logic 0. From I²C perspective, the bits can be reset to 0b.

### 8.3.8 Capability Container (CC bytes)

The Capability Container CC (page 03h) is programmed during the IC production according to the NFC Forum Type 2 Tag specification (see Ref. 1). These bytes may be bit-wise modified by a WRITE command from the I²C or RF interface. Once set to 1b, it is only possible to reset it to 0b from I²C perspective. I²C address (byte 0) and static lock bytes (byte 10 and byte 11) are coded in block 0 and may be changed unintentionally.

See examples for NTAG I²C 1k version in Figure 10 and for NTAG I²C 2k version in Figure 11.

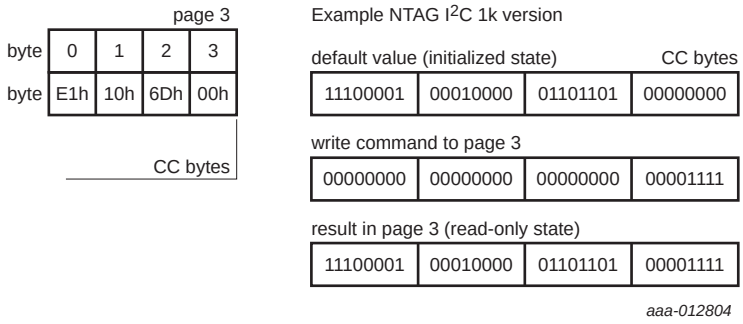



**Fig 10. CC bytes of NTAG I²C 1k version**

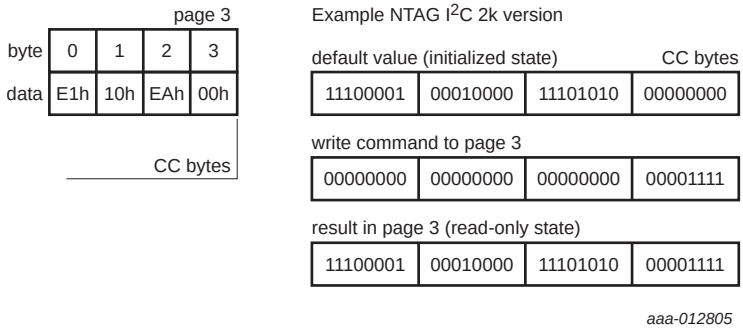



**Fig 11. CC bytes of NTAG I²C 2k version**

The default values of the CC bytes at delivery are defined in Section 8.3.10.

### 8.3.9 User Memory pages

Pages 04h to E1h via the RF interface - Block 01h to 37h, plus the first 8 bytes of block 38h via the I²C interface are the user memory read/write areas for NTAG I²C 1k version.

Pages 04h (sector 0) to DFh (sector 1) via the RF interface - Block 1h to 77h via the I²C interface are the user memory read/write areas for NTAG I²C 2k version.

The default values of the data pages at delivery are defined in Section 8.3.10.

### 8.3.10 Memory content at delivery

The capability container in page 03h and the page 04h and 05h of NTAG I²C is pre-programmed to the initialized state according to the NFC Forum Type 2 Tag specification (see Ref. 1) as defined in Table 8 (NTAG I²C 1k version) and Table 9 (NTAG I²C 2k version). This content is READ only from the RF side and READ&WRITE from the I²C side.

The User memory contains an empty NDEF TLV.

**Remark:** The default content of the data pages from page 05h onwards is not defined at delivery.

**Table 8. Memory content at delivery NTAG I²C 1k version**

| Page Address | Byte number within page | | | |
|---|---|---|---|---|
| | 0 | 1 | 2 | 3 |
| 03h | E1h | 10h | 6Dh | 00h |
| 04h | 03h | 00h | FEh | 00h |
| 05h | 00h | 00h | 00h | 00h |

**Table 9. Memory content at delivery NTAG I²C 2k version**

| Page Address | Byte number within page | | | |
|---|---|---|---|---|
| | 0 | 1 | 2 | 3 |
| 03h | E1h | 10h | EAh | 00h |
| 04h | 03h | 00h | FEh | 00h |
| 05h | 00h | 00h | 00h | 00h |

### 8.3.11 NTAG I²C configuration and session registers

NTAG I²C functionalities can be configured and read in two separate locations depending if the configurations shall be effective within the communication session (session registers) or by default after Power On Reset (POR) (configuration bits).

The configuration registers of pages E8h to E9h (sector 0 - see Table 10, or 1 - see Table 11, depending if it is for NTAG I²C 1k or 2k) via the RF interface or block 3Ah or 7Ah (depending if it is for NTAG I²C 1k or 2k) via the I²C interface are used to configure the default functionalities of the NTAG I²C. Those bit values are stored in the EEPROM and represent the default settings to be effective after POR. Their values can be read & written by both interfaces when applicable and when not locked by the register lock bits (see REG_LOCK in Table 13).

**Table 10. Configuration registers NTAG I²C 1k**

| RF address (sector 0) | | I²C Address | | Byte number | | | |
|---|---|---|---|---|---|---|---|
| Dec | Hex | Dec | Hex | 0 | 1 | 2 | 3 |
| 232 | E8h | 58 | 3Ah | NC_REG | LAST_NDEF_BLOCK | SRAM_MIRROR_BLOCK | WDT_LS |
| 233 | E9h | | | WDT_MS | I2C_CLOCK_STR | REG_LOCK | 00h fixed |

**Table 11. Configuration registers NTAG I²C 2k**

| RF address (sector 1) | | I²C Address | | Byte number | | | |
|---|---|---|---|---|---|---|---|
| Dec | Hex | Dec | Hex | 0 | 1 | 2 | 3 |
| 232 | E8h | 122 | 7Ah | NC_REG | LAST_NDEF_BLOCK | SRAM_MIRROR_BLOCK | WDT_LS |
| 233 | E9h | | | WDT_MS | I2C_CLOCK_STR | REG_LOCK | 00h fixed |

The session registers Pages F8h to F9h (sector 3) via the RF interface or block FEh via I²C, see Table 12, are used to configure or monitor the values of the current communication session. Those bits can only be read via the RF interface but both read and written via the I²C interface.

**Table 12. Session registers NTAG I²C 1k and 2k**

| RF address (sector 3) | | I²C Address | | Byte number | | | |
|---|---|---|---|---|---|---|---|
| Dec | Hex | Dec | Hex | 0 | 1 | 2 | 3 |
| 248 | F8h | 254 | FEh | NC_REG | LAST_NDEF_BLOCK | SRAM_MIRROR_BLOCK | WDT_LS |
| 249 | F9h | | | WDT_MS | I2C_CLOCK_STR | NS_REG | 00h fixed |

Both the session and the configuration bits have the same register except the REG_LOCK bits, which are only available in the configuration bits and the NS_REG bits which are only available in the session registers. After POR, the configuration bits are loaded into the session registers. During the communication session, the values can be changed, but the related effect will only be visible within the communication session for the session registers or after POR for the configuration bits. After POR, the registers values will be again brought back to the default configuration values.

All registers and configuration default values, access conditions and descriptions are defined in Table 13 and Table 14.

Reading and writing the session registers via I²C can only be done via the READ and WRITE registers operation - see Section 9.8.

**Table 13. Configuration bytes**

| Bit | Field | Access via RF | Access via I²C | Default values | Description |
|---|---|---|---|---|---|
| Configuration register: NC_REG | | | | | |
| 7 | I2C_RST_ON_OFF | R&W | R&W | 0b | enables soft reset through I²C repeated start - see Section 9.3 |
| 6 | RFU | READ | R&W | 0b | reserved for future use - keep at 0b |
| 5 | FD_OFF | R&W | R&W | 00b | defines the event upon which the signal output on the FD pin is brought up<br>00b… if the field is switched off<br>01b… if the field is switched off or the tag is set to the HALT state<br>10b… if the field is switched off or the last page of the NDEF message has been read (defined in LAST_NDEF_BLOCK)<br>11b... (if FD_ON = 11b) if the field is switched off or if last data is read by I²C (in Pass-through mode RF ---> I²C) or last data is written by I²C (in Pass-through mode I²C---> RF)<br>11b... (if FD_ON = 00b or 01b or 10b) if the field is switched off<br>See Section 8.4 for more details |
| 4 | | | | | |
| 3 | FD_ON | R&W | R&W | 00b | defines the event upon which the signal output on the FD pin is brought down<br>00b… if the field is switched on<br>01b... by first valid start of communication (SoC)<br>10b... by selection of the tag<br>11b (in Pass-through mode RF-->I²C) if the data is ready to be read from the I²C interface<br>11b (in Pass-through mode I²C--> RF) if the data is read by the RF interface<br>See Section 8.4for more details |
| 2 | | | | | |
| 1 | RFU | READ | R&W | 0b | reserved for future use - keep at 0b |
| 0 | TRANSFER_DIR | R&W | R&W | 1b | defines the data flow direction for the data transfer<br>0b… From I²C to RF interface<br>1b… From RF to I²C interface<br>In case the Pass-through mode is not enabled<br>0b… no WRITE access from the RF side |

**Table 13.** *…continued* **Configuration bytes**

| Bit | Field | Access via RF | Access via I²C | Default values | Description |
|---|---|---|---|---|---|
| **Configuration register: LAST_NDEF_BLOCK** | | | | | |
| 7-0 | LAST_NDEF_BLOCK | R&W | R&W | 00h | Address of last BLOCK (16bytes) of NDEF message from I²C addressing. An RF read of the last page of the I2C block, specified by LAST_NDEF_BLOCK sets the register NDEF_DATA_READ to 1b and triggers FD_OFF if FD_OFF is set to 10b<br>01h is page 04h (first page of the User Memory) from RF addressing<br>02h is page 08h<br>03h is page 0Ch<br>……<br>37h is page DCh - memory sector 0 (last possible page of User memory for NTAG I²C 1k)<br>.....<br>77h is page DCh - memory sector 1 (last page possible of the User Memory for NTAG I²C 2k) |
| **Configuration register: SRAM_MIRROR_BLOCK** | | | | | |
| 7-0 | SRAM_MIRROR_<br>BLOCK | R&W | R&W | F8h | Address of first BLOCK (16bytes) of SRAM buffer when mirrored into the User memory from I²C addressing<br>01h is page 04h (first page of the User Memory) from RF addressing<br>02h is page 08h<br>03h is page 0Ch<br>……<br>34h is page D0h - memory sector 0 (last possible page of User memory for NTAG I²C 1k)<br>.....<br>74h is page D0h - memory sector 1 (last page possible of the User Memory for NTAG I²C 2k) |
| **Configuration register: WDT_LS** | | | | | |
| 7-0 | WDT_LS | R&W | R&W | 48h | Least Significant byte of watchdog time control register |

**Table 13.** *…continued* **Configuration bytes**

| Bit | Field | Access via RF | Access via I²C | Default values | Description |
|---|---|---|---|---|---|
| **Configuration register: WDT_MS** | | | | | |
| 7-0 | WDT_MS | R&W | R&W | 08h | Most Significant byte of watchdog time control register.<br>When writing WDT_MS byte, the content of WDT_MS and WDT_LS gets active for the watchdog timer. |
| **Configuration register: I2C_CLOCK_STR** | | | | | |
| 7-1 | RFU | READ | READ | 0...0b | reserved for future use, all 7 bits locked to 0b |
| 0 | I2C_CLOCK_STR | R&W | R&W | 1b | Enables (1b) or disable (0b) the I²C clock stretching |
| **Configuration register: REG_LOCK** | | | | | |
| 7-2 | RFU | READ | READ | 000000b | reserved for future use, all 6 bits locked to 0b |
| 1 | REG_LOCK_I2C | R&W | R&W | 0b | 0b… Enable writing of the configuration bytes via I²C<br>1b… Disable writing of the configuration bytes via I²C<br>Once set to 1b, cannot be reset to 0b anymore. |
| 0 | REG_LOCK_RF | R&W | R&W | 0b | 0b… Enable writing of the configuration bytes via RF<br>1b… Disable writing of the configuration bytes via RF<br>Once set to 1b, cannot be reset to 0b anymore. |

**Table 14. Session register bytes**

| Bit | Field | Access via RF | Access via I²C | Default values | Description |
|---|---|---|---|---|---|
| **Session register: NC_REG** | | | | | |
| 7 | I2C_RST_ON_OFF | READ | R&W | - | see configuration bytes description |
| 6 | PTHRU_ON_OFF | READ | R&W | 0b | 1b… enables data transfer via the SRAM buffer (Pass-through mode) |
| 5 | FD_OFF | READ | R&W | - | see configuration bytes description |
| 4 | | | | | |
| 3 | FD_ON | READ | R&W | | |
| 2 | | | | | |
| 1 | SRAM_MIRROR_ON_OFF | READ | R&W | 0b | 1b enables SRAM mirroring |
| 0 | PTHRU_DIR | READ | R&W | | see configuration bytes description |
| **Session register: LAST_NDEF_BLOCK** | | | | | |
| 7-0 | LAST_NDEF_BLOCK | READ | R&W | - | see configuration bytes description |
| **Session register: SRAM_MIRROR_BLOCK** | | | | | |
| 7-0 | SRAM_MIRROR_BLOCK | READ | R&W | - | see configuration bytes description |
| **Session register: WDT_LS** | | | | | |
| 7-0 | WDT_LS | READ | R&W | - | see configuration bytes description |

**Table 14.** *…continued* **Session register bytes**

| Bit | Field | Access via RF | Access via I²C | Default values | Description |
|---|---|---|---|---|---|
| **Session register: WDT_MS** | | | | | |
| 7-0 | WDT_MS | READ | R&W | - | see configuration bytes description |
| **Session register: I2C_CLOCK_STR** | | | | | |
| 7-1 | RFU | READ | READ | - | reserved for future use, all 7 bits locked to 0b |
| 0 | I2C_CLOCK_STR | READ | READ | | See configuration bytes description |
| **Session register: NS_REG** | | | | | |
| 7 | NDEF_DATA_READ | READ | READ | 0b | 1b… all data bytes read from the address specified in LAST_NDEF_BLOCK. value is reset to 0b when read |
| 6 | I2C_LOCKED | READ | R&W | 0b | 1b… Memory access is locked to the I²C interface |
| 5 | RF_LOCKED | READ | READ | 0b | 1b… Memory access is locked to the RF interface |
| 4 | SRAM_I2C_READY | READ | READ | 0b | 1b… data is ready in SRAM buffer to be read by I2C |
| 3 | SRAM_RF_READY | READ | READ | 0b | 1b… data is ready in SRAM buffer to be read by RF |
| 2 | EEPROM_WR_ERR | READ | R&W | 0b | 1b… HV voltage error during EEPROM write or erase cycle<br>Needs to be written back via I²C to 0b to be cleared |
| 1 | EEPROM_WR_BUSY | READ | READ | 0b | 1b… EEPROM write cycle in progress - access to EEPROM disabled<br>0b… EEPROM access possible |
| 0 | RF_FIELD_PRESENT | READ | READ | 0b | 1b… RF field is detected |

## 8.4 Configurable Field Detection Pin

The field detection feature provides the capability to trigger an external device (e.g. μController) or switch on the connected circuitry by an external power management unit depending on activities on the RF interface.

The conditions for the activation of the field detection signal (FD_ON) can be:

- The presence of the RF field
- The detection of a valid command (Start of Communication)
- The selection of the IC.

The conditions for the de-activation of the field detection signal (FD_OFF) can be:

- The absence of the RF field
- The detection of the HALT state
- The RF interface has read the last part of the NDEF message defined with LAST_NDEF_BLOCK

All the various combinations of configurations are described in Table 13 and illustrated in Figure 12, Figure 13 and Figure 14 for all various combination of the filed detection signal configuration.

The field detection pin can also be used as a handshake mechanism in the Pass-through mode to signal to the external microcontroller if

- New data are written to SRAM on the RF interface
- Data written to SRAM from the microcontroller are read via the RF interface.

See Section 11 for more information on this handshake mechanism.

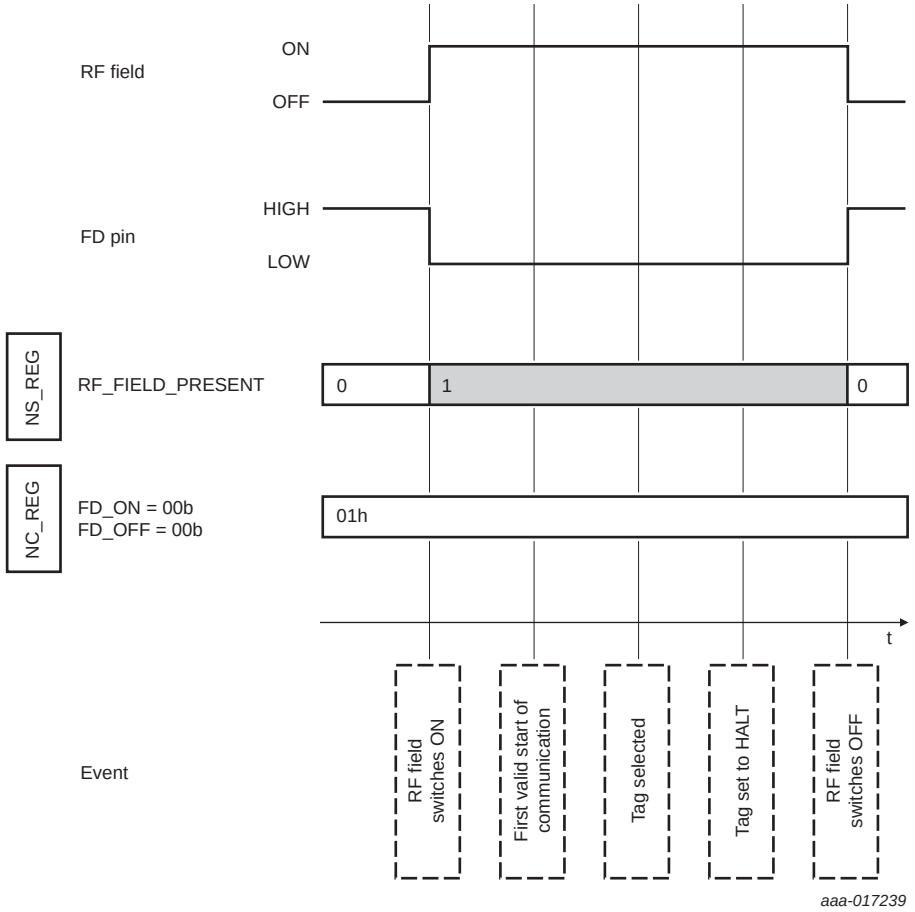



**Fig 12. Illustration of the field detection feature when configured for simple field detection**

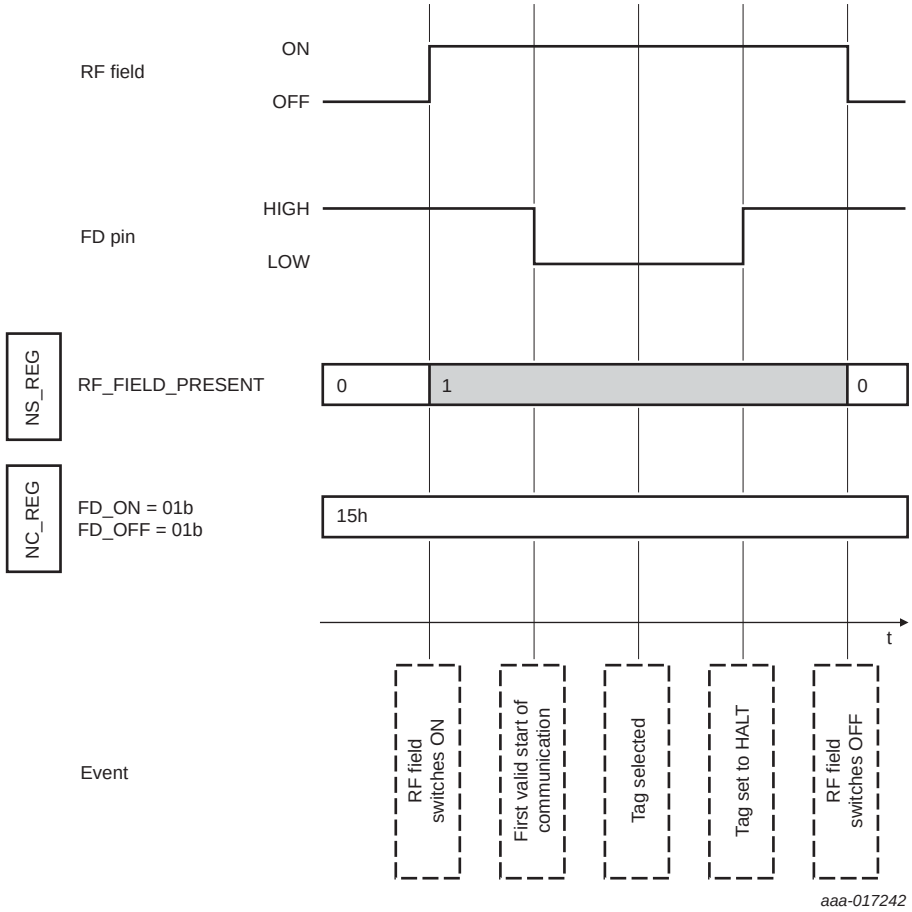



**Fig 13. Illustration of the field detection feature when configured for first valid start of communication detection**

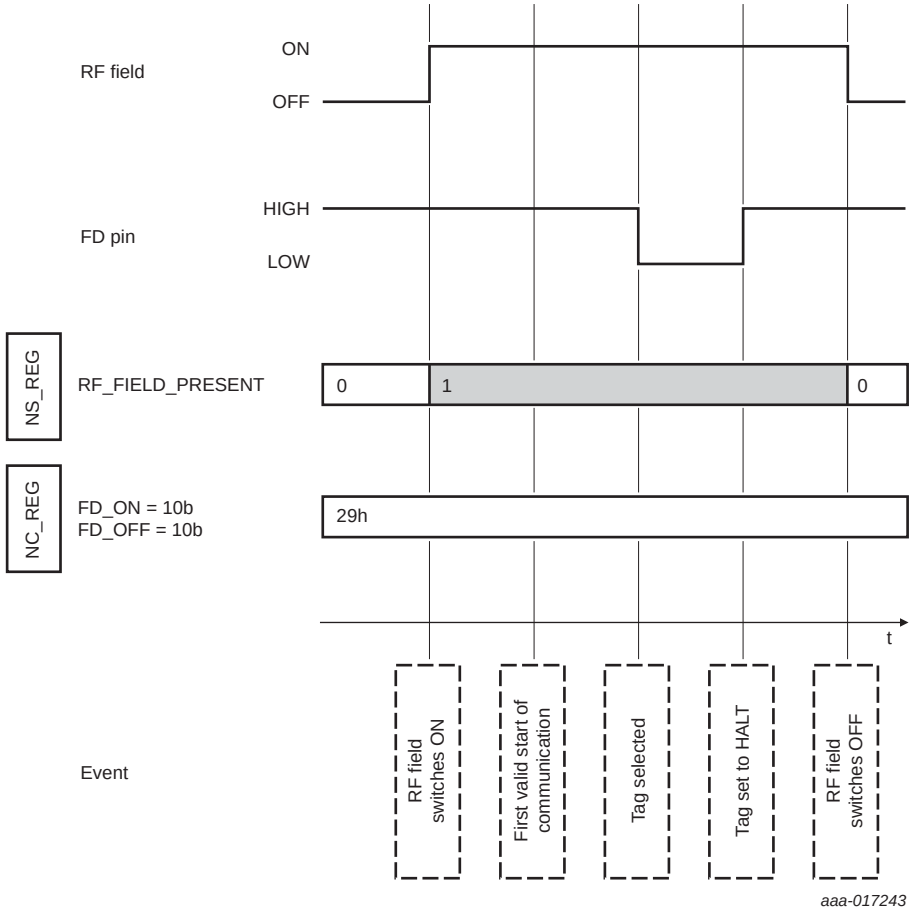



**Fig 14. Illustration of the field detection feature when configured for selection of the tag detection**

## 8.5 Watchdog timer

In order to allow the I²C interface to perform all necessary commands (READ, WRITE...), the memory access remains locked to the I²C interface until the register I2C_LOCKED is cleared by the host - see Table 14.

In order however to avoid that the memory stays 'locked' to the I²C for a long period of time, it is possible to program a watchdog timer to unlock the I²C host from the tag, so that the RF reader can access the tag after a period of time of inactivity. The host itself will not be notified of this event directly, but the NS_REG register is updated accordingly (the register bit I2C_LOCKED will be cleared - see Table 14).

The default value is set to 20 ms (848h), but the watch dog timer can be freely set from 0001h (9.43 μs) up to FFFFh (617.995 ms). The timer starts ticking when the communication between the NTAG I²C and the I²C interface starts. In case the communication with the I²C is still going on after the watchdog timer expires, the communication will continue until the communication has completed. Then the status register I2C_LOCKED will be immediately cleared.

In the case where the communication with the I²C interface has completed before the end of the timer and the status register I2C_LOCKED was not cleared by the host, it will be cleared at the end of the watchdog timer.

The watchdog timer is only effective if the VCC pin is powered and will be reset and stopped if the NTAG I²C is not VCC powered or if the register status I2C_LOCKED is set to 0b and RF_LOCKED is set to 1b.

## 8.6 Energy harvesting

The NTAG I²C provides the capability to supply external low power devices with energy generated from the RF field of a NFC device.

The voltage and current from the energy harvesting depend on various parameters, such as the strength of the RF field, the tag antenna size, or the distance from the NFC device. At room temperature, NTAG I²C could provide typically 5 mA at 2 V on the VOUT pin with an NFC Phone.

Operating NTAG I²C in energy harvesting mode requires a number of precautions:

- A significant capacitor is needed to guarantee operation during RF communication. The total capacitor between VOUT and GND shall be in the range of 150nF to 200 nF.
- If NTAG I²C also powers the I²C bus, then VCC must be connected to VOUT, and pull-up resistors on the SCL and SDA pins must be sized to control SCL and SDA sink current when those lines are pulled low by NTAG I²C or the I²C host
- If NTAG I²C also powers the Field Detect bus, then the pull-up resistor on the Field Detect line must be sized to control the sink current into the Field Detect pin when NTAG I²C pulls it low
- The NFC reader device communicating with NTAG I²C shall apply polling cycles including an RF Field Off condition of at least 5.1 ms as defined in NFC Forum Activity specification (see Ref. 4, chapter 6).

Note that increasing the output current on the $V_{out}$ decreases the RF communication range.

# 9. I²C commands

For details about I²C interface refer to Ref. 3.

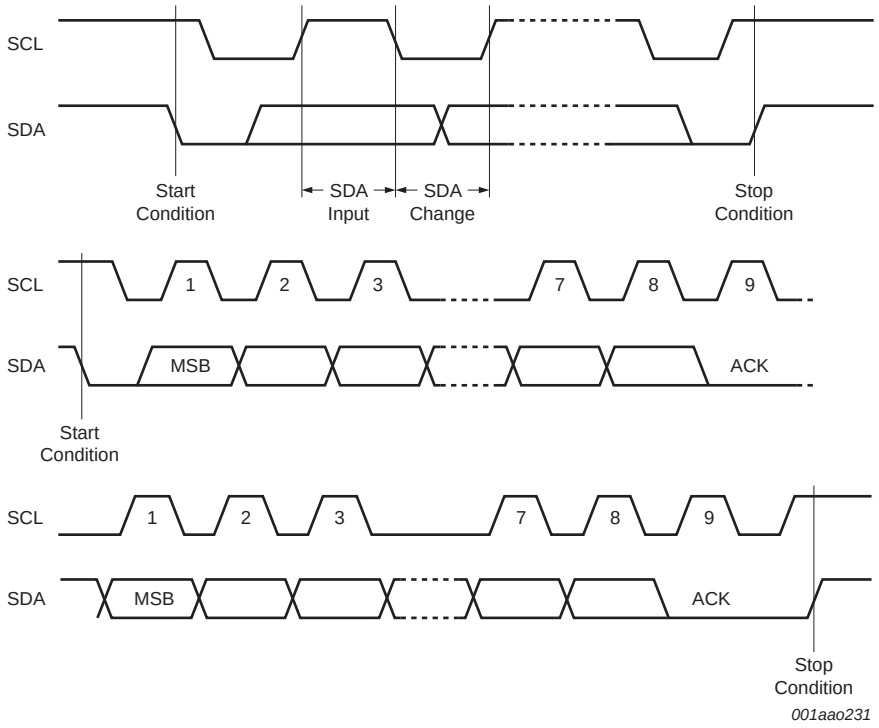



**Fig 15. I²C bus protocol**

The NTAG I²C supports the I²C protocol. This protocol is summarized in Figure 15. Any device that sends data onto the bus is defined as a transmitter, and any device that reads the data from the bus is defined as a receiver. The device that controls the data transfer is known as the “bus master”, and the other as the “slave” device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The NTAG I²C is always a slave in all communications.

## 9.1 Start condition

Start is identified by a falling edge of Serial Data (SDA), while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer command. The NTAG I²C continuously monitors SDA (except during a Write cycle) and SCL for a Start condition, and will not respond unless one is given.

## 9.2 Stop condition

Stop is identified by a rising edge of SDA while SCL is stable and driven high. A Stop condition terminates communication between the NTAG I²C and the bus master. A Stop condition at the end of a Write command triggers the internal Write cycle.

## 9.3 Soft reset feature

In the case where the I²C interface is constantly powered on, NTAG I²C can trigger a reset of the I²C interface via its soft reset feature- see Table 13.

When this feature is enabled, if the microcontroller does not issue a stop condition between two start conditions, this situation will trigger a reset of the I²C interface and hence may hamper the communication via the I²C interface.

## 9.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it is the bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

## 9.5 Data input

During data input, the NTAG I²C samples SDA on the rising edge of SCL. For correct device operation, SDA must be stable during the rising edge of SCL, and the SDA signal must change only when SCL is driven low.

## 9.6 Addressing

To start communication between a bus master and the NTAG I²C slave device, the bus master must initiate a Start condition. Following this initiation, the bus master sends the device address. The NTAG I²C address from I²C consists of a 7-bit device identifier (see Table 15 for default value).

The 8th bit is the Read/Write bit (RW). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device address, the NTAG I²C gives an acknowledgment on SDA during the 9th bit time. If the NTAG I²C does not match the device select code, it deselects itself from the bus and clear the register I2C_LOCKED (see Table 12).

**Table 15. Default NTAG I²C address from I²C**

| | **Device address** | | | | | | | **R/W** |
|---|---|---|---|---|---|---|---|---|
| | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Value | 1[1] | 0[1] | 1[1] | 0[1] | 1 [1] | 0 [1] | 1 [1] | 1/0 |

[1] Initial values - can be changed.

The I²C address of the NTAG I²C (byte 0 - block 0h) can only be modified by the I²C interface. Both interfaces have no READ access to this address and a READ command from the RF or I²C interface to this byte will only return 04h (manufacturer ID for NXP Semiconductors - see Figure 6).

## 9.7 READ and WRITE Operation

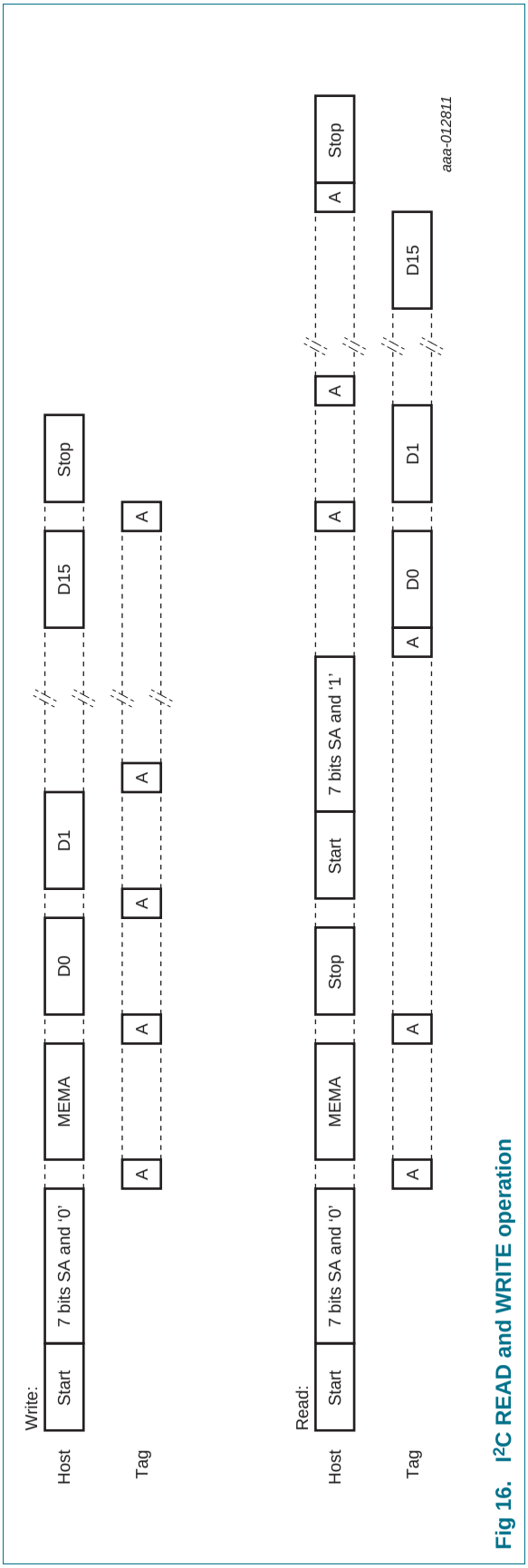



**Fig 16. I²C READ and WRITE operation**

The READ and WRITE operation handle always 16 bytes to be read or written (one block - see Table 7)

For the READ operation (see Figure 16), following a Start condition, the bus master/host sends the NTAG I²C slave address code (SA - 7 bits) with the Read/Write bit (RW) reset to 0. The NTAG I²C acknowledges this (A), and waits for one address byte (MEMA), which should correspond to the address of the block of memory (SRAM or EEPROM) that is intended to be read. The NTAG I²C responds to a valid address byte with an acknowledge (A). A Stop condition can be then issued. Then the host again issues a start condition followed by the NTAG I²C slave address with the Read/Write bit set to 1b. When I2C_CLOCK_STR is set to 0b, a pause of at least 50 μs shall be kept before this start condition. The NTAG I²C acknowledges this (A) and sends the first byte of data read (D0).The bus master/host acknowledges it (A) and the NTAG I²C will subsequently transmit the following 15 bytes of memory read with an acknowledge from the host after every byte. After the last byte of memory data has been transmitted by the NTAG I²C, the bus master/host will acknowledge it and issue a Stop condition.

For the WRITE operation (see Figure 16), following a Start condition, the bus master/host sends the NTAG I²C slave address code (SA - 7 bits) with the Read/Write bit (RW) reset to 0. The NTAG I²C acknowledges this (A), and waits for one address byte (MEMA), which should correspond to the address of the block of memory (SRAM or EEPROM) that is intended to be written. The NTAG I²C responds to a valid address byte with an acknowledge (A) and, in the case of a WRITE operation, the bus master/host starts transmitting each 16 bytes (D0...D15) that shall be written at the specified address with an acknowledge of the NTAG I²C after each byte (A). After the last byte acknowledge from the NTAG I²C, the bus master/host issues a Stop condition.

The memory address accessible via the READ and WRITE operations can only correspond to the EEPROM or SRAM (respectively 00h to 3Ah or F8h to FBh for NTAG I²C 1k and 00h to 7Ah or F8h to FBh for NTAG I²C 2k).

## 9.8 WRITE and READ register operation

In order to modify or read the session register bytes (see Table 14), NTAG I²C requires the WRITE and READ register operation (see Figure 17).




**Fig 17. WRITE and READ register operation**

For the READ register operation, following a Start condition the bus master/host sends the NTAG I²C slave address code (SA - 7 bits) with the Read/Write bit (RW) reset to 0. The NTAG I²C acknowledges this (A), and waits for one address byte (MEMA) which corresponds to the address of the block of memory with the session register bytes (FEh). The NTAG I²C responds to the address byte with an acknowledge (A). Then the bus master/host issues a register address (REGA), which corresponds to the address of the targeted byte inside the block FEh (00h, 01h...to 07h) and then waits for the Stop condition.

Then the bus master/host again issues a start condition followed by the NTAG I²C slave address with the Read/Write bit set to 1b. The NTAG I²C acknowledges this (A), and sends the selected byte of session register data (REGDAT) within the block FEh. The bus master/host will acknowledge it and issue a Stop condition.

For the WRITE register operation, following a Start condition, the bus master/host sends the NTAG I²C slave address code (SA - 7 bits) with the Read/Write bit (RW) reset to 0. The NTAG I²C acknowledges this (A), and waits for one address byte (MEMA), which corresponds to the address of the block of memory within the session register bytes (FEh). After the NTAG I²C acknowledge (A), the bus master/host issues a register address (REGA), which corresponds to the address of the targeted byte inside the block FEh (00h, 01h...to 07h). After acknowledgement (A) by NTAG I²C, the bus master/host issues a MASK byte that defines exactly which bits shall be modified by a 1b bit value at the corresponding bit position. Following the NTAG I²C acknowledge (A), the new register data (one byte - REGDAT) to be written is transmitted by the bus master/host. The NTAG I²C acknowledges it (A), and the bus master/host issues a stop condition.

# 10. RF Command

NTAG activation follows the ISO/IEC 14443 Type A specification. After NTAG I²C has been selected, it can either be deactivated using the ISO/IEC 14443 HALT command, or NTAG commands (e.g., READ or WRITE) can be performed. For more details about the card activation refer to Ref. 2.

## 10.1 NTAG I²C command overview

All available commands for NTAG I²C are shown in Table 16.

**Table 16. Command overview**

| Command[1] | ISO/IEC 14443 | NFC FORUM | Command code (hexadecimal) |
|---|---|---|---|
| Request | REQA | SENS_REQ | 26h (7 bit) |
| Wake-up | WUPA | ALL_REQ | 52h (7 bit) |
| Anticollision CL1 | Anticollision CL1 | SDD_REQ CL1 | 93h 20h |
| Select CL1 | Select CL1 | SEL_REQ CL1 | 93h 70h |
| Anticollision CL2 | Anticollision CL2 | SDD_REQ CL2 | 95h 20h |
| Select CL2 | Select CL2 | SEL_REQ CL2 | 95h 70h |
| Halt | HLTA | SLP_REQ | 50h 00h |
| GET_VERSION | - | - | 60h |
| READ | - | READ | 30h |
| FAST_READ | - | - | 3Ah |
| WRITE | - | WRITE | A2h |
| SECTOR_SELECT | | SECTOR_SELECT | C2h |

[1] Unless otherwise specified, all commands use the coding and framing as described in Ref. 1.

## 10.2 Timing

The command and response timing shown in this document are not to scale and values are rounded to 1 μs.

All given command and response times refer to the data frames, including start of communication and end of communication. They do not include the encoding (like the Miller pulses). An NFC device data frame contains the start of communication (1 “start bit”) and the end of communication (one logic 0 + 1 bit length of unmodulated carrier). An NFC tag data frame contains the start of communication (1 “start bit”) and the end of communication (1 bit length of no subcarrier).

The minimum command response time is specified according to Ref. 1 as an integer n, which specifies the NFC device to NFC tag frame delay time. The frame delay time from NFC tag to NFC device is at least 87 μs. The maximum command response time is specified as a time-out value. Depending on the command, the $T_{ACK}$ value specified for command responses defines the NFC device to NFC tag frame delay time. It does it for either the 4-bit ACK value specified or for a data frame.

All timing can be measured according to the ISO/IEC 14443-3 frame specification as shown for the Frame Delay Time in Figure 18. For more details refer to Ref. 2.

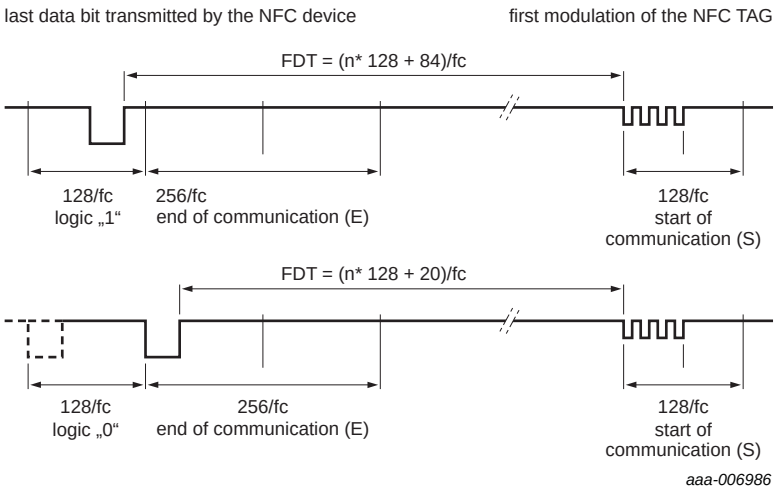



**Fig 18. Frame Delay Time (from NFC device to NFC tag), $T_{ACK}$ and $T_{NAK}$**

**Remark:** Due to the coding of commands, the measured timings usually excludes (a part of) the end of communication. Consider this factor when comparing the specified with the measured times.

## 10.3 NTAG ACK and NAK

NTAG uses a 4 bit ACK / NAK as shown in Table 17.

**Table 17. ACK and NAK values**

| Code (4-bit) | ACK/NAK |
|---|---|
| Ah | Acknowledge (ACK) |
| 0h | NAK for invalid argument (i.e. invalid page address) |
| 1h | NAK for parity or CRC error |
| 3h | NAK for Arbiter locked to I²C |
| 7h | NAK for EEPROM write error |

## 10.4 ATQA and SAK responses

NTAG I²C replies to a REQA or WUPA command with the ATQA value shown in Table 18. It replies to a Select CL2 command with the SAK value shown in Table 19. The 2-byte ATQA value is transmitted with the least significant byte first (44h).

**Table 18. ATQA response of the NTAG I²C**

| | | Bit number | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Sales type** | **Hex value** | **16** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** |
| NTAG I²C | 00 44h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

**Table 19. SAK response of the NTAG I²C**

| | | Bit number | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Sales type** | **Hex value** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** |
| NTAG I²C | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Remark:** The ATQA coding in bits 7 and 8 indicate the UID size according to ISO/IEC 14443 independent from the settings of the UID usage.

**Remark:** The bit numbering in the ISO/IEC 14443 specification starts with LSB = bit 1 and not with LSB = bit 0. So 1 byte counts bit 1 to bit 8 instead of bit 0 to bit 7.

## 10.5 GET_VERSION

The GET_VERSION command is used to retrieve information about the NTAG family, the product version, storage size and other product data required to identify the specific NTAG I²C.

This command is also available on other NTAG products to have a common way of identifying products across platforms and evolution steps.

The GET_VERSION command has no arguments and returns the version information for the specific NTAG I²C type. The command structure is shown in Figure 19 and Table 20.

Table 21 shows the required timing.

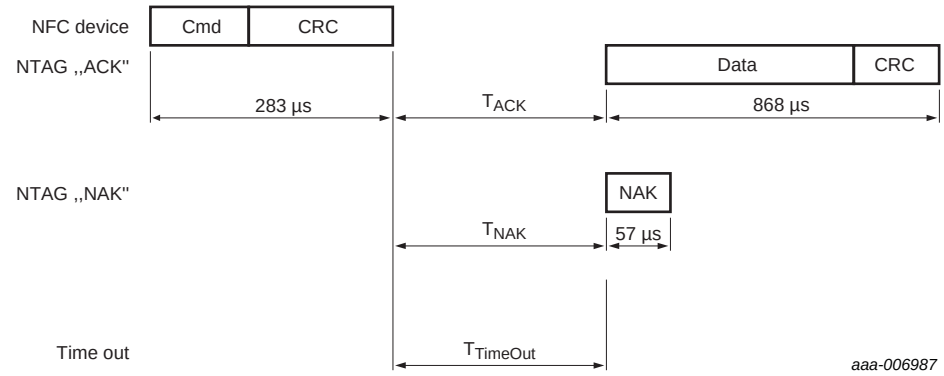



**Fig 19. GET_VERSION command**

**Table 20. GET_VERSION command**

| Name | Code | Description | Length |
|---|---|---|---|
| Cmd | 60h | Get product version | 1 byte |
| CRC | - | CRC according to Ref. 1 | 2 bytes |
| Data | - | Product version information | 8 bytes |
| NAK | see Table 17 | see Section 10.3 | 4-bit |

**Table 21. GET_VERSION timing**

*These times exclude the end of communication of the NFC device.*

| | $T_{ACK/NAK}$ min | $T_{ACK/NAK}$ max | $T_{TimeOut}$ |
|---|---|---|---|
| GET_VERSION | n=9[1] | $T_{TimeOut}$ | 5 ms |

[1] Refer to Section 10.2 “Timing”.

Table 22. GET_VERSION response for NTAG I²C 1k and 2k

| Byte no. | Description | NTAG I²C 1k | NTAG I²C 2k | Interpretation |
|---|---|---|---|---|
| 0 | fixed Header | 00h | 00h | |
| 1 | vendor ID | 04h | 04h | NXP Semiconductors |
| 2 | product type | 04h | 04h | NTAG |
| 3 | product subtype | 05h | 05h | 50 pF I²C, Field detection |
| 4 | major product version | 02h | 02h | 2 |
| 5 | minor product version | 01h | 01h | V1 |
| 6 | storage size | 13h | 15h | see following information |
| 7 | protocol type | 03h | 03h | ISO/IEC 14443-3 compliant |

The most significant 7 bits of the storage size byte are interpreted as an unsigned integer value n. As a result, it codes the total available user memory size as $2^n$. If the least significant bit is 0b, the user memory size is exactly $2^n$. If the least significant bit is 1b, the user memory size is between $2^n$ and $2^{n+1}$.

The user memory for NTAG I²C 1k is 888 bytes. This memory size is between 512 bytes and 1024 bytes. Therefore, the most significant 7 bits of the value 13h, are interpreted as 9d, and the least significant bit is 1b.

The user memory for NTAG I²C 2k is 1904 bytes. This memory size is between 1024 bytes and 2048 bytes. Therefore, the most significant 7 bits of the value 15h, are interpreted as 10d, and the least significant bit is 1b.

## 10.6 READ

The READ command requires a start page address, and returns the 16 bytes of four NTAG I²C pages. For example, if address (Addr) is 03h then pages 03h, 04h, 05h, 06h are returned. Special conditions apply if the READ command address is near the end of the accessible memory area. For details on those cases and the command structure refer to Figure 20 and Table 23.

Table 24 shows the required timing.

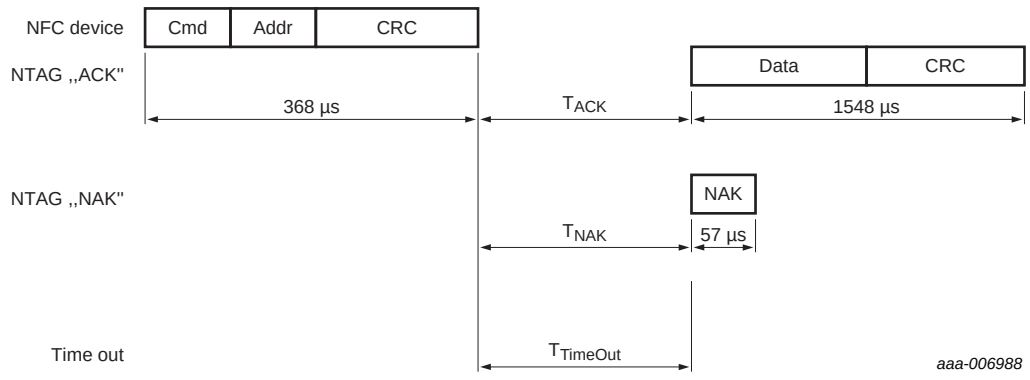



Fig 20. READ command

**Table 23. READ command**

| Name | Code | Description | Length |
|---|---|---|---|
| Cmd | 30h | read four pages | 1 byte |
| Addr | - | start page address | 1 byte |
| CRC | - | CRC according to Ref. 1 | 2 bytes |
| Data | - | Data content of the addressed pages | 16 bytes |
| NAK | see Table 17 | see Section 10.3 | 4-bit |

**Table 24. READ timing**

*These times exclude the end of communication of the NFC device.*

| | $T_{ACK/NAK}$ min | $T_{ACK/NAK}$ max | $T_{TimeOut}$ |
|---|---|---|---|
| READ | n=9[1] | $T_{TimeOut}$ | 5 ms |

[1] Refer to Section 10.2 “Timing”.

In the initial state of NTAG I²C, all memory pages are allowed as Addr parameter to the READ command:

- Page address from 00h to E2h and E8h for NTAG I²C 1k
- Page address from 00h to FFh (sector 0), from page 00h to E0h and E8h (sector 1) for NTAG I²C 2k
- SRAM buffer address when Pass-through mode is enabled

Addressing a start memory page beyond the limits above results in a NAK response from NTAG I²C.

In case a READ command addressing start with a valid memory area but extends over an invalid memory area, the content of the invalid memory area will be reported as 00h.

## 10.7 FAST_READ

The FAST_READ command requires a start page address and an end page address and returns all n*4 bytes of the addressed pages. For example, if the start address is 03h and the end address is 07h, then pages 03h, 04h, 05h, 06h and 07h are returned.

For details on those cases and the command structure, refer to Figure 21 and Table 25.

Table 26 shows the required timing.

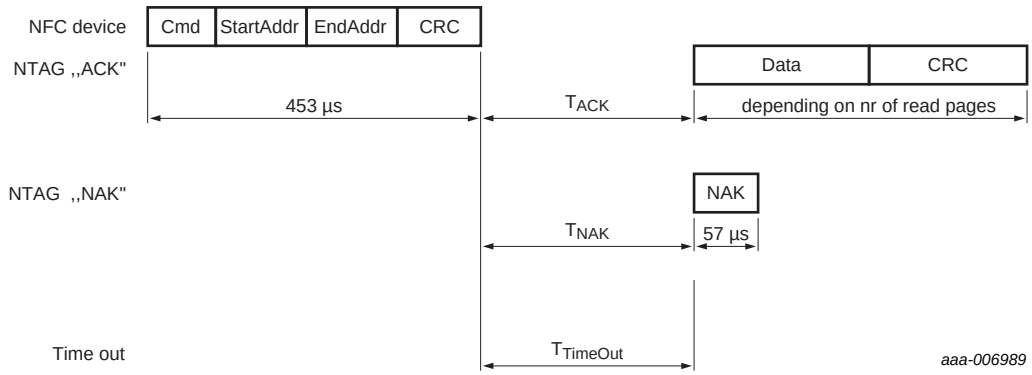



**Fig 21. FAST_READ command**

**Table 25. FAST_READ command**

| Name | Code | Description | Length |
|---|---|---|---|
| Cmd | 3Ah | read multiple pages | 1 byte |
| StartAddr | - | start page address | 1 byte |
| EndAddr | - | end page address | 1 byte |
| CRC | - | CRC according to Ref. 1 | 2 bytes |
| Data | - | data content of the addressed pages | n*4 bytes |
| NAK | see Table 17 | see Section 10.3 | 4-bit |

**Table 26. FAST_READ timing**

*These times exclude the end of communication of the NFC device.*

| | $T_{ACK/NAK}$ min | $T_{ACK/NAK}$ max | $T_{TimeOut}$ |
|---|---|---|---|
| FAST_READ | n=9[1] | $T_{TimeOut}$ | 5 ms |

[1] Refer to Section 10.2 “Timing”.

In the initial state of NTAG I²C, all memory pages are allowed as StartAddr parameter to the FAST_READ command:

- Page address from 00h to E2h and E8h for NTAG I²C 1k
- Page address from 00h to FFh (sector 0), from page 00h to E0h and E8h (sector 1) for NTAG I²C 2k
- SRAM buffer address when Pass-through mode is enabled

If the start addressed memory page (StartAddr) is outside of accessible area, NTAG I²C replies a NAK.

In case the FAST_READ command starts with a valid memory area but extends over an invalid memory area, the content of the invalid memory area will be reported as 00h.

The EndAddr parameter must be equal to or higher than the StartAddr.

**Remark:** The FAST_READ command is able to read out the entire memory of one sector with one command. Nevertheless, the receive buffer of the NFC device must be able to handle the requested amount of data as no chaining is possible.

## 10.8 WRITE

The WRITE command requires a block address, and writes 4 bytes of data into the addressed NTAG I²C page. The WRITE command is shown in Figure 22 and Table 27.

Table 28 shows the required timing.

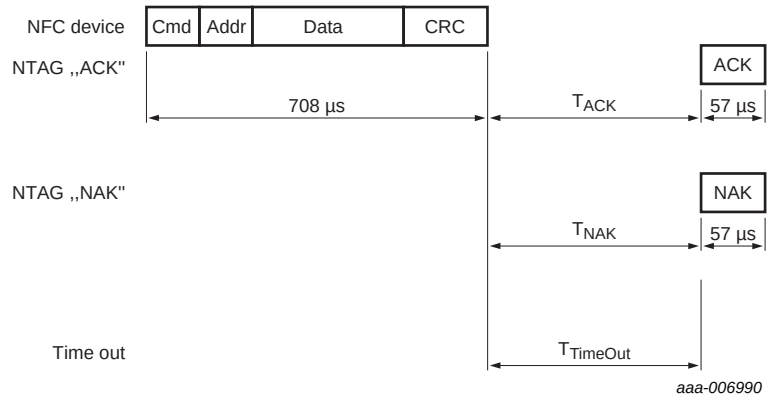



**Fig 22. WRITE command**

**Table 27. WRITE command**

| Name | Code | Description | Length |
|---|---|---|---|
| Cmd | A2h | write one page | 1 byte |
| Addr | - | page address | 1 byte |
| CRC | - | CRC according to Ref. 1 | 2 bytes |
| Data | - | data | 4 bytes |
| NAK | see Table 17 | see Section 10.3 | 4-bit |

**Table 28. WRITE timing**

*These times exclude the end of communication of the NFC device.*

| | $T_{ACK/NAK}$ min | $T_{ACK/NAK}$ max | $T_{TimeOut}$ |
|---|---|---|---|
| WRITE | n=9[1] | $T_{TimeOut}$ | 10 ms |

[1] Refer to Section 10.2 “Timing”.

In the initial state of NTAG I²C, the following memory pages are valid Addr parameters to the WRITE command:

- Page address from 02h to E2h, E8h and E9h (sector 0) for NTAG I²C 1k
- Page address from 02h to FFh (sector 0), from 00h to E0h, E8h and E9h (sector 1) for NTAG I²C 2k
- SRAM buffer addresses when Pass-through mode is enabled

Addressing a memory page beyond the limits above results in a NAK response from NTAG I²C.

Pages that are locked against writing cannot be reprogrammed using any write command. The locking mechanisms include static and dynamic lock bits, as well as the locking of the configuration pages.

## 10.9 SECTOR SELECT

The SECTOR SELECT command consists of two commands packet: the first one is the SECTOR SELECT command (C2h), FFh and CRC. Upon an ACK answer from the Tag, the second command packet needs to be issued with the related sector address to be accessed and 3 bytes RFU.

To successfully access to the requested memory sector, the tag shall issue a passive ACK, which is sending NO REPLY for more than 1ms after the CRC of the second command set.

The SECTOR SELECT command is shown in Figure 23 and Table 29.

Table 30 shows the required timing.

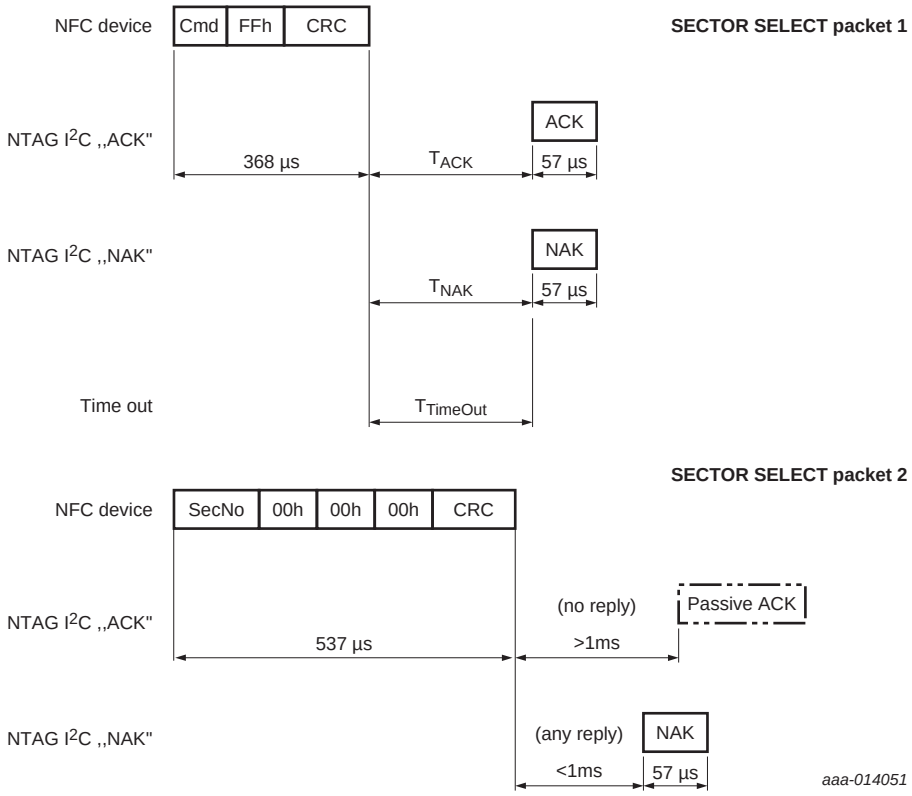



**Fig 23. SECTOR_SELECT command**

**Table 29. SECTOR_SELECT command**

| Name | Code | Description | Length |
|---|---|---|---|
| Cmd | C2h | sector select | 1 byte |
| FFh | - | | 1 byte |
| CRC | - | CRC according to Ref. 1 | 2 bytes |
| SecNo | - | Memory sector to be selected (00h-FEh) | 1 byte |
| NAK | see Table 17 | see Section 10.3 | 4-bit |

**Table 30. SECTOR_SELECT timing**

*These times exclude the end of communication of the NFC device.*

| | $T_{ACK/NAK}$ min | $T_{ACK/NAK}$ max | $T_{TimeOut}$ |
|---|---|---|---|
| SECTOR SELECT | n=9[1] | $T_{TimeOut}$ | 10 ms |

[1] Refer to Section 10.2 “Timing”.

# 11. Communication and arbitration between RF and I²C interface

If both interfaces are powered by their corresponding source, only one interface shall have access according to the "first-come, first-serve" principle.

In NS_REG, the two status bits I2C_LOCKED and RF_LOCKED reflect the status of the NTAG I²C memory access and indicate which interface is locking the memory access. At power on, both bits are 0, setting the arbitration in idle mode.

In the case arbiter locks to the I²C interface, an RF reader still can access the session registers. If the ISO state machine is in ACTIVE state, only the SECTOR SELECT command is allowed. But any other command requiring EEPROM access like READ or WRITE is handled as an illegal command and replied to with a special NAK value.

In the case where the memory access is locked to the RF interface, the I²C host still can access the NFC register, by issuing a 'Register READ/WRITE' command. All other read or write commands will be replied to with a NACK to the I²C host.

## 11.1 Non-Pass-through mode

PTHRU_ON_OFF = 0b (see Table 14) indicates non-Pass-through mode.

### 11.1.1 I²C interface access

If the tag is in the IDLE or HALT state (RF state after POR or HALT-command) and the correct I²C slave address of NTAG I²C is specified following the START condition, the bit I2C_LOCKED will be automatically set to 1b. If I2C_LOCKED = 1b, the I²C interface has access to the tag memory and the tag will respond with a NACK to any memory READ/WRITE command on the RF interface other than reading the register bytes command during this time.

I2C_LOCKED must be either reset to 0b at the end of the I²C sequence or wait until the end of the watch dog timer.

### 11.1.2 RF interface access

The arbitration will allow the RF interface read and write accesses to EEPROM only when I2C_LOCKED is set to 0b.

RF_LOCKED is automatically set to 1b if the tag receives a valid command (EEPROM Access Commands) on the RF interface. If RF_LOCKED = 1b, the tag is locked to the RF interface and will not respond to any command from the I²C interface other than READ register command (see Table 14).

RF_LOCKED is automatically set to 0b in one of the following conditions

- At POR or if the RF field is switched off
- If the tag is set to the HALT state with a HALT command on the RF interface
- If the memory access command is finished on the RF interface

When the RF interface has read the last page of the NDEF message specified in LAST_NDEF_BLOCK (see Table 13 and Table 14) the bit NDEF_DATA_READ - in the register NS_REG see Table 14 - is set to 1b and indicates to the I²C interface that, for example, new NDEF data can be written.

## 11.2 SRAM buffer mapping with Memory Mirror enabled

With SRAM_MIRROR_ON_OFF= 1b, the SRAM buffer mirroring is enabled. This mode cannot be combined with the Pass-through mode (see Section 11.3).

With the memory mirror enabled, the SRAM is now mapped into the user memory from the RF interface perspective using the SRAM mirror lower page address specified in SRAM_MIRROR_BLOCK byte (Table 13 and Table 14). See Table 31 (NTAG I²C 1k) and Table 32 (NTAG I²C 2k) for an illustration of this SRAM memory mapping when SRAM_MIRROR_BLOCK is set to 01h. The SRAM buffer will be then available in two locations: inside the user memory and at the end of the first or second memory sector (respectively NTAG I²C 1k or NTAG I²C 2k).

The tag must be VCC powered to make this mode work, because without VCC, the SRAM will not be accessible via RF powered only.

When mapping the SRAM buffer to the user memory, the user shall be aware that all data written into the SRAM part of the user memory will be lost once the NTAG I²C is no longer powered from the I²C side (as SRAM is a volatile memory).

**Table 31. Illustration of the SRAM memory addressing via the RF interface (with SRAM_MIRROR_ON_OFF set to 1b and SRAM_MIRROR_BLOCK set to 01h) for the NTAG I²C 1k**

| Sector address | Page address | | Byte number within a page | | | | Access conditions |
|---|---|---|---|---|---|---|---|
| | Dec. | Hex. | 0 | 1 | 2 | 3 | |
| 0 | 0 | 00h | Serial number | | | | READ |
| | 1 | 01h | Serial number | | | Internal | READ |
| | 2 | 02h | Internal | | Static lock bytes | | READ/R&W |
| | 3 | 03h | Capability Container (CC) | | | | READ&WRITE |
| | 4 | 04h | SRAM memory (16 blocks) | | | | READ&WRITE |
| | ... | ... | | | | | |
| | 19 | 13h | | | | | |
| | ... | ... | User memory | | | | READ&WRITE |
| | 225 | E1h | | | | | |
| | 226 | E2h | Dynamic lock bytes | | | 00h | R&W/READ |
| | 227 | E3h | Invalid access - returns NAK | | | | n.a. |
| | 228 | E4h | | | | | |
| | 229 | E5h | | | | | |
| | 230 | E6h | | | | | |
| | 231 | E7h | | | | | |
| | 232 | E8h | Configuration registers | | | | see 8.3.11 |
| | 233 | E9h | | | | | |
| | 234 | EAh | Invalid access - returns NAK | | | | n.a. |
| | ... | ... | | | | | |
| | 255 | FFh | | | | | |
| 1 | ... | ... | Invalid access - returns NAK | | | | n.a. |
| 2 | ... | ... | Invalid access - returns NAK | | | | n.a. |
| 3 | 0 | 00h | Invalid access - returns NAK | | | | n.a. |
| | ... | ... | | | | | |
| | 248 | F8h | Session registers | | | | see 8.3.11 |
| | 249 | F9h | | | | | |
| | ... | ... | Invalid access - returns NAK | | | | n.a. |
| | 255 | FFh | | | | | |

**Table 32. Illustration of the SRAM memory addressing via the RF interface (with SRAM_MIRROR_ON_OFF set to 1b and SRAM_MIRROR_BLOCK set to 01h) for the NTAG I²C 2k**

| Sector address | Page address | | Byte number within a page | | | | Access conditions |
|---|---|---|---|---|---|---|---|
| | Dec. | Hex. | 0 | 1 | 2 | 3 | |
| 0 | 0 | 00h | Serial number | | | | READ |
| | 1 | 01h | Serial number | | | Internal | READ |
| | 2 | 02h | Internal | | Static lock bytes | | READ/R&W |
| | 3 | 03h | Capability Container (CC) | | | | READ&WRITE |
| | 4 | 04h | SRAM memory (16 blocks) | | | | READ&WRITE |
| | ... | ... | | | | | |
| | 19 | 13h | | | | | |
| | ... | ... | User memory | | | | READ&WRITE |
| | ... | ... | | | | | |
| | 255 | FFh | | | | | |
| 1 | 0 | ... | | | | | |
| | 1 | ... | | | | | |
| | ... | ... | | | | | |
| | ... | ... | | | | | |
| | 223 | DFh | | | | | |
| | 224 | E0h | Dynamic lock bytes | | | 00h | R&W/READ |
| | 225 | E1h | Invalid access - returns NAK | | | | n.a. |
| | 226 | E2h | | | | | |
| | 227 | E3h | | | | | |
| | 228 | E4h | | | | | |
| | 229 | E5h | | | | | |
| | 230 | E6h | | | | | |
| | 231 | E7h | | | | | |
| | 232 | E8h | Configuration registers | | | | see 8.3.11 |
| | 233 | E9h | | | | | |
| | 234 | EAh | Invalid access - returns NAK | | | | n.a. |
| | ... | ... | | | | | |
| | 255 | FFh | | | | | |
| 2 | ... | ... | Invalid access - returns NAK | | | | n.a. |
| 3 | 0 | 00h | Invalid access - returns NAK | | | | n.a. |
| | ... | ... | | | | | |
| | 248 | F8h | Session registers | | | | see 8.3.11 |
| | 249 | F9h | | | | | |
| | ... | ... | Invalid access - returns NAK | | | | n.a. |
| | 255 | FFh | | | | | |

## 11.3 Pass-through mode

PTHRU_ON_OFF = 1b (see Table 14) enables and indicates Pass-through mode.

To handle large amount of data transfer from one interface to the other, NTAG I²C offers the Pass-through mode where data is transferred via a 64 byte SRAM buffer. This buffer offers fast write access and unlimited write endurance as well as an easy handshake mechanism between the two interfaces.

This buffer is mapped directly at the end of the sector 0 (NTAG I²C 1k) or sector 1 (NTAG I²C 2k) of the memory (from the RF interface perspective).

In both cases, the principle of access to the SRAM buffer via the RF and I²C interface is exactly the same (see Section 11.3.2 and Section 11.3.3).

The data flow direction must be set with the PTHRU_DIR bit (see Table 14) within the current communication session with the session registers (in this case, it can only be set via the I²C interfaces) or for the configuration bits after POR (in this case both RF and I²C interface can set it). This Pass-through direction settings avoids locking the memory access during the data transfer from one interface to the SRAM buffer.

The Pass-through mode can only be enabled via I²C interface when both interfaces are powered. The PTHRU_ON_OFF bit, located in the session registers NC_REG (see Section 8.3.11), needs to be set to 1b. In case one interface powers off, the Pass-through mode is disabled automatically.

### 11.3.1 SRAM buffer mapping

In Pass-through mode, the SRAM is mirrored to pages F0h to FFh sector 0 for the NTAG I²C 1k - see Table 33 - or sector 1 for the NTAG I²C 2k - see Table 34 - outside the user memory.

The last page/block of the SRAM buffer (page 16) is used as the terminator page. Once the terminator page/block in the respective interfaces is read/written, the control would be transferred to other interface (RF/I²C) - see Section 11.3.2 and Section 11.3.3 for more details.

Accordingly, the application can align on the Reader & Host side to transfer 16/32/48/64 bytes of data in one Pass-through step by only using the last blocks/page of the SRAM buffer.

When using FAST_READ to read the SRAM buffer from RF, the EndAddr input of the FAST_READ command has to be always set to FFh.

**Table 33. Illustration of the SRAM memory addressing via the RF interface in Pass-through mode (PTHRU_ON_OFF set to 1b) for the NTAG I²C 1k**

| Sector address | Page address | | Byte number within a page | | | | Access conditions |
|---|---|---|---|---|---|---|---|
| | Dec. | Hex. | 0 | 1 | 2 | 3 | |
| 0 | 0 | 00h | Serial number | | | | READ |
| | 1 | 01h | Serial number | | | Internal | READ |
| | 2 | 02h | Internal | | Static lock bytes | | READ/R&W |
| | 3 | 03h | Capability Container (CC) | | | | READ&WRITE |
| | 4 | 04h | User memory | | | | READ&WRITE |
| | ... | ... | | | | | |
| | 15 | 0Fh | | | | | |
| | ... | ... | | | | | |
| | 225 | E1h | | | | | |
| | 226 | E2h | Dynamic lock bytes | | | 00h | R&W/READ |
| | 227 | E3h | Invalid access - returns NAK | | | | n.a. |
| | 228 | E4h | | | | | |
| | 229 | E5h | | | | | |
| | 230 | E6h | | | | | |
| | 231 | E7h | | | | | |
| | 232 | E8h | Configuration registers | | | | see 8.3.11 |
| | 233 | E9h | | | | | |
| | 234 | EAh | Invalid access - returns NAK | | | | n.a. |
| | ... | ... | | | | | |
| | 240 | F0h | SRAM memory (16 pages) | | | | READ&WRITE |
| | ... | ... | | | | | |
| | 255 | FFh | | | | | |
| 1 | ... | ... | Invalid access - returns NAK | | | | n.a. |
| 2 | ... | ... | Invalid access - returns NAK | | | | n.a. |
| 3 | 0 | 00h | Invalid access - returns NAK | | | | n.a. |
| | ... | ... | | | | | |
| | 248 | F8h | Session registers | | | | see 8.3.11 |
| | 249 | F9h | | | | | |
| | ... | ... | Invalid access - returns NAK | | | | n.a. |
| | 255 | FFh | | | | | |

**Table 34. Illustration of the SRAM memory addressing via the RF interface in Pass-through mode (PTHRU_ON_OFF set to 1b) for the NTAG I²C 2k**

| Sector address | Page address | | Byte number within a page | | | | Access conditions |
|---|---|---|---|---|---|---|---|
| | Dec. | Hex. | 0 | 1 | 2 | 3 | |
| 0 | 0 | 00h | Serial number | | | | READ |
| | 1 | 01h | Serial number | | | Internal | READ |
| | 2 | 02h | Internal | | Static lock bytes | | READ/R&W |
| | 3 | 03h | Capability Container (CC) | | | | READ&WRITE |
| | 4 | 04h | User memory | | | | READ&WRITE |
| | ... | ... | | | | | |
| | 19 | 13h | | | | | |
| | ... | ... | | | | | |
| | ... | ... | | | | | |
| | 255 | FFh | | | | | |
| 1 | 0 | ... | | | | | |
| | 1 | ... | | | | | |
| | ... | ... | | | | | |
| | ... | ... | | | | | |
| | 223 | DFh | | | | | |
| | 224 | E0h | Dynamic lock bytes | | | 00h | R&W/READ |
| | 225 | E1h | Invalid access - returns NAK | | | | n.a. |
| | 226 | E2h | | | | | |
| | 227 | E3h | | | | | |
| | 228 | E4h | | | | | |
| | 229 | E5h | | | | | |
| | 230 | E6h | | | | | |
| | 231 | E7h | | | | | |
| | 232 | E8h | Configuration registers | | | | see 8.3.11 |
| | 233 | E9h | | | | | |
| | 234 | EAh | Invalid access - returns NAK | | | | n.a. |
| | ... | ... | | | | | |
| | 240 | F0h | SRAM (16 pages) | | | | READ&WRITE |
| | ... | ... | | | | | |
| | 255 | FFh | | | | | |
| 2 | ... | ... | Invalid access - returns NAK | | | | n.a. |
| 3 | 0 | 00h | Invalid access - returns NAK | | | | n.a. |
| | ... | ... | | | | | |
| | 248 | F8h | Session registers | | | | see 8.3.11 |
| | 249 | F9h | | | | | |
| | ... | ... | Invalid access - returns NAK | | | | n.a. |
| | 255 | FFh | | | | | |

### 11.3.2 RF to I²C Data transfer

If the RF interface is enabled (RF_LOCKED = 1b) and data is written to the terminator block/page of the SRAM via the RF interface, at the end of the WRITE command, bit SRAM_I2C_READY is set to 1b and bit RF_LOCKED is set to 0b automatically, and the NTAG I²C is locked to the I²C interface.

To signal to the host that data is ready to be read following mechanisms are in place:

- The host polls/reads bit SRAM_I2C_READY from NS_REG (see Table 14) to know if data is ready in SRAM
- A trigger on the FD pin indicates to the host that data is ready to be read from SRAM. This feature can be enabled by programming bits 5:2 (FD_OFF, FD_ON) of the NC_REG appropriately (see Table 13)

This is illustrated in the Figure 24.

If the tag is addressed with the correct I²C slave address, the I2C_LOCKED bit is automatically set to 1b (according to the interface arbitration). After a READ from the terminator page of the SRAM, bit SRAM_I2C_READY and bit I2C_LOCKED are automatically reset to 0b, and the tag returns to the arbitration idle mode where, for example, further data from the RF interface can be transferred.

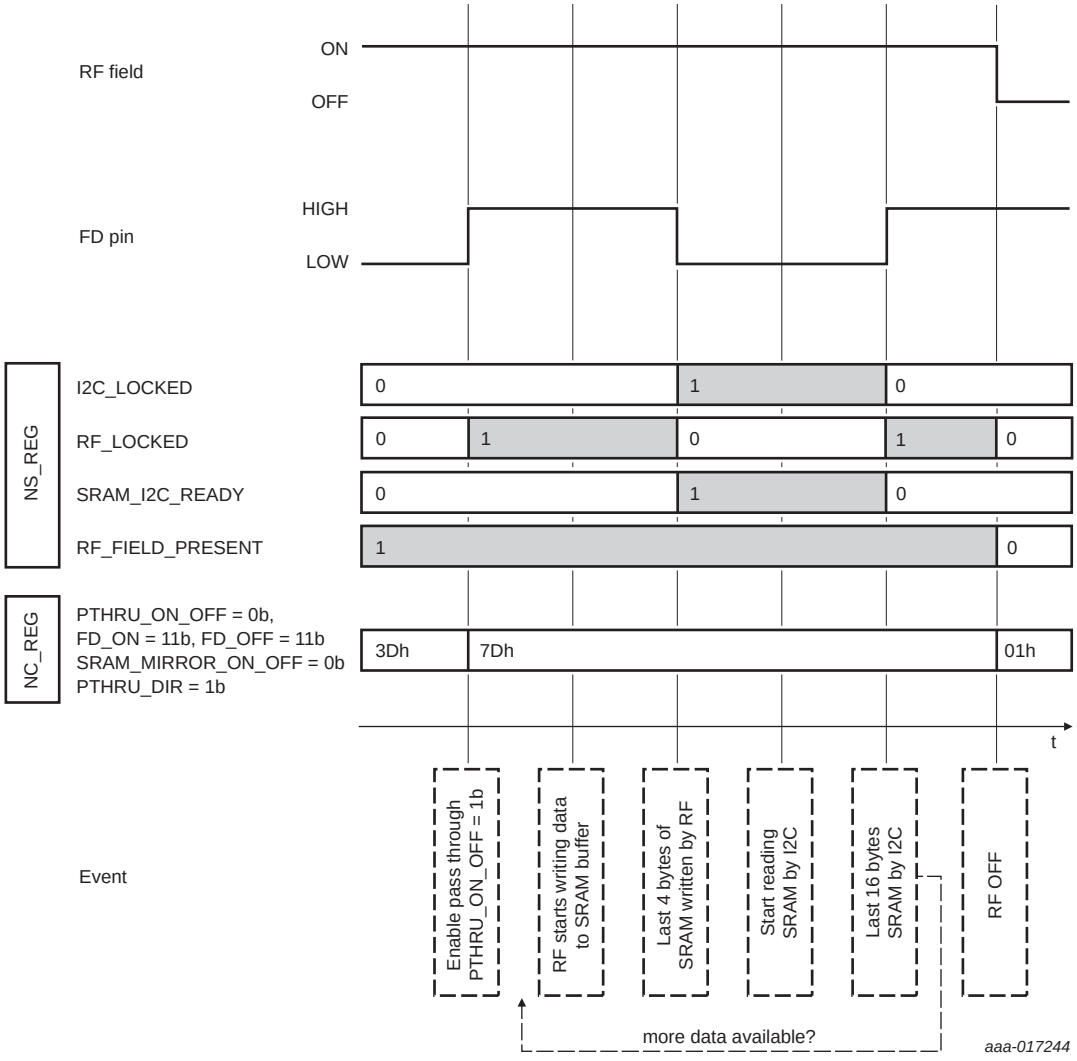



**Fig 24. Illustration of the Field detection feature in combination with the Pass-through mode for data transfer from RF to I²C**

### 11.3.3 I²C to RF Data transfer

If the I²C interface is enabled (I2C_LOCKED is 1b) and data is written to the terminator page of the SRAM via the I²C interface, at the end of the WRITE command, bit SRAM_RF_READY is set to 1b and bit I2C_LOCKED is automatically reset to 0b to set the tag in the arbitration idle state.

The RF_LOCKED bit is then automatically set to 1b (according to the interface arbitration). After a READ or FAST_READ command involving the terminator block/page of the SRAM, bit SRAM_RF_READY and bit RF_LOCKED are automatically reset to 0b allowing the I²C interface to further write data into the SRAM buffer.

To signal to the host that further data is ready to be written, the following mechanisms are in place:

- The RF interface polls/reads the bit SRAM_RF_READY from NS_REG (see Table 14) to know if new data has been written by the I²C interface in the SRAM
- A trigger on the FD pin indicates to the host that data has been read from SRAM by the RF interface. This feature can be enabled by programming bits 5:2 (FD_OFF, FD_ON) of the NC_REG appropriately (see Table 13)

The above mechanism is illustrated in the Figure 25.

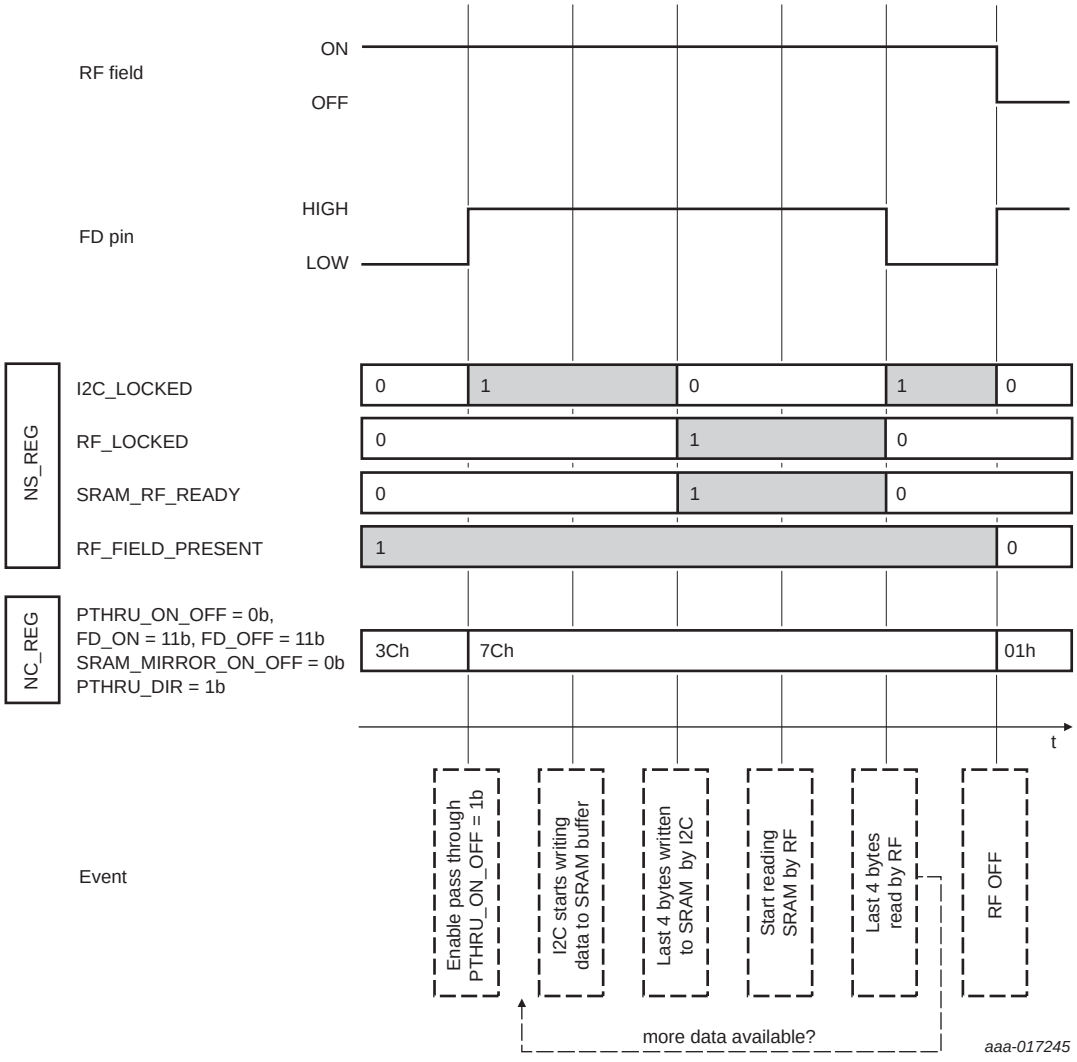



**Fig 25. Illustration of the Field detection signal feature in combination with Pass-through mode for data transfer from I²C to RF**

# 12. Limiting values

Exceeding the limits of one or more values in reference may cause permanent damage to the device. Exposure to limiting values for extended periods may affect device reliability.

**Table 35. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*[1][2][3]

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_I$ | input current LA - LB | | - | 40 | mA |
| $T_{stg}$ | storage temperature | | –55 | +125 | °C |
| $V_{ESD}$ | electrostatic discharge voltage | [3] | 2 | - | kV |
| VFD | Voltage on the FD pin | | - | 3.6 | V |
| VSDA | Voltage on the SDA line | | - | 3.6 | V |
| VSCL | Voltage on the SCL line | | - | 3.6 | V |

[1] Stresses above one or more of the limiting values may cause permanent damage to the device.

[2] Exposure to limiting values for extended periods may affect device reliability.

[3] ANSI/ESDA/JEDEC JS-001; Human body model: C = 100 pF, R = 1.5 kΩ.

# 13. Characteristics

## 13.1 Electrical characteristics

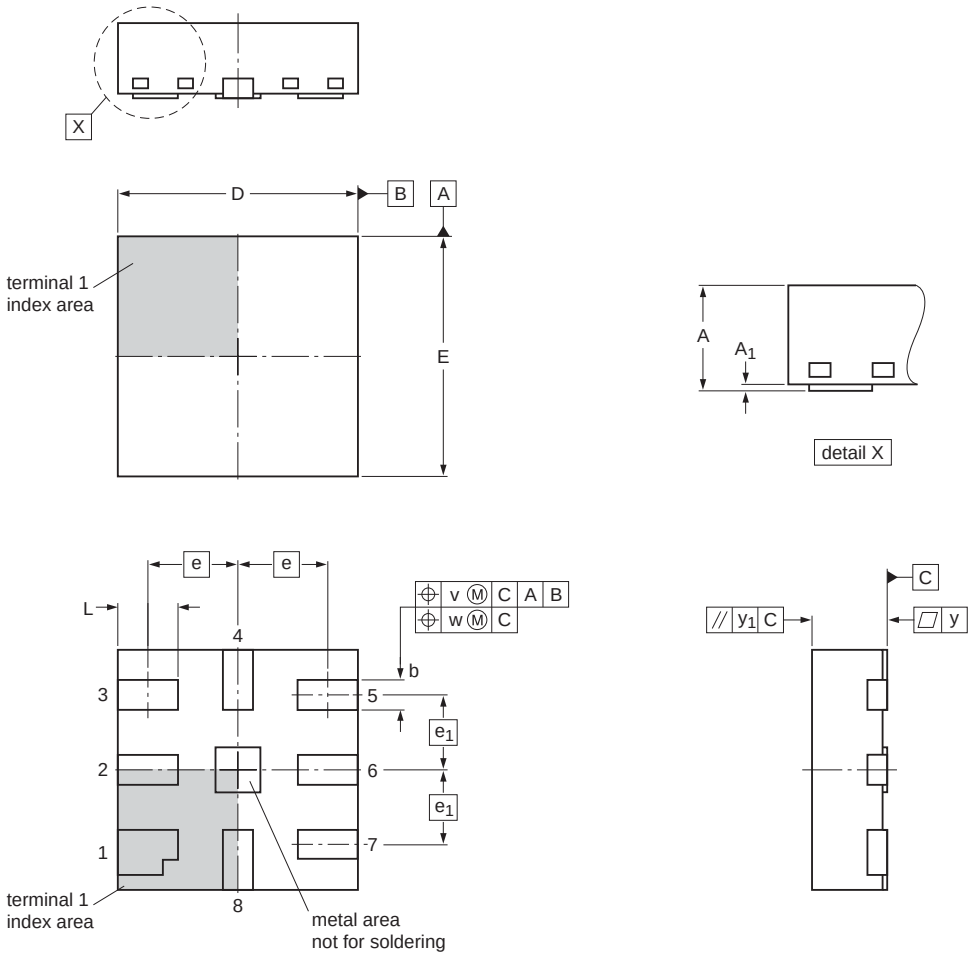
**Table 36. Characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_i$ | input capacitance | LA - LB | 44 | 50 | 56 | pF |
| $f_i$ | input frequency | | - | 13.56 | - | MHz |
| $T_{oper}$ | operating temperature | | –40 | - | +95 | °C |
| **Energy harvesting characteristics** | | | | | | |
| $V_{out}$ | voltage generated at the $V_{out}$ pin | | - | - | 3.2 | V |
| **I²C interface characteristics** | | | | | | |
| $V_{CC}$ | supply voltage | NTAG I²C supplied via $V_{CC}$ only | 1.7 [1] | | 3.6 | V |
| IDD | supply current | | - | 155 | - | µA |
| **EEPROM characteristics** | | | | | | |
| $t_{ret}$ | retention time | full operating temperature range | 20 | - | - | year |
| $N_{endu(W)}$ | write endurance | full operating temperature range | 500000 | - | - | cycle |

[1] A minimum supply voltage of 1.8 V is required, when RF field is present.

# 14. Package outline

**XQFN8: plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm** **SOT902-3**




Dimensions

| Unit | | A | $A_1$ | b | D | E | e | $e_1$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.5 | 0.05 | 0.25 | 1.65 | 1.65 | | | 0.45 | | | | |
| | nom | | | 0.20 | 1.60 | 1.60 | 0.6 | 0.5 | 0.40 | 0.1 | 0.05 | 0.05 | 0.05 |
| | min | | 0.00 | 0.15 | 1.55 | 1.55 | | | 0.35 | | | | |

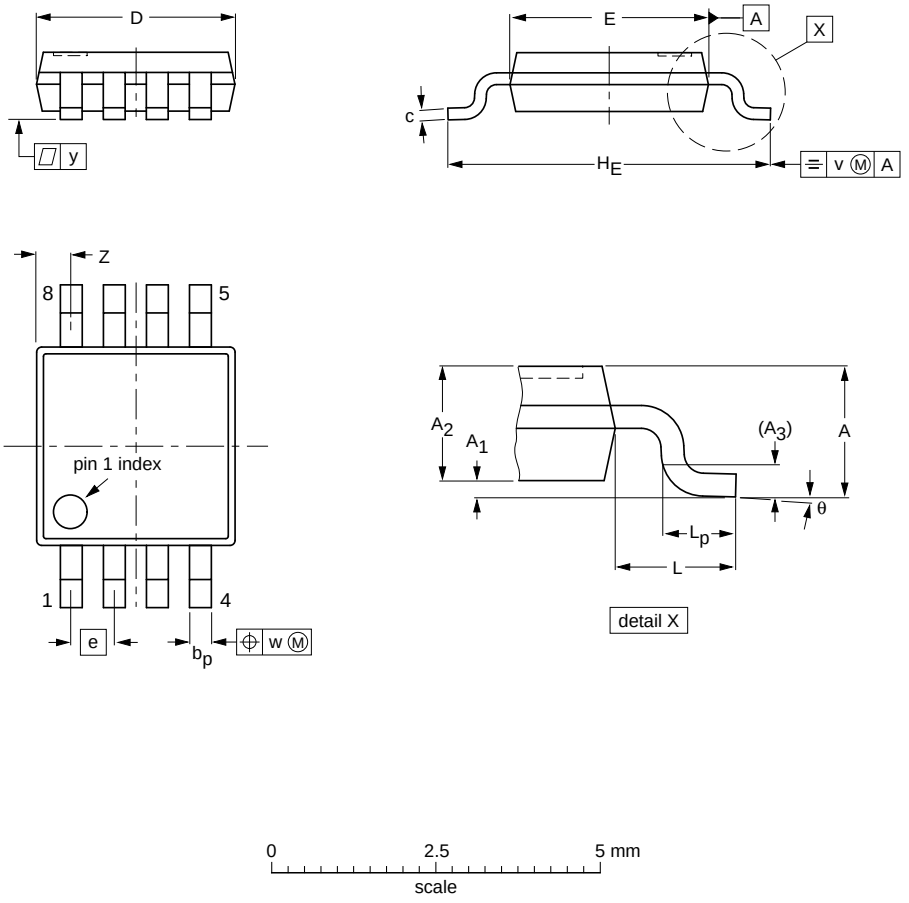
Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

*sot902-3_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT902-3 | - - - | MO-255 | - - - | | | ~~11-08-16~~ 11-08-18 |

**Fig 26. Package outline SOT902-3 (XQFN8)**

**TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm** **SOT505-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.45<br>0.25 | 0.28<br>0.15 | 3.1<br>2.9 | 3.1<br>2.9 | 0.65 | 5.1<br>4.7 | 0.94 | 0.7<br>0.4 | 0.1 | 0.1 | 0.1 | 0.70<br>0.35 | 6°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT505-1 | | | | | | ~~99-04-09~~<br>03-02-18 |

**Fig 27. Package outline SOT501-1 (TSSOP8)**

**Table 37. Pin description**

| Pin no. | Symbol | Description |
|---|---|---|
| 1 | LA | Antenna connection LA |
| 2 | VSS | GND |
| 3 | SCL | Serial Clock I²C |
| 4 | FD | Field detection |
| 5 | SDA | Serial data I²C |
| 6 | VCC | VCC in connection (external power supply) |
| 7 | $V_{out}$ | Voltage out (energy harvesting) |
| 8 | LB | Antenna connection LB |

# 15. Abbreviations

**Table 38. Abbreviations**

| Acronym | Description |
|---|---|
| POR | Power On Reset |

# 16. References

[1] NFC Forum - Type 2 Tag Operation V1.2
Technical Specification

[2] ISO/IEC 14443 - Identification cards - Contactless integrated circuit cards - Proximity cards
International Standard

[3] I2C-bus specification and user manual
NXP standard UM10204

[4] NFC Forum - Activity V1.1
Technical Specification

# 17. Revision history

**Table 39. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| NT3H1101_1201 v. 3.3 | 20150715 | Product data sheet | - | NT3H1101_1201 v. 3.2 |
| Modifications: | • Table 1 “Ordering information”: updated<br>• Capacitor value for energy harvesting corrected<br>• Table 35 “Limiting values”: updated<br>• Table 36 “Characteristics”: updated | | | |
| NT3H1101_1201 v. 3.2 | 20150325 | Product data sheet | - | NT3H1101_1201 v. 3.1 |
| Modifications: | • Table 1 “Ordering information”: updated<br>• Table 2 “Marking codes”: updated<br>• Section 7.1: Figure 4 added<br>• Section 14 “Package outline”: Figure 27 added<br>• General update | | | |
| NT3H1101_1201 v. 3.1 | 20141009 | Product data sheet | - | NT3H1101_1201 v. 3.0 |
| Modifications: | • Section 8.6 “Energy harvesting”: updated<br>• Section 10.5 “GET_VERSION”: updated<br>• Figure 24 and Figure 25: updated<br>• Section 12 “Limiting values” and Section 13 “Characteristics”: remark removed | | | |
| NT3H1101_1201 v. 3.0 | 20140806 | Product data sheet | - | NT3H1101_1201 v. 2.3 |
| Modifications: | • Section 8.6 “Energy harvesting” updated<br>• Section 16 “References”: updated<br>• Data sheet status changed to “Product data sheet” | | | |
| NT3H1101_1201 v. 2.3 | 20140708 | Objective data sheet | - | NT3H1201_1101 v. 2.2 |
| Modifications: | • Figures updated<br>• General update | | | |
| NT3H1101_1201 v. 2.2 | 20140306 | Objective data sheet | - | NT3H1201_1101 v. 2.1 |
| Modifications: | • General updates | | | |
| NT3H1101_1201 v. 2.1 | 20131218 | Objective data sheet | - | NT3H1201_1101 v. 2.0 |
| Modifications: | • Section 4 “Ordering information”: type number corrected | | | |
| NT3H1101_1201 v. 2.0 | 20131212 | Objective data sheet | | NT3H1201 v. 1.4 |
| Modifications: | • Additional description for the Field detection functionality for Pass-through mode<br>• General update | | | |
| NT3H1201 v. 1.4 | 20130802 | Objective data sheet | - | NT3H1201 v. 1.3 |
| Modifications: | • Update for 1k memory version and RF commands | | | |
| NT3H1201 v. 1.3 | 20130613 | Objective data sheet | - | |
| Modifications: | • Pinning package update | | | NT3H1201 v. 1.0 |
| NT3H1201 v. 1.0 | 20130425 | Objective data sheet | - | - |

# 18. Legal information

## 18.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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# 20. Contents





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