PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 00

Model No: WK80028

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

□ Approved Product Specification only
■ Approved Product Specification and Samples

Prepared By	Checked By	Approved By
陈潇潇	雷新金	侯育博

Contents

1. General Description

WK80028 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 8.0 inch and the resolution is 800(RGB)*1280, the panel can display up to 16M colors.

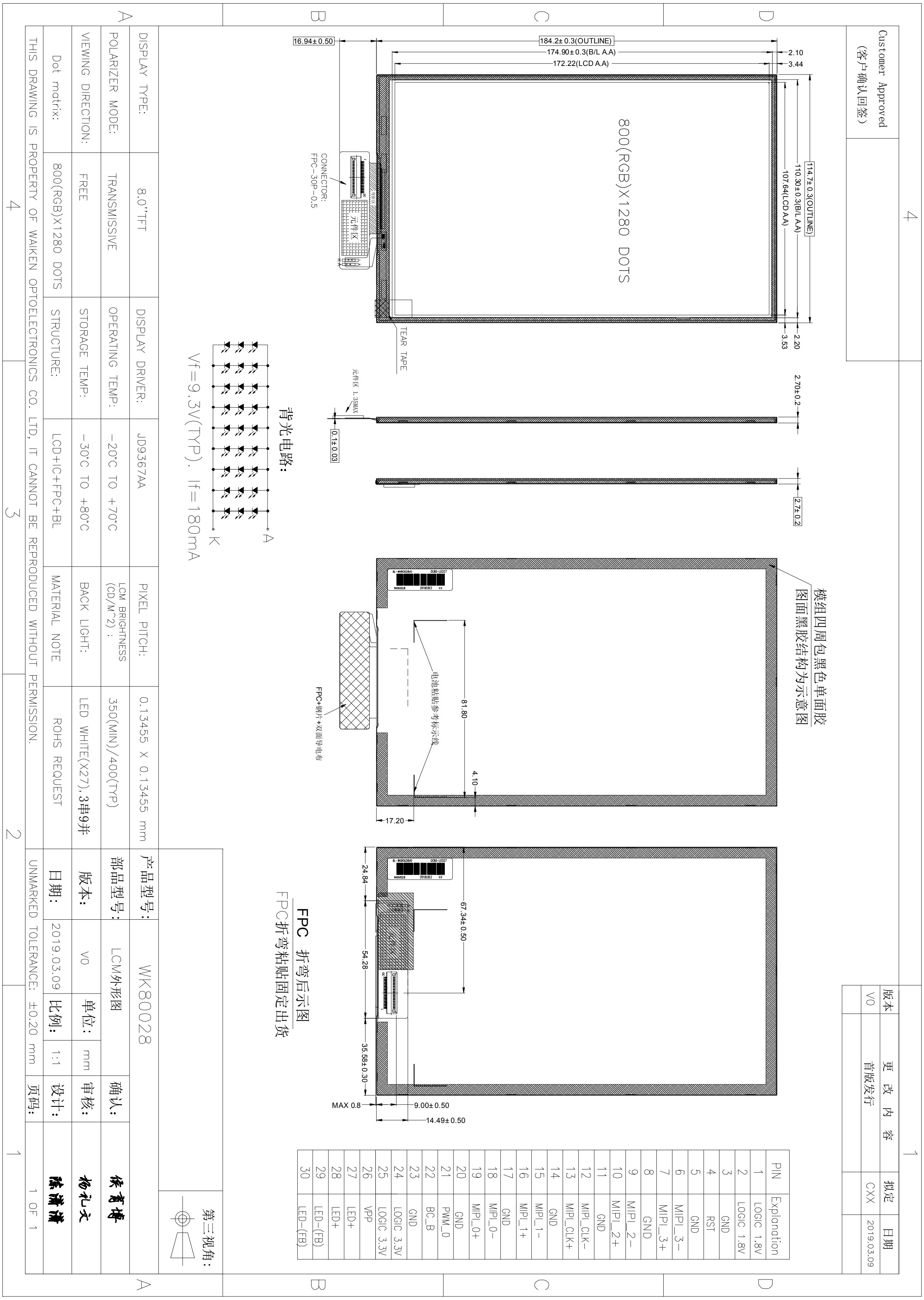
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 800×RGB×1280 Dot-matrix
Input Data	MIPI
Viewing Direction	Free

3. Mechanical Specification

Item	Contents	Unit
Module size (W×H×T)	114.70 × 184.20× 2.70	mm
Number of dots	800(RGB) × 1280	---
Active area (W×H)	107.64×172.22	mm

4. Outline Dimension



DISPLAY TYPE:	8.0"TFT	DISPLAY DRIVER:	JD9367AA
POLARIZER MODE:	TRANSMISSIVE	OPERATING TEMP:	-20℃ TO +70℃
VIEWING DIRECTION:	FREE	STORAGE TEMP:	-30℃ TO +80℃
Dot matrix:	800(RGB)X1280 DOTS	STRUCTURE:	LCD+IC+FPC+BL
PIXEL PITCH:	0.13455 X 0.13455 mm		
LCM BRIGHTNESS (CD/M^2):	350(MIN)/400(TYP)		
BACK LIGHT:	LED WHITE(X27),3串9并		
MATERIAL NOTE	ROHS REQUEST		

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产品型号:	WK80028				
部品型号:	LCM外形图			确认:	
版本:	V0	单位:	mm	审核:	
日期:	2019.03.09	比例:	1:1	设计:	
UNMARKED TOLERANCE: ±0.20 mm				页码:	1 OF 1

版本	更改内容	拟定	日期
V0	首版发行	CXX	2019.03.09

PIN	Explanation
1	LOGIC 1.8V
2	LOGIC 1.8V
3	GND
4	RST
5	GND
6	MIPI_3-
7	MIPI_3+
8	GND
9	MIPI_2-
10	MIPI_2+
11	GND
12	MIPI_CLK-
13	MIPI_CLK+
14	GND
15	MIPI_1-
16	MIPI_1+
17	GND
18	MIPI_0-
19	MIPI_0+
20	GND
21	PWM_0
22	BC_B
23	GND
24	LOGIC 3.3V
25	LOGIC 3.3V
26	VPP
27	LED+
28	LED+
29	LED-(FB)
30	LED-(FB)

5. Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit	Remark
Interface Supply Voltage	IOVCC	-0.3	3.6	V	Note1
Analog Power Supply Voltage	VCI	-0.3	6.6	V	

Remark:

Note1：IOVCC, VSSD must be maintained.
To make sure IOVCC ≥ VSSD.
To make sure VCI≥ AVSS.

6. Electrical Characteristics

6.1 Typical Operation Conditions

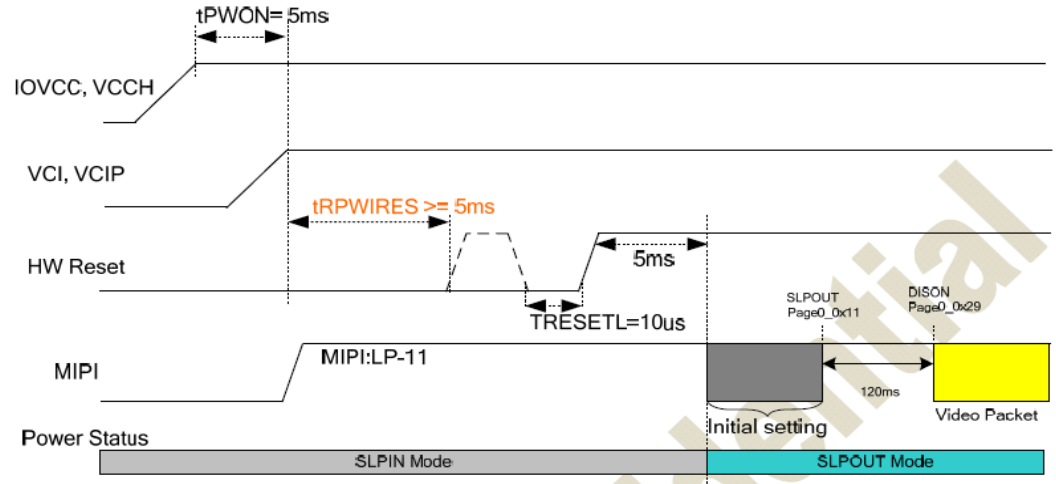
Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Interface Supply Voltage	Logic	IOVCC	1.65	1.8	3.6	V	
Analog Power Supply Voltage	Analog	VCI	2.5	3.3	6.0	V	

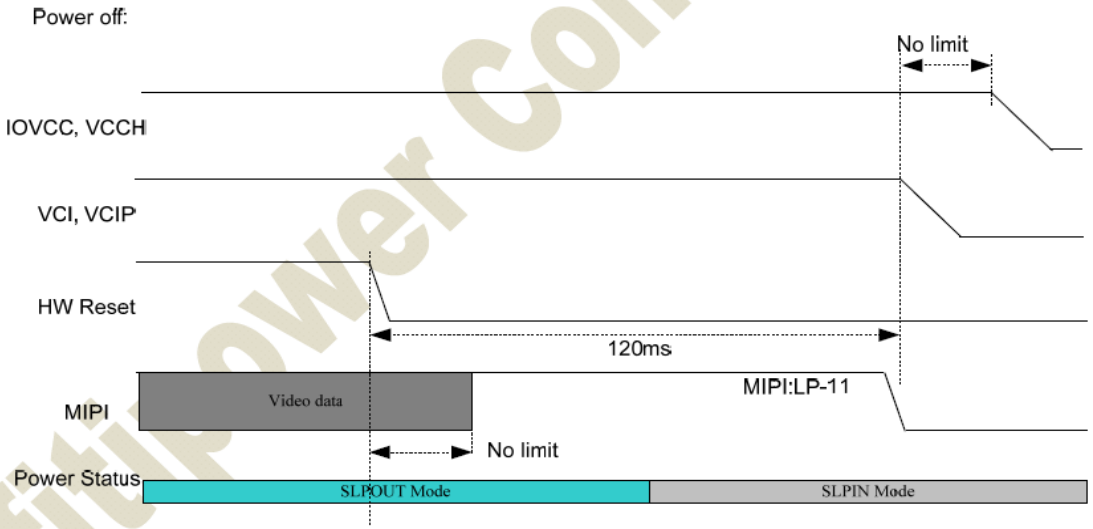
6.2 TFT-LCD Current Consumption

Item	Symbol	Min	TYP	Max	Unit	Remark
Current For Driver	I_{IOVCC}	-	TBD	-	mA	
	I_{VCI}	-	TBD	-	mA	

6.3 Power、Signal Sequence

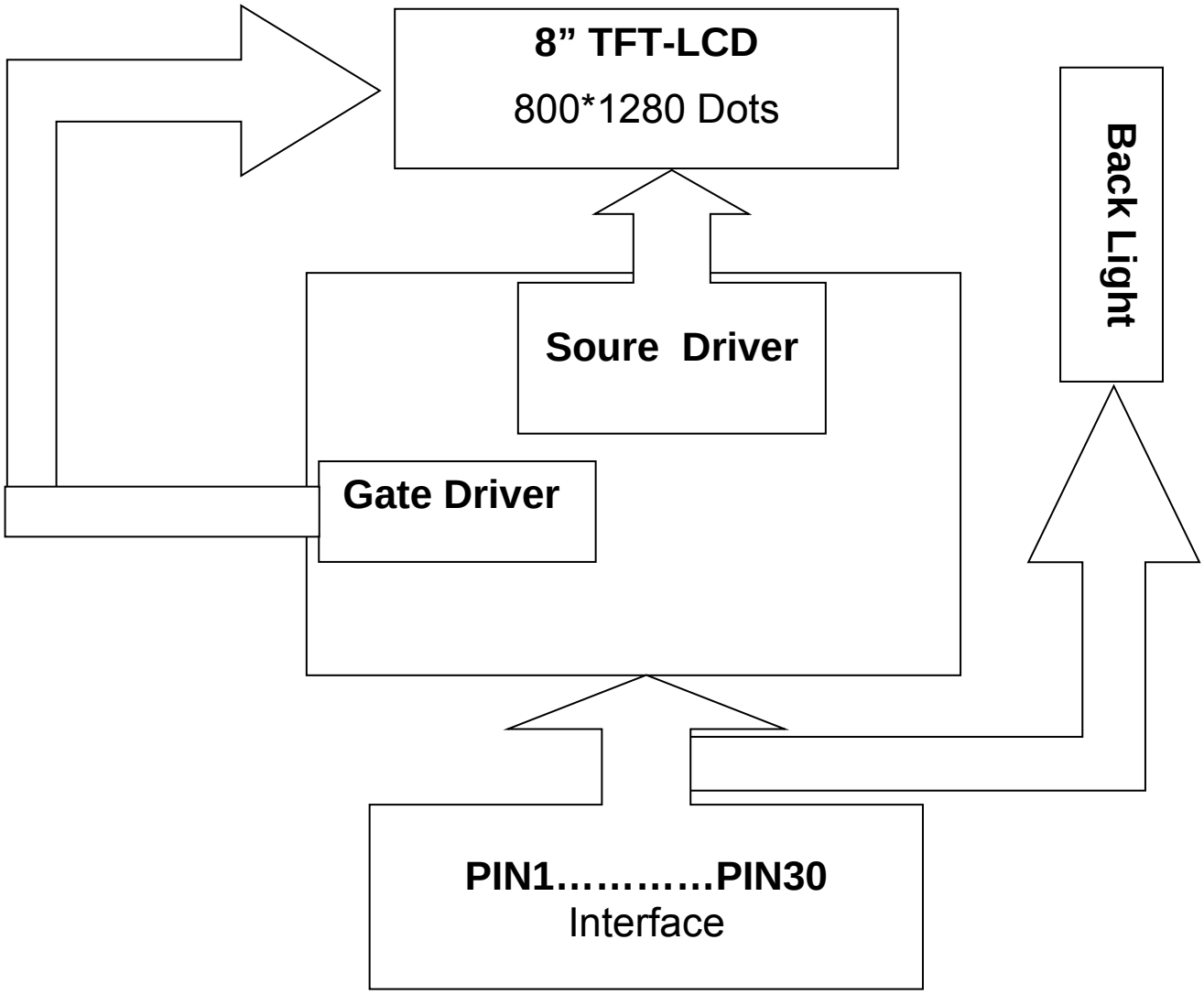
IOVCC=VCCH=1.65V ~ 3.6V, VCI=VCIP=2.5V ~ 4.8V.





7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

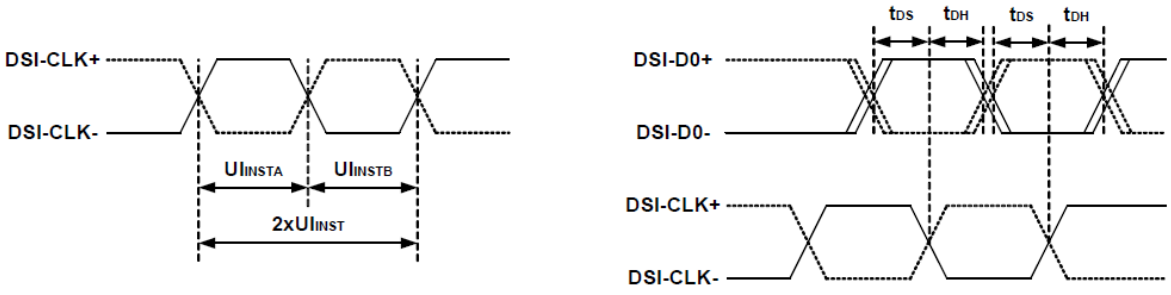
PIN NO.	Symbol	Description
1	LOGIC-1.8V	Power supply
2	LOGIC-1.8V	Power supply
3	GND	Power ground
4	RST	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied (Must be connected to VSSD or IOVCC).
5	GND	Power ground
6	MIPI_3-	MIPI-DSI Data differential signal input pins. (Data lane 0)
7	MIPI_3+	MIPI-DSI Data differential signal input pins. (Data lane 0)
8	GND	Power ground
9	MIPI_2-	MIPI-DSI Data differential signal input pins. (Data lane 1)
10	MIPI_2+	MIPI-DSI Data differential signal input pins. (Data lane 1)
11	GND	Power ground
12	MIPI_CLK-	MIPI-DSI CLOCK differential signal input pins.
13	MIPI_ CLK +	MIPI-DSI CLOCK differential signal input pins.
14	GND	Power ground
15	MIPI_1-	MIPI-DSI Data differential signal input pins. (Data lane 2)
16	MIPI_1+	MIPI-DSI Data differential signal input pins. (Data lane 2)
17	GND	Power ground
18	MIPI_0-	MIPI-DSI Data differential signal input pins. (Data lane 3)
19	MIPI_0+	MIPI-DSI Data differential signal input pins. (Data lane 3)
20	GND	Power ground
21	PWM_O	Backlight on/off control pin. If use CABC function, the pin can connect to external LED driver IC. The output voltage range=0 to IOVCC.
22	BC-B	NC
23	GND	Power ground
24	LOGIC_3.3V	Power supply
25	LOGIC_3.3V	Power supply
26	VPP	External high voltage pin used in OTP mode and operates at 7.5V. If not used, let it open.
27	LED+	LED Anode
28	LED+	LED Anode
29	LED-	LED Cathode
30	LED-	LED Cathode

7-3. Timing Characteristics

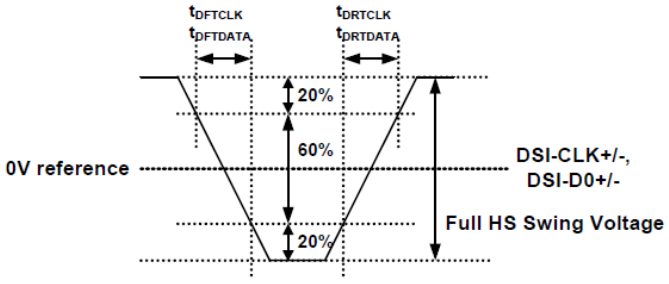
High Speed Mode

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	2xUIINST	Double UI instantaneous	4	-	8	ns	4 Lane (Note 2)
			3	-	8	ns	3 Lane (Note 2)
			2.352	-	8	ns	2 Lane (Note 3)
DSI-CLK+/-	UIINSTA UIINSTB	UI instantaneous halfs (UI = UIINSTA = UIINSTB)	2	-	4	ns	4 Lane (Note 2)
			1.5	-	4	ns	3 Lane (Note 2)
			1.176	-	4	ns	2 Lane (Note 3)
DSI-Dn+/-	tDS	Data to clock setup time	0.15x UI	-	-	ps	
DSI-Dn+/-	tDH	Data to clock hold time	0.15x UI	-	-	ps	
DSI-CLK+/-	tDRTCLK	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	tDRTDATA	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	tDFTCLK	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	tDFTDATA	Differential fall time for data	150	-	0.3xUI	ps	

Note 1) Dn = D0, D1, D2 and D3.
Note 2) Maximum total bit rate is 2Gbps for 24-bit data format, 1.5Gbps for 18-bit data format and 1.33Gbps for 16-bit data format in 3 lanes or 4 lanes application which support to 800RGBx 1280 resolution.
Note 3) Maximum total bit rate is 1.7Gbps for 24-bit data format, 1.275Gbps for 18-bit data format and 1.13Gbps for 16-bit data format in 2 lanes application which support to 720RGBx1280 resolution.



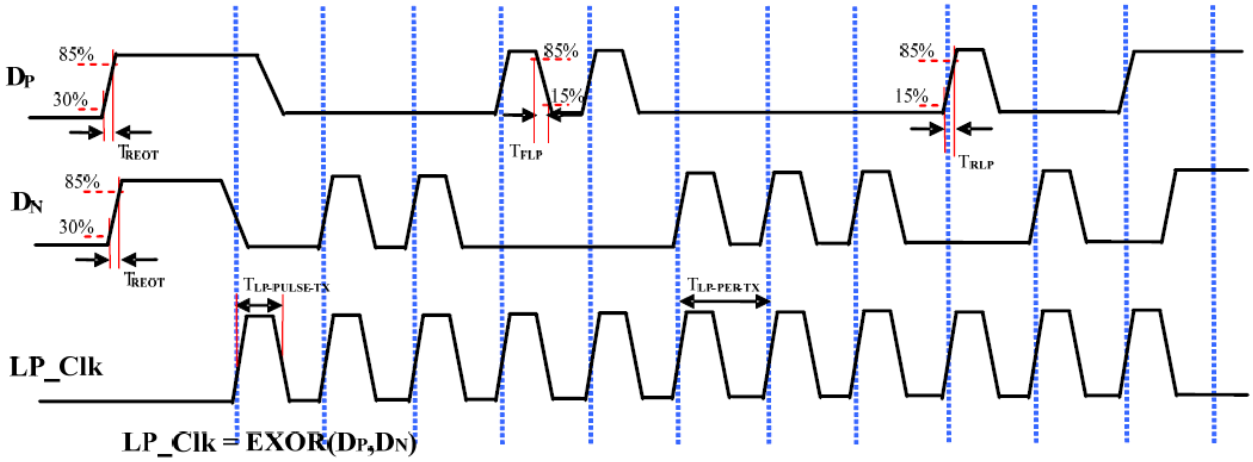
DSI clock channel timing



Rising and fall time on clock and data channel

LP Transmission

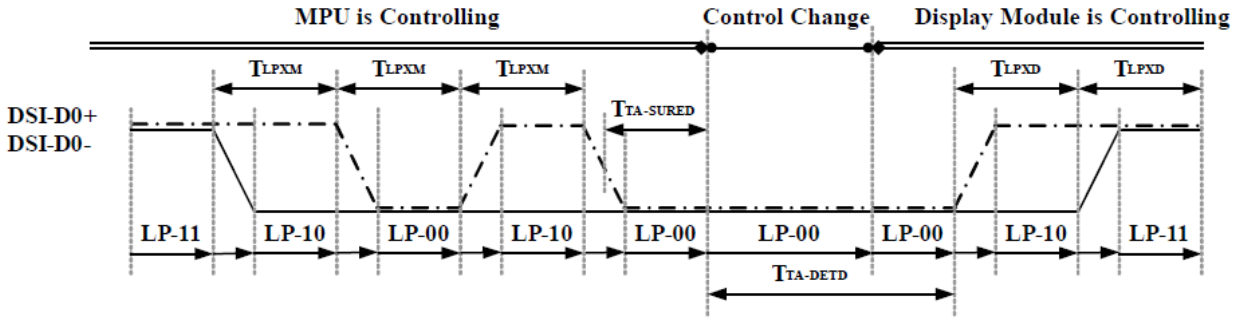
Parameter	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
DSI CLK frequency(LP)	F_{DSICLK_LP}			10	MHz	
DSI CLK Cycle Time(LP)	t_{CLKC_LP}	100			ns	
DSI Data Transfer Rate(LP)	t_{DSIR_LP}			10	Mbps	
15%-85% rise time and fall time	T_{RLP} / T_{FLP}	-	-	35	ns	
30%-85% rise time(from HS to LP)	T_{REOT}	-	-	35	ns	
Pulse width of the LP exclusive-OR clock	$t_{LP\text{-}PULSE\text{-}TX}$	50	65	-	ns	
Period of the LP exclusive-OR clock	$t_{LP\text{-}PRE\text{-}TX}$	100	130	-	ns	

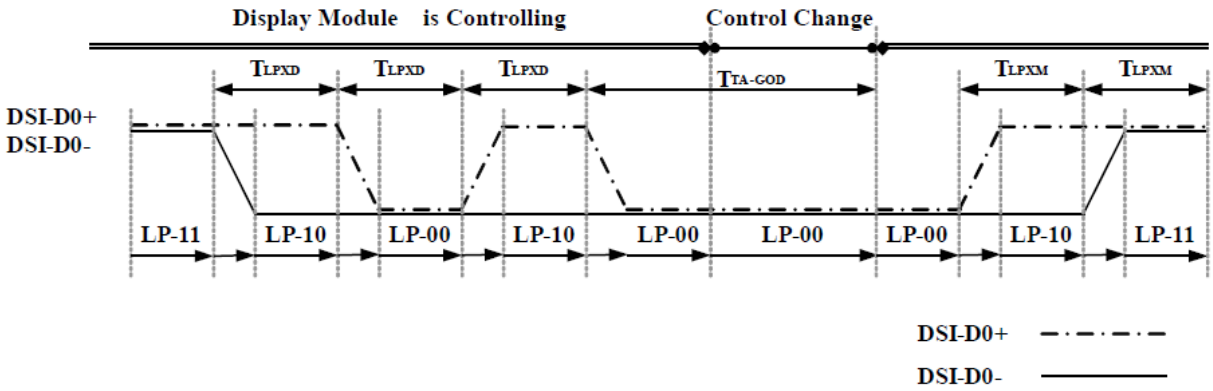


Low Power Mode

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+ /-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU (Display Module	50	-	75	ns	Input
DSI-D0+ /-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (MPU	50	-	75	ns	Output
DSI-D0+ /-	TTA-SURED	Time-out before the MPU start driving	TLPXD	-	2xTLPXD	ns	Output
DSI-D0+ /-	TTA-GETD	Time to drive LP-00 by display module	5xTLPXD	-	-	ns	Input
DSI-D0+ /-	TTA-GOD	Time to drive LP-00 after turnaround request - MPU	4xTLPXD	-	-	ns	Output

Bus Turnaround (BAT) from MPU to display module Timing





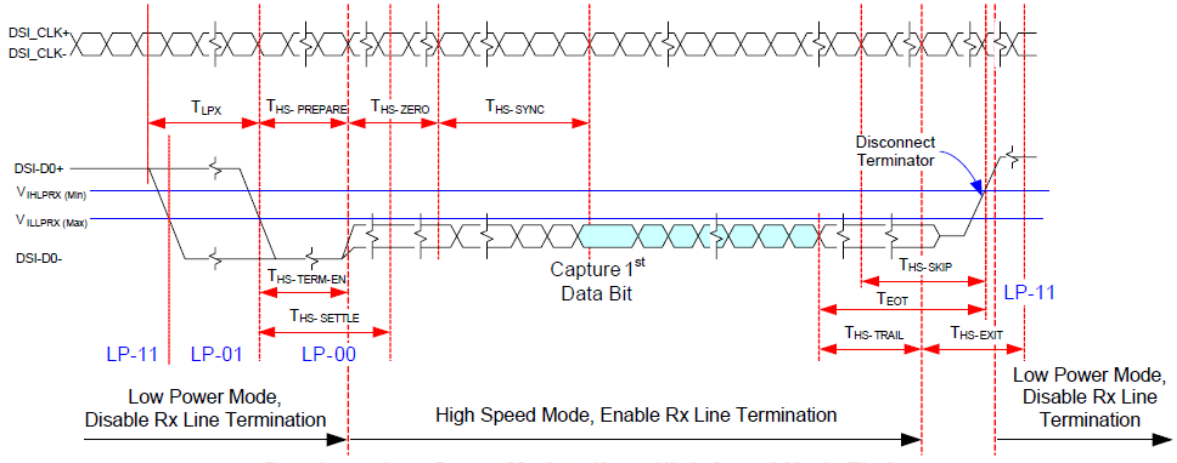
Bus Turnaround (BAT) from display module to MPU Timing

DSI Bursts

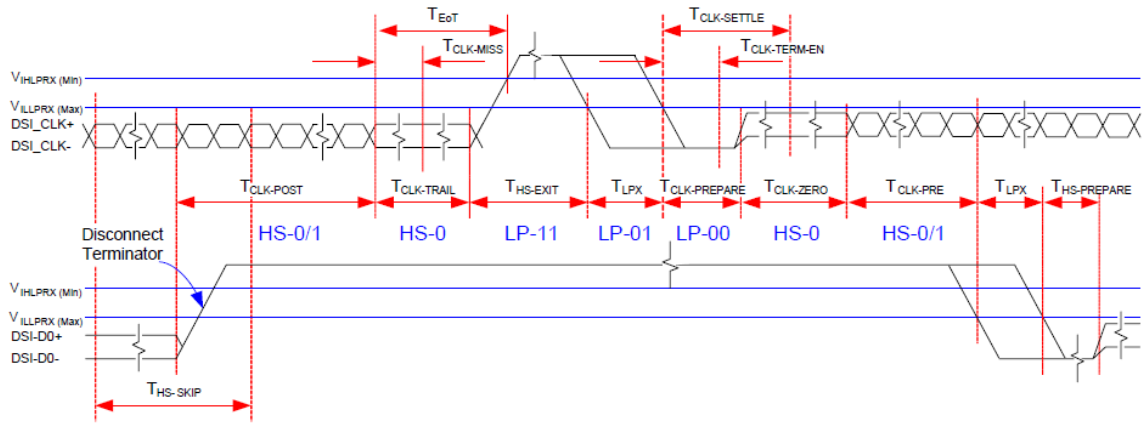
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to	60+52xUI	-	-	ns	Input

		LP mode					
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE+ TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note 1) Dn = D0, D1, D2 and D3.
Note 2) Two HS transmission can be sent with a break as short as THS-EXIT from each other in continuous clock mode. In discontinuous mode, the break is longer which account TCLK-POS, TCLK-TRAIL and THS-EXIT, before activity in clock and data lanes again.

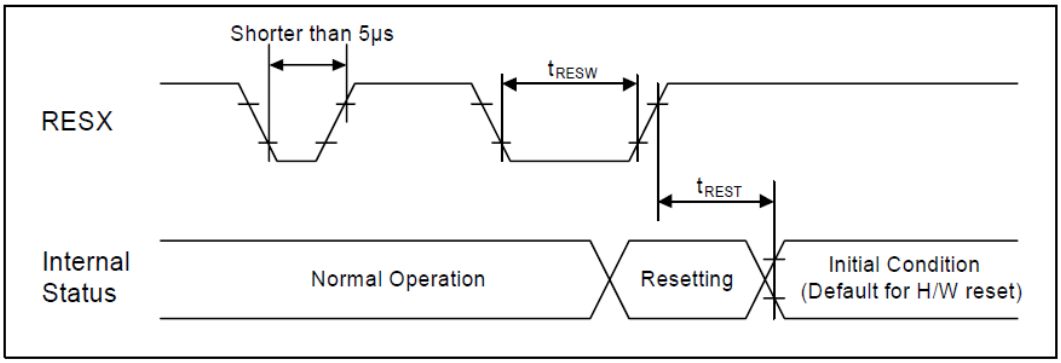


Data lanes-Low Power Mode to/from High Speed Mode Timing



Clock lanes- High Speed Mode to/from Low Power Mode Timing

Reset Input Timing



Reset input timing
(VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	t_{RESW}	Reset "L" pulse width (Note 1)	10	-	-	µs	
	t_{REST}	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode and Note 5

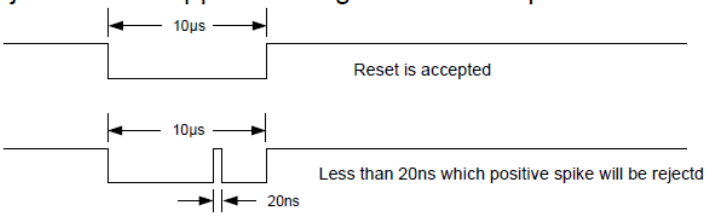
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset Start

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

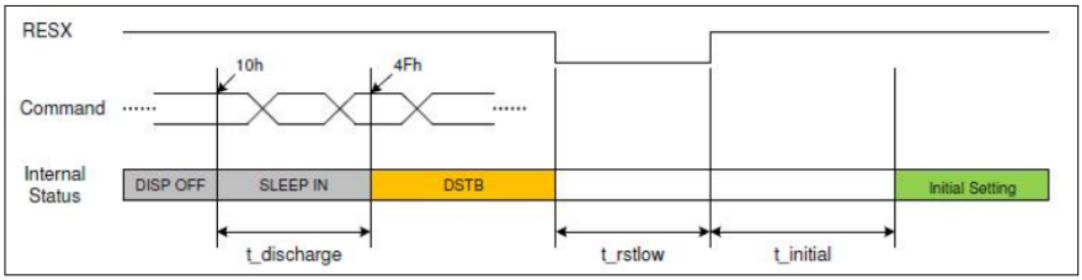
Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:



Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

Deep Standby Mode Timing



(***VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V***,Ta = -30 to 70°C)

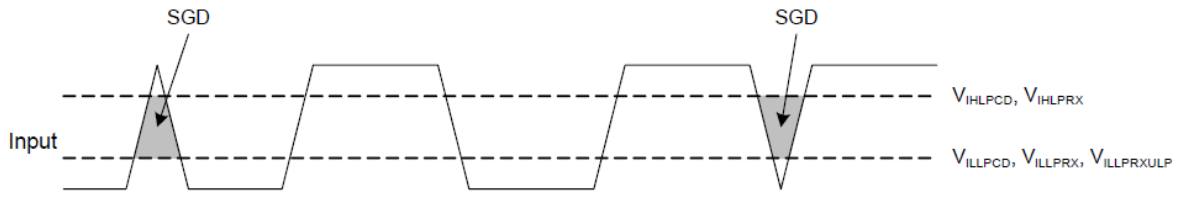
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	tdischarge	Sleep in into DSTB delay time	-	-	100	ms	
	trstlow	Reset low pulse	3	-	-	ms	
	tinitial	Reset high to initial setting delay time	-	-	120	ms	

Note 1) t_discharge suggested delay time over 100ms.
Note 2) t_initial suggested delay time over 120ms..

DC Characteristics for DSI LP Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK, D0, D1)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0, D1)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic high level input current	I_{IH}	LP-CD, LP-RX	-	-	10	μA
Logic low level input current	I_{IL}	LP-CD, LP-RX	-10	-	-	μA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	300	Vps

Note 1) VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta=-30 to 70 ºC (to +85 ºC no damage)
Note 2) DSI high speed is off.
Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.

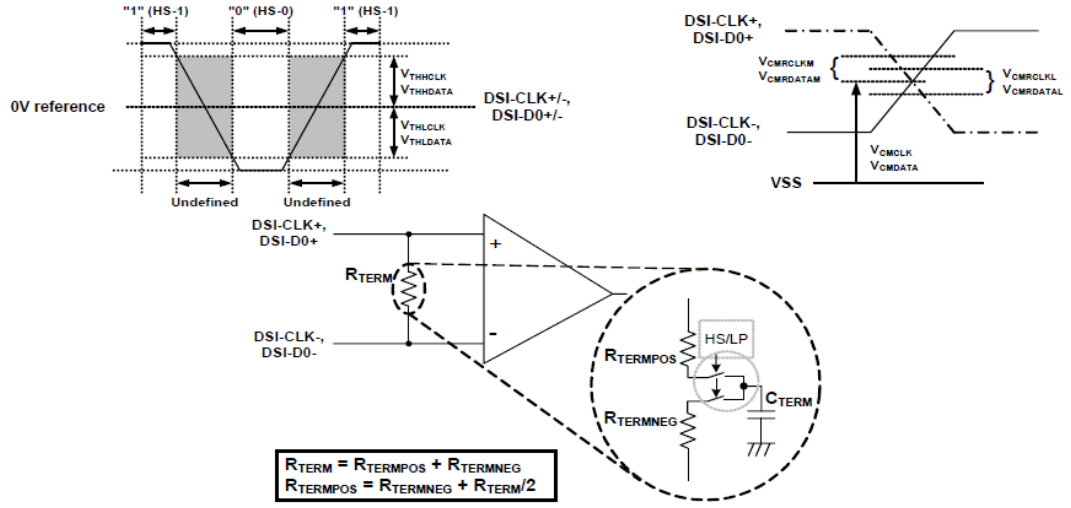


Spike/Glitch rejection-DSI

DC Characteristics for DSI HS Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Input voltage common mode range	VCMCLK VCMDATA	DSI-CLK+/-, DSI-Dn+/- (Note2, 3)	70	-	330	mV
Input voltage common mode variation (≤ 450MHz)	VCMRCLKL VCMRDATAL	DSI-CLK+/-, DSI-Dn+/- (Note 4)	-50	-	50	mV
Input voltage common mode variation (≥ 450MHz)	VCMRCLKM VCMRDATAM	DSI-CLK+/-, DSI-Dn+/-	-	-	100	mV
Low-level differential input voltage threshold	VTHLCLK VTHLDATA	DSI-CLK+/-, DSI-Dn+/-	-70	-	-	mV
High-level differential input voltage threshold	VTHHCLK VTHHDATA	DSI-CLK+/-, DSI-Dn+/-	-	-	70	mV
Single-ended input low voltage	VILHS	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	VIHHS	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	460	mV
Differential input termination resistor	RTERM	DSI-CLK+/-, DSI-Dn+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	VTERM-EN	DSI-CLK+/-, DSI-Dn+/-	-	-	450	mV
Termination capacitor	CTERM	DSI-CLK+/-, DSI-Dn+/-	-	-	14	pF

Note 1) VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta=-30 to 70 ºC (to +85 ºC no damage).
Note 2) Includes 50mV (-50mV to 50mV) ground difference.
Note 3) Without VCMRCLKM / VCMRDATAM.
Note 4) Without 50mV (-50mV to 50mV) ground difference.
Note 5) Dn=D0, D1, D2 and D3.



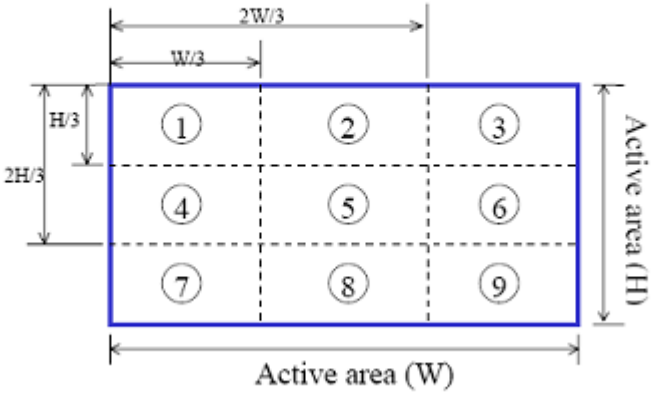
Differential voltage range, termination resistor and Common mode voltage

8. Backlight Characteristics

Item	Symbol	Min	Typ	Max	Unit	Condition	Remark
Forward voltage	V_{BL}	8.7	9.3	9.9	V	IF=180mA（恒定电流测试）	-
Current	I_{BL}		180		mA		-
ICE	X				-		-
	Y				-		
Brightness of LCM	-	350	400		cd/m²		★1
Uniformity	-	80	-	-	%		★2

★1 Uniform measure condition:

(1)Measure 9 point. Measure location is show below :
(2)Uniform = (Min. brightness / Max. brightness)×100%
(3)Best Contrast.

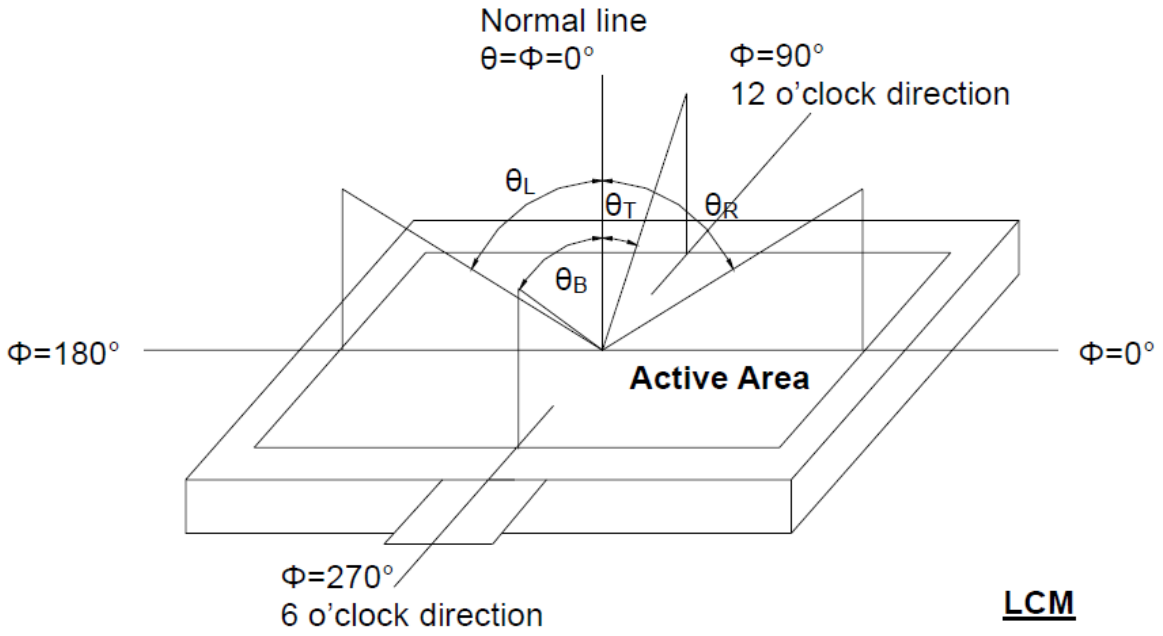


9. Electro-Optical Characteristics

Item	Symbol	Condition	Values			Unit	Remark
			Min.	Typ.	Max.		
Viewing angle (CR≥ 10)	θ_L	Φ=180°(9 o'clock)	75	85	-	degree	Note 1f
	θ_R	Φ=0°(3 o'clock)	75	85	-		
	θ_T	Φ=90°(12 o'clock)	75	85	-		
	θ_B	Φ=270°(6 o'clock)	75	85	-		
Response time	T_{R+} T_F	Normal θ=Φ=0°	-	25	35	msec	Note 3
Contrast ratio	CR		600	800	-	-	Note 4
Color chromaticity	W_X		0.273	0.313	0.353		Note 2 Note 5 Note 6
	W_Y		0.289	0.329	0.369		
NTSC			55	60		%	
Transmittance	Tr		4.3	4.7		%	

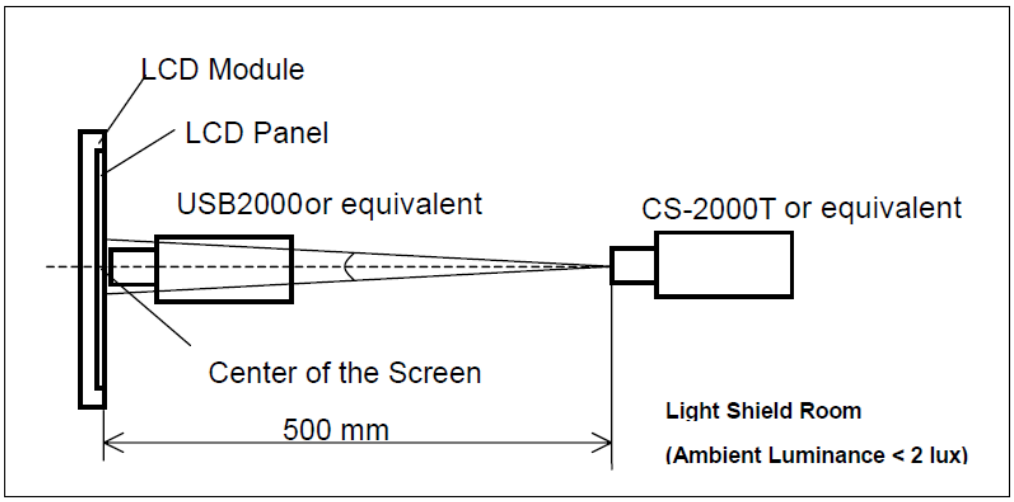
Test Conditions:
The test systems refer to Note 2.

Note 1: Definition of viewing angle range

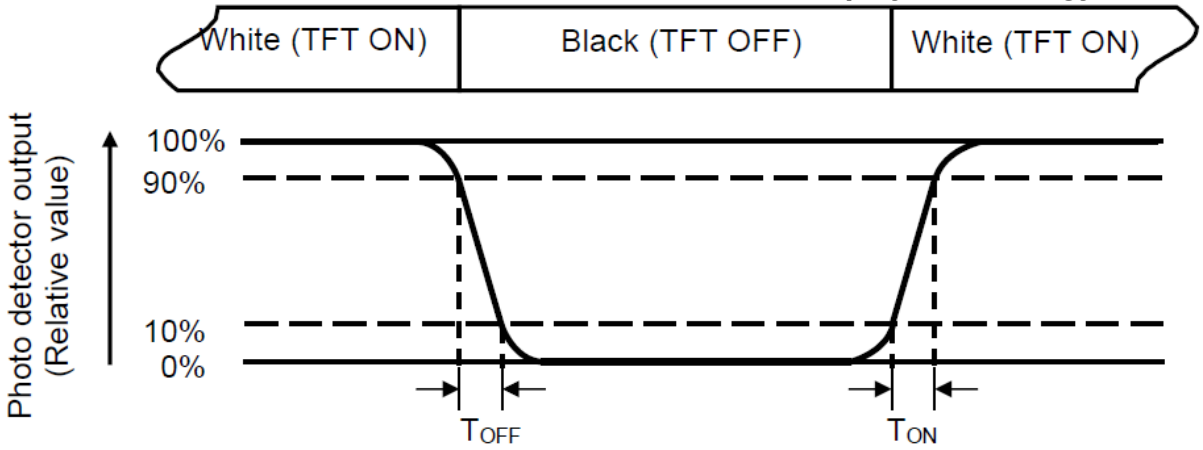


LCM

Note 2: Definition of optical measurement system.
The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Viewing angle is measured by ELDIM-EZ contrast/Height :1.2mm, Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/ Field of view: 1° /Height: 500mm.)



Note 3: Definition of Response time
The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Fall time (T_{OFF}) is the time between photo detector output intensity changed from 90% to 10%. And rise time (T_{ON}) is the time between photo detector output intensity changed from 10% to 90%.



Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of color chromaticity (CIE1931)
Color coordinates measured at center point of LCD.
Note 6: All input terminals LCD panel must be ground while measuring the center area of the panel.

10. Reliability

10. 1. MTBF

The LCD module shall be designed to meet a minimum MTBF value of 50000 hours with normal. (25°C in the room without sunlight)

10. 2. Test condition

ITEM	CONDITIONS	CRITERION
OPERATING TEMPERATURE	HIGH TEMPERTURE +70℃ 48HRS	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
	LOW TEMPERTURE -20℃ 48HRS	
STORAGE TEMPERATURE	HIGH TEMPERTURE +80℃ 48HRS	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
	LOW TEMPERTURE -30℃ 48HRS	
HUMIDITY	40℃ 90%RH 48HRS	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION

Note：The need to restore at room temperature for 2 hours after the test。

11. Inspection Standards

1. AQL(Acceptable Quality Level)

AQL of major and minor defect

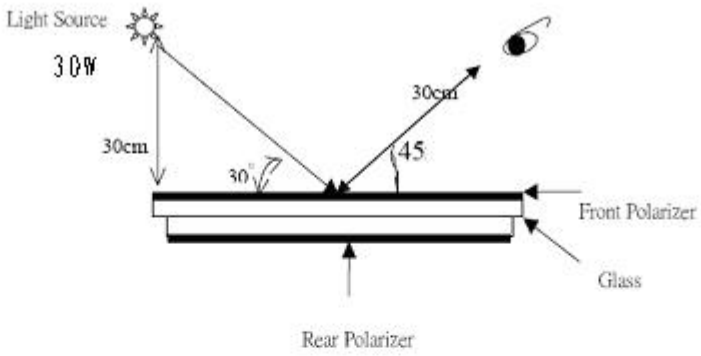
According to GB/T 2828-2003 ; , normal inspection, Class Ⅱ

MAJOR DEFECT	MINORDEFECT
0.65	1.5

2. Basic conditions for inspection

The LCM face to us, in normal environment, About an angle of incidence 30, a distance of 30cm with normal eye,with an angle of 45 degree to check the products without uncovering the film!

(As shown below)

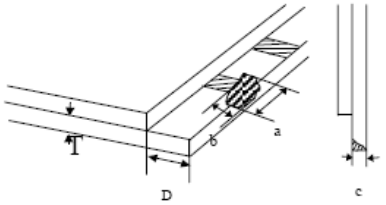
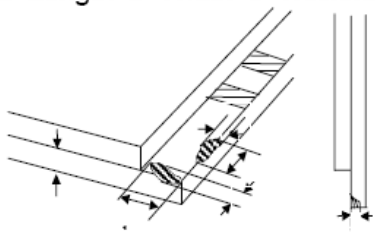


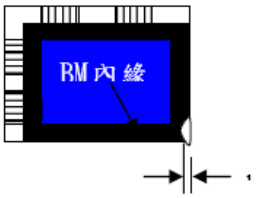
3. Inspection item and criteria

3.1 Visual inspection criterion in immobility

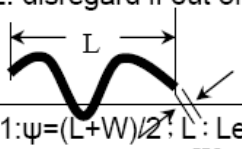
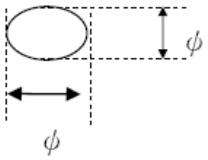
3.1.1 Glass defect

No	Defect item	Criteria	Remark
1	Dimension Unconformity (Major defect)	By Engineering Drawing	

No	Defect item	Criteria	Remark
2	Cracks (Major defect)	1.Linear cracks on panel 【Reject】 2. Nonlinear crack contrast by limited sample	
3	Glass extrude the conductive area (minor defect)	a: disregards and no influence assemblage 1) b≦1/3Pin width(non bonding area) 【Accept】 2) bonding area≦0.5mm 【Accept】	a:Length, b:Width
4	Pin-side，conductive area damaged (minor defect)	(a c：disregards) b≦ 1/3 of effective length for bonding electrode 【Accept】	a:Length，b:Width，c:Thickness 
5	Pin-side，non-conductive area damaged (minor defect)	1) Damage area don't touch the ITO (Inclueling contraposition mark,except scribing mark) 【Accept】 2) c<T b≦BM 1/3 of width 【Accept】 3) c=T b not touch the seal glue 【Accept】 4) a disregards	a:Length，b:Width，c:Thickness 

No	Defect item	Criteria	Remark
6	Non-pin-side damage (minor defect)	c<T 1) b exceeds 1/3 BM 【Reject】 c=T b not touch the seal glue 【Reject】	c : Thickness b: width of damage 

3.1.2 LCD appearance defect (View area)

No	Defect item	Criteria		Remark
1	Fiber、glass cratch、polarizer scratch/folded (minor defect)	Specification	Allowable	note1: L：Length，W：Width note2: disregard if out of AA 
		0.05mm<W≦0.1mm; L≦3.0mm	1	
		W>0.1mm ; L>3.0mm	0	
2	Polarizer bubble、concave and convex (minor defect)	ψ≦0.2mm	disregard	note 1:ψ=(L+W)/2；L：Length，W：Width note2: disregard if out of AA
		0.2mm<ψ ≦ 0.3mm	2	
		0.3mm<ψ ≦ 0.5mm	1	
		0.5mm<ψ	0	
3	Black dots、dirty dots、impurities、eyewinker (Major defect)	ψ≦0.15mm	disregard	note2: disregard if out of AA 
		0.15mm<ψ ≦ 0.25mm	2	
		0.25mm<ψ ≦ 0.3mm	1	
		0.3mm<ψ	0	
4	Polarizer prick (Major defect)	ψ≦0.1mm	disregard	note1:ψ=(L+W)/2 ；L= Length，W=Width note2: the distance between two dots ＞5mm
		0.1mm<ψ≦0.25mm	3	
		ψ＞0.25mm	0	

3.1.3 .FPC

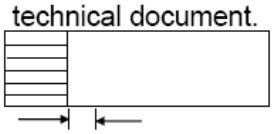
No	Defect item	Criteria		Remark
1	Copper screen peel (Major defect)	Copper screen peel 【Reject】		
2	No release tape or peel (Major defect)	No release tape or peel 【Reject】		
3	Dirty dot and impurity of FPC for customer using side (minor defect)	Specification	Allowable	note1: Cannot have stride ITO impurities
		ψ≦0.25mm	2	
		ψ>0.25	0	

3.1.4 Black tape & Mara tape

1	FPC or H/S black tape shift (minor defect)	1.shift spec: 1)glue to the polarize 【Reject】 2) IC bare 【Reject】 2. left-and-right spec: 1) exceed of FPC edge or H-S edge 【Reject】 2)IC bare 【Reject】	
2	No black tape (Major defect)	No black tape 【Reject】	
3	Tape position mistake (minor defect)	Not by engineering drawing 【Reject】	
4	Mara tape defect (minor defect)	Peel before pulling the protecting film. 【Reject】	

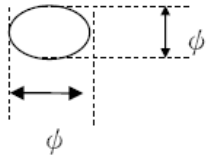
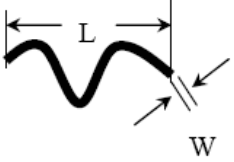
3.1.5 Silicon and Tuffy glue

No	Defect item	Criteria	Remark
1	Quantity of silicon (minor defect)	Uncover the ITO and circuit area. 【Reject】	note: compared by engineering drawing.

No	Defect item	Criteria	Remark
2	Tuffy glue (minor defect)	1. Uncover the reveal copper area 【Reject】 2. Cover layer 0.3mm(Min) ~ 3.0mm(Max) 【accept】	note:if customer has special requirement , refer to the technical document. 
3	Depth of glue covering (minor defect)	Depth of glue covering overtop front Polarizer 【Reject】	Except of the special requirement。

3.2 Electrical criteria

No	Defect item	Criteria	Remark
1	No display (Major defect)	No display 【Reject】	
2	Missing line (Major defect)	Missing line 【Reject】	
3	Seg-com light and dark (Major defect)	Seg-com light and dark 【Reject】	ND filter 2% test
4	No display in immobility (Major defect)	No display in immobility 【Reject】	
5	Flicker of Pattern (Major defect)	Flicker of Pattern 【Reject】	
6	Mura (Major defect)	ND filter 2% test	
7	Over current (Major defect)	Over current 【Reject】	
8	Voltage out of specification (Major defect)	Voltage out of specification 【Reject】	
9	Pattern blur ,error code (Major defect)	Pattern blur ,error code 【Reject】	
10	Dark light, Flicker (Major defect)	Dark light, Flicker 【Reject】	

No	Defect item	Criteria	Remark	
11	Black/White dots 、Dirty dots 、eyewinker (Major defect)	Specification	Allowable	Note1: disregard if out of AA 
		ψ≦0.15mm	disregard	
		0.15mm<ψ ≦ 0.25mm	2	
		0.25mm<ψ ≦ 0.3mm	1	
		0.3mm<ψ	0	
12	Fiber 、glass cratch 、 polarizer scratch/folded (minor defect)	W≦0.03mm	disregard	note1: L : Length 、W : Width note2: disregard if out of AA 
		0.03mm<W≦0.05mm ; L≦3.0mm	2	
		0.05mm<W≦0.1mm; L≦3.0mm	1	
		W>0.1mm ; L>3.0mm	0	

12. Precautions For Using LCD Modules

Please pay attentions to the followings as using the LCD module.

12.1 Handling

(a) Do not apply strong mechanical stress like drop, shock or any force to LCD module. It may cause improper operation, even damage.

(b) Because the ITO film very fragile and easy to be damaged, do not hit, press or rub the display surface with hard materials.

(c) Do not put heavy or hard material on the display surface, and do not stack LCD modules.

(d) If the display surface is dirty, please wipe the surface softly with cotton swab or clean cloth.

(e) Wipe off water droplets or oil immediately.

(f) Protect the LCD module from ESD. It will damage the LSI and the electronic circuit.

(g) Do not touch the output pins directly with bare hands.

(h) Do not disassemble the LCD module.

12.2 Storage

(a) Do not leave the LCD modules in high temperature, especially in high humidity for a long time.

(b) Do not expose the LCD modules to sunlight directly.

(c) The liquid crystal is deteriorated by ultraviolet. Do not leave it in strong ultraviolet ray for a long time.

(d) Avoid condensation of water. It may cause improper operation.

(e) Please stack only up to the number stated on carton box for storage and transportation. Excessive weight will cause deformation and damage of carton box.

12.3 Operation

(a) When mounting or dismounting the LCD modules, turn the power off.

(b) Protect the LCD modules from electric shock.

(c) The Driver IC control algorithms stated above should always obeyed to avoid damaging the LSI and electronic circuit.

(d) Be careful to avoid mixing up the polarity of power supply for backlight.

(e) Absolute maximum rating specified above has to be always kept in any case. Exceeding it may cause non-recoverable damage of electronic components or, nevertheless, burning.

(f) When a static image is displayed for a long time, remnant image is likely to occur.

(g) Be sure to avoid bending the FPC to an acute shape, it might break FPC.

12.4 Others

(a) If the liquid crystal leaks from the panel, it should be kept away from the eyes or mouth.

(b) It is recommended to peel off the protection film on the ITO film slowly so that the electrostatic charge can be minimized.

(c) It is recommended to peel off the protection film on the polarizer slowly so that the electrostatic charge can be minimized.

13. Records Of Version

Version	Revise Date	Page	Content
00	2019-03-19	All	New released