东莞市慧勤光电科技有限公司

Waiken Optoelectronics Technology Co,.Ltd

PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 00

Model No: WK70259

Module Type: COG+FPC+B/L+CTP

APPROVED SIGNATURE

□ Approved Product Specification only

■ Approved Product Specification and Samples

Prepared By	Checked By	Approved By
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Contents

1. General Description

WK70259 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 7.0 inch and the resolution is 800(RGB)*1280, the panel can display up to 16M colors.

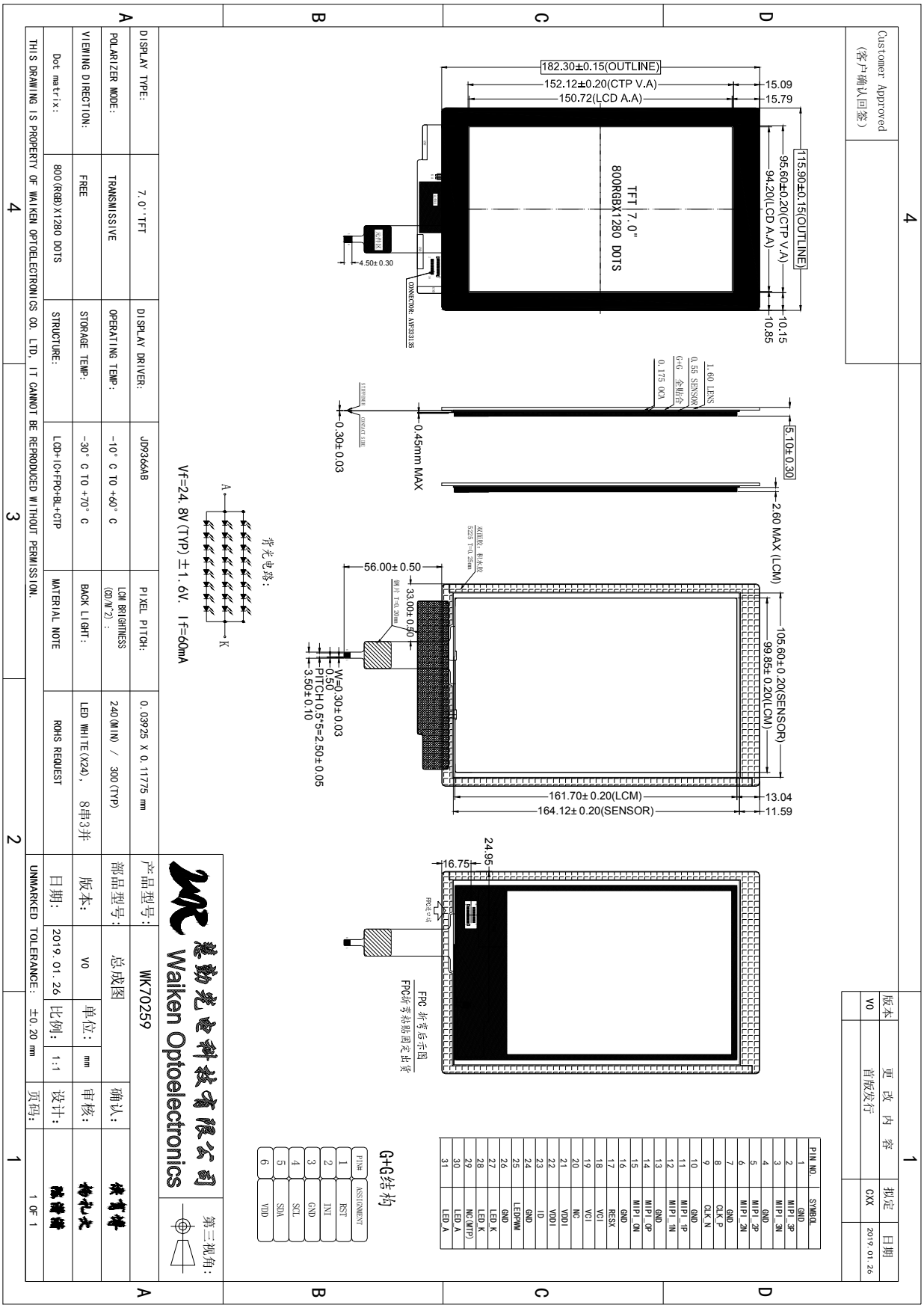
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 800×RGB×1280 Dot-matrix
Input Data	MIPI
Viewing Direction	Free

3. Mechanical Specification

Item	Contents	Unit
Module size (W×H×T)	115.90 × 182.30× 5.10	mm
Number of dots	800(RGB) × 1280	---
Active area (W×H)	94.20 × 150.72	mm

4. Outline Dimension



5. Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit	Remark
Interface Supply Voltage	VDDI	-0.3	3.6	V	
Analog Power Supply Voltage	VCI	-0.3	6.6	V	

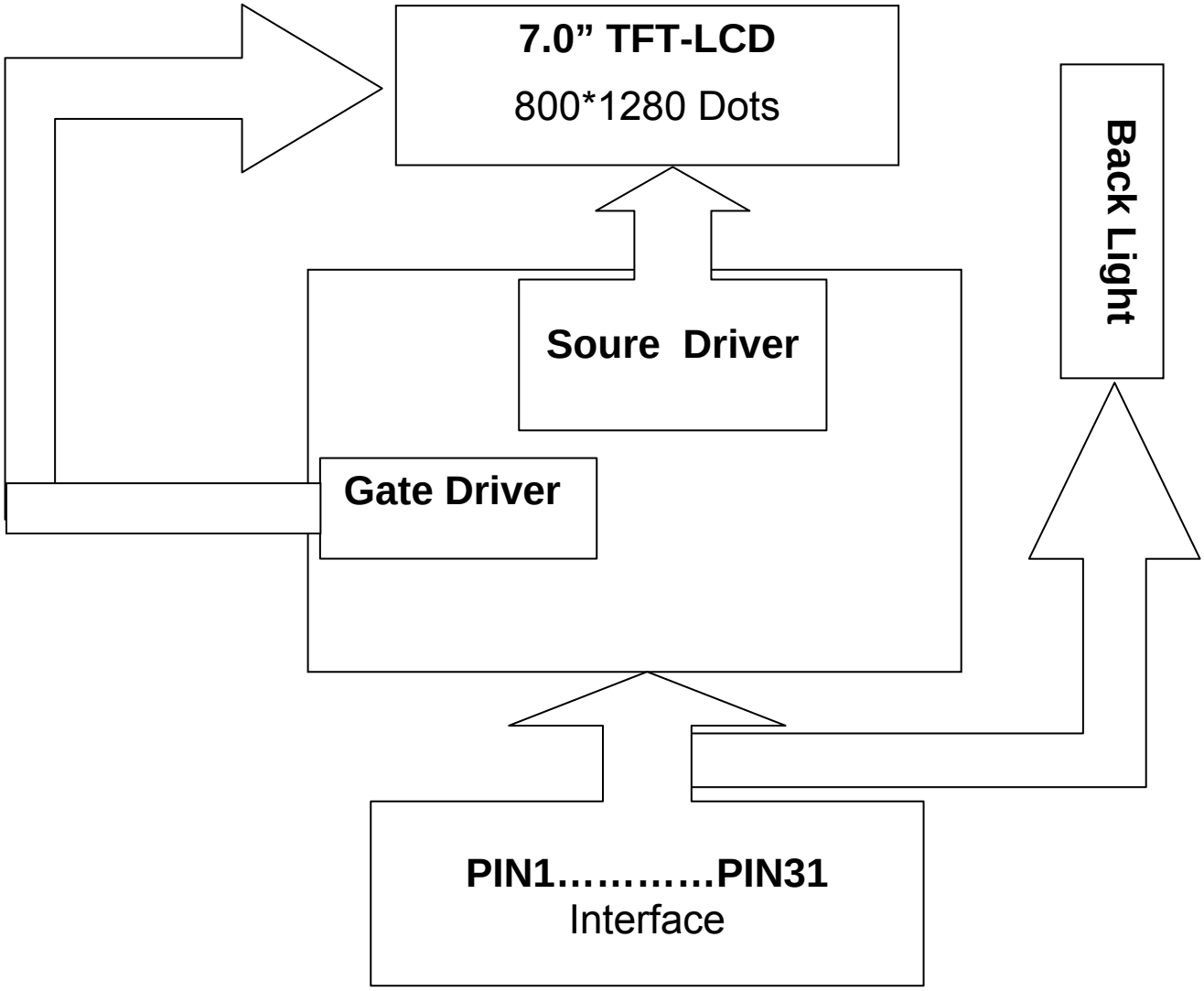
6. Electrical Characteristics

Typical Operation Conditions

Item	Symbol	Min.	Type	Max.	Unit	Remark
Analog Operating Voltage	VCI	3.0	3.3	3.6	V	
Digital Operating Voltage	VDDI	1.7	1.8	1.9	V	
Input Supply Voltage	V_{IH}	0.7* V_{DD}	-	V_{DD}	V	
	V_{IL}	Vss	-	0.3* V_{DD}	V	
Oouput Supply Voltage	V_{OH}	0.8* V_{DD}	-	V_{DD}	V	
	V_{OL}	Vss	-	0.3* V_{DD}	V	
Power Supply Current	I_{DD}	-	TBD	-	mA	

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	Description
1	GND	Ground
2	MIPI_3P	MIPI Positive data signal (+)
3	MIPI_3N	MIPI Negative data signal (-)
4	GND	Ground
5	MIPI_2P	MIPI Positive data signal (+)
6	MIPI_2N	MIPI Negative data signal (-)
7	GND	Ground
8	CLK_P	MIPI Positive data signal (+)
9	CLK_N	MIPI Negative data signal (-)
10	GND	Ground
11	MIPI_1P	MIPI Positive data signal (+)
12	MIPI_1N	MIPI Negative data signal (-)
13	GND	Ground
14	MIPI_0P	MIPI Positive data signal (+)
15	MIPI_0N	MIPI Negative data signal (-)
16	GND	Ground
17	RESX	Reset signal active low
18	VCI	Analog Power Supply Voltage
19	VCI	Analog Power Supply Voltage
20	NC	No connection
21	VDDI	Power Supply Voltage
22	VDDI	Power Supply Voltage
23	ID	Ground
24	GND	Ground
25	LEDPWM	PWM control signal for LED driver (CABC)
26	GND	Ground
27	LED_K	Cathode for light bar
28	LED_K	Cathode for light bar
29	NC(MTP)	No connection
30	LED_A	Anode for light bar
31	LED_A	Anode for light bar

7-3. MIPI Timing Characteristics

Burst Mode Data Transmission

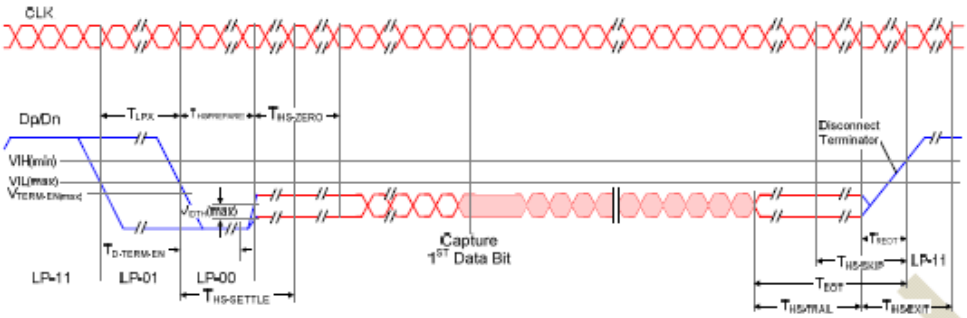


Figure 11.7: High-Speed Data Transmission in Bursts

Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 + n*4*UI)	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

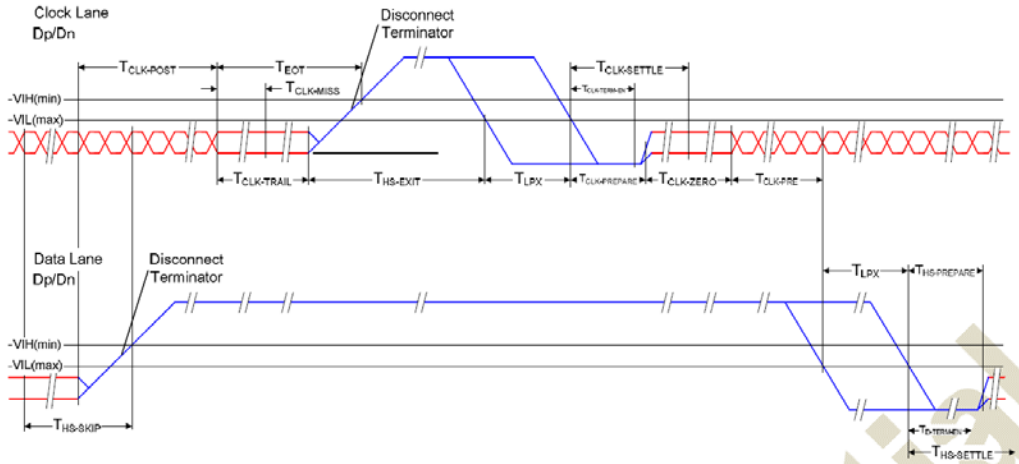


Figure 11.8: Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

Vertical Timings

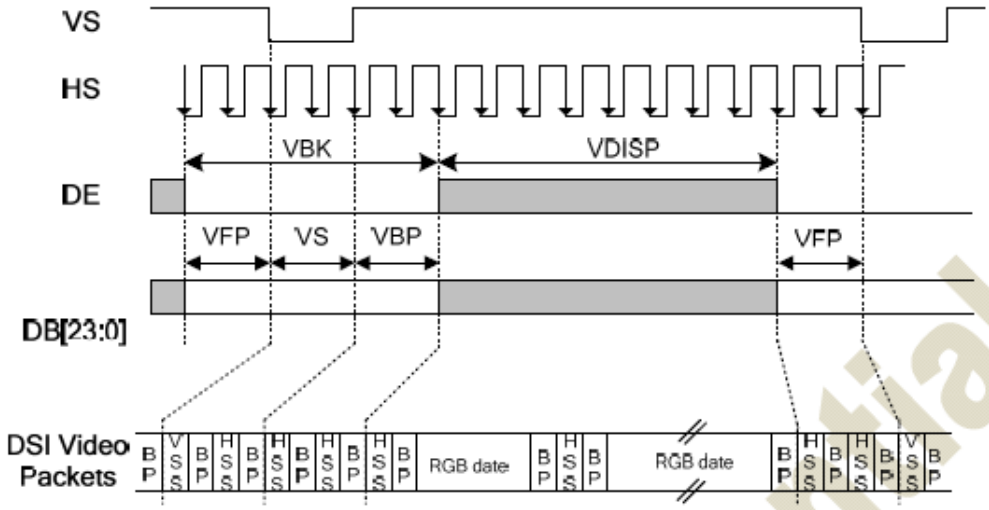


Figure 11.9: Vertical Timings for DPI I/F

Resolution=800x1280(T_A=25°C, IOVCC=1.8V, VCIP=2.8V, VCI=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical low pulse width	VS	-	2	-	Note(1)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(1)	Line
Vertical blanking period	VBK	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	1280	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GIP start pulse and GIP clock pulse timing. The GIP start pulse and GIP clock pulse must be set at corresponding position for LCD normal display.

Horizontal Timings

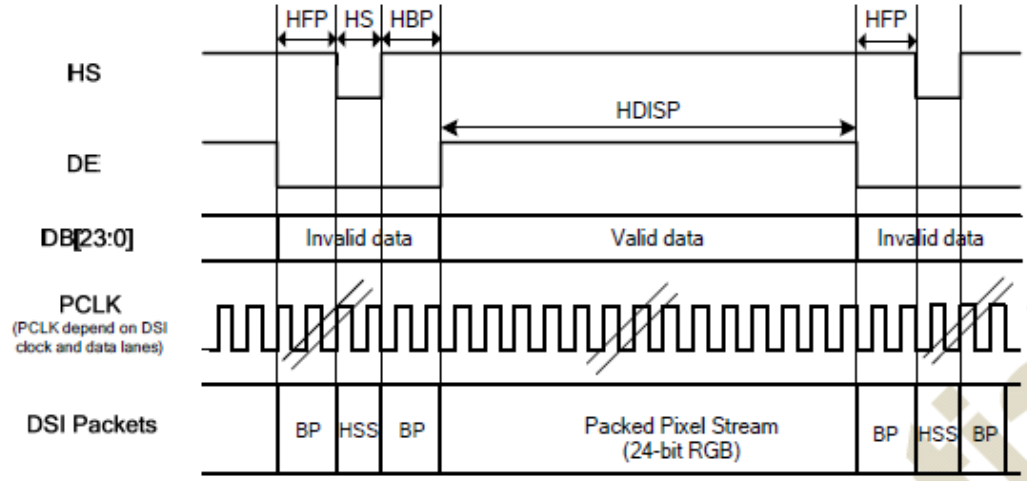


Figure 11.10: Horizontal Timing for DSI Video mode I/F

Resolution=800x1280 (T_A=25°C, IOVCC=1.8V, VCIP=VCI=VCCH=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	6	-	78	DCK
Horizontal back porch	HBP	-	5	-	78	DCK
Horizontal front porch	HFP	-	5	-	78	DCK
Horizontal blanking period	HBLK	HS+HBP+HFP	16	-	88	DCK
Horizontal active area	HDISP	-	-	800	-	DCK

Reset Timing

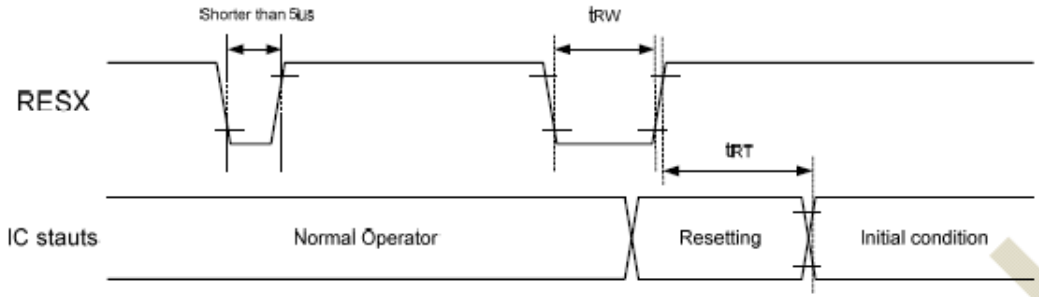


Figure 11.1: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width(2)	RESX	10	-	µs
t_{RT}	Reset complete time(3)	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

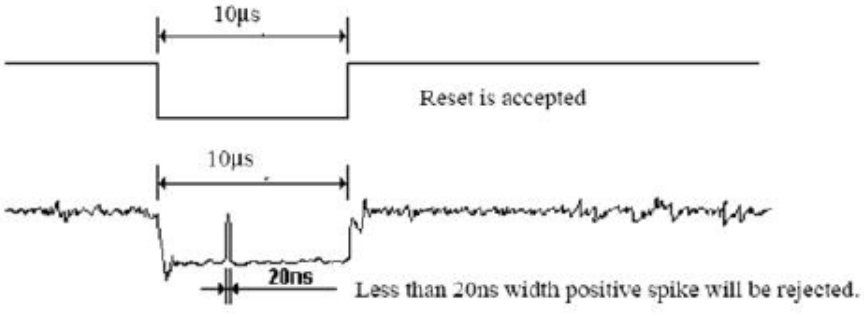
Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

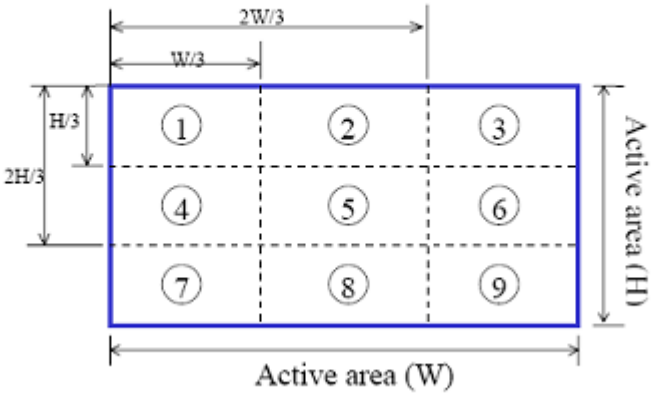
(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. Backlight Characteristics

Item	Symbol	Min	Typ	Max	Unit	Condition	Remark
Forward voltage	V_{BL}	23.2	24.8	26.4	V	IF=60mA（恒定电流测试）	-
Current	I_{BL}		60		mA		-
ICE	X	0.23	-	0.33	-		-
	Y	0.29	-	0.39	-		
Brightness of LCM	-	240	300		cd/m²		★1
Uniformity	-	75	-	-	%		

★1 Uniform measure condition:

(1)Measure 9 point. Measure location is show below :
(2)Uniform = (Min. brightness / Max. brightness)×100%
(3)Best Contrast.



9. Electro-Optical Characteristics

The test of Optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2℃) with the equipment of Luminance meter system (CA-310、BM-5A) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to $\theta_{Ø=0}$ ($=\theta_3$) as the 3 o'clock direction (the "right"), $\theta_{Ø=90}$ ($=\theta_{12}$) as the 12 o'clock direction ("upward"), $\theta_{Ø=180}$ ($=\theta_9$) as the 9 o'clock direction ("left") and $\theta_{Ø=270}$($=\theta_6$) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 3.3V +/-10% at 25°C. Optimum viewing angle direction is 6 'clock.

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	**80**	**89**	-	Deg.	Note 1
		Θ_9		**80**	**89**	-	Deg.	
	Vertical	Θ_{12}		**80**	**89**	-	Deg.	
		Θ_6		**80**	**89**	-	Deg.	
Color Gamut				45	**50**	55	%	-
Tr.				-	6.8	-	%	With APF
Luminance Contrast ratio		CR	Θ = 0°	700	850	-	-	Note 2
Luminance of White	Center Points	Y_w	Θ = 0°	-	-	-	cd/m²	Note 3
White Luminance uniformity	9 Points	ΔY5		-	-	-	%	Note 4
White balance		Color Temp	Θ = 0°	-	-	-	K	Note 5
		Δuv		-	-	-	-	
Reproduction of color	Red	R_x	Θ = 0°		**0.610**		-	Note6
		R_y			**0.350**			
	Green	G_x			**0.340**			
		G_y			**0.570**			
	Blue	B_x			**0.160**			
		B_y			**0.120**			
Response Time (Rising + Falling)		T_{RT}	Ta= 25° C Θ = 0°	-	30	**35**	ms	Note 7
Gamma Scale		CT	Θ = 0°	-	-	-	-	-

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as luminance values of 1point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 2 for a total of the measurements per display. The luminance is measured by CA310 when the LED current is set at 16.8mA.

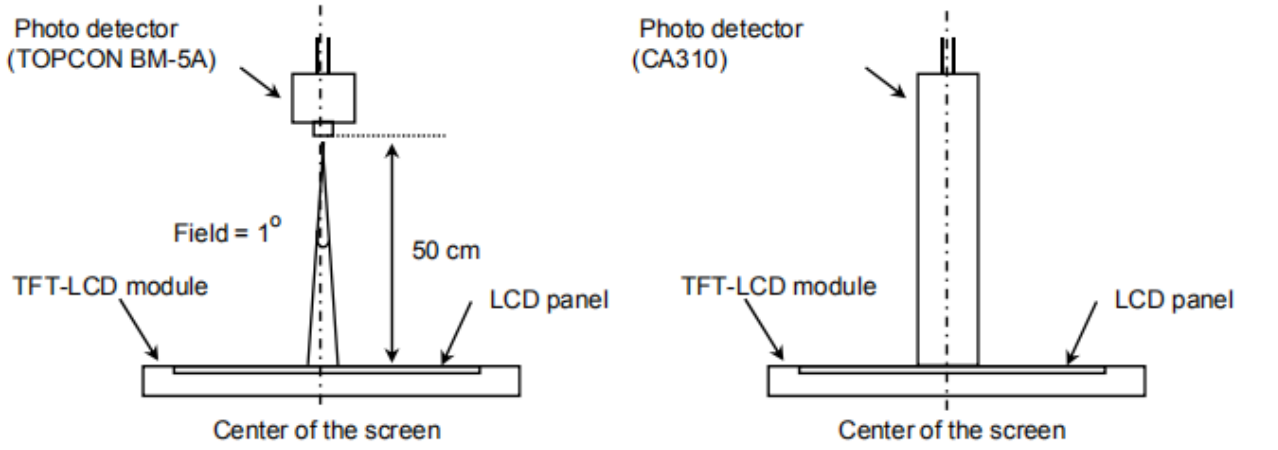
4. The White luminance uniformity on LCD surface is then expressed as : ΔY = Minimum Luminance of 9points / Maximum Luminance of 9points (see FIGURE 2).

5. The color chromaticity coordinates specified shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

6. The color chromaticity coordinates specified shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

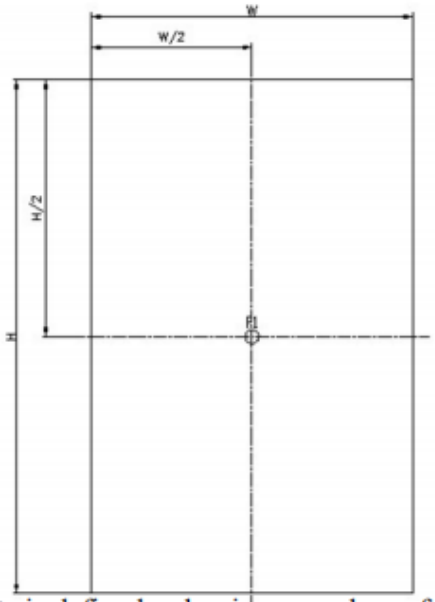
7. The electro-optical response time measurements shall be made as FIGURE 4 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

Figure 1. Measurement Set Up



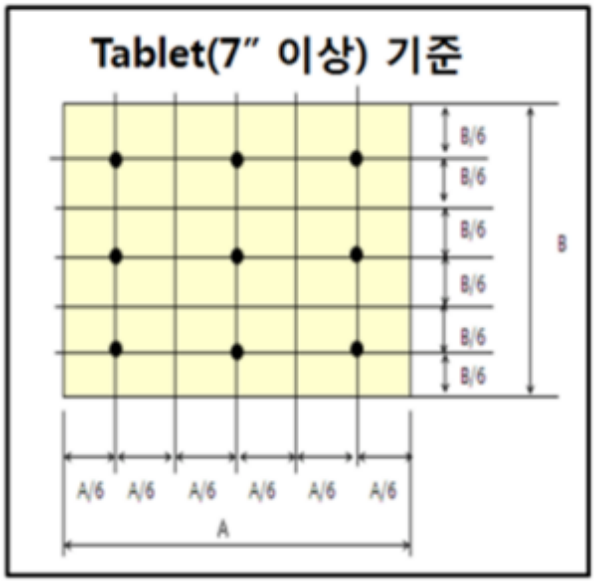
View angel range measurement setup Luminance , uniformity and color measurement setup

Figure 2. White Luminance and Uniformity Measurement Locations (Center point)



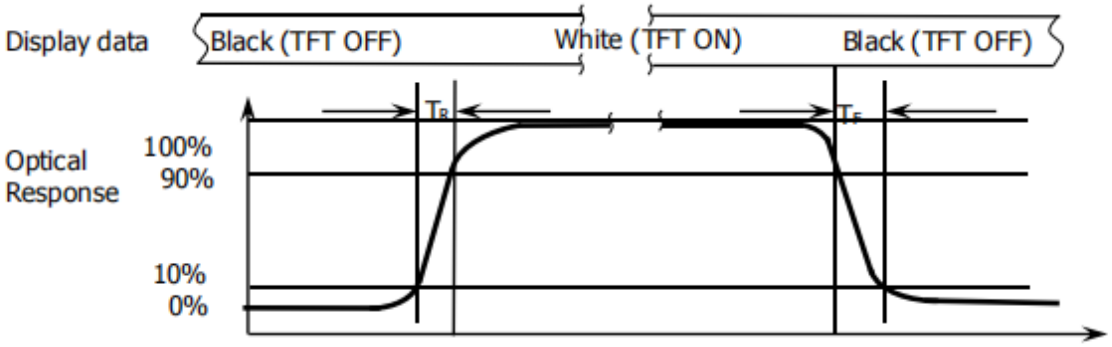
Center Luminance of white is defined as luminance values of center point across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE for a total of the measurements per display.

Figure 3. Uniformity Measurement Locations (9 points)



The White luminance uniformity on LCD surface is then expressed as : ΔY9= Minimum Luminance of five points / Maximum Luminance of five points (see FIGURE 3)

Figure 4. Response Time Testing



The electro-optical response time measurements shall be made as shown in FIGURE 3 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr and 90% to 10% is Td.

10. Reliability

10. 1. MTBF

The LCD module shall be designed to meet a minimum MTBF value of 50000 hours with normal. (25°C in the room without sunlight)

10. 2. Test condition

ITEM	CONDITIONS	CRITERION
OPERATING TEMPERATURE	HIGH TEMPERTURE +60℃ 48HRS	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
	LOW TEMPERTURE -10℃ 48HRS	
STORAGE TEMPERATURE	HIGH TEMPERTURE +70℃ 48HRS	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
	LOW TEMPERTURE -30℃ 48HRS	
HUMIDITY	40℃ 90%RH 48HRS	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION

Note：The need to restore at room temperature for 2 hours after the test。

11. Inspection Standards

1. AQL(Acceptable Quality Level)

AQL of major and minor defect

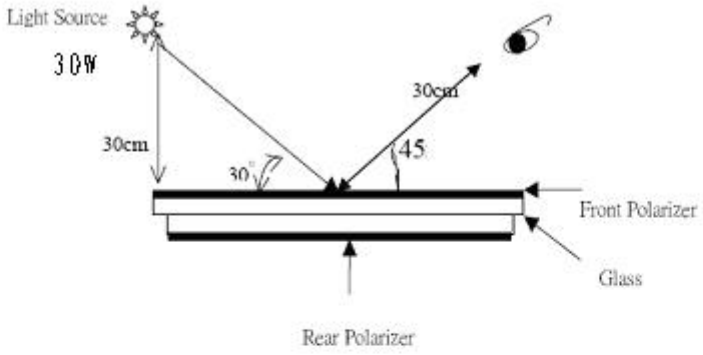
According to GB/T 2828-2003 ; , normal inspection, Class Ⅱ

MAJOR DEFECT	MINORDEFECT
0.65	1.5

2. Basic conditions for inspection

The LCM face to us, in normal environment, About an angle of incidence 30, a distance of 30cm with normal eye,with an angle of 45 degree to check the products without uncovering the film!

(As shown below)

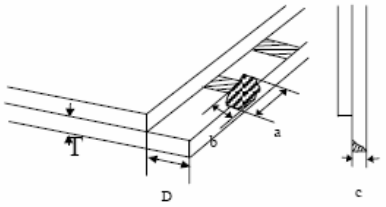
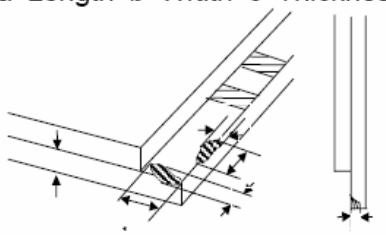


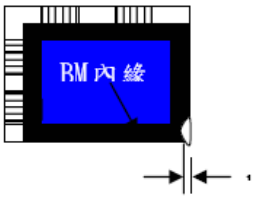
3. Inspection item and criteria

3.1 Visual inspection criterion in immobility

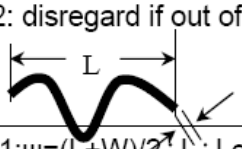
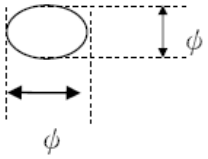
3.1.1 Glass defect

No	Defect item	Criteria	Remark
1	Dimension Unconformity (Major defect)	By Engineering Drawing	

No	Defect item	Criteria	Remark
2	Cracks (Major defect)	1.Linear cracks on panel 【Reject】 2. Nonlinear crack contrast by limited sample	
3	Glass extrude the conductive area (minor defect)	a: disregards and no influence assemblage 1) b≦1/3Pin width(non bonding area) 【Accept】 2) bonding area≦0.5mm 【Accept】	a:Length, b:Width
4	Pin-side，conductive area damaged (minor defect)	(a c：disregards) b≦ 1/3 of effective length for bonding electrode 【Accept】	a:Length，b:Width，c:Thickness 
5	Pin-side，non-conductive area damaged (minor defect)	1) Damage area don't touch the ITO (Inclueling contraposition mark,except scribing mark) 【Accept】 2) c<T b≦BM 1/3 of width 【Accept】 3) c=T b not touch the seal glue 【Accept】 4) a disregards	a:Length，b:Width，c:Thickness 

No	Defect item	Criteria	Remark
6	Non-pin-side damage (minor defect)	c<T 1) b exceeds 1/3 BM 【Reject】 c=T b not touch the seal glue 【Reject】	c : Thickness b: width of damage 

3.1.2 LCD appearance defect (View area)

No	Defect item	Criteria		Remark
1	Fiber、glass cratch、polarizer scratch/folded (minor defect)	Specification	Allowable	note1: L：Length，W：Width note2: disregard if out of AA 
		0.05mm<W≦0.1mm; L≦3.0mm	1	
		W>0.1mm ; L>3.0mm	0	
2	Polarizer bubble、concave and convex (minor defect)	ψ≦0.2mm	disregard	note 1:ψ=(L+W)/2；L：Length，W：Width note2: disregard if out of AA
		0.2mm<ψ ≦ 0.3mm	2	
		0.3mm<ψ ≦ 0.5mm	1	
		0.5mm<ψ	0	
3	Black dots、dirty dots、impurities、eyewinker (Major defect)	ψ≦0.15mm	disregard	note2: disregard if out of AA 
		0.15mm<ψ ≦ 0.25mm	2	
		0.25mm<ψ ≦ 0.3mm	1	
		0.3mm<ψ	0	
4	Polarizer prick (Major defect)	ψ≦0.1mm	disregard	note1:ψ=(L+W)/2 ；L= Length，W=Width note2: the distance between two dots ＞5mm
		0.1mm<ψ≦0.25mm	3	
		ψ＞0.25mm	0	

3.1.3 .FPC

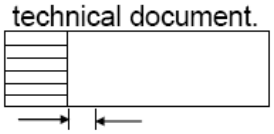
No	Defect item	Criteria		Remark
1	Copper screen peel (Major defect)	Copper screen peel 【Reject】		
2	No release tape or peel (Major defect)	No release tape or peel 【Reject】		
3	Dirty dot and impurity of FPC for customer using side (minor defect)	Specification	Allowable	note1: Cannot have stride ITO impurities
		ψ≦0.25mm	2	
		ψ>0.25	0	

3.1.4 Black tape & Mara tape

1	FPC or H/S black tape shift (minor defect)	1.shift spec: 1)glue to the polarize 【Reject】 2) IC bare 【Reject】 2. left-and-right spec: 1) exceed of FPC edge or H-S edge 【Reject】 2)IC bare 【Reject】	
2	No black tape (Major defect)	No black tape 【Reject】	
3	Tape position mistake (minor defect)	Not by engineering drawing 【Reject】	
4	Mara tape defect (minor defect)	Peel before pulling the protecting film. 【Reject】	

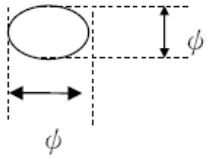
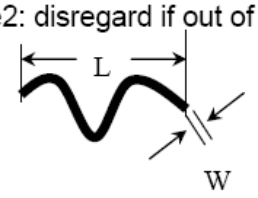
3.1.5 Silicon and Tuffy glue

No	Defect item	Criteria	Remark
1	Quantity of silicon (minor defect)	Uncover the ITO and circuit area. 【Reject】	note: compared by engineering drawing.

No	Defect item	Criteria	Remark
2	Tuffy glue (minor defect)	1. Uncover the reveal copper area 【Reject】 2. Cover layer 0.3mm(Min) ~ 3.0mm(Max) 【accept】	note:if customer has special requirement , refer to the technical document. 
3	Depth of glue covering (minor defect)	Depth of glue covering overtop front Polarizer 【Reject】	Except of the special requirement。

3.2 Electrical criteria

No	Defect item	Criteria	Remark
1	No display (Major defect)	No display 【Reject】	
2	Missing line (Major defect)	Missing line 【Reject】	
3	Seg-com light and dark (Major defect)	Seg-com light and dark 【Reject】	ND filter 2% test
4	No display in immobility (Major defect)	No display in immobility 【Reject】	
5	Flicker of Pattern (Major defect)	Flicker of Pattern 【Reject】	
6	Mura (Major defect)	ND filter 2% test	
7	Over current (Major defect)	Over current 【Reject】	
8	Voltage out of specification (Major defect)	Voltage out of specification 【Reject】	
9	Pattern blur ,error code (Major defect)	Pattern blur ,error code 【Reject】	
10	Dark light, Flicker (Major defect)	Dark light, Flicker 【Reject】	

No	Defect item	Criteria	Remark	
11	Black/White dots 、Dirty dots 、eyewinker (Major defect)	Specification	Allowable	Note1: disregard if out of AA 
		ψ≦0.15mm	disregard	
		0.15mm<ψ ≦ 0.25mm	2	
		0.25mm<ψ ≦ 0.3mm	1	
		0.3mm<ψ	0	
12	Fiber 、glass cratch 、polarizer scratch/folded (minor defect)	W≦0.03mm	disregard	note1: L : Length 、W : Width note2: disregard if out of AA 
		0.03mm<W≦0.05mm ; L≦3.0mm	2	
		0.05mm<W≦0.1mm; L≦3.0mm	1	
		W>0.1mm ; L>3.0mm	0	

12. Precautions For Using LCD Modules

Please pay attentions to the followings as using the LCD module.

12.1 Handling

(a) Do not apply strong mechanical stress like drop, shock or any force to LCD module. It may cause improper operation, even damage.

(b) Because the ITO film very fragile and easy to be damaged, do not hit, press or rub the display surface with hard materials.

(c) Do not put heavy or hard material on the display surface, and do not stack LCD modules.

(d) If the display surface is dirty, please wipe the surface softly with cotton swab or clean cloth.

(e) Wipe off water droplets or oil immediately.

(f) Protect the LCD module from ESD. It will damage the LSI and the electronic circuit.

(g) Do not touch the output pins directly with bare hands.

(h) Do not disassemble the LCD module.

12.2 Storage

(a) Do not leave the LCD modules in high temperature, especially in high humidity for a long time.

(b) Do not expose the LCD modules to sunlight directly.

(c) The liquid crystal is deteriorated by ultraviolet. Do not leave it in strong ultraviolet ray for a long time.

(d) Avoid condensation of water. It may cause improper operation.

(e) Please stack only up to the number stated on carton box for storage and transportation. Excessive weight will cause deformation and damage of carton box.

12.3 Operation

(a) When mounting or dismounting the LCD modules, turn the power off.

(b) Protect the LCD modules from electric shock.

(c) The Driver IC control algorithms stated above should always obeyed to avoid damaging the LSI and electronic circuit.

(d) Be careful to avoid mixing up the polarity of power supply for backlight.

(e) Absolute maximum rating specified above has to be always kept in any case. Exceeding it may cause non-recoverable damage of electronic components or, nevertheless, burning.

(f) When a static image is displayed for a long time, remnant image is likely to occur.

(g) Be sure to avoid bending the FPC to an acute shape, it might break FPC.

12.4 Others

(a) If the liquid crystal leaks from the panel, it should be kept away from the eyes or mouth.

(b) It is recommended to peel off the protection film on the ITO film slowly so that the electrostatic charge can be minimized.

(c) It is recommended to peel off the protection film on the polarizer slowly so that the electrostatic charge can be minimized.

13. Records Of Version

Version	Revise Date	Page	Content
00	2019-05-12	All	New released