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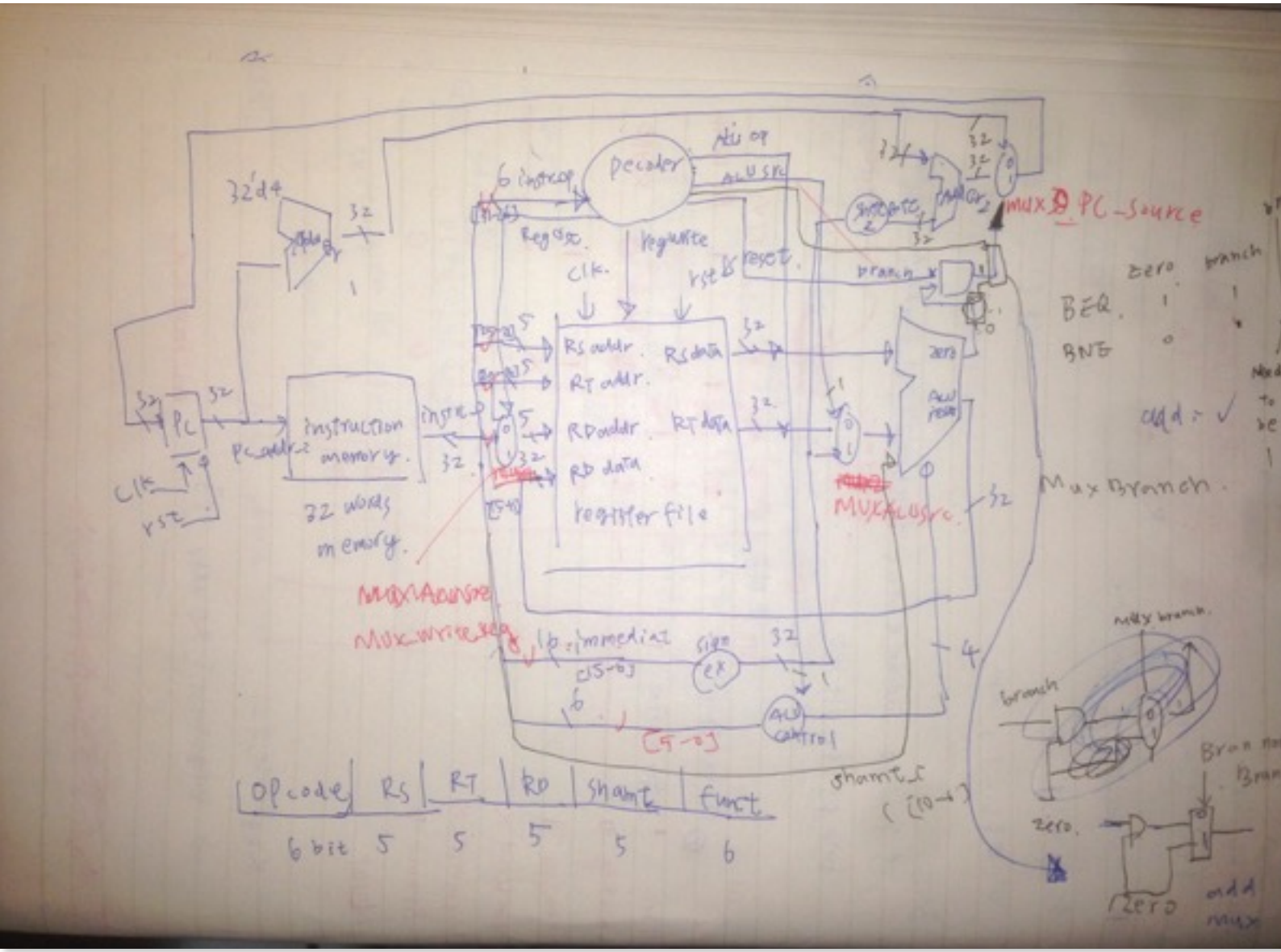
Computer Organization

Architecture diagram:



description of the implementation:

1. build element instruction memory , decoder, adder ALU, sing extension mux
2. linked the line in simple cpu
3. add additional mix for branch and branch or not

Problems encountered and solutions:

1.can not differentiate the beq and BNE
solution is adding a mux after ALU, decoder will have another output branchOrNot to determine the output of the mix is come from the AND gate or directly inverse of the Zero in ALU.

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2.
the third task
ori r10 =3
lui r11 = 10X2^16
srl r11 = 10X2^8
srlv r11 = 10X2^5
addi r10 =2 <—test file end
bne
srlv r11 =80 <—program stop at this line
addi r10 =1
bne r11 =40
addi r10 =0
bne —finish
resolution : I find out the control(decoder output) for branchOrNot mux should also set by other instruction

Lesson learnt (if any):

1. it's hard to debug
2. be care for the #of bits
3. always @ is not like assign, the block is trigger by event
4. thought all of details then start to write code
5. when debugging simulate each step of the mips instruction to see when goes wrong
6. Add Addi or Or Ori in implementation is very similar, the difference is only the write back register