

DC Lab1 Report

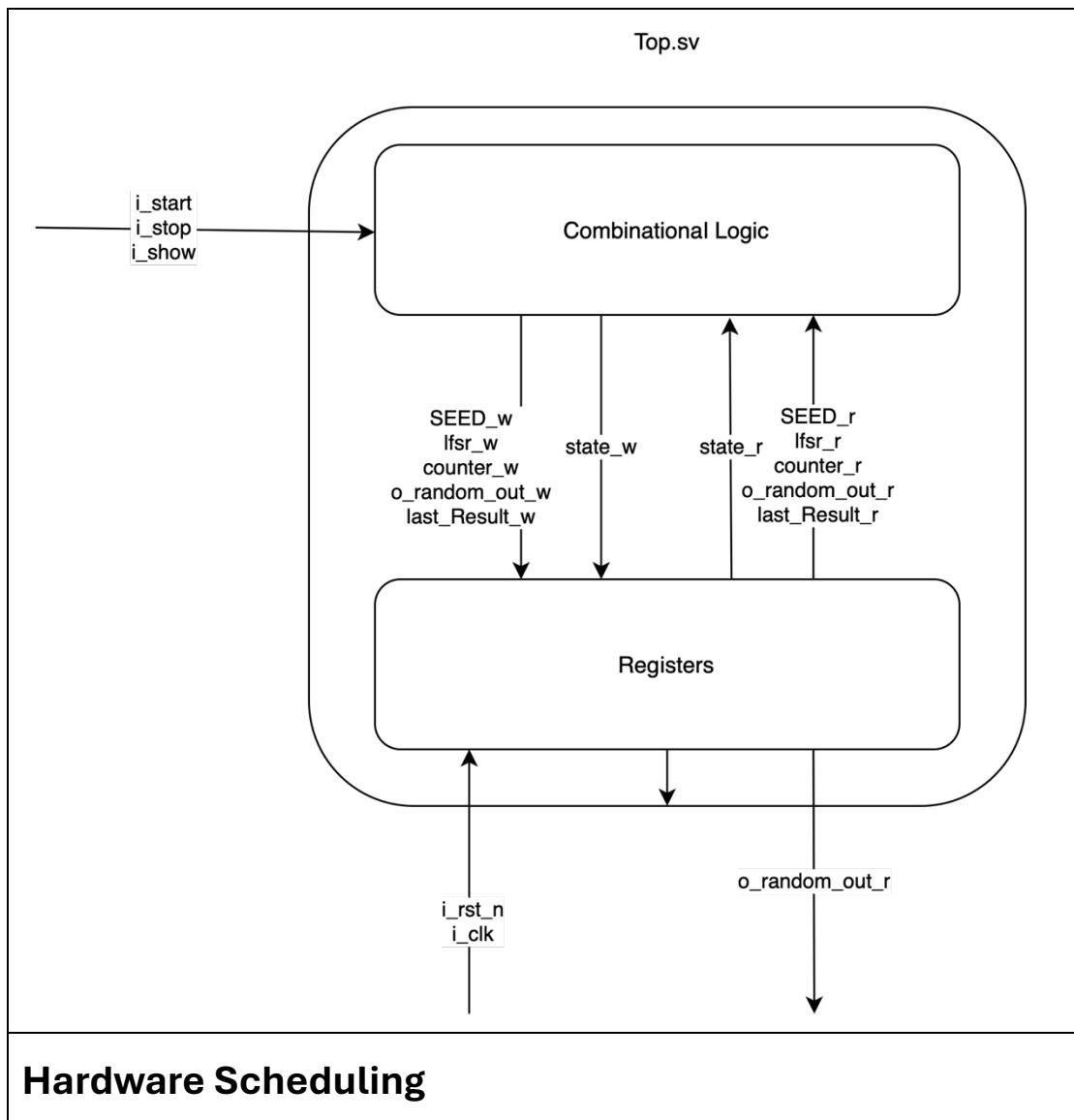
Team 04

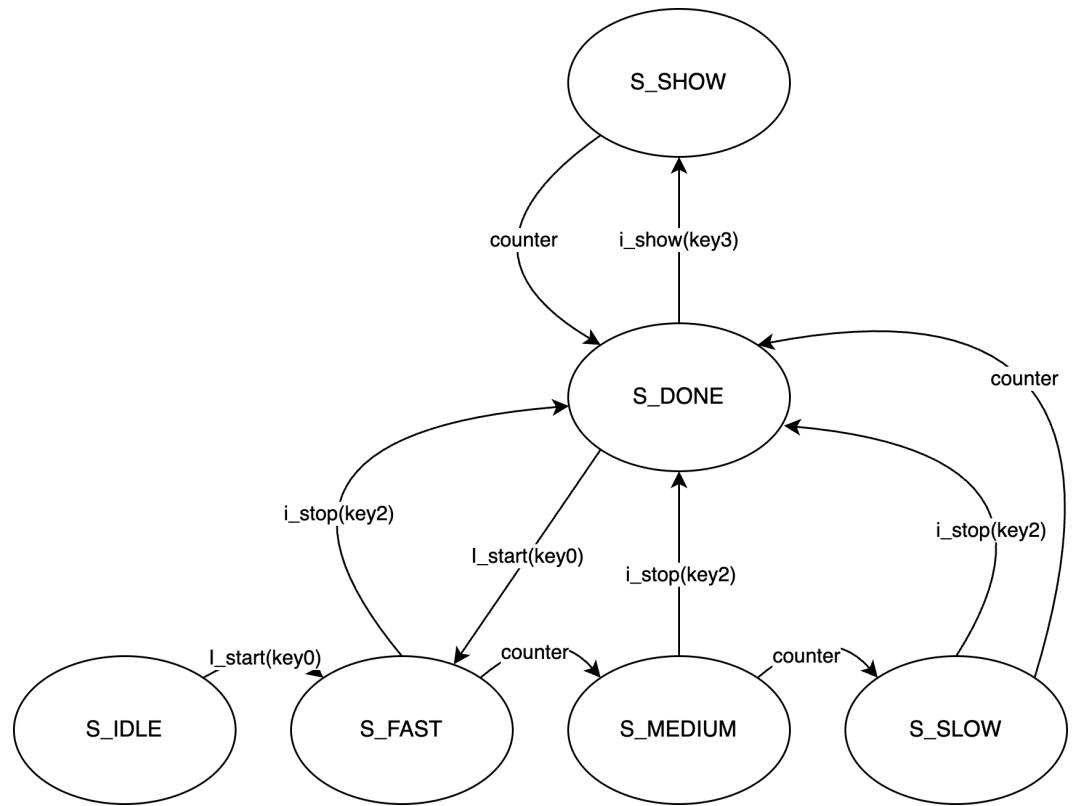
B10901163 張顥譽 B10901176 蔡弘祥 B10901179 鄭承瑞

File Structure

- team04_lab1
 - team04_lab1_report
 - src
 - Top.sv
 - DE2_115.qsf
 - DE2_115.sdc
 - DE2_115.sv
 - SevenHexDecoder.sv
 - Debounce.sv

System Architecture





Signal and Button Explanation

Button	Signal	Description
None	i_clk	Clock signal
key1	i_RST_N	Reset the machine
key0	i_start	Start the machine
key2	i_stop	Freeze the current result
key3	i_show	Display the last result
None	o_random_out	Output signal

State Transition Explanation

The machine operates with several states. The initial state is **S_IDLE**, and pressing the **key0** (**i_start**) will move it into the **S_FAST** state. The machine goes through different processing states such as **S_FAST**, **S_MEDIUM**, and **S_SLOW**. If **key2** (**i_stop**) is pressed in any of these states, the machine transitions to **S_DONE**, freezing the result. After the result is frozen, pressing **key3** (**i_show**)

will transition the machine to S_SHOW, where the last result is displayed. To start the next operation, pressing key0 will take the machine back to S_FAST.

The machine's state transitions automatically based on the clock cycle counts. These transitions are:

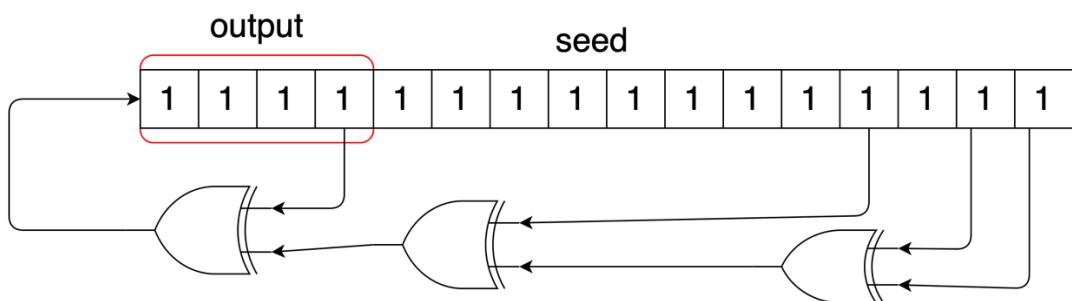
- S_FAST to S_MEDIUM after 2^{25} cycles.
- S_MEDIUM to S_SLOW after 2^{25} cycles.
- S_SLOW to S_DONE after 2^{25} cycles.
- S_SHOW to S_DONE after 2^{24} cycles.

Additionally, pressing key1 (i_rst_n) will reset the machine to the initial state S_IDLE.

Pseudo Random Number Generation Explanaion

We implement the machine by 16-bit XOR LFSR.

- Feedback polynomial is $x^{16}+x^{15}+x^{13}+x^4+1$
- SEED is set to 2^{15} when pressing key1, and it will increase 1 every cycle.
When it equals to 0 it will reset to 2^{15}
- Output the last four bit as the result

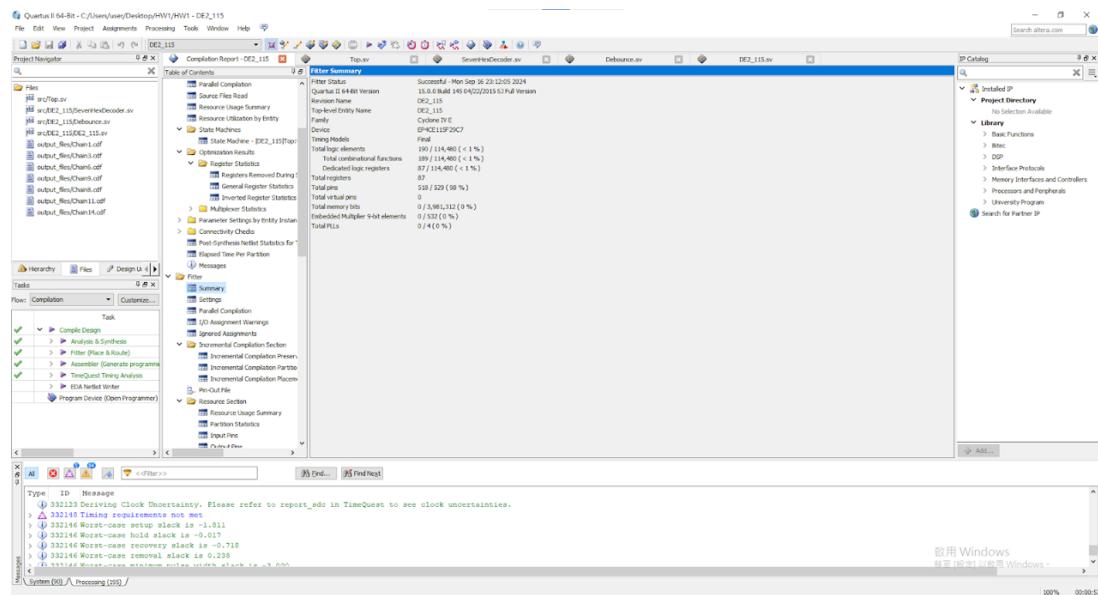


Display Change Rate Explanation

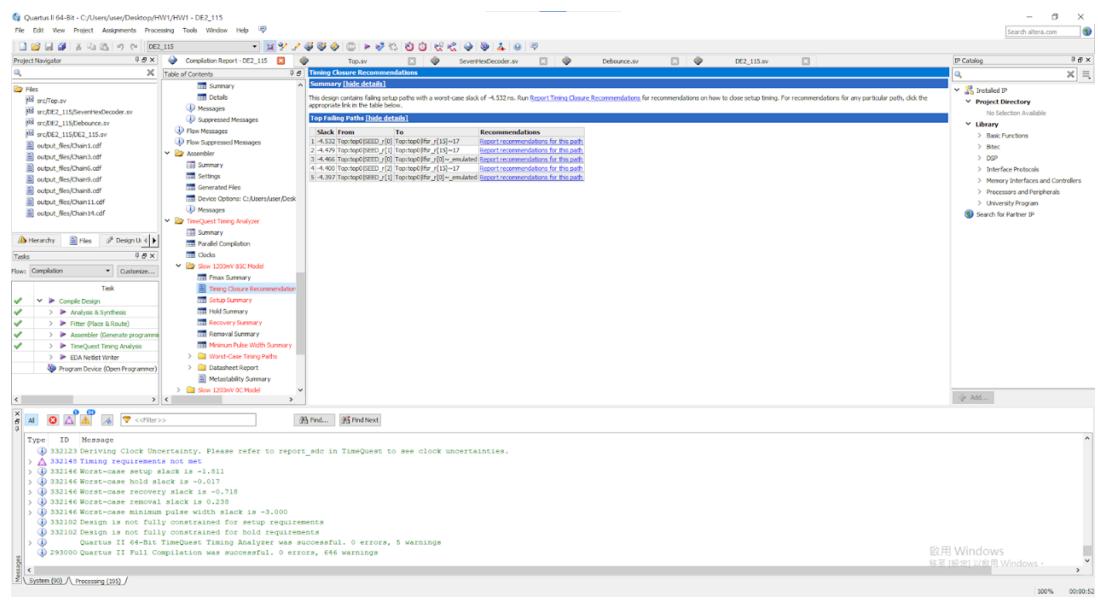
The machine changes its display output at different rates depending on the state it is in:

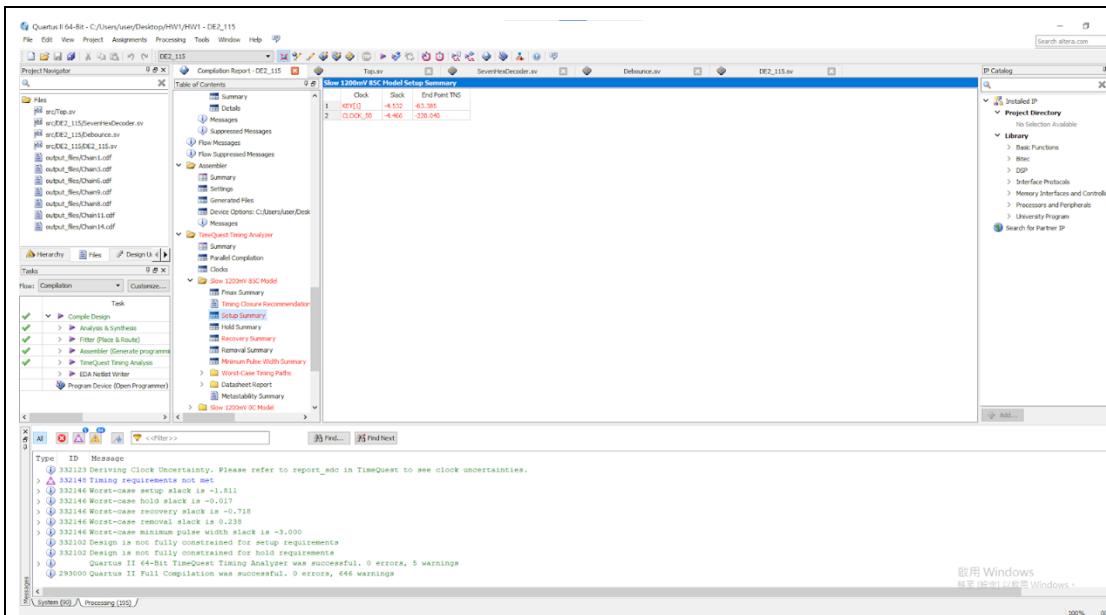
State	Change Period
S_FAST	2^{19} clock cycles
S_MEDIUM	2^{21} clock cycles
S_SLOW	2^{23} clock cycles

fitter analyzer

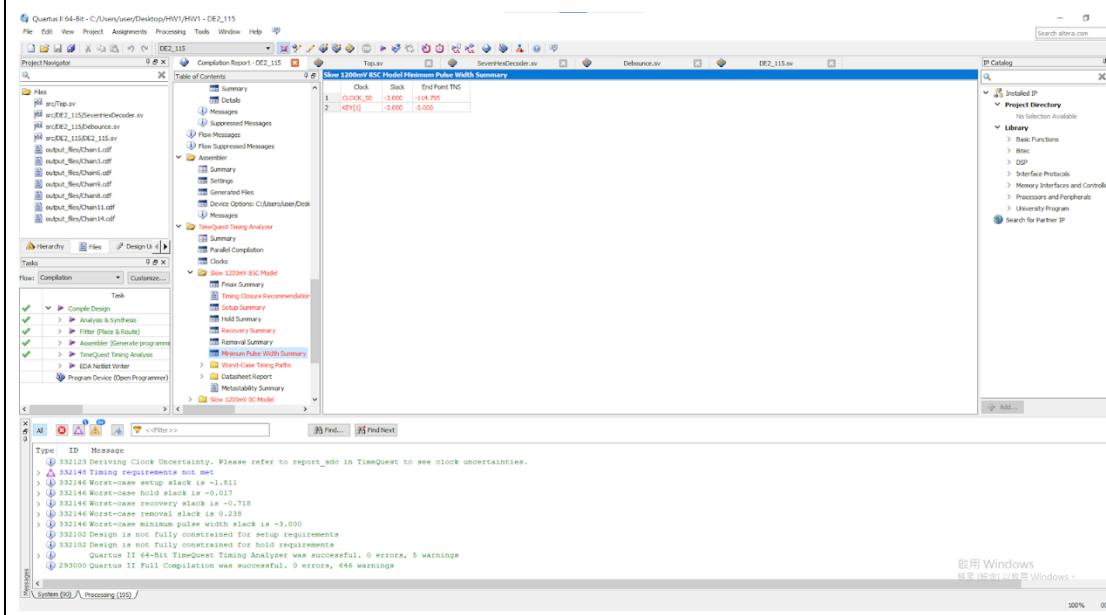


timing analyze





setup clock50



Quartus II 64-Bit - C:/Users/uyue/Desktop/HW1/HW1 - DE2_115

File Edit View Project Assignments Processing Tools Window Help

Project Navigator 0 x Compilation Report - DE2_115 Top.vy SevenBitDecoder.av Debounce.av DE2_115.sv IP Catalog

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Slew 1200Wt I^C Model

Tasks

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How Compilation Customer...

Task

Compile Design

Analysis & Synthesis

Place & Route

Assembler Generate program

TimeQuest Timing Analysis

EDA Netlist Writer

Program Device (Open Program)

Hierarchy Files Design Up

Worst Case Timing Paths

Task

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File Design Up

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Type ID Message

332123 Deriving Clock Uncertainty. Please refer to report_adc in TimeQuest to see clock uncertainties.

332146 Timing requirements not met

332146 Worst-case setup slack is -1.011

332146 Worst-case hold slack is -0.17

332146 Worst-case recovery slack is -0.718

332146 Worst-case removal slack is 0.238

332146 Worst-case minimum pulse width slack is -3.000

332102 Design is not fully constrained for setup requirements

332102 Design is not fully constrained for hold requirements

Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 5 warnings

293000 Quartus II Full Compilation was successful. 0 errors, 446 warnings

Messages

System (65) Processing (195) /

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Project Navigator 0 x Compilation Report - DE2_115 Top.vy SevenBitDecoder.av Debounce.av DE2_115.sv IP Catalog

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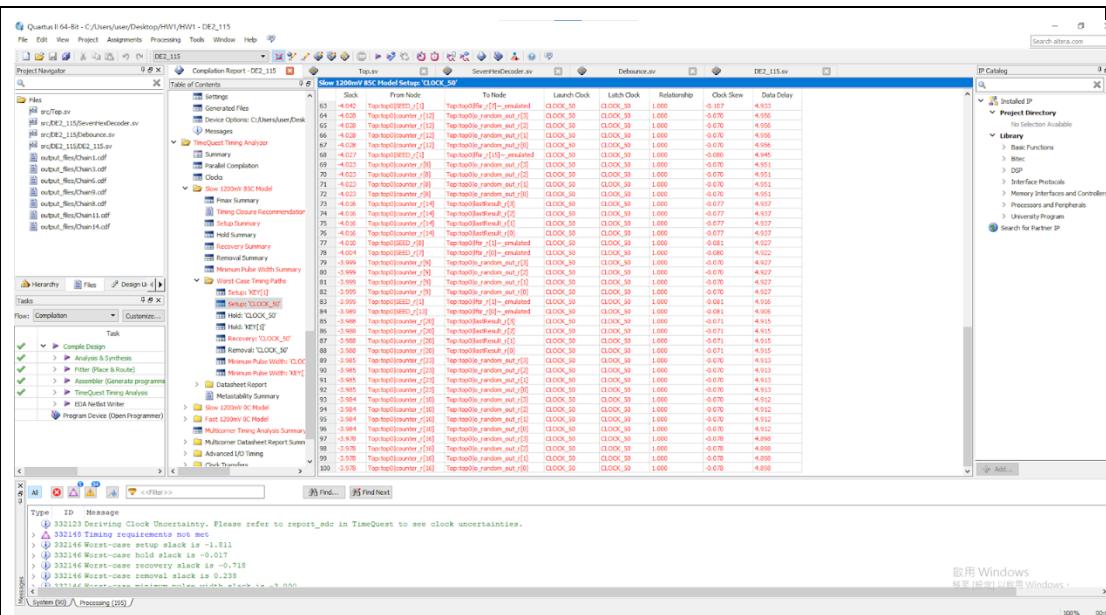
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Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 5 warnings

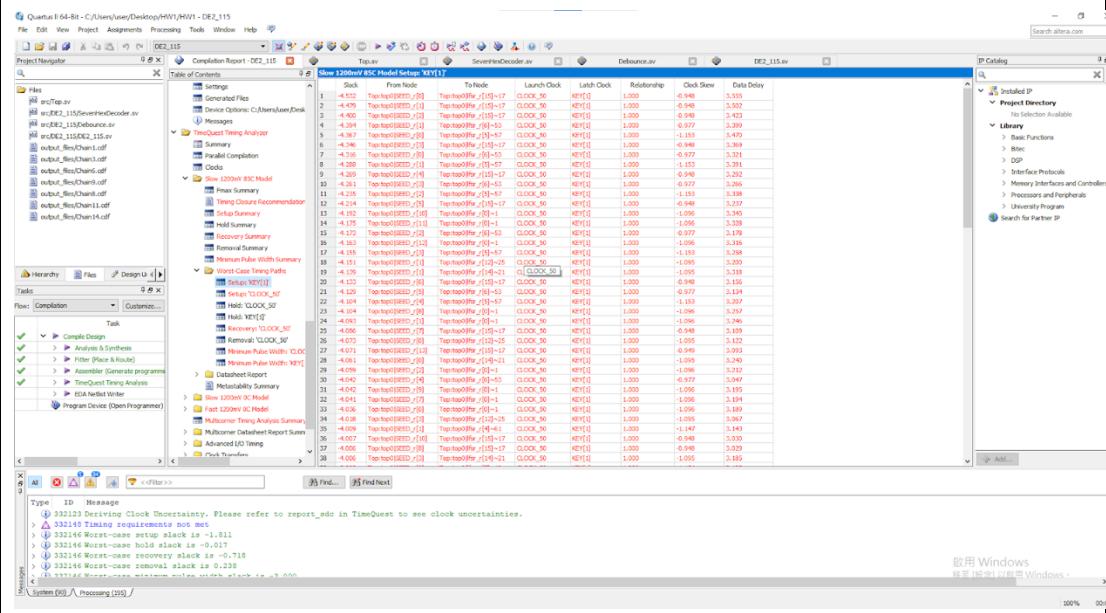
293000 Quartus II Full Compilation was successful. 0 errors, 446 warnings

Messages

System (65) Processing (195) /



setup key[1]



minimum pulse width clock50

The screenshot displays two instances of the Quartus II software interface, each showing the 'TimeQuest Timing Analyzer' report for the project 'DE2_115'. The left window provides a detailed view of the timing constraints, while the right window offers a more summarized overview. Both windows include a 'Messages' panel at the bottom, which contains several warning messages related to clock requirements and setup/hold times.

Left Window (Detailed View):

Constraint ID	Type	Source	Destination	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
37	Setup	From Node	To Node	NET[0]	NET[0]	1.000	-0.948	3.029
38	-4.056	Top.toplevel[1]-9	Top.toplevel[1]-17	QCLK[50]	NET[0]	1.000	-1.095	3.185
39	3.958	Top.toplevel[1]-9	Top.toplevel[1]-17	QCLK[50]	NET[0]	1.000	-0.948	3.125
40	3.958	Top.toplevel[1]-9	Top.toplevel[1]-17	QCLK[50]	NET[0]	1.000	-0.948	3.069
41	-3.930	Top.toplevel[1]-9	Top.toplevel[1]-17	QCLK[50]	NET[0]	1.000	-0.948	2.993
42	-3.965	Top.toplevel[1]-9	Top.toplevel[1]-17	QCLK[50]	NET[0]	1.000	-1.154	3.092
43	3.965	Top.toplevel[1]-9	Top.toplevel[1]-17	QCLK[50]	NET[0]	1.000	-0.948	3.075
44	-3.511	Top.toplevel[1]-9	Top.toplevel[1]-17	QCLK[50]	NET[0]	1.000	-1.147	3.065
45	3.500	Top.toplevel[1]-9	Top.toplevel[1]-25	QCLK[50]	NET[0]	1.000	-0.995	2.979
46	3.500	Top.toplevel[1]-9	Top.toplevel[1]-25	QCLK[50]	NET[0]	1.000	-0.995	2.907
47	-3.912	Top.toplevel[1]-9	Top.toplevel[1]-25	QCLK[50]	NET[0]	1.000	-0.973	3.049
48	-3.886	Top.toplevel[1]-9	Top.toplevel[1]-25	QCLK[50]	NET[0]	1.000	-1.095	2.935
49	3.886	Top.toplevel[1]-9	Top.toplevel[1]-25	QCLK[50]	NET[0]	1.000	-0.948	2.935
50	3.874	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-1.095	3.031
51	-3.874	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-1.095	3.031
52	3.840	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-1.095	3.027
53	-3.840	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-1.095	2.962
54	3.886	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-0.948	2.988
55	-3.848	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-1.095	3.031
56	3.848	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-0.948	2.977
57	-3.842	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-1.095	2.977
58	3.840	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.918	3.030
59	-3.840	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.918	3.030
60	3.840	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.948	3.031
61	-3.832	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-1.154	2.959
62	3.832	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.948	2.966
63	-3.832	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-1.095	2.988
64	-3.792	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.918	2.982
65	3.792	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.918	2.982
66	-3.792	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-1.095	2.982
67	3.792	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-1.095	2.966
68	-3.792	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-0.918	2.937
69	3.792	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-0.948	2.971
70	-3.792	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-1.095	2.980
71	-3.792	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-1.095	2.867
72	3.792	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-1.095	2.867
73	-3.792	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-1.095	2.905
74	3.792	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-0.948	2.985
75	-3.792	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-1.095	2.985
76	3.792	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-0.948	2.922
77	-3.792	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-1.095	2.922
78	3.792	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.918	2.898
79	-3.792	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.918	2.898
80	3.792	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.948	2.899
81	-3.691	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.973	2.849
82	3.672	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-1.095	2.771
83	-3.660	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-1.095	2.839
84	3.660	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.918	2.839
85	-3.698	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.948	2.852
86	-3.647	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.973	2.855
87	3.647	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-1.095	2.855
88	-3.632	Top.toplevel[1]-9	Top.toplevel[1]-37	QCLK[50]	NET[0]	1.000	-0.918	2.837
89	3.632	Top.toplevel[1]-9	Top.toplevel[1]-37	QCLK[50]	NET[0]	1.000	-0.918	2.792
90	-3.632	Top.toplevel[1]-9	Top.toplevel[1]-37	QCLK[50]	NET[0]	1.000	-1.095	2.792
91	-3.667	Top.toplevel[1]-9	Top.toplevel[1]-41	QCLK[50]	NET[0]	1.000	-1.242	2.639
92	-3.599	Top.toplevel[1]-9	Top.toplevel[1]-41	QCLK[50]	NET[0]	1.000	-1.154	2.802
93	3.599	Top.toplevel[1]-9	Top.toplevel[1]-41	QCLK[50]	NET[0]	1.000	-1.154	2.795
94	-3.598	Top.toplevel[1]-9	Top.toplevel[1]-41	QCLK[50]	NET[0]	1.000	-1.242	2.642
95	-3.598	Top.toplevel[1]-9	Top.toplevel[1]-41	QCLK[50]	NET[0]	1.000	-1.242	2.642
96	-3.514	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.918	2.768
97	3.514	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.918	2.768
98	-3.572	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-1.095	2.715
99	3.560	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.973	2.715
100	-3.541	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-1.097	2.693

Right Window (Summary):

Constraint ID	Type	Source	Destination	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
64	Setup	From Node	To Node	NET[0]	NET[0]	1.000	-0.948	2.848
65	-4.056	Top.toplevel[1]-9	Top.toplevel[1]-17	QCLK[50]	NET[0]	1.000	-1.095	3.029
66	3.788	Top.toplevel[1]-9	Top.toplevel[1]-41	QCLK[50]	NET[0]	1.000	-1.147	2.985
67	-3.792	Top.toplevel[1]-9	Top.toplevel[1]-41	QCLK[50]	NET[0]	1.000	-1.095	2.985
68	3.792	Top.toplevel[1]-9	Top.toplevel[1]-17	QCLK[50]	NET[0]	1.000	-0.948	2.937
69	-3.792	Top.toplevel[1]-9	Top.toplevel[1]-17	QCLK[50]	NET[0]	1.000	-1.095	2.937
70	3.792	Top.toplevel[1]-9	Top.toplevel[1]-25	QCLK[50]	NET[0]	1.000	-0.948	2.867
71	-3.792	Top.toplevel[1]-9	Top.toplevel[1]-25	QCLK[50]	NET[0]	1.000	-1.095	2.867
72	3.792	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-0.948	2.905
73	-3.792	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-1.095	2.905
74	3.792	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-0.948	2.905
75	-3.792	Top.toplevel[1]-9	Top.toplevel[1]-21	QCLK[50]	NET[0]	1.000	-1.095	2.905
76	3.792	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.918	2.899
77	-3.792	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.918	2.899
78	3.792	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.948	2.899
79	-3.792	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-1.095	2.899
80	3.792	Top.toplevel[1]-9	Top.toplevel[1]-33	QCLK[50]	NET[0]	1.000	-0.948	2.899
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88	-3.632	Top.toplevel[1]-9	Top.toplevel[1]-37	QCLK[50]	NET[0]	1.000	-0.918	2.837
89	3.632	Top.toplevel[1]-9	Top.toplevel[1]-37	QCLK[50]	NET[0]	1.000	-0.918	2.792
90	-3.632	Top.toplevel[1]-9	Top.toplevel[1]-37	QCLK[50]	NET[0]	1.000	-1.095	2.792
91	-3.667	Top.toplevel[1]-9	Top.toplevel[1]-41	QCLK[50]	NET[0]	1.000	-1.242	2.639
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100	-3.541	Top.toplevel[1]-9	Top.toplevel[1]-37	QCLK[50]	NET[0]	1.000	-1.097	2.693

Quantum II 64-Bit - C:/Users/user/Desktop/HW1/HW1 - DE2_115

File Edit View Project Assignments Processing Tools Window Help

Project Navigator 0 x Compilation Report - DE2_115 Top.vr SevenBitDecoder.av Debounce.av DE2_115.vr IP Catalog

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TimeQuest Timing Analyzer

- Summary Parallel Completion Clocks
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- Timing Closure Recommender
- Setup Summary
- Hold Summary
- Recovery Summary
- Removal Summary
- Minimum Pulse Width Summary
- Worst Case Timing Paths
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- DataSheet Report
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- Fast 1200W IC Model
- Multicorner Timing Analysis Summary
- Multicorner Datedsheet Report Summary
- Advanced I/O Timing
- Clock Transfers

Hierarchy Files Design Use Task

Compilation Customized...

All O P F Find... Find Next

Type ID Message

- 332123 Deriving Clock Uncertainty. Please refer to report_mdo in TimeQuest to see clock uncertainties.
- > 332146 Timing requirements not met.
- > 332146 Worst-case setup slack is -1.011
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- > 332146 Worst-case recovery slack is -0.718
- > 332146 Worst-case removal slack is 0.238
- < 332146 Worst-case minimum pulse width slack is -1.000

System (65) Processing (199)

啟用 Windows

Quantum II 64-Bit - C:/Users/user/Desktop/HW1/HW1 - DE2_115

File Edit View Project Assignments Processing Tools Window Help

Project Navigator 0 x Compilation Report - DE2_115 Top.vr SevenBitDecoder.av Debounce.av DE2_115.vr IP Catalog

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Compilation Customized...

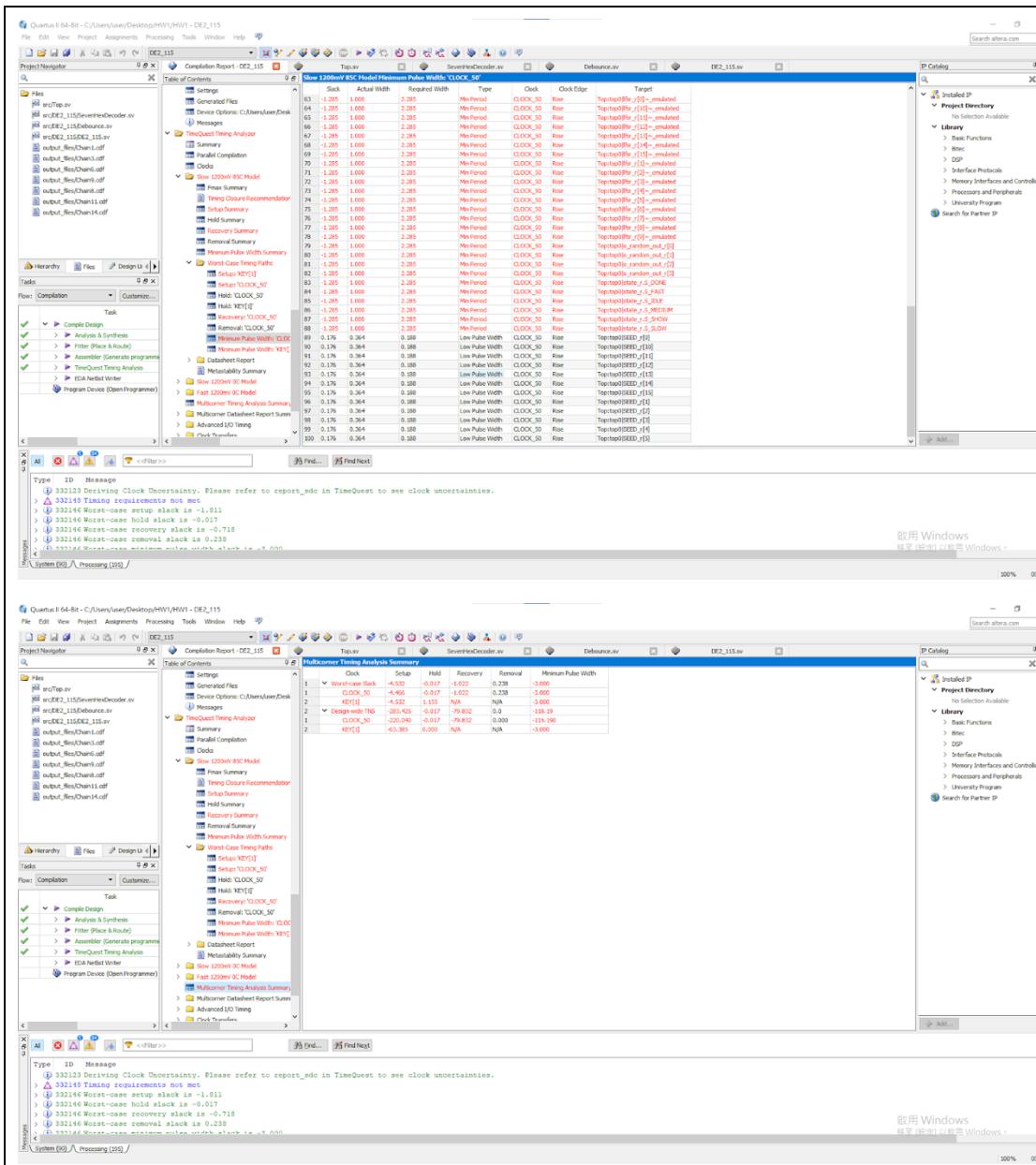
All O P F Find... Find Next

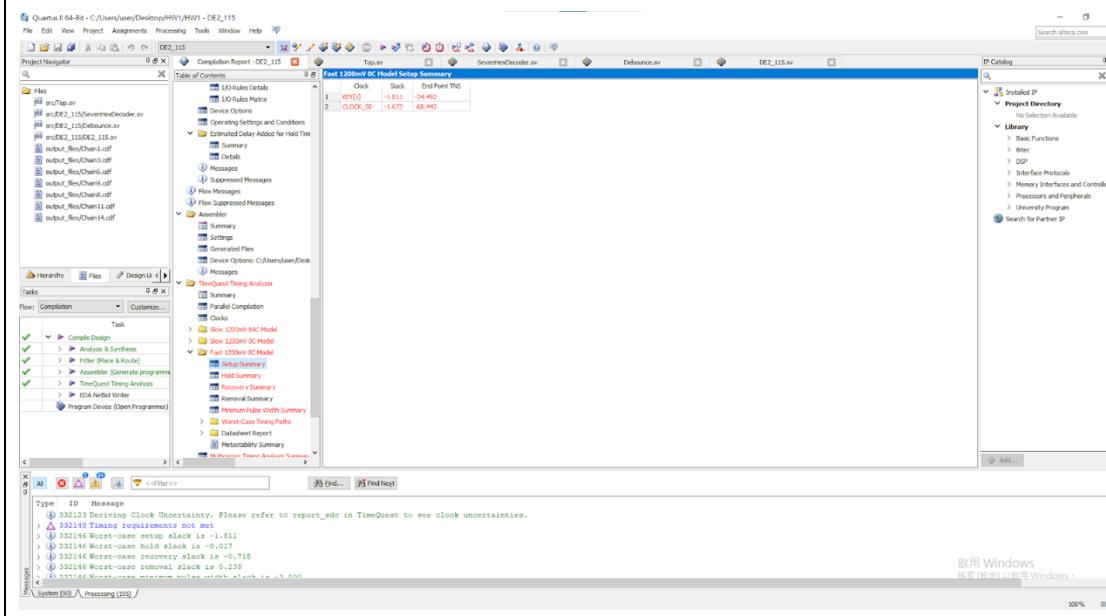
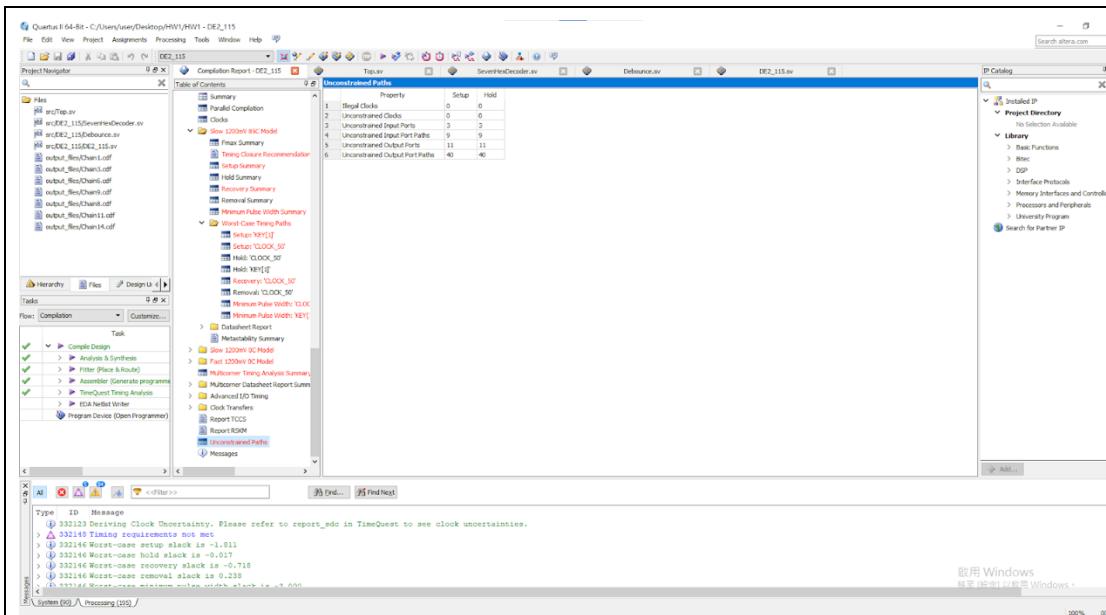
Type ID Message

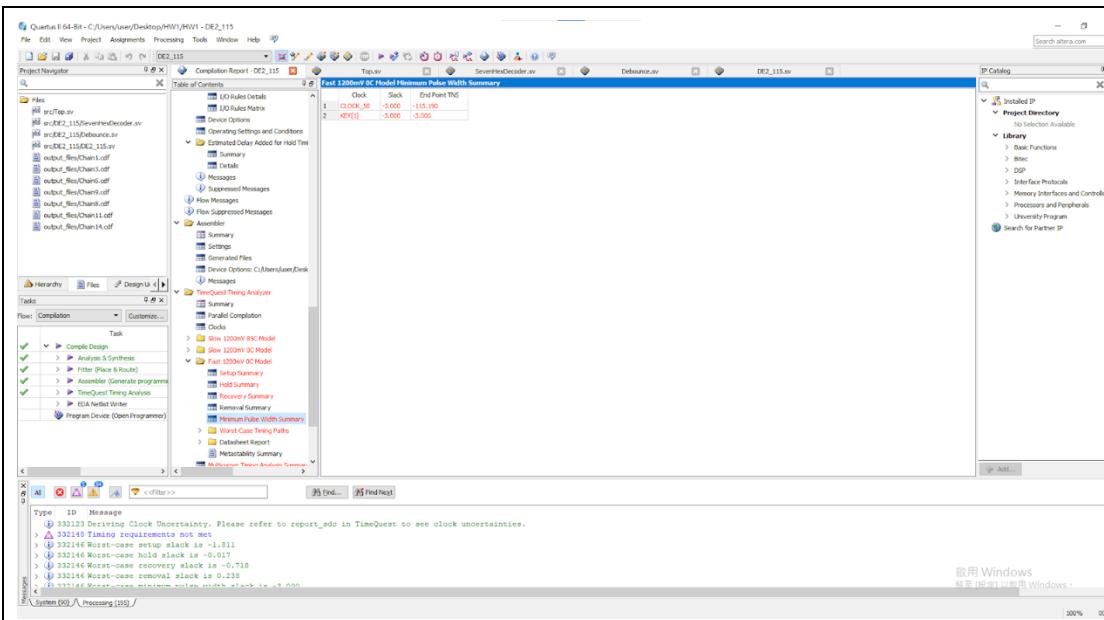
- 332123 Deriving Clock Uncertainty. Please refer to report_mdo in TimeQuest to see clock uncertainties.
- > 332146 Timing requirements not met.
- > 332146 Worst-case setup slack is -1.011
- > 332146 Worst-case hold slack is 0.017
- > 332146 Worst-case recovery slack is -0.718
- > 332146 Worst-case removal slack is 0.238
- < 332146 Worst-case minimum pulse width slack is -1.000

System (65) Processing (199)

啟用 Windows







問題解決

時間長度不合適

因為一開始沒有抓好 **clock timing**，因此一開始以為有
bug，把很多正確邏輯改的很怪，但是後來調整到一個適
合的時間後，七段顯示器看起來就正常多了

心得

這是第一次用 **FPGA**，真的是非常難用，原本寫好 **verilog**
以為寫好就直接燒上去就很 **arduino** 一樣簡單，沒想到還
是出了一堆 bug