Verilog Simulation & Debugging Tools

數位電路實驗

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Outline

- VCS
- nWave
- Verdi

VCS

Introduction to VCS

- The Synopsys VCS® functional verification solution is a Verilog digital logic simulator.
- We can use VCS to
  - Compiles the Verilog source files.
  - Elaborates the design and generates a simulation snapshot.
  - Simulates the snapshot.

Before Using VCS

- Source the environment settings of CAD tools.

  > source /usr/cad/synopsys/CIC/vcs.cshrc

- If you try entering the command “vcs" but it turns out "command not found," it means there's something wrong with the "*.cshrc" file or the software license is out of date.

Running VCS (1/3)

- Run the Verilog simulation:

```
vcs -full64 -R +v2k ./Lab0_alu_tb.v ./Lab0_alu.v –debug_access+all \
-P /usr/cad/synopsys/verdi/cur/share/PLI/VCS/LINUX64/novas.tab \
/usr/cad/synopsys/verdi/cur/share/PLI/VCS/LINUX64/pli.a
```

- Another choice of running Verilog simulation:

```
vcs -full64 -R -f Lab0_alu_file.f
```

In Lab0_alu_file.f

```
1  +v2k
2  -debug_access+all
3  -P /usr/cad/synopsys/v
4  /usr/cad/synopsys/verd
5
6  Lab0_alu_tb.v
7  Lab0_alu.v
```

Running VCS (2/3)

- For Verilog-2001 support, add
  - +v2k
- For SystemVerilog support, add
  - -sverilog

Running VCS (3/3)

Waveform dumping example for testbench

```
initial begin
    $fsdbDumpfile("exp2_rsa.fsdb");
    $fsdbDumpvars;
end
```

or

```
initial begin
    $dumpfile("exp2_rsa.vcd");
    $dumpvars;
end
```

- *.fsdb has smaller file size than *.vcd. But $fsdbDumpfile cannot work without sourcing verdi.cshrc.

  > source /usr/cad/synopsys/CIC/verdi.cshrc

Simulation Results

- Check the simulation result to see if the Verilog design is finished correctly.

```
*Verdi* : Create FSDB file 'alu.fsdb'
*Verdi* : Begin traversing the scope (test_alu), layer (0).
*Verdi* : Enable +mda and +parameter dumping.
*Verdi* : End of traversing.

Congratulations!! Your Verilog Code is correct!!

$finish called from file "./Lab0_alu_tb.v", line 314.
$finish at simulation time             26214620
           V C S   S i m u l a t i o n   R e p o r t
Time: 2621462000 ps
CPU Time:      2.010 seconds;       Data structure size:   0.0Mb
Thu Sep  7 14:20:26 2023
```

nWave

Introduction to nWave

- nWave is one of the best waveform (*.vcd or *.fsdb) viewer.
- We can debug easily by checking the waveform file dumped during simulation.

Before Using nWave

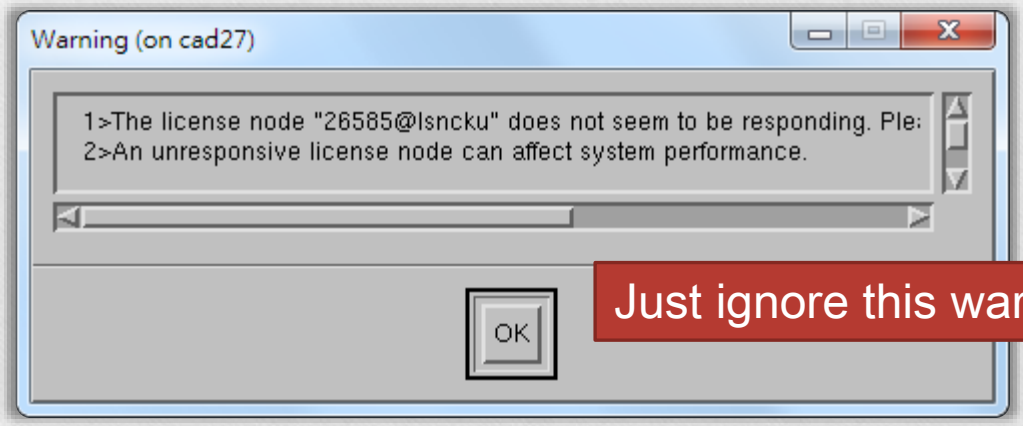
- Source the environment settings of CAD tools.
  - > source /usr/cad/synopsys/CIC/license.csh
  - > source /usr/spring_soft/CIC/verdi.cshrc

Start nWave

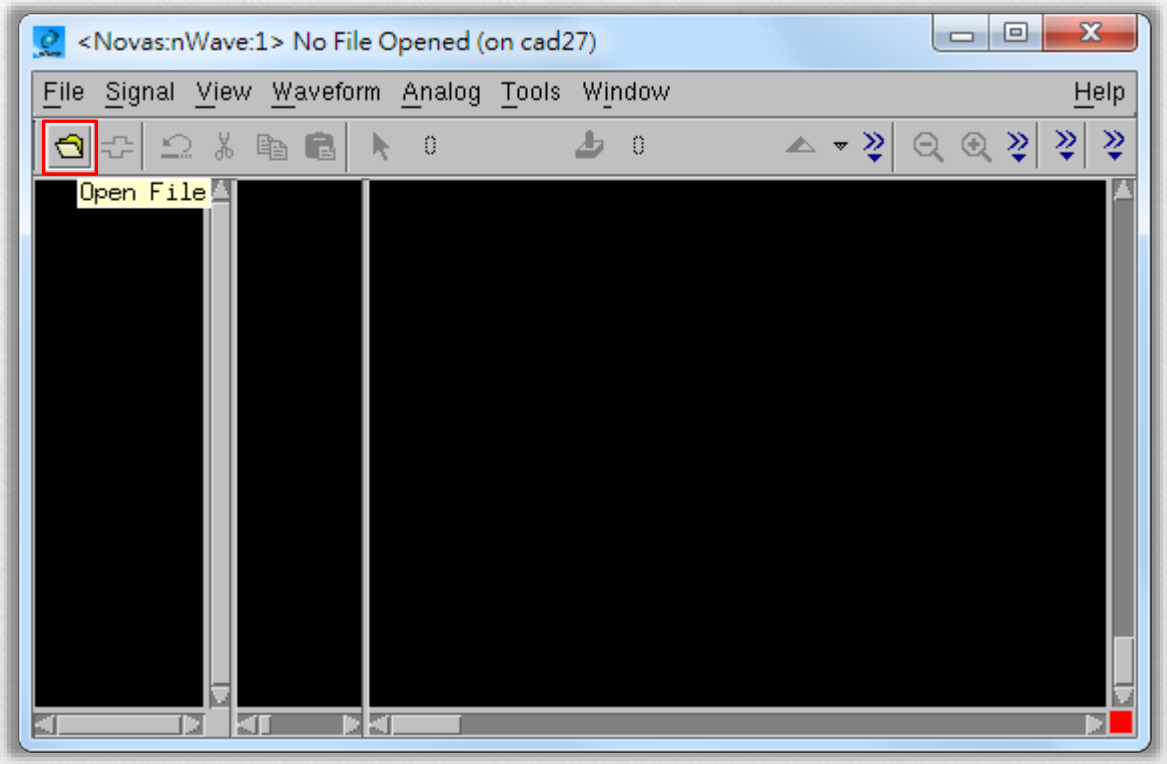
- Type the following command:

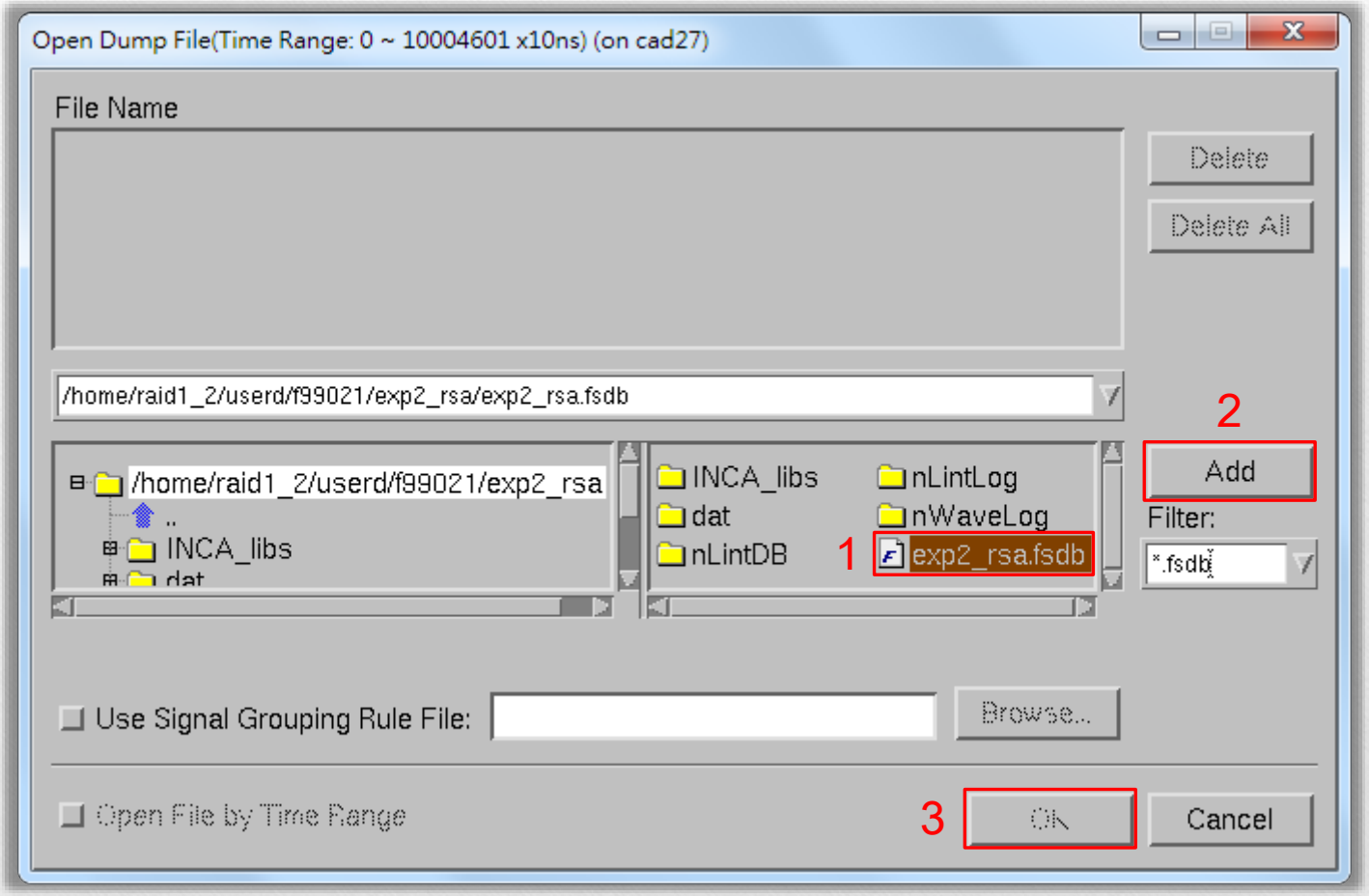
```
nWave &
```

  - Also, the token "&" enable you to use the terminal while Verdi is running in the background.

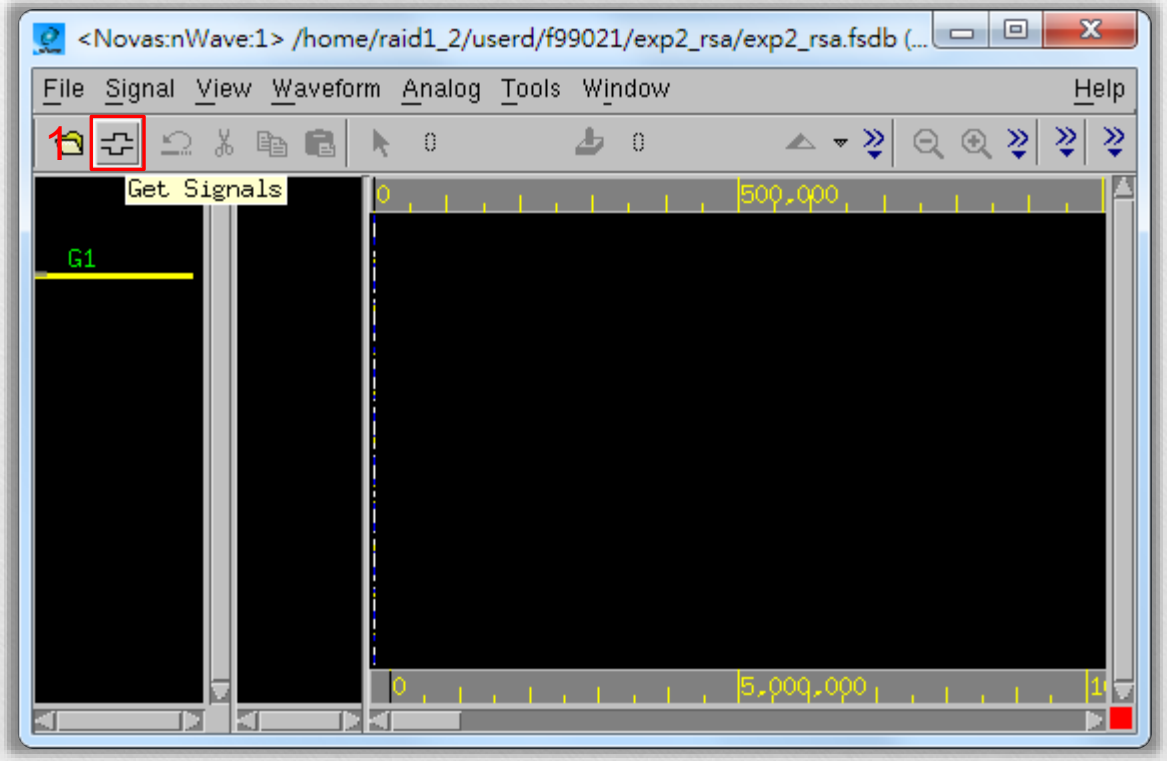


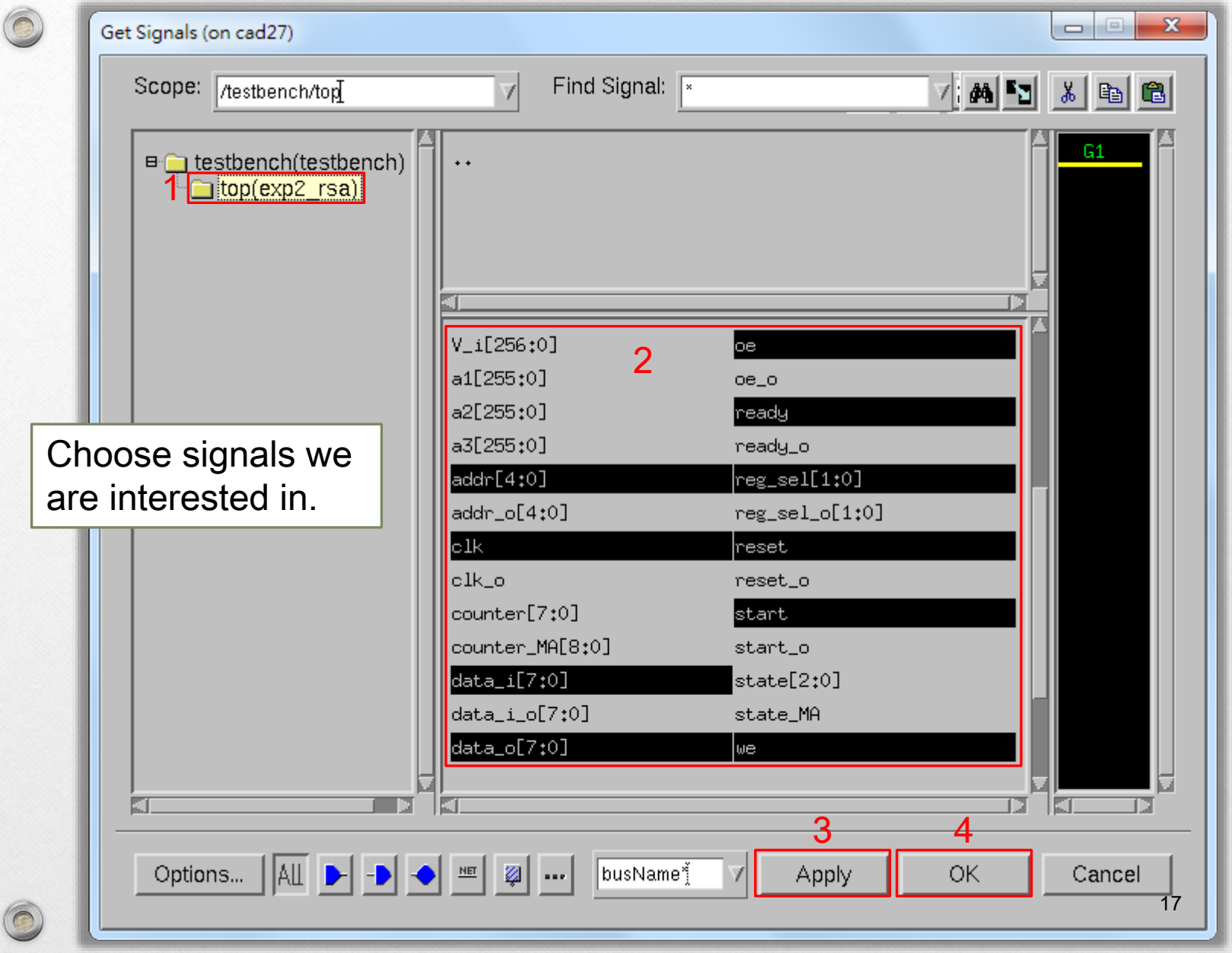
Open the FSDB File




Open Dump File(Time Range: 0 ~ 10004601 x10ns) (on cad27)
File Name
Delete
Delete All
/home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.fsdb
2
/home/raid1_2/userd/f99021/exp2_rsa
..
INCA_libs
dat
INCA_libs
dat
nLintDB
nLintLog
nWaveLog
1
exp2_rsa.fsdb
Add
Filter:
*.fsdb
Use Signal Grouping Rule File:
Browse...
Open File by Time Range
3
OK
Cancel

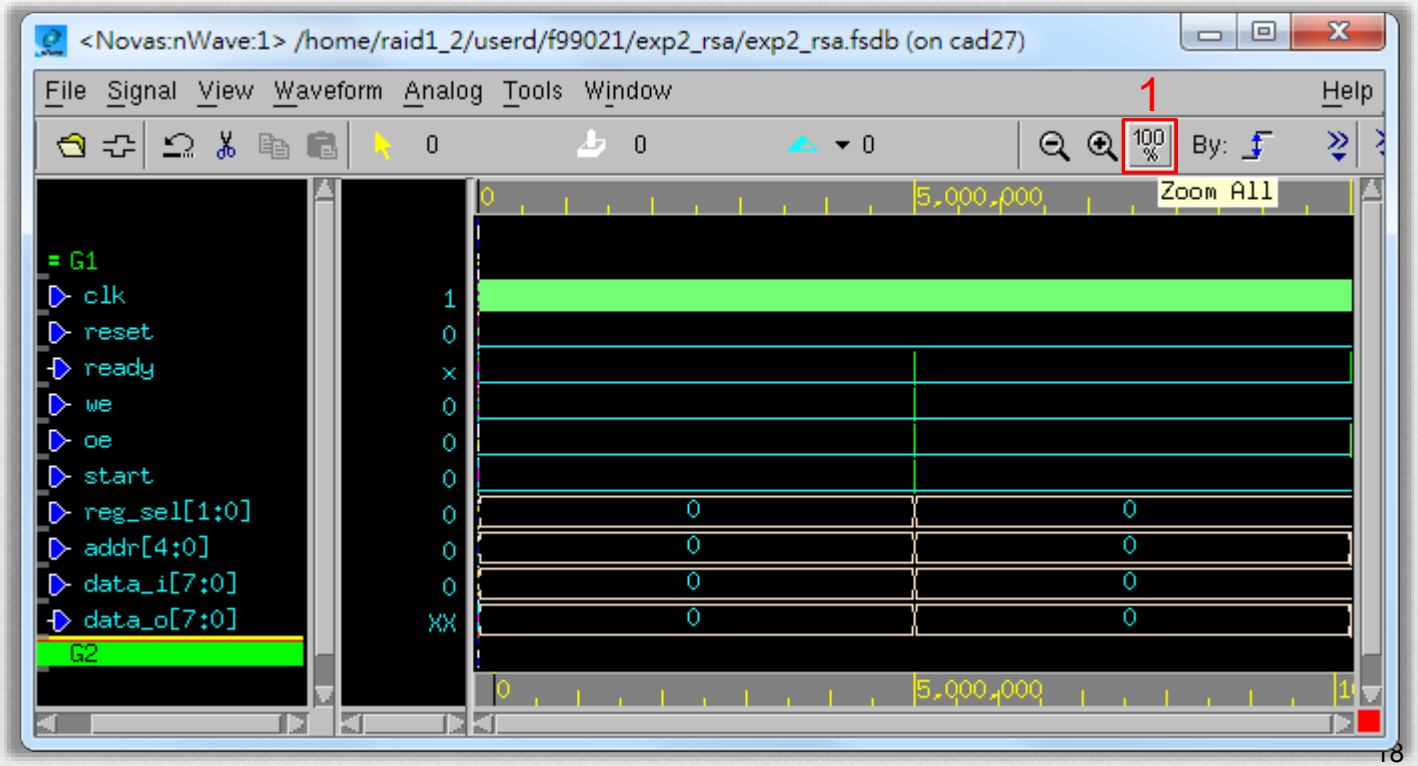
Choose Signals



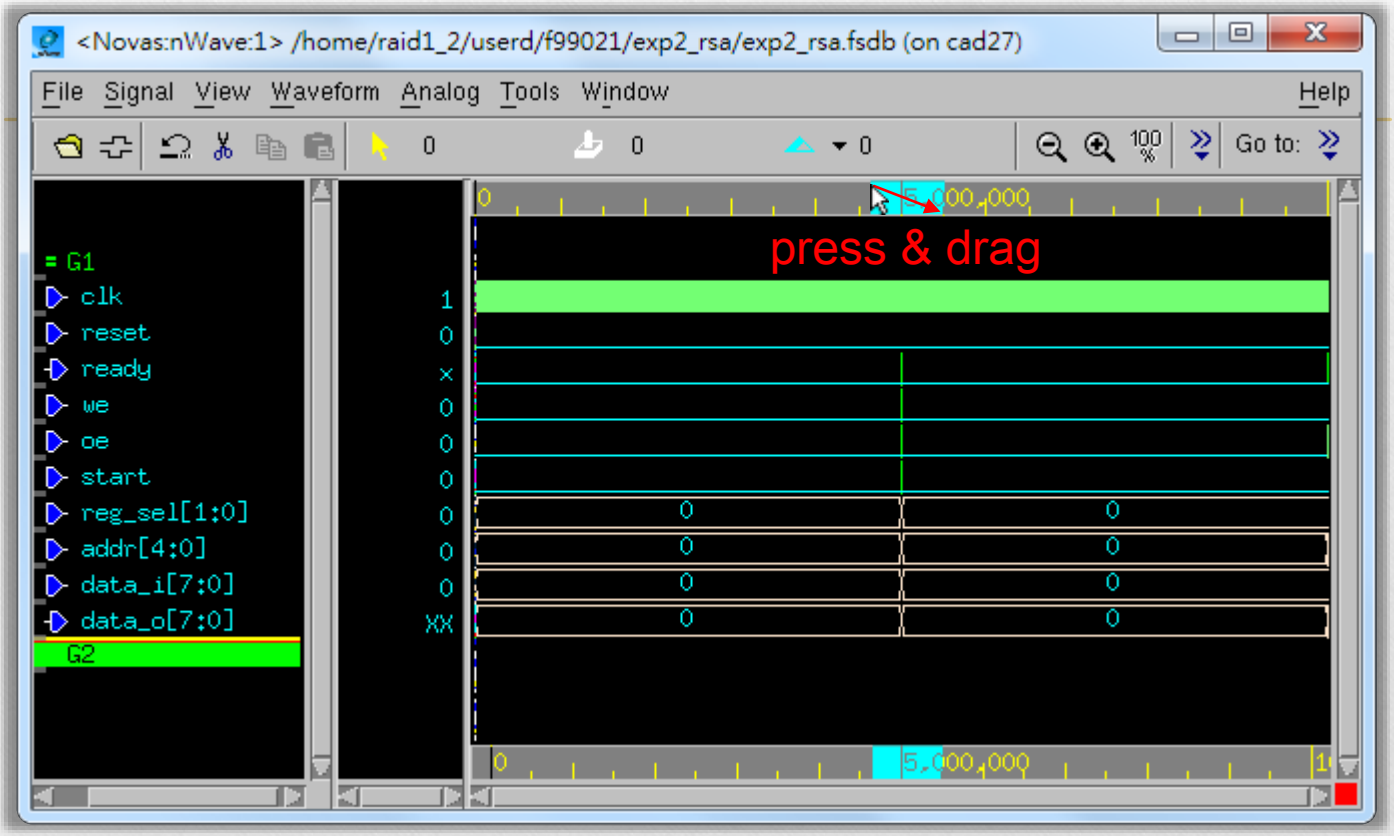


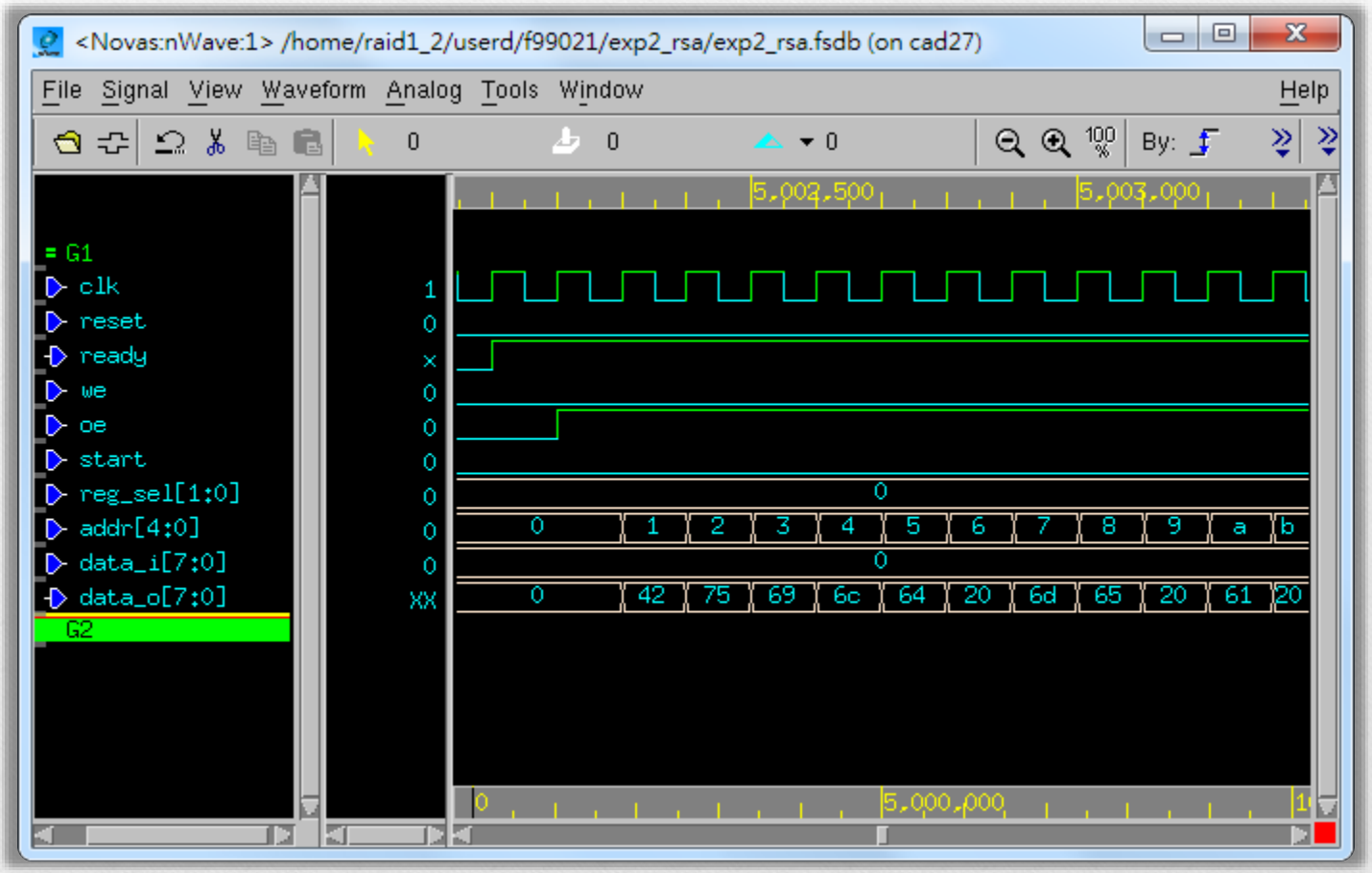
Choose signals we are interested in.

Browse the Whole Waveform

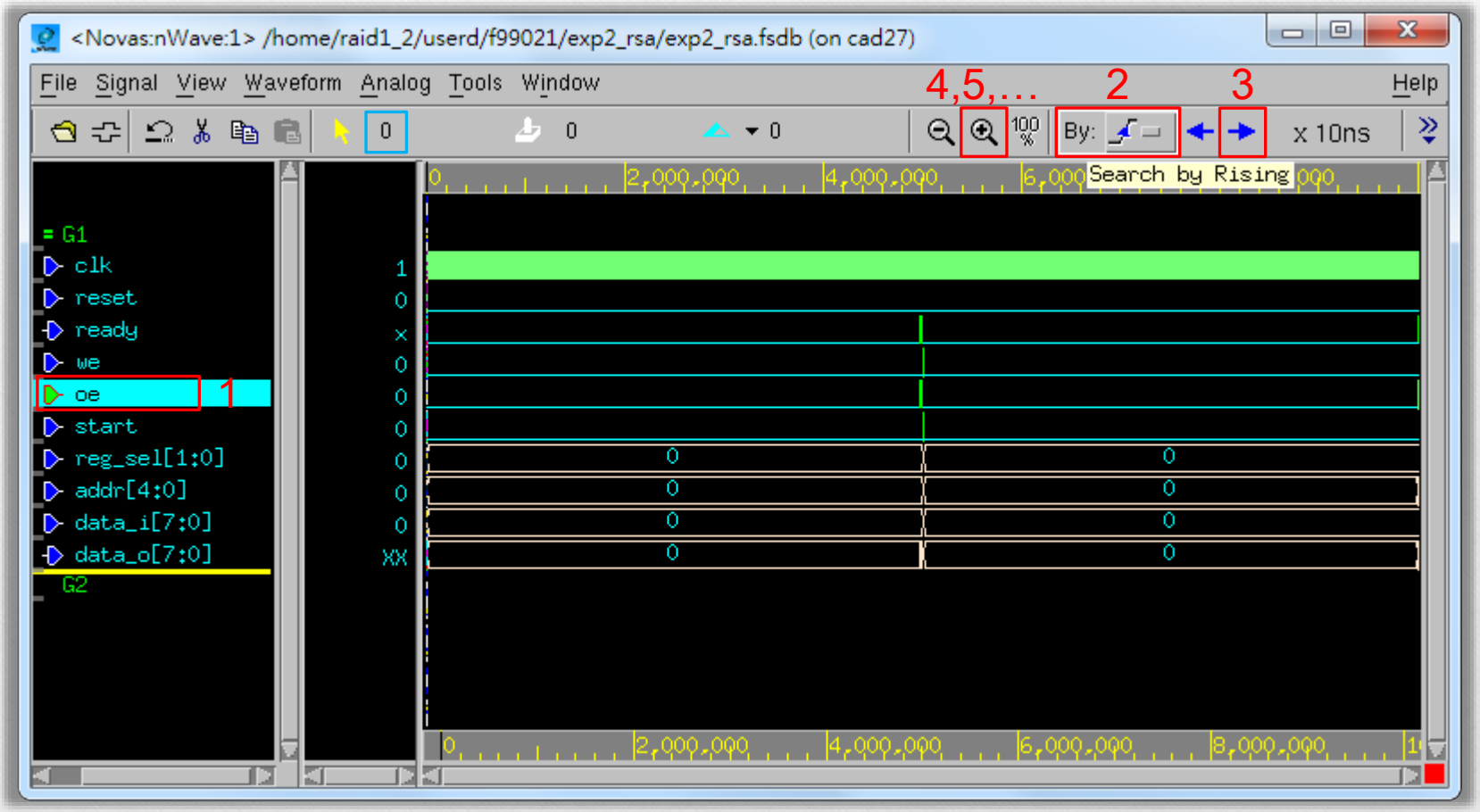


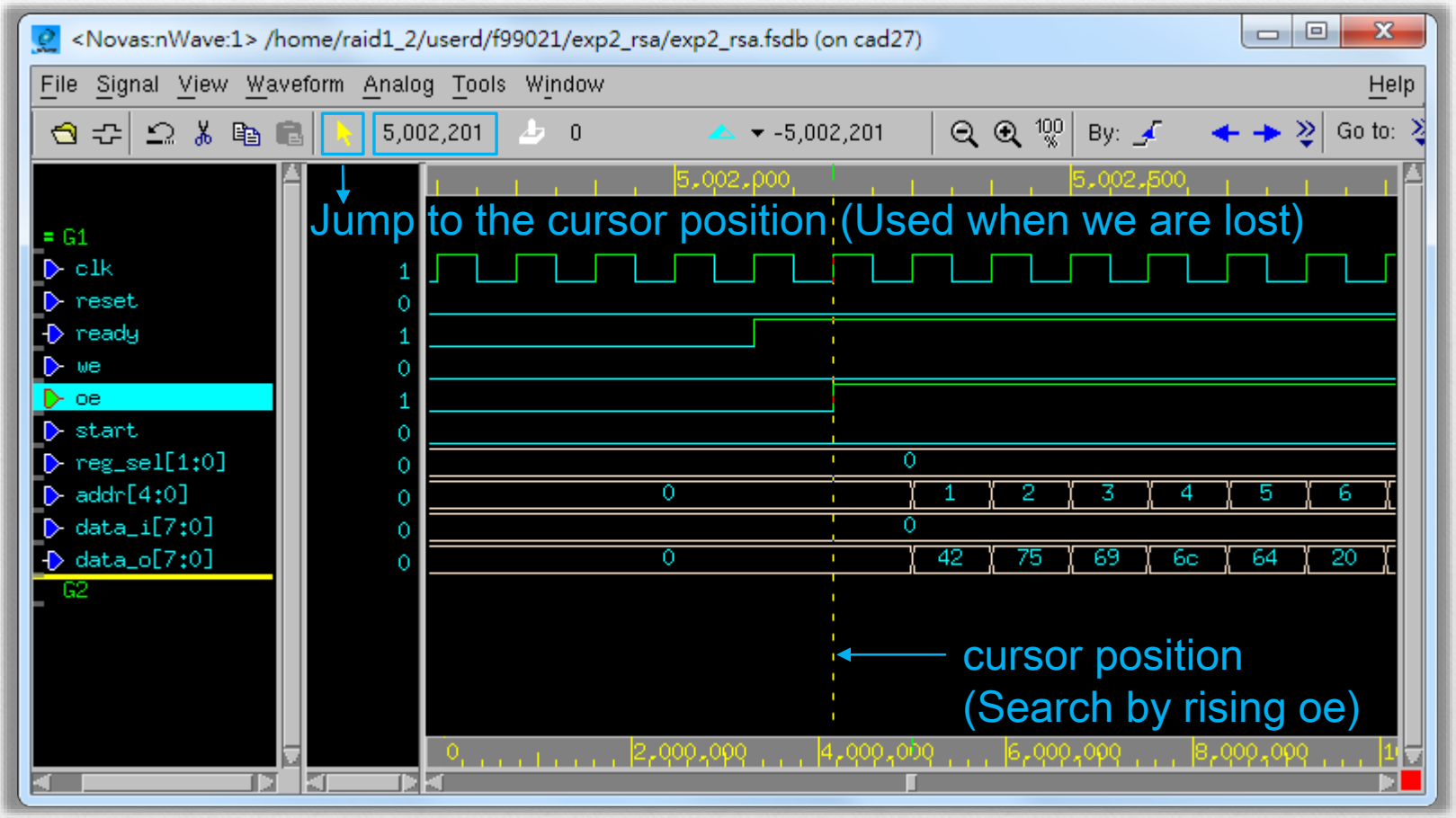
Browse the Specified Interval



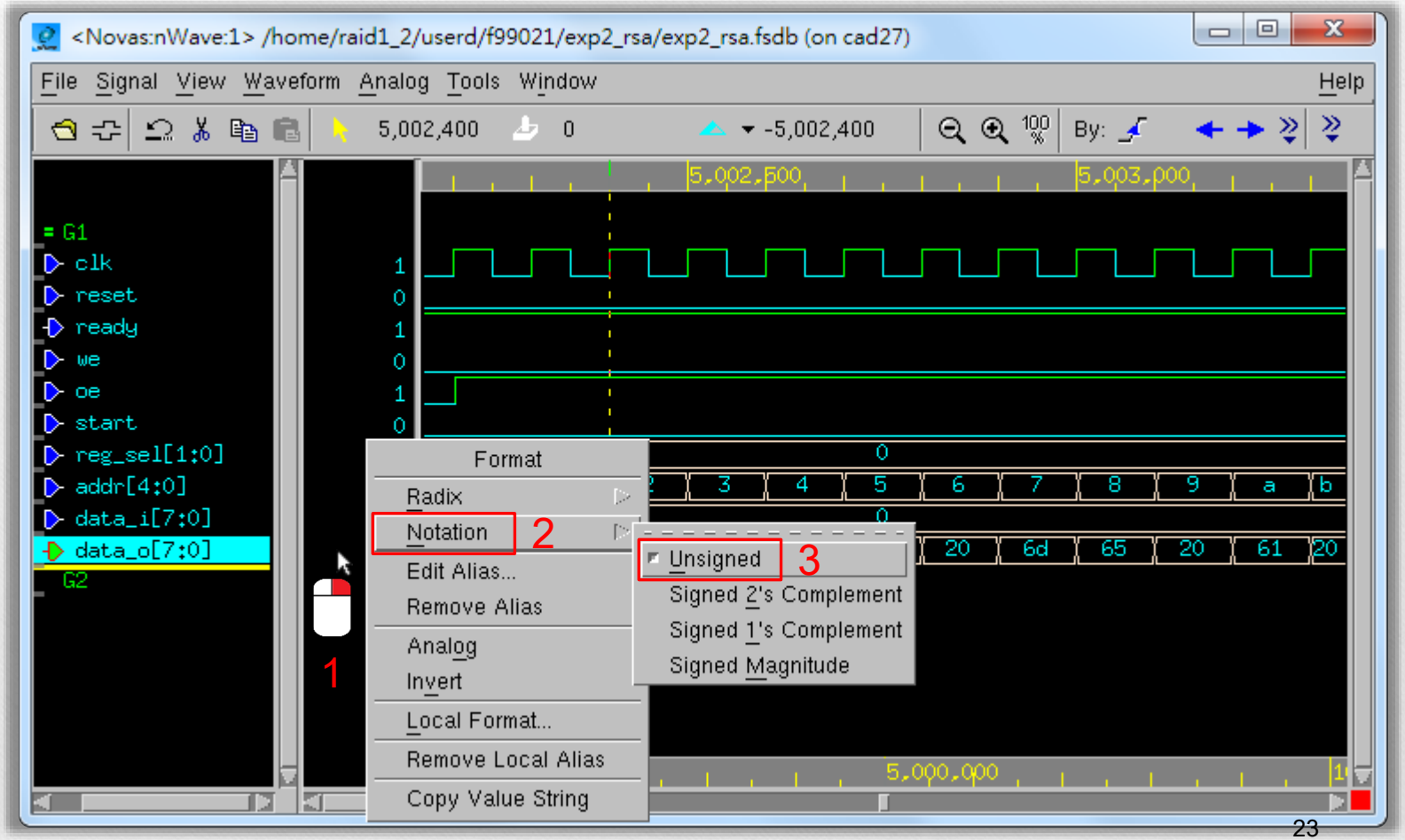

<Novas:nWave:1> /home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.fsdb (on cad27)
File Signal View Waveform Analog Tools Window Help
By:
5,002,500
5,003,000
G1
clk
reset
ready
we
oe
start
reg_sel[1:0]
addr[4:0]
data_i[7:0]
data_o[7:0]
G2
1
0
x
0
0
0
0
0
0
XX
0 1 2 3 4 5 6 7 8 9 a b
0
0 42 75 69 6c 64 20 6d 65 20 61 20
0
5,000,000

Search for Specified Signal

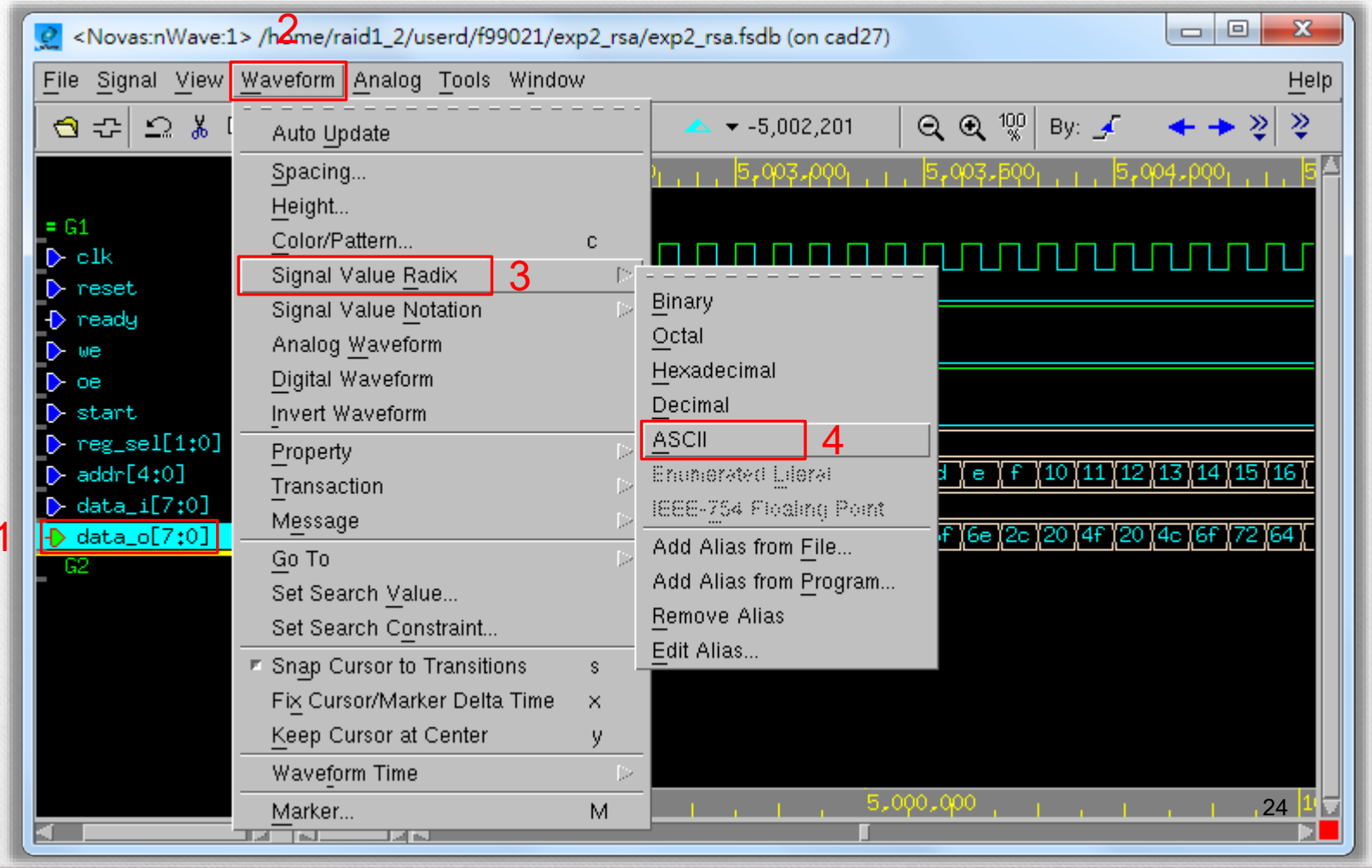


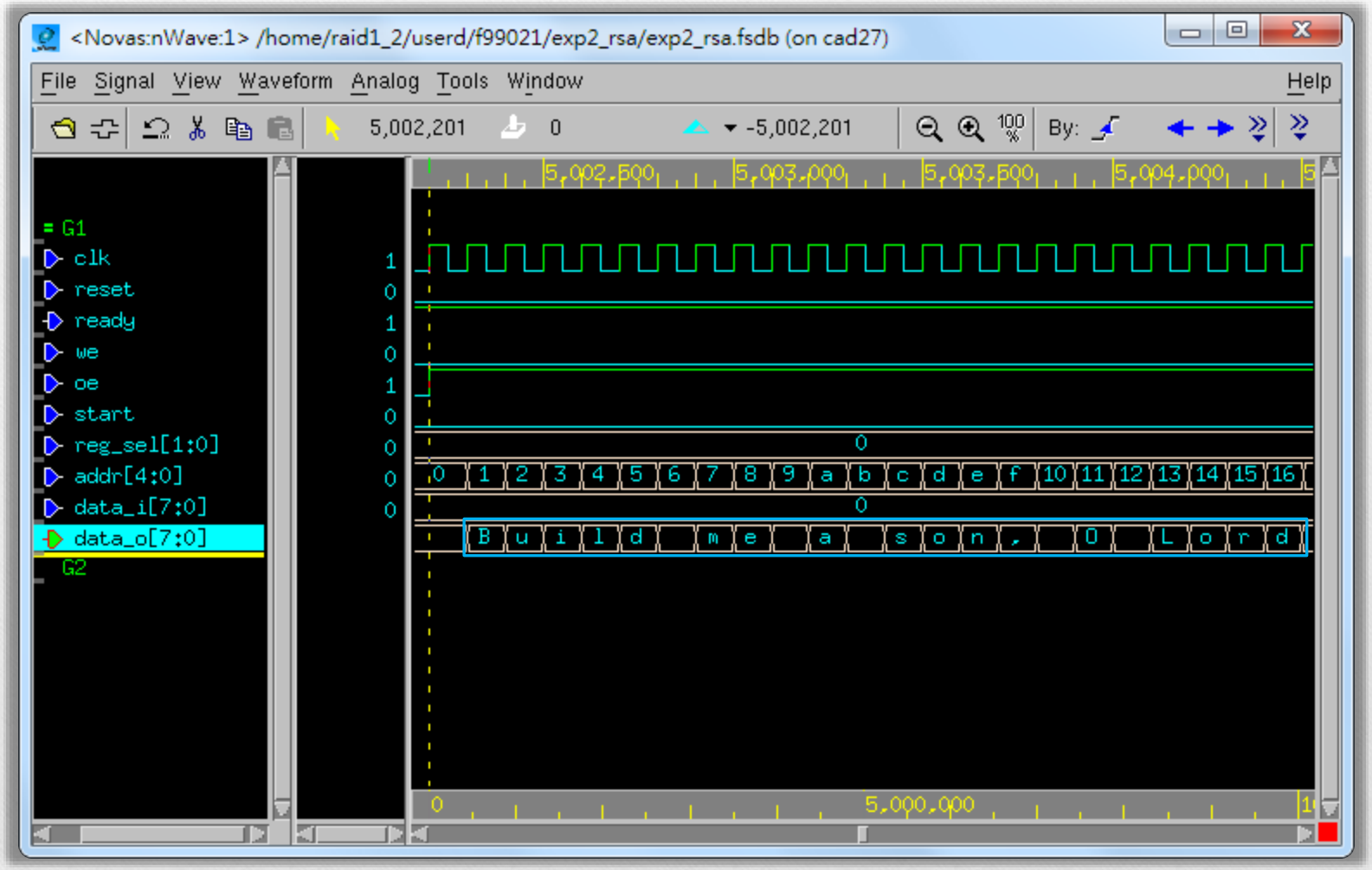

<Novas:nWave:1> /home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.fsdb (on cad27)
File Signal View Waveform Analog Tools Window
Help
5,002,201
0
-5,002,201
By:
Go to:
Jump to the cursor position (Used when we are lost)
5,002,000
5,002,500
G1
clk
reset
ready
we
oe
start
reg_sel[1:0]
addr[4:0]
data_i[7:0]
data_o[7:0]
G2
1
0
1
0
1
0
0
0
0
0
0
1
2
3
4
5
6
42
75
69
6c
64
20
cursor position
(Search by rising oe)
0
2,000,000
4,000,000
6,000,000
8,000,000

Change Sign Representation

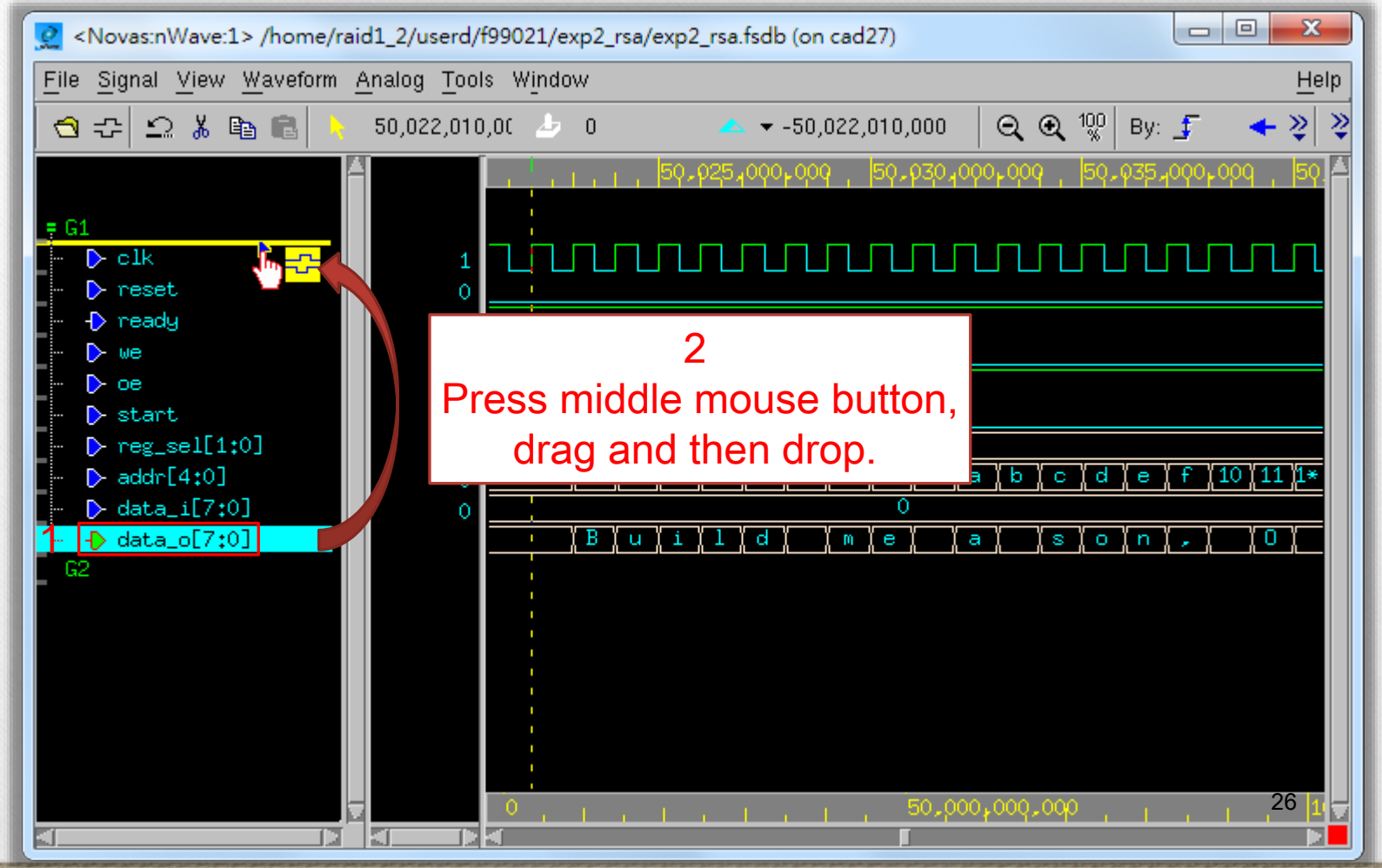


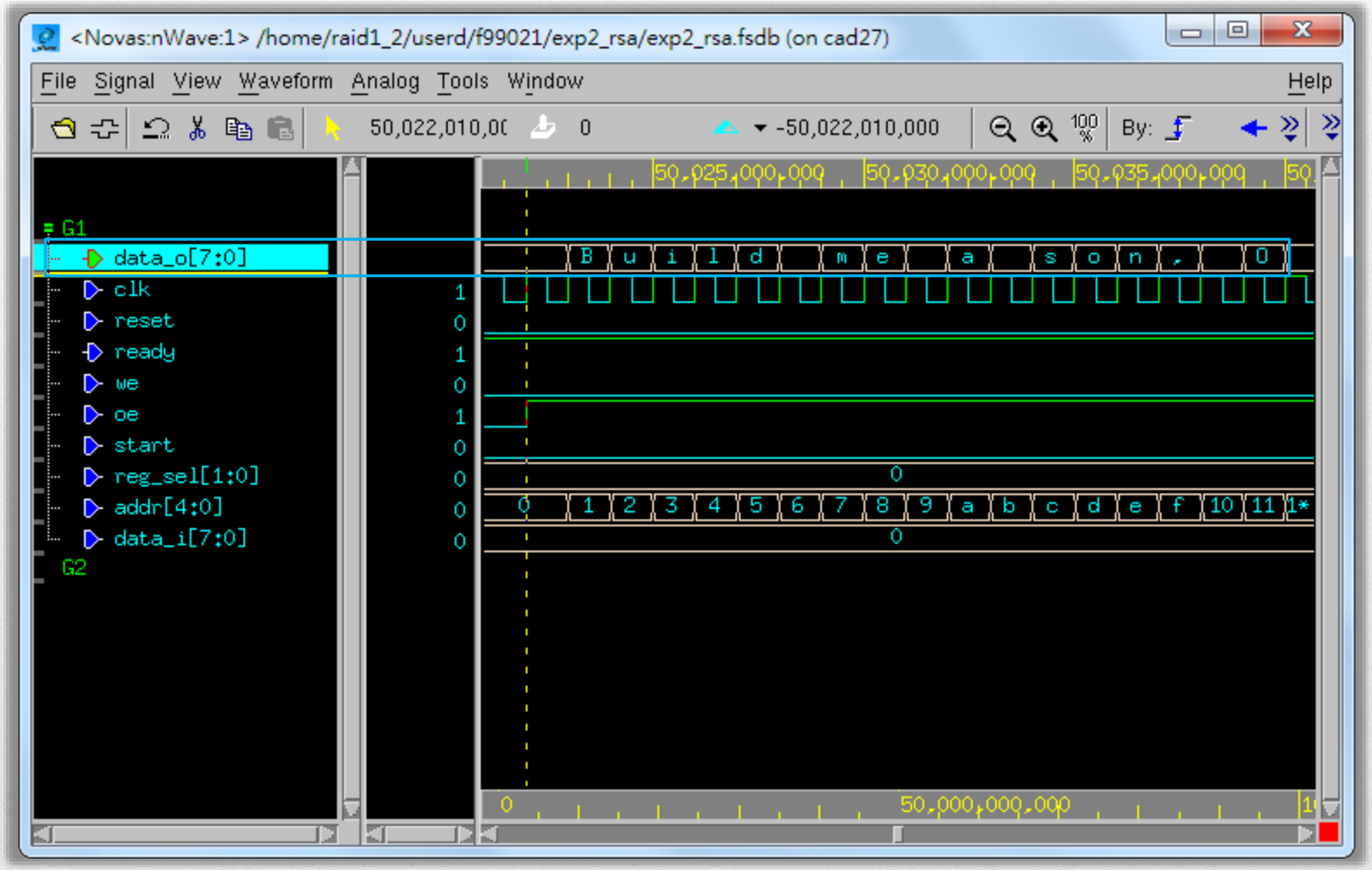
Change Radix Representation



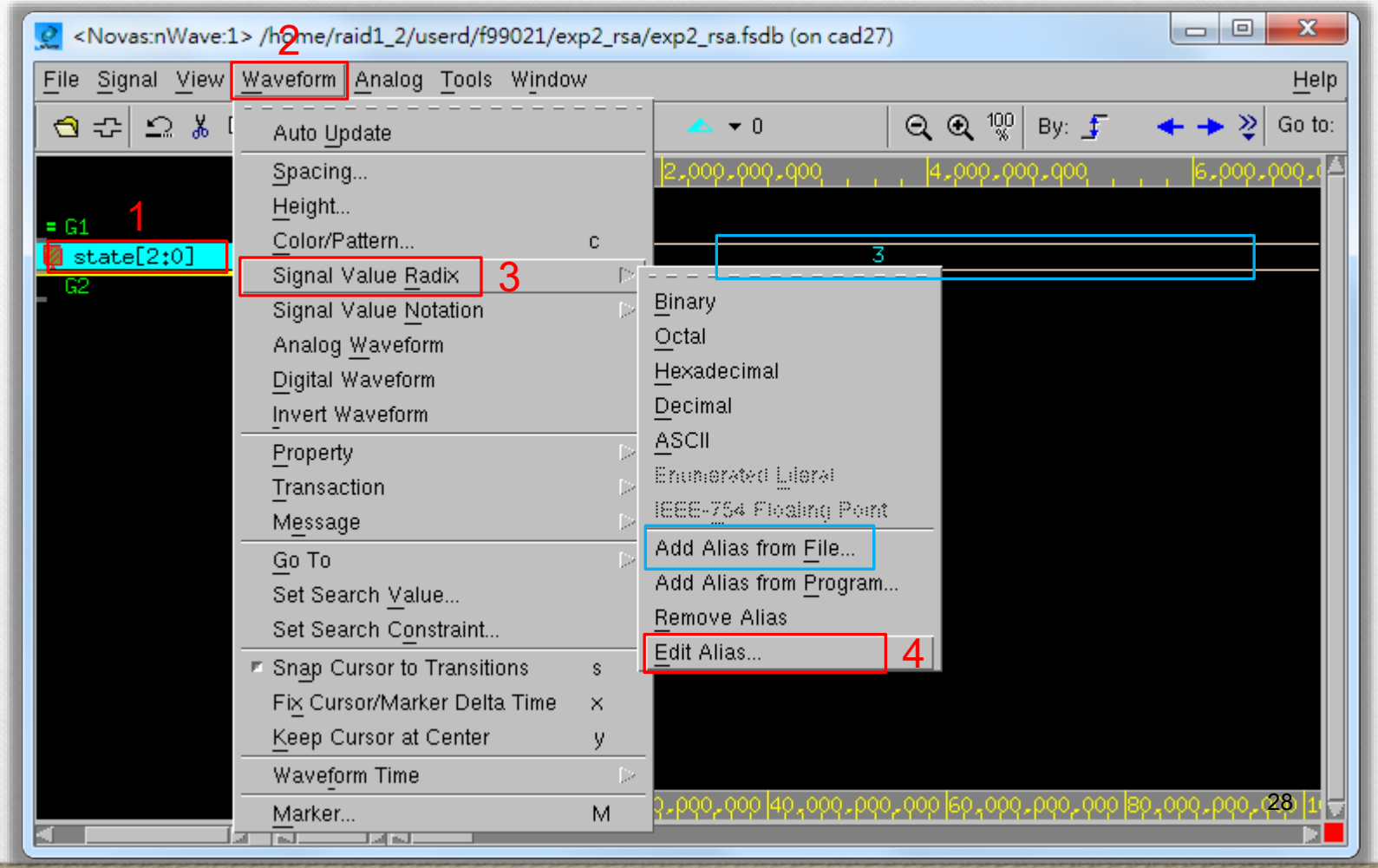

<Novas:nWave:1> /home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.fsdb (on cad27)
File Signal View Waveform Analog Tools Window Help
5,002,201
0
-5,002,201
By:
5,002,500
5,003,000
5,003,500
5,004,000
G1
clk
reset
ready
we
oe
start
reg_sel[1:0]
addr[4:0]
data_i[7:0]
data_o[7:0]
G2
1
0
1
0
1
0
0
0
0
0 1 2 3 4 5 6 7 8 9 a b c d e f 10 11 12 13 14 15 16
B u i l d m e a s o n , 0 L o r d
0
5,000,000

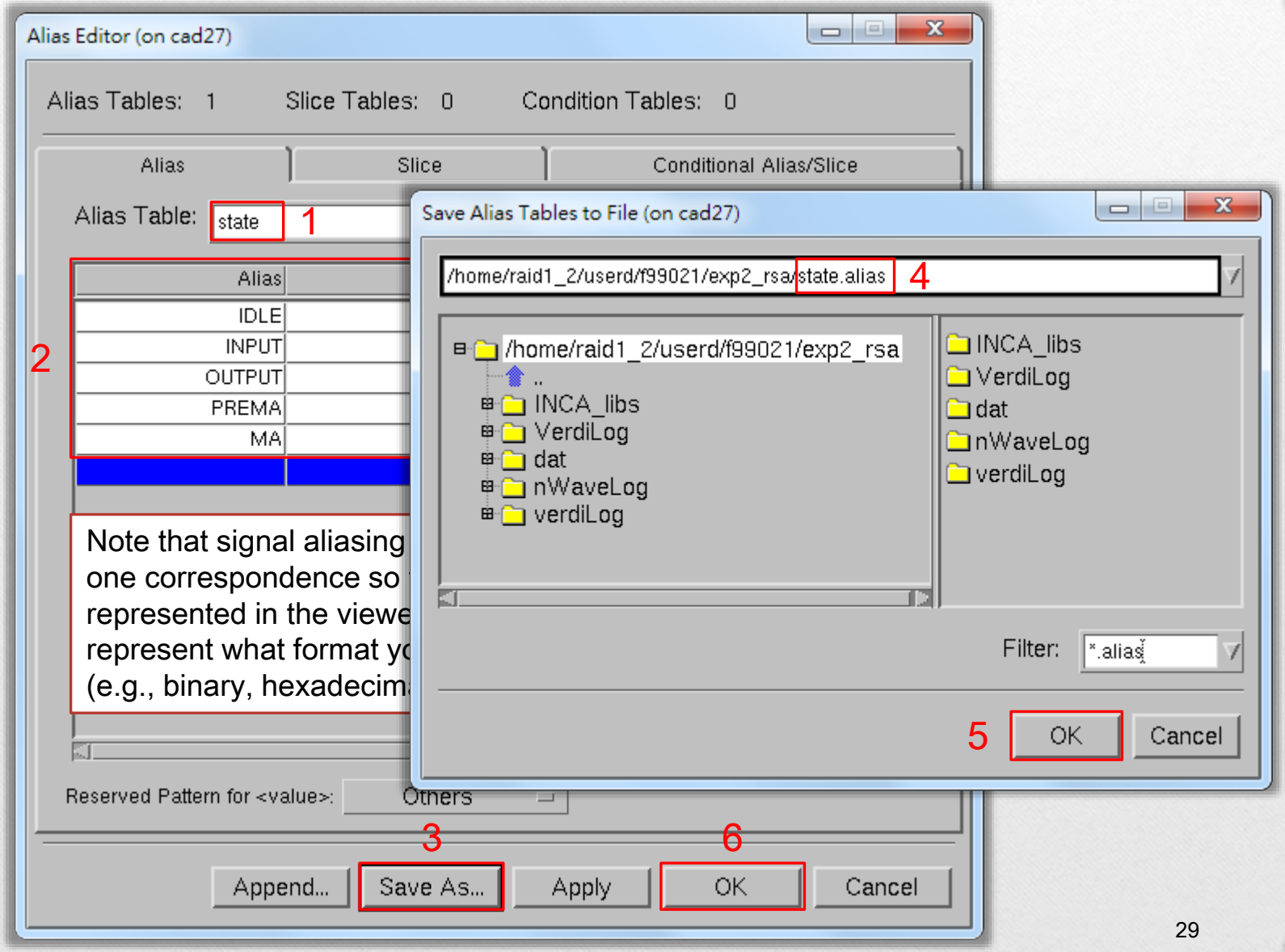
Change Signal Position

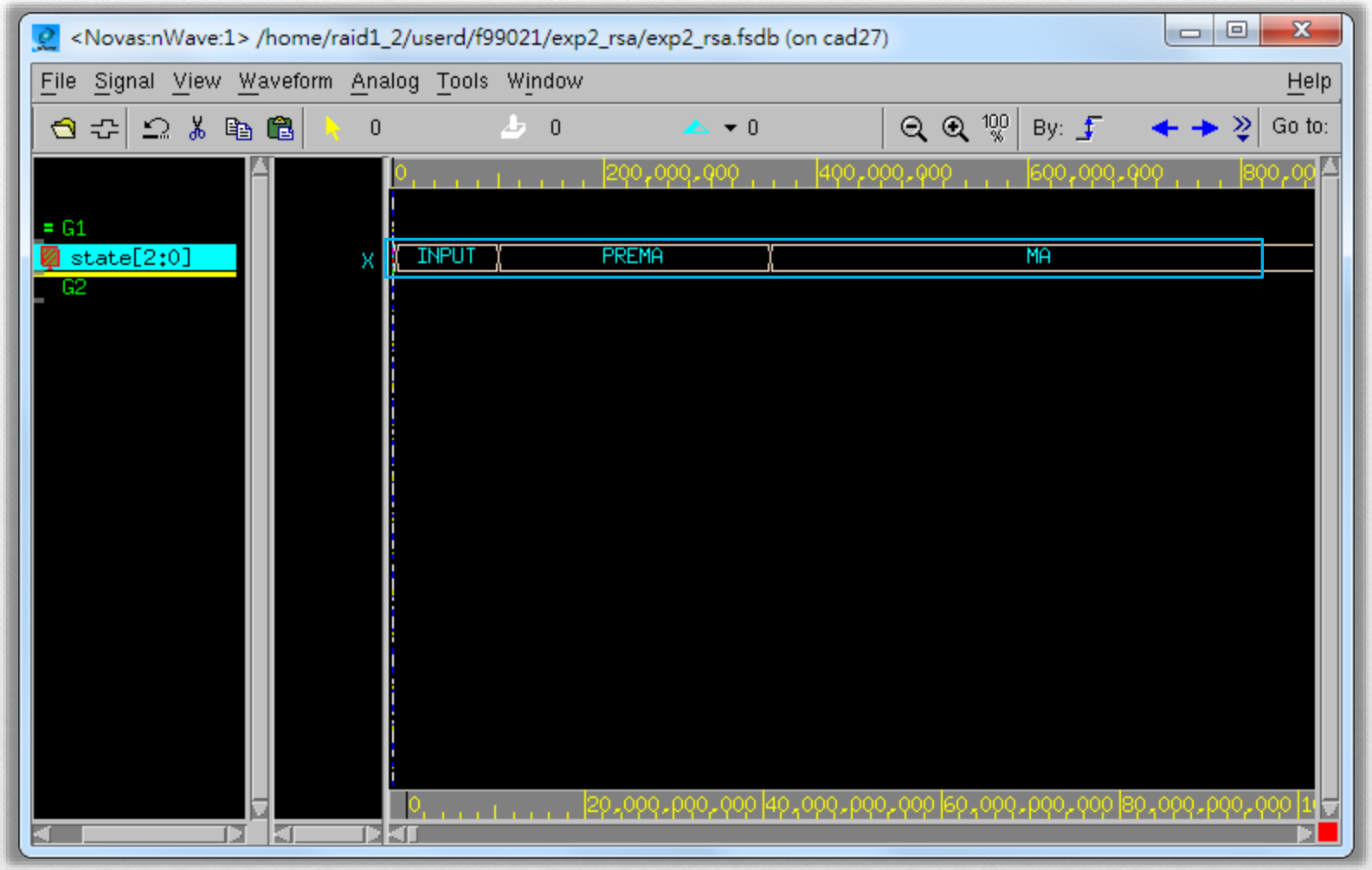



<Novas:nWave:1> /home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.fsdb (on cad27)
File Signal View Waveform Analog Tools Window Help
50,022,010,0(
0
-50,022,010,000
By:
50,025,000,000
50,030,000,000
50,035,000,000
G1
data_o[7:0]
clk
reset
ready
we
oe
start
reg_sel[1:0]
addr[4:0]
data_i[7:0]
G2
B u i l d m e a s o n , 0
1
0
1
0
1
0
0
0
0 1 2 3 4 5 6 7 8 9 a b c d e f 10 11 1*
0
0
50,000,000,000

Signal Aliasing

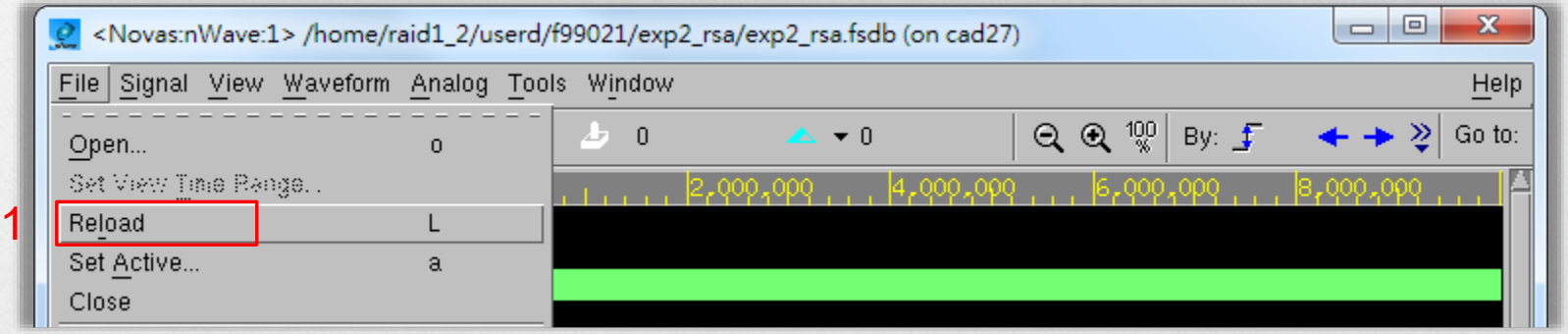



Alias Editor (on cad27)
Alias Tables: 1
Slice Tables: 0
Condition Tables: 0
Alias
Slice
Conditional Alias/Slice
Alias Table: state
1
Alias
IDLE
INPUT
OUTPUT
PREMA
MA
2
Note that signal aliasing
one correspondence so
represented in the viewe
represent what format yc
(e.g., binary, hexadecim
Reserved Pattern for <value>:
Others
3
Append...
Save As...
Apply
6
OK
Cancel
Save Alias Tables to File (on cad27)
/home/raid1_2/userd/f99021/exp2_rsa/state.alias
4
/home/raid1_2/userd/f99021/exp2_rsa
..
INCA_libs
VerdiLog
dat
nWaveLog
verdiLog
INCA_libs
VerdiLog
dat
nWaveLog
verdiLog
Filter:
*.alias
5
OK
Cancel


<Novas:nWave:1> /home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.fsdb (on cad27)
File Signal View Waveform Analog Tools Window Help
Go to:
G1
state[2:0]
G2
INPUT
PREMA
MA

Reload the Waveform

- Remember to reload the waveform whenever finishing another Verilog simulation.



The End.

Any question?

Reference

1. "Cadence NC-Verilog Simulator Tutorial“ by Cadence
2. "Introduction to Verdi" by Abel Hu
3. "Verdi^3 datasheet" by Synopsys