# DC Lab3 Report
# Team 04

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## File Structure

team04_lab3

|- src

|- DE2_115

|- DE2_115.sv

|- FastSlow.sv

|- SevenHexDecoder.sv

|- Debounce.sv

|- AudPlayer.sv

|- AudDSP.sv

|-  AudRecorder.sv

|-  I2cInitializer.sv

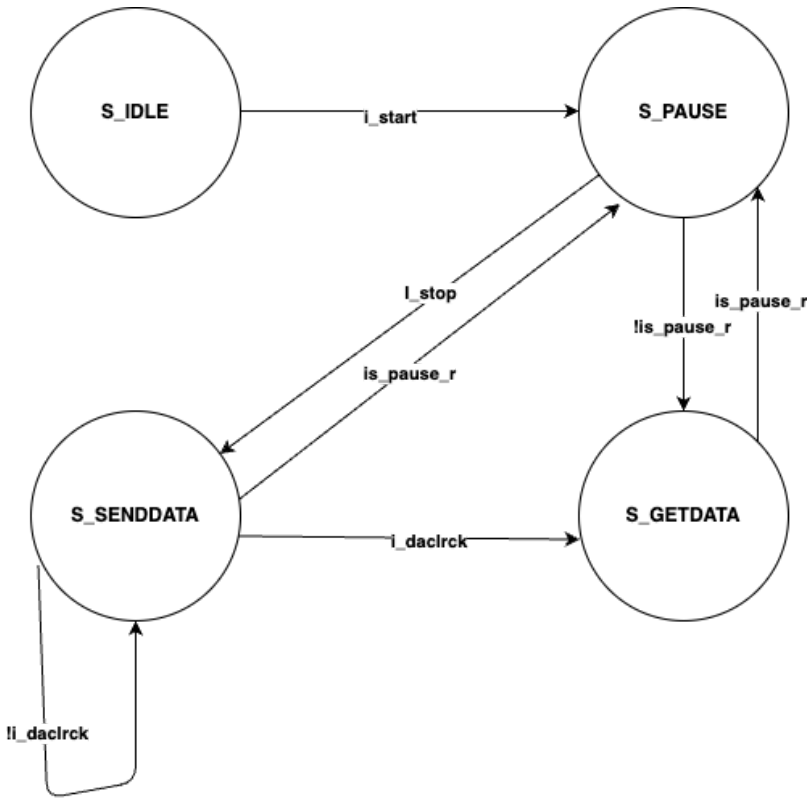
|- Top.sv

team04_lab3_report

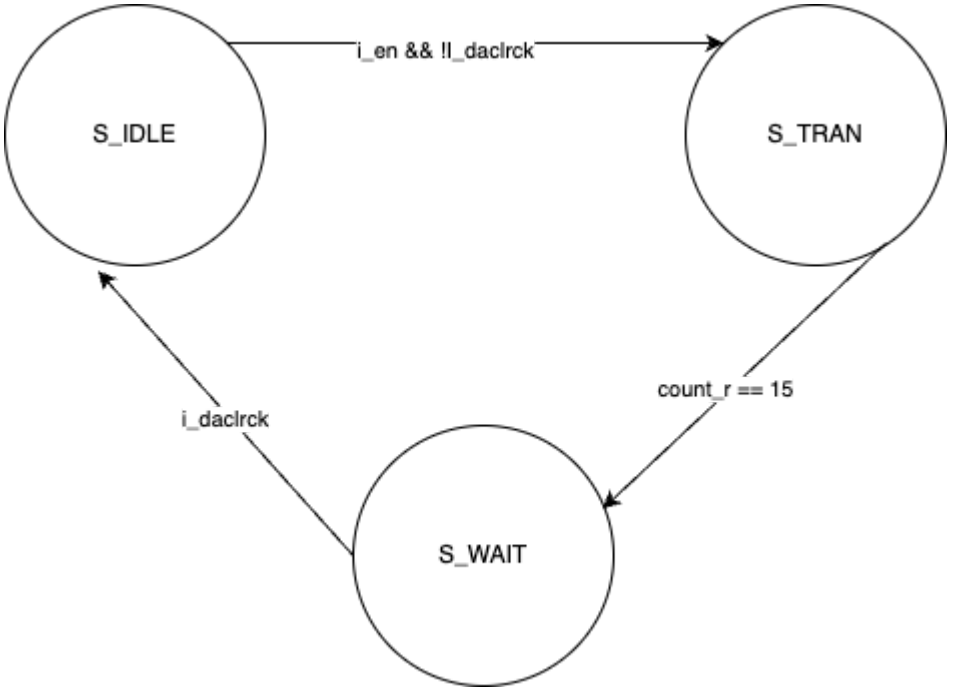
# Hardware Scheduling

# Modules / Submodules

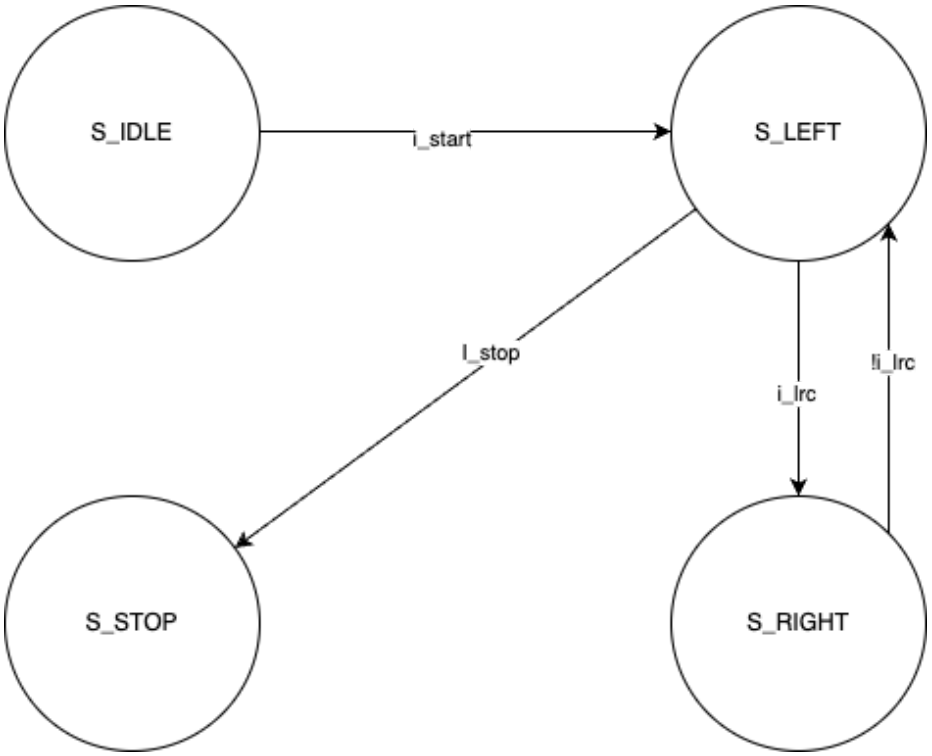
|- AudDSP sv



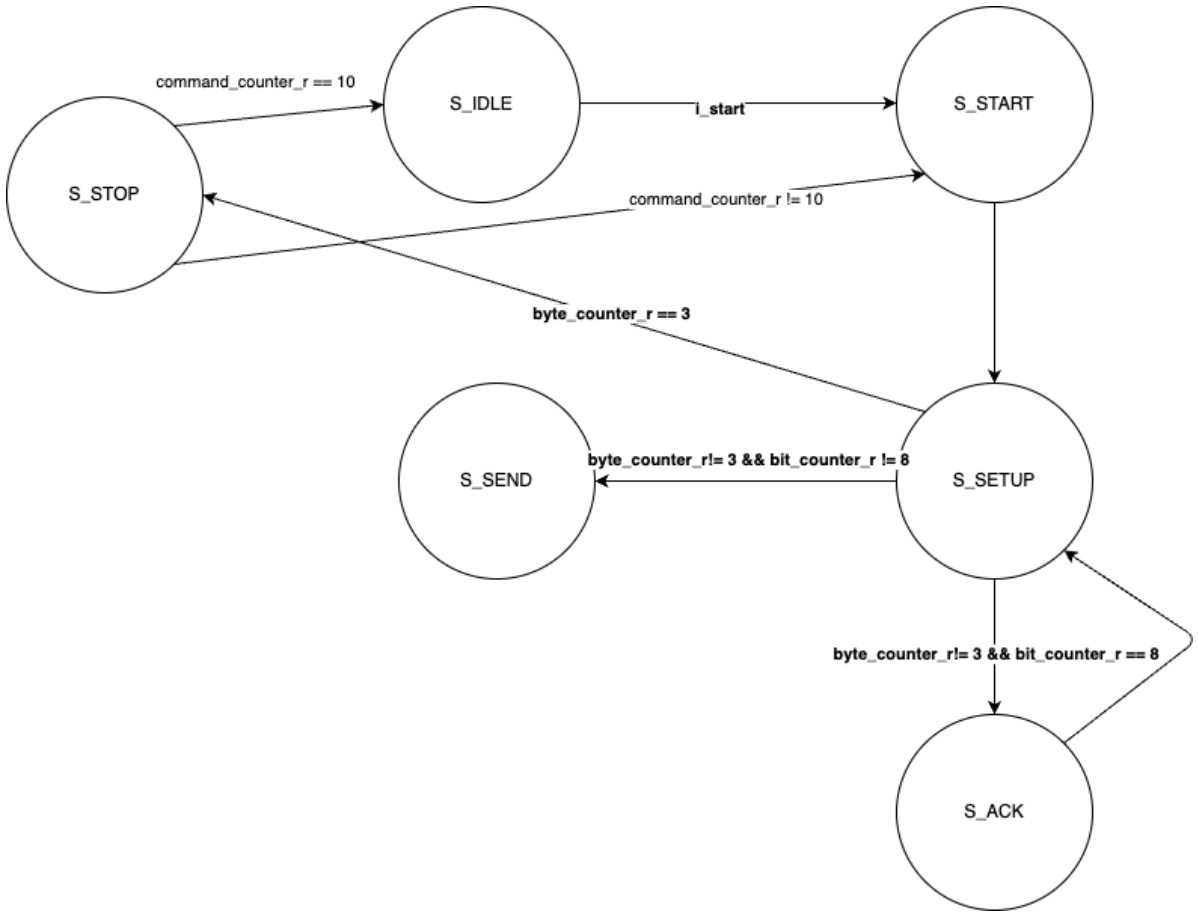
|- AudPlayer.sv



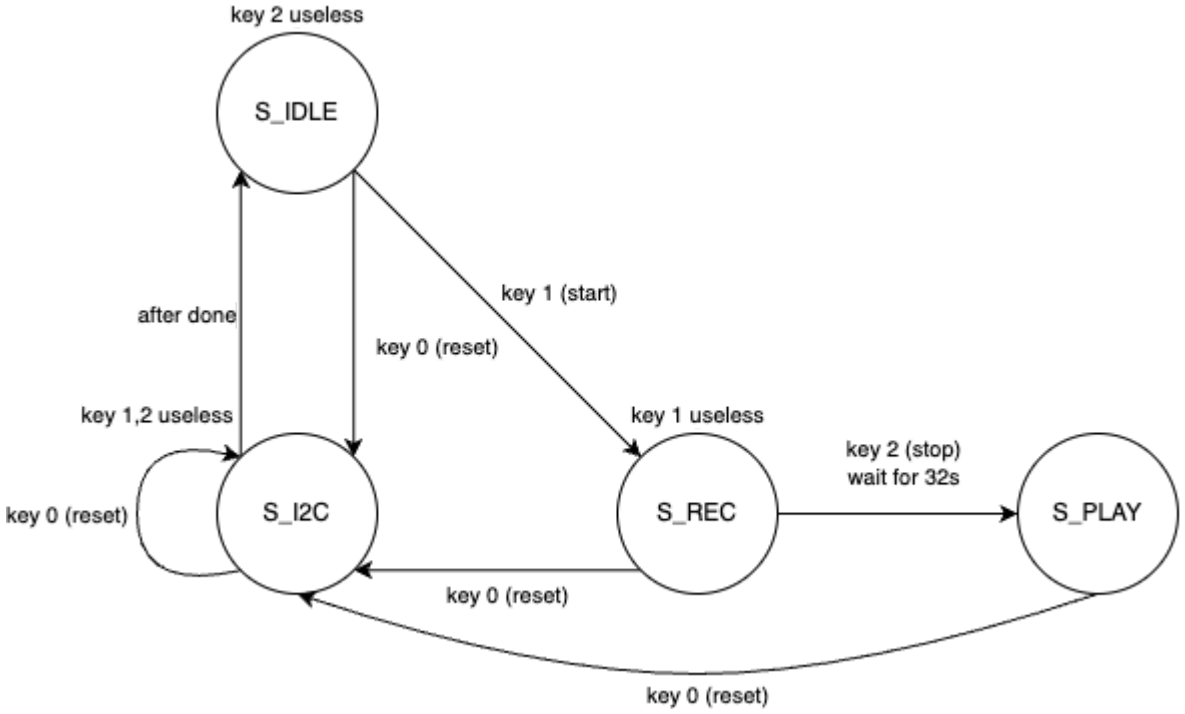

|- AudRecorder.sv



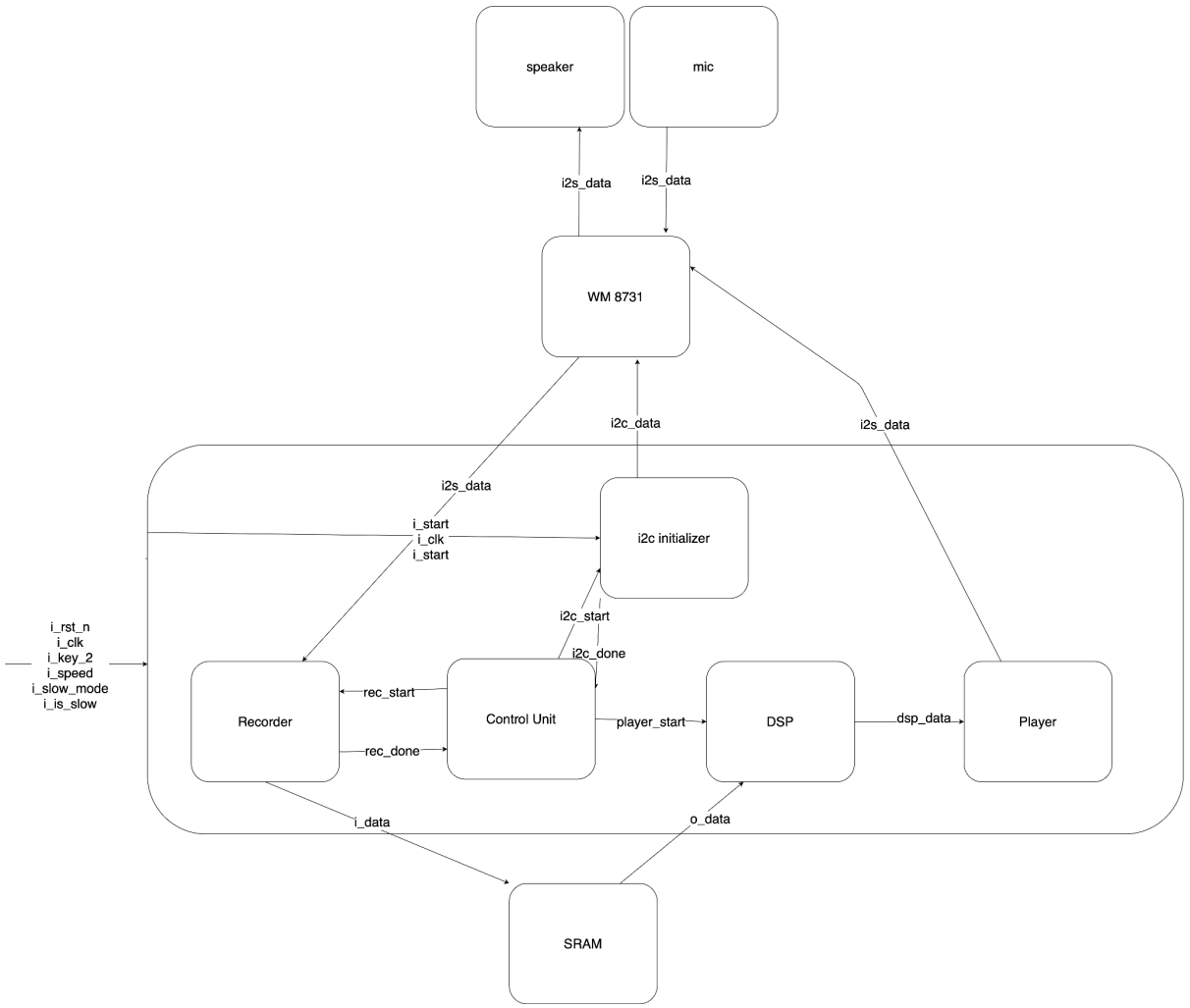
|- I2cInitializer.sv



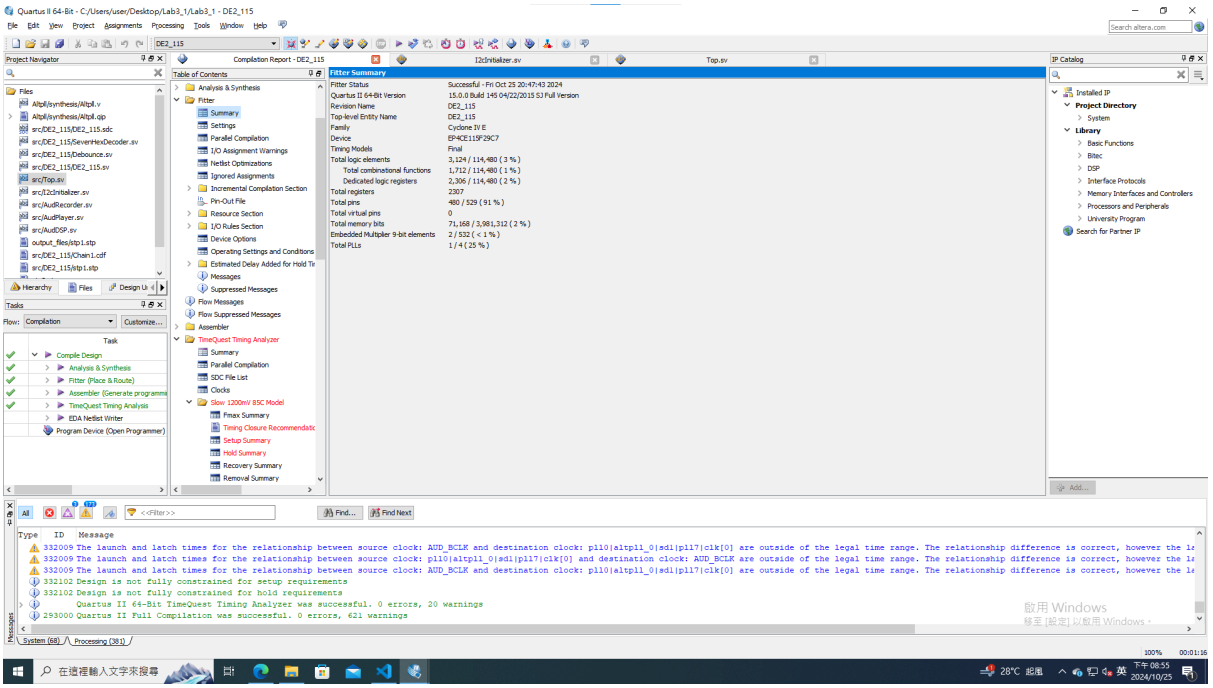

|- Top.sv



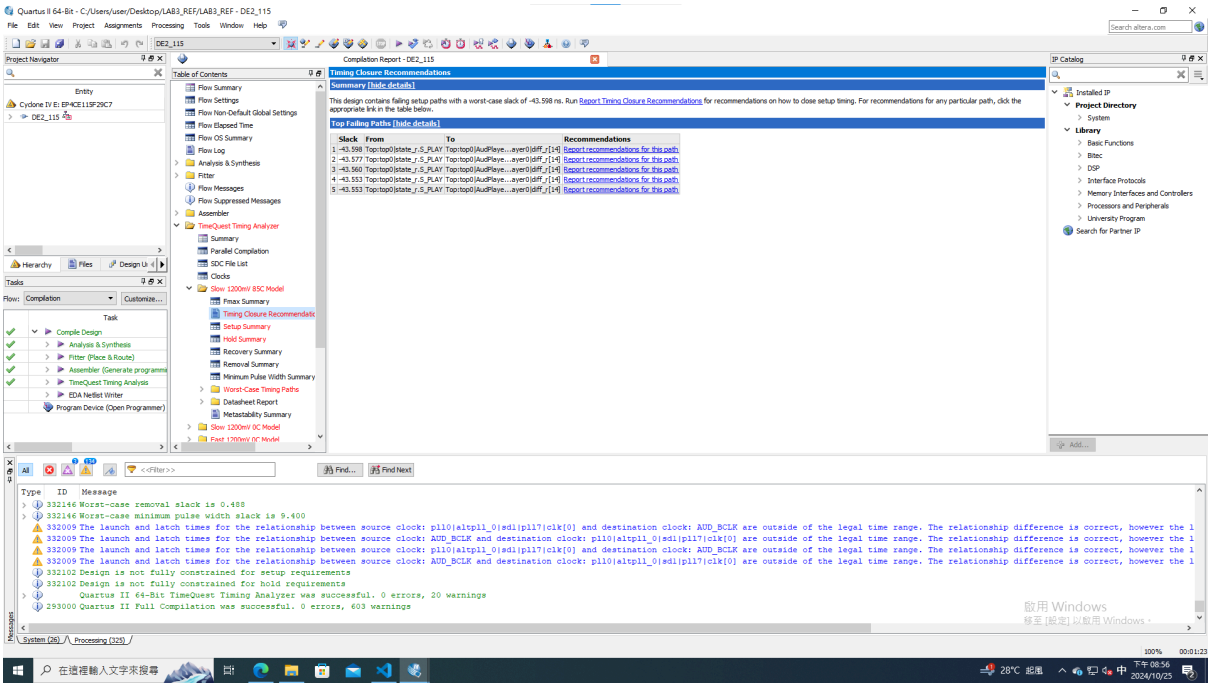
# System Architecture

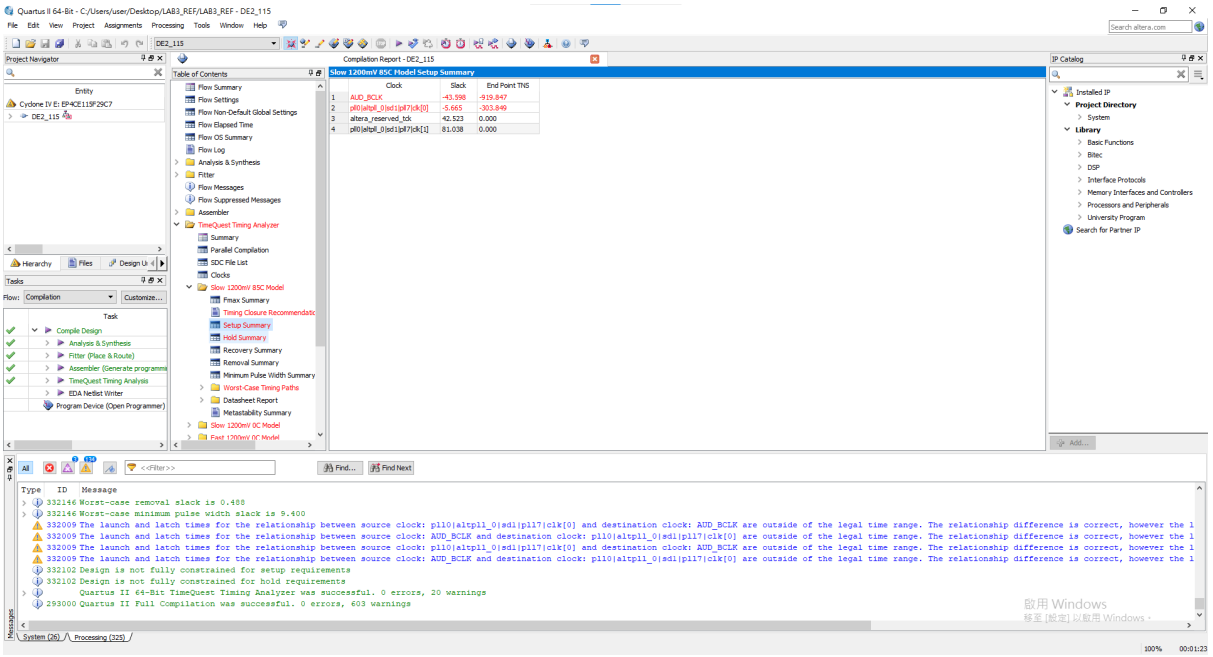



# Fitter summary




# TIMING SUMMARY




Quartus II 64-Bit - C:/Users/user/Desktop/LAB3_REF/LAB3_REF - DE2_115
Slow 1200mV 85C Model Setup Summary
Clock Slack End Point TNS
AUD_BCLK -43.998 -919.847
pll0|altpll_0|sd1|pll7|clk[0] -5.665 -303.849
altera_reserved_tck 42.523 0.000
pll0|altpll_0|sd1|pll7|clk[1] 81.038 0.000
Type ID Message
332146 Worst-case removal slack is 0.488
332146 Worst-case minimum pulse width slack is 9.400
332009 The launch and latch times for the relationship between source clock: pll0|altpll_0|sd1|pll7|clk[0] and destination clock: AUD_BCLK are outside of the legal time range. The relationship difference is correct, however the l
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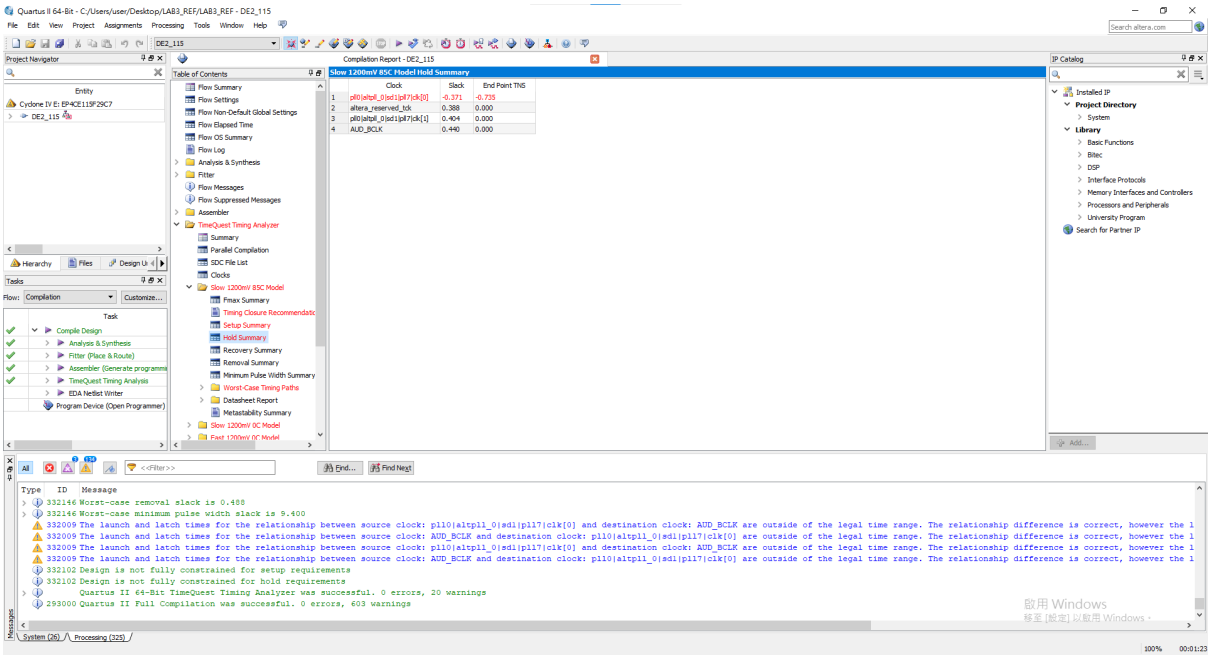
332009 The launch and latch times for the relationship between source clock: AUD_BCLK and destination clock: pll0|altpll_0|sd1|pll7|clk[0] are outside of the legal time range. The relationship difference is correct, however the l
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 20 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 603 warnings


Quartus II 64-Bit - C:/Users/user/Desktop/LAB3_REF/LAB3_REF - DE2_115
Slow 1200mV 85C Model Hold Summary
Clock Slack End Point TNS
pll0|altpll_0|sd1|pll7|clk[0] -0.371 -0.735
altera_reserved_tck 0.388 0.000
pll0|altpll_0|sd1|pll7|clk[1] 0.404 0.000
AUD_BCLK 0.440 0.000
Type ID Message
332146 Worst-case removal slack is 0.488
332146 Worst-case minimum pulse width slack is 9.400
332009 The launch and latch times for the relationship between source clock: pll0|altpll_0|sd1|pll7|clk[0] and destination clock: AUD_BCLK are outside of the legal time range. The relationship difference is correct, however the l
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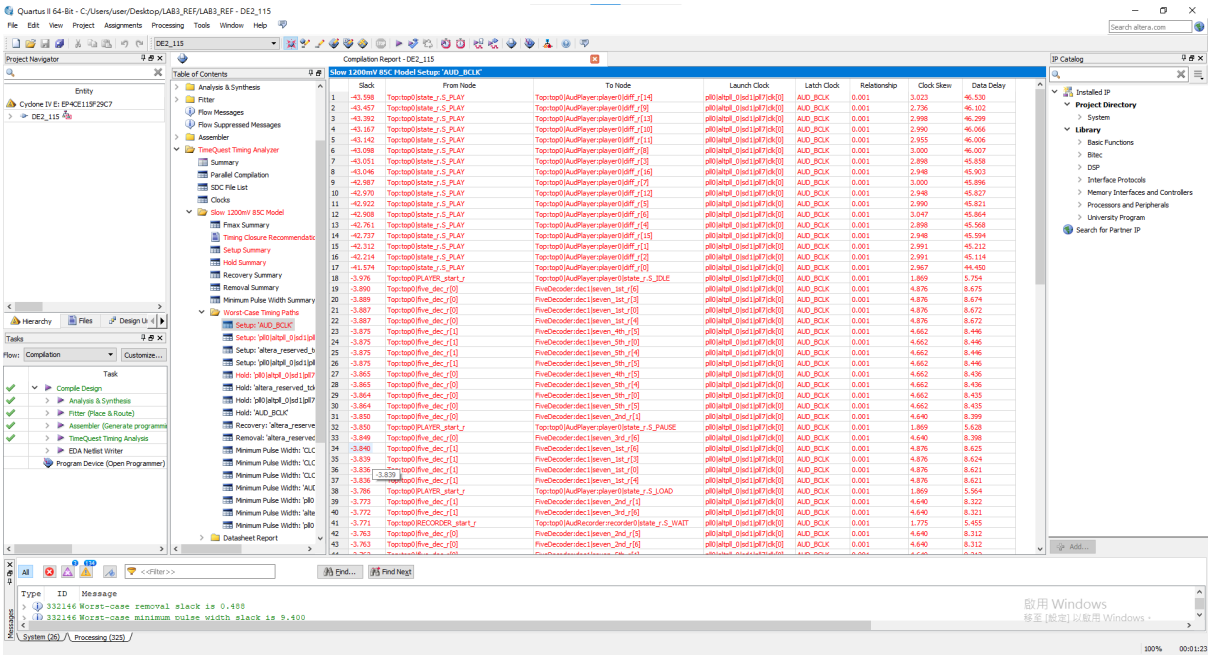
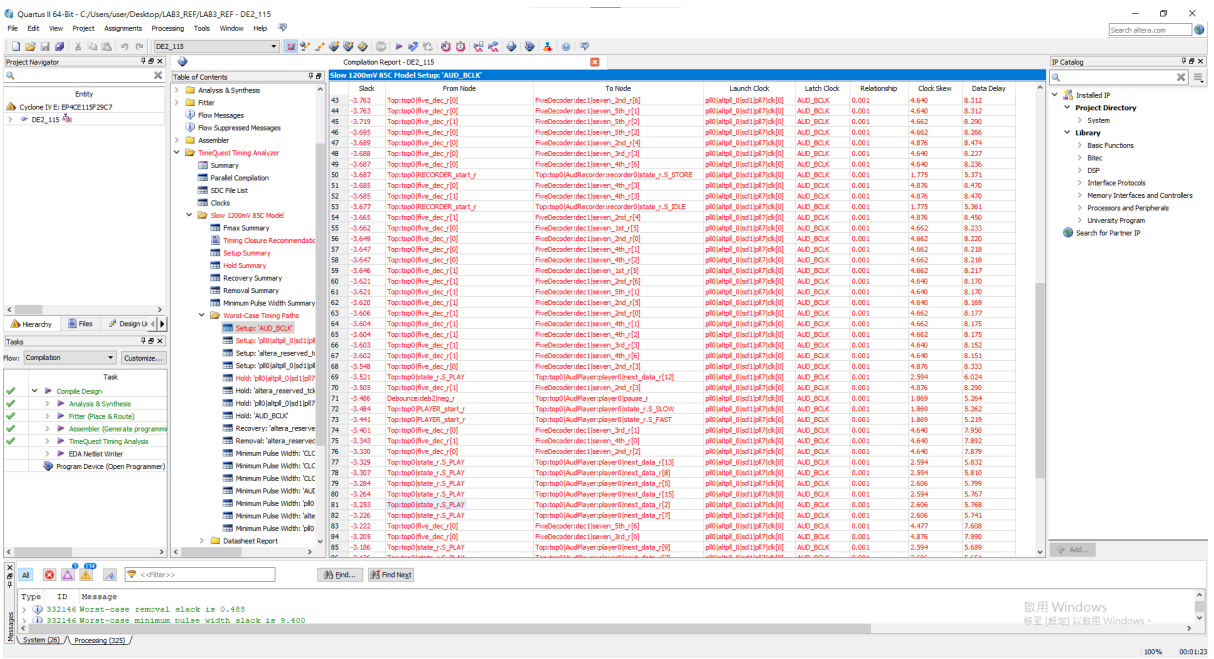
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 20 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 603 warnings


Quartus II 64-Bit - C:/Users/user/Desktop/LAB3_REF/LAB3_REF - DE2_115
Slow 1200mV 85C Model Setup: 'AUD_BCLK'
Type ID Message
332146 Worst-case removal slack is 0.488
332146 Worst-case minimum pulse width slack is 9.400


Quartus II 64-Bit - C:/Users/user/Desktop/LAB3_REF/LAB3_REF - DE2_115
Slow 1200mV 85C Model Setup: 'AUD_BCLK'
Type ID Message
332146 Worst-case removal slack is 0.488
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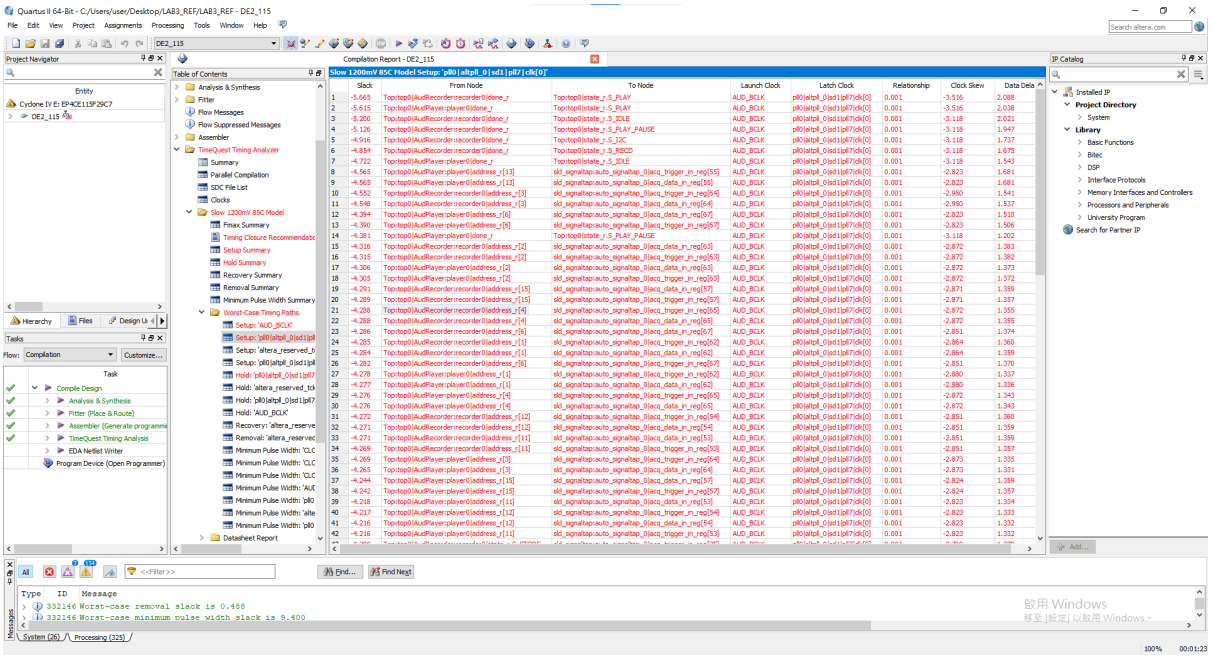
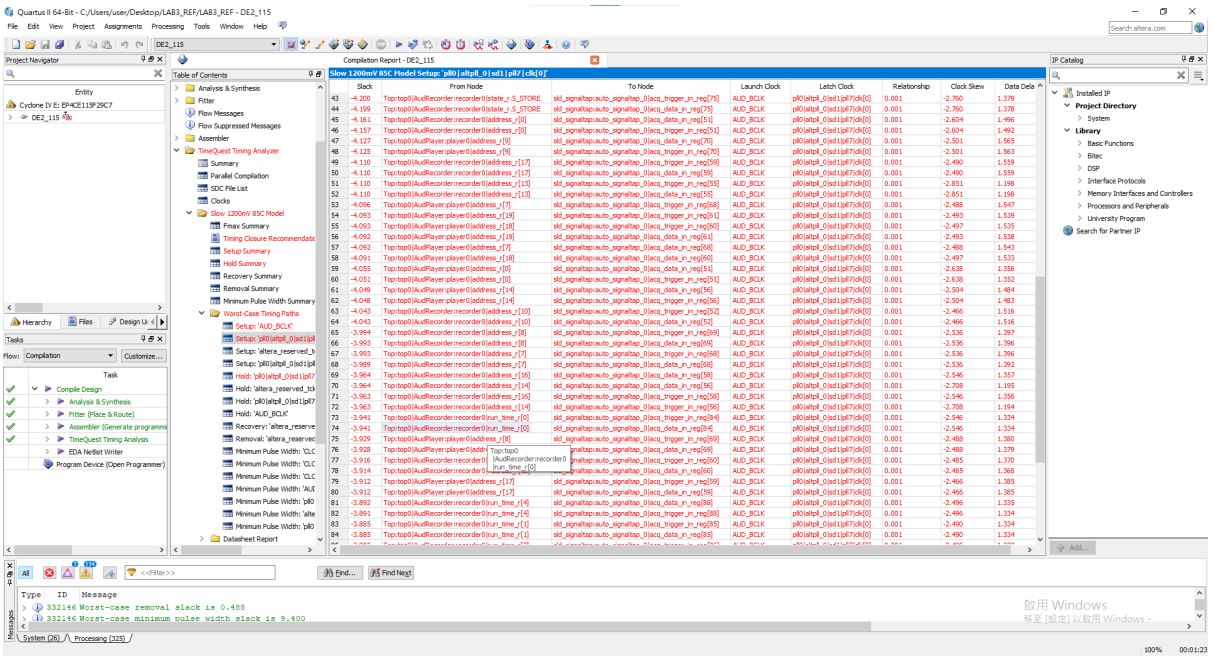

Quartus II 64-Bit - C:/Users/user/Desktop/LAB3_REF/LAB3_REF - DE2_115
Slow 1200mV 85C Model Setup: 'pll0|altpll_0|sd1|pll7|clk[0]'
Worst-case removal slack is 0.488
Worst-case minimum pulse width slack is 9.400


Quartus II 64-Bit - C:/Users/user/Desktop/LAB3_REF/LAB3_REF - DE2_115
Slow 1200mV 85C Model Setup: 'pll0|altpll_0|sd1|pll7|clk[0]'
Worst-case removal slack is 0.488
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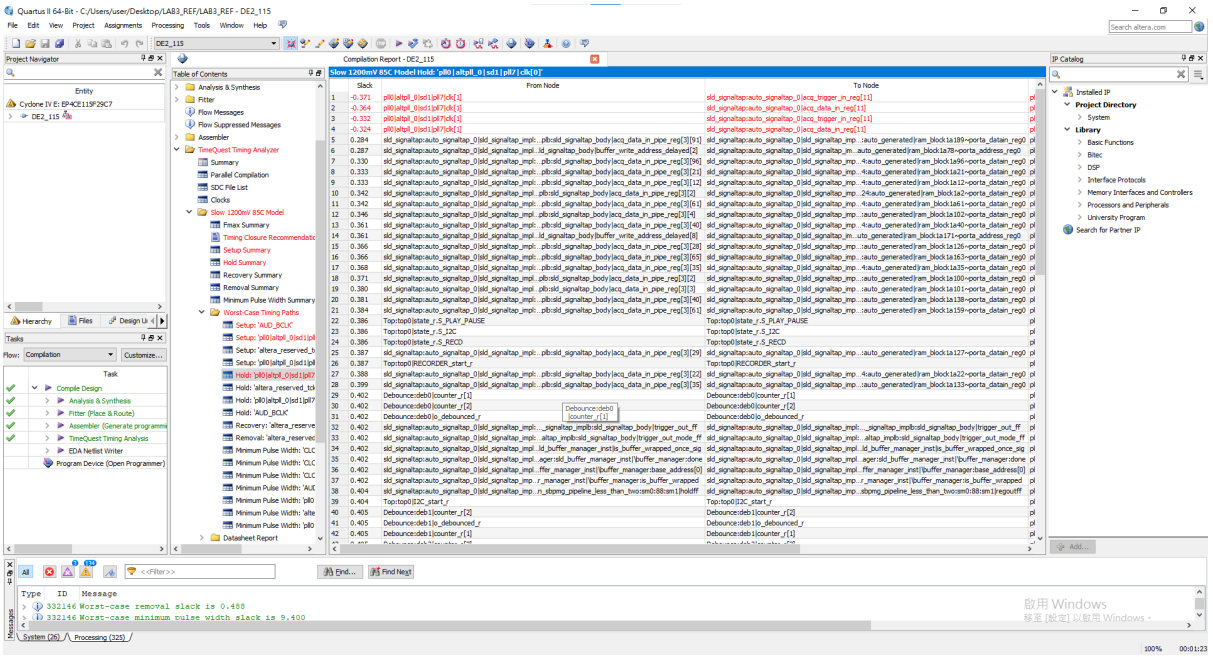
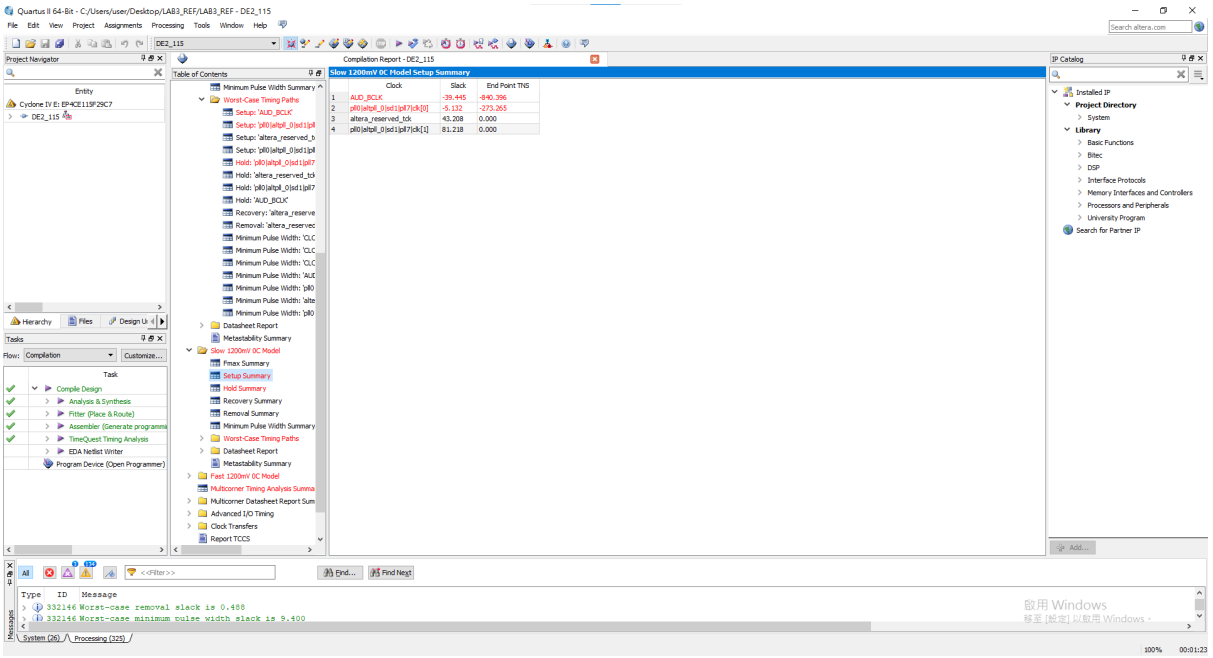
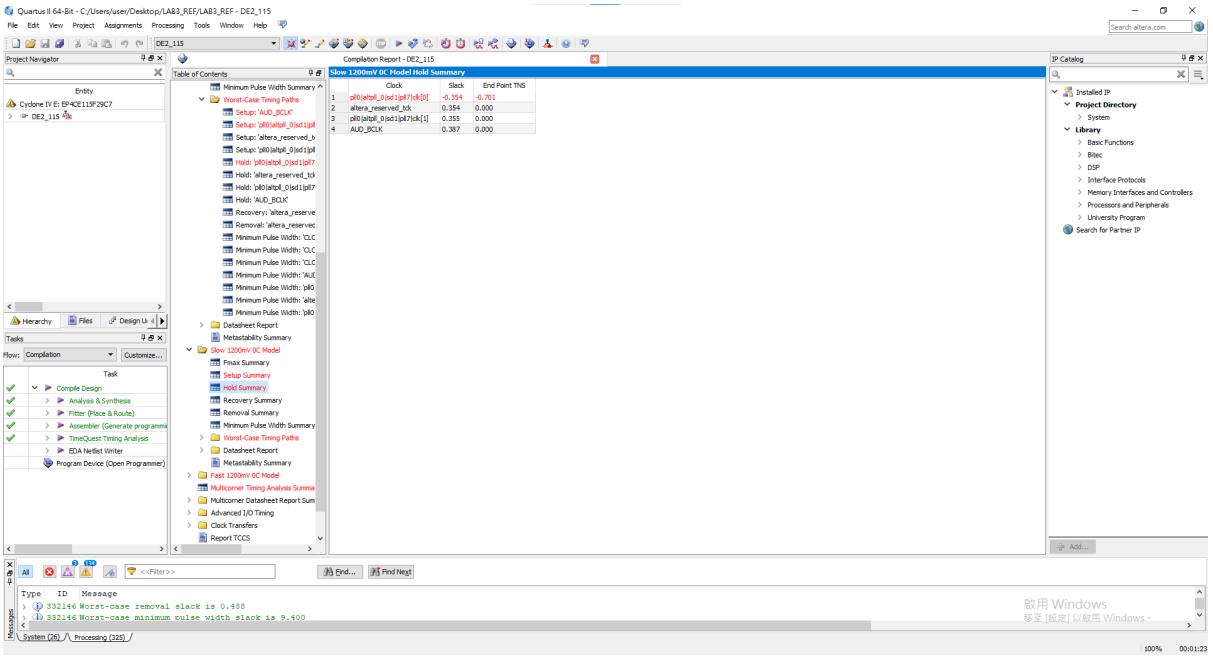
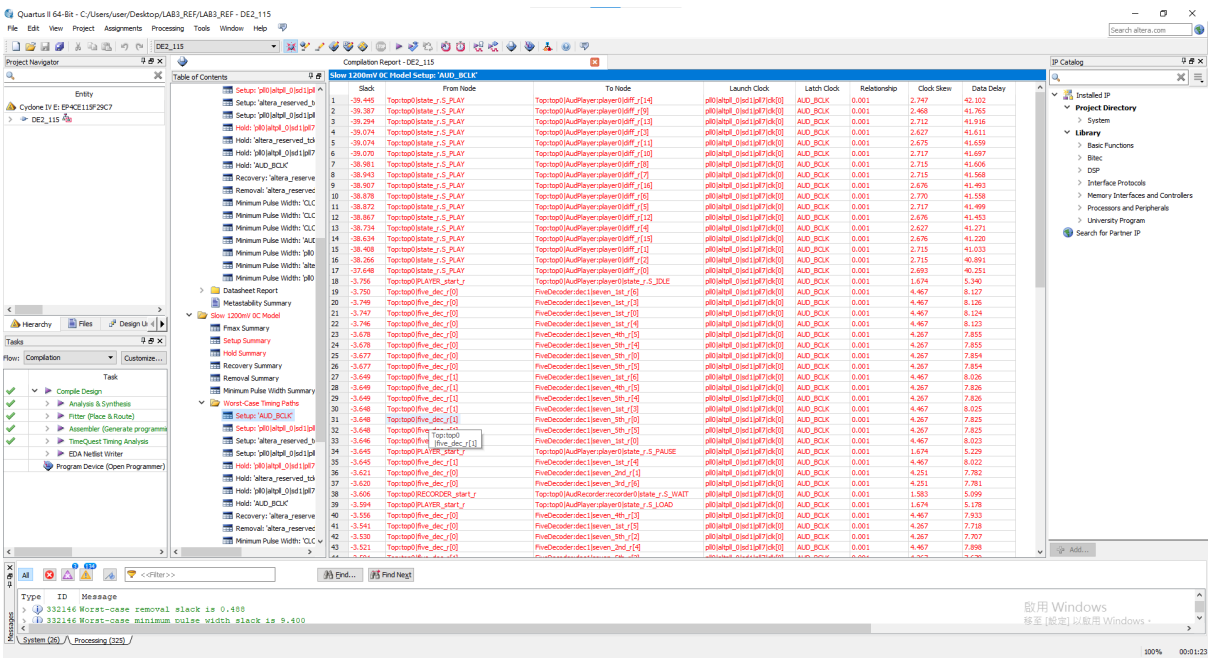
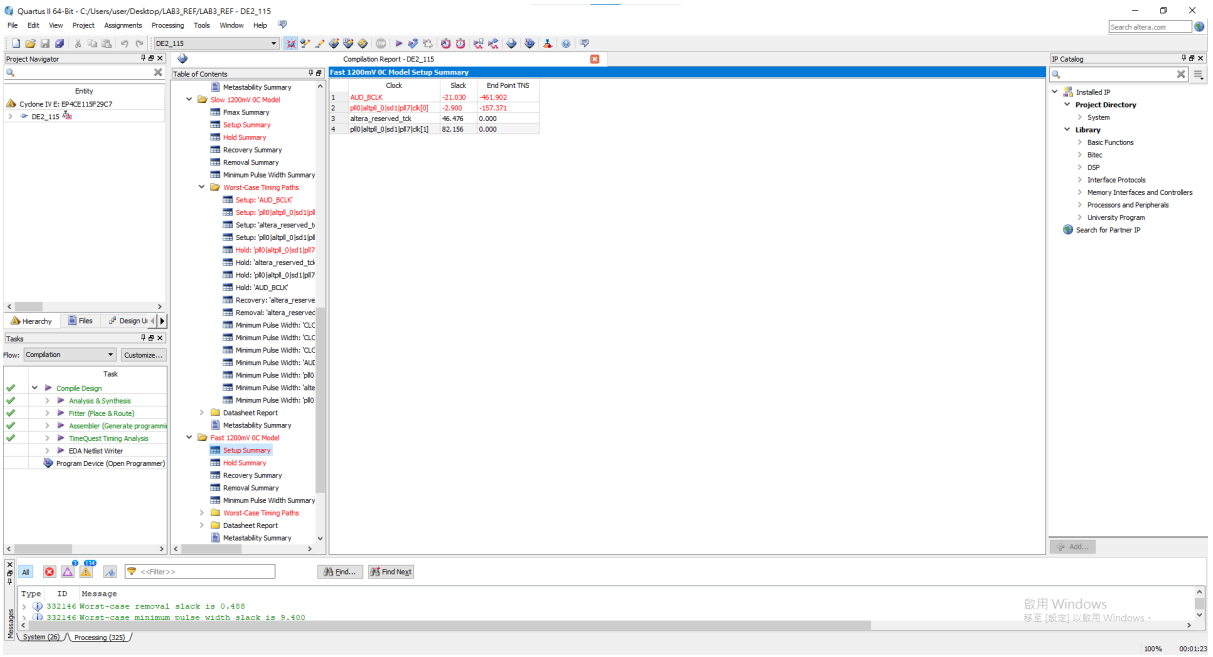
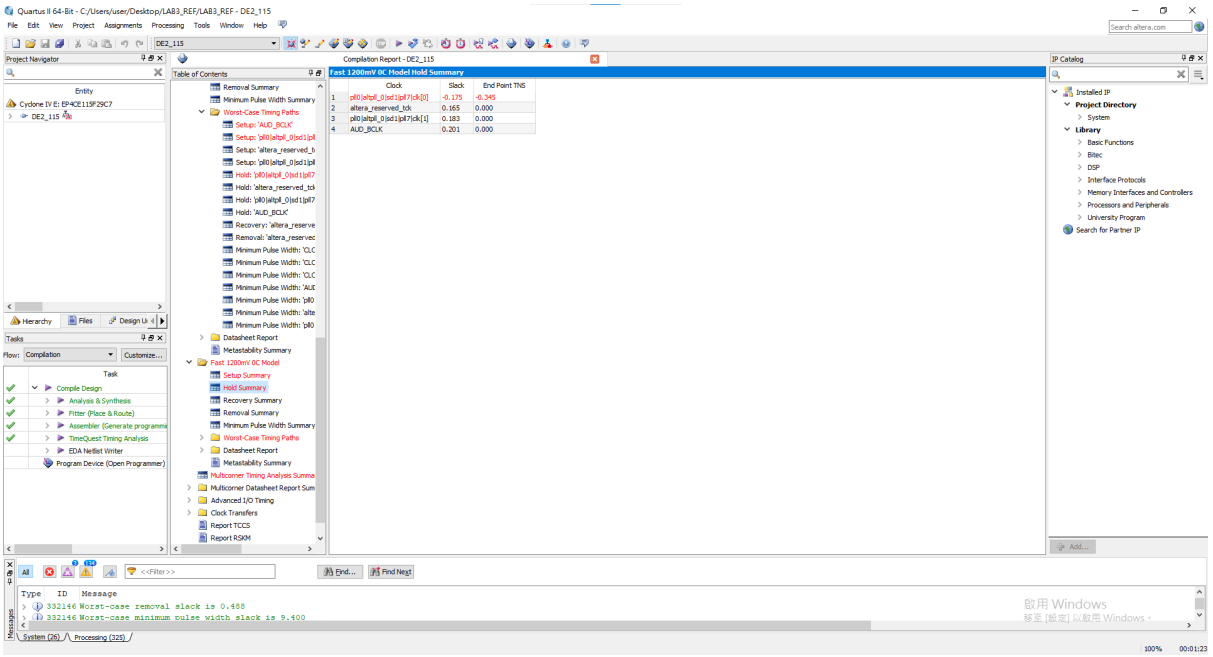

Quartus II 64-Bit - C:/Users/user/Desktop/LAB3_REF/LAB3_REF - DE2_115
Slow 1200mV 85C Model Hold: 'pll0|altpll_0|sd1|pll7|clk[0]'
Slack
From Node
To Node
Type
ID
Message
332146 Worst-case removal slack is 0.488
332146 Worst-case minimum pulse width slack is 9.400


Quartus II 64-Bit - C:/Users/user/Desktop/LAB3_REF/LAB3_REF - DE2_115
Slow 1200mV 0C Model Setup Summary
Clock
Slack
End Point TNS
AUD_BCLK
-39.445
-840.396
pll0|altpll_0|sd1|pll7|clk[0]
-5.132
-273.265
altera_reserved_tck
43.208
0.000
pll0|altpll_0|sd1|pll7|clk[1]
81.218
0.000
Type
ID
Message
332146 Worst-case removal slack is 0.488
332146 Worst-case minimum pulse width slack is 9.400


Quartus II 64-Bit - C:/Users/user/Desktop/LAB3_REF/LAB3_REF - DE2_115
Compilation Report - DE2_115
Slow 1200mV 0C Model Hold Summary
Clock
Slack
End Point TNS
pll0|altpll_0|sd1|pll7|clk[0]
-0.354
-0.701
altera_reserved_tck
0.354
0.000
pll0|altpll_0|sd1|pll7|clk[1]
0.355
0.000
AUD_BCLK
0.387
0.000
Type
ID
Message
332146 Worst-case removal slack is 0.488
332146 Worst-case minimum pulse width slack is 9.400


Quartus II 64-Bit - C:/Users/user/Desktop/LAB3_REF/LAB3_REF - DE2_115
Compilation Report - DE2_115
Slow 1200mV 0C Model Setup: 'AUD_BCLK'
Slack
From Node
To Node
Launch Clock
Latch Clock
Relationship
Clock Skew
Data Delay
Type
ID
Message
332146 Worst-case removal slack is 0.488
332146 Worst-case minimum pulse width slack is 9.400


Quartus II 64-Bit - C:/Users/user/Desktop/LAB3_REF/LAB3_REF - DE2_115
File Edit View Project Assignments Processing Tools Window Help
Compilation Report - DE2_115
Fast 1200mV 0C Model Setup Summary
Clock Slack End Point TNS
1 AUD_BCLK -21.030 -461.902
2 pll0|altpll_0|sd1|pll7|clk[0] -2.900 -157.371
3 altera_reserved_tck 46.476 0.000
4 pll0|altpll_0|sd1|pll7|clk[1] 82.156 0.000
Table of Contents
Fast 1200mV 0C Model
Setup Summary
Hold Summary
Recovery Summary
Removal Summary
Minimum Pulse Width Summary
Worst-Case Timing Paths
Datasheet Report
Metastability Summary
IP Catalog
Installed IP
Project Directory
Library
Basic Functions
Bitec
DSP
Interface Protocols
Memory Interfaces and Controllers
Processors and Peripherals
University Program
Search for Partner IP
Tasks
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
Type ID Message
332146 Worst-case removal slack is 0.488
332146 Worst-case minimum pulse width slack is 9.400
System (26) Processing (325)
100% 00:01:23


Quartus II 64-Bit - C:/Users/user/Desktop/LAB3_REF/LAB3_REF - DE2_115
File Edit View Project Assignments Processing Tools Window Help
Compilation Report - DE2_115
Fast 1200mV 0C Model Hold Summary
Clock Slack End Point TNS
1 pll0|altpll_0|sd1|pll7|clk[0] -0.175 -0.345
2 altera_reserved_tck 0.165 0.000
3 pll0|altpll_0|sd1|pll7|clk[1] 0.183 0.000
4 AUD_BCLK 0.201 0.000
Table of Contents
Fast 1200mV 0C Model
Setup Summary
Hold Summary
Recovery Summary
Removal Summary
Minimum Pulse Width Summary
Worst-Case Timing Paths
Datasheet Report
Metastability Summary
Multicorner Timing Analysis Summary
Multicorner Datasheet Report Summary
Advanced I/O Timing
Clock Transfers
Report TCCS
Report RSKM
IP Catalog
Installed IP
Project Directory
Library
Basic Functions
Bitec
DSP
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Processors and Peripherals
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332146 Worst-case removal slack is 0.488
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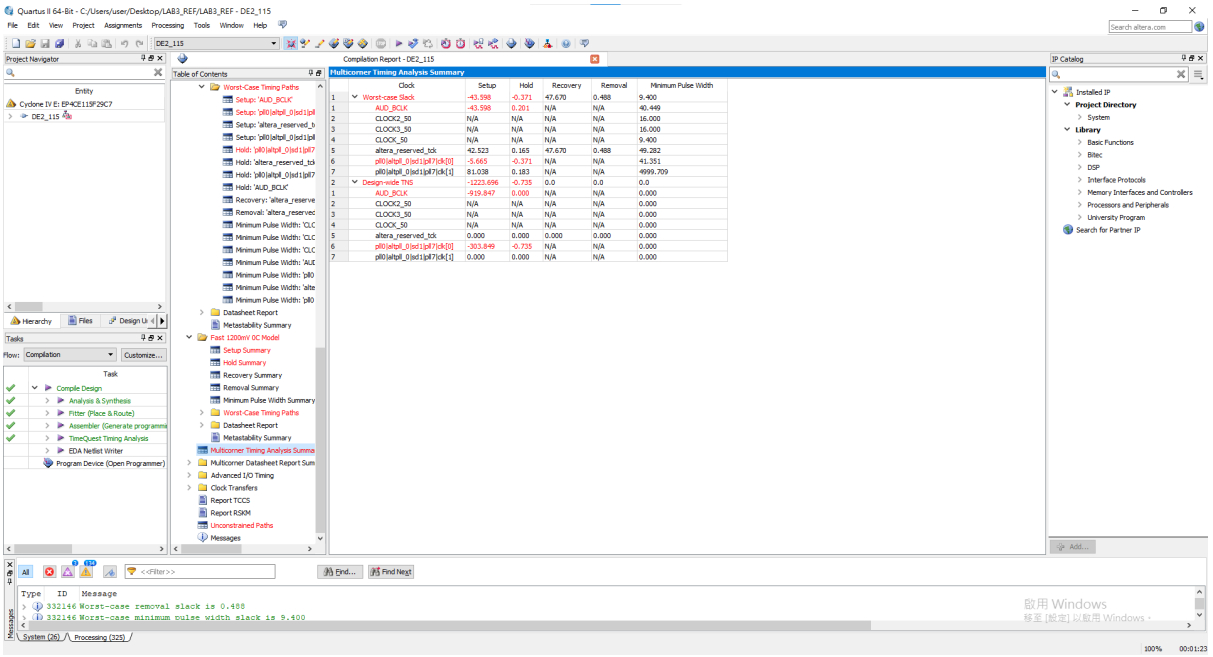
100% 00:01:23




遇到問題的解決方法

debug一開始沒有很好的方式，後來發現軟體內建有示波器signal tab，所以可以直接透過軟體的示波器去看。不然坑很多會很易出事。另外一個問題是pll module沒有特別說他的名字，所以定義pll的時候名字要按照那個或是自己手動改，否則clock會無法出來。坑太多，族繁不及備載。

心得：

這次作業真的太狠了，放出來的瞬間就是心情的最高點了。