

DC Lab1 Report

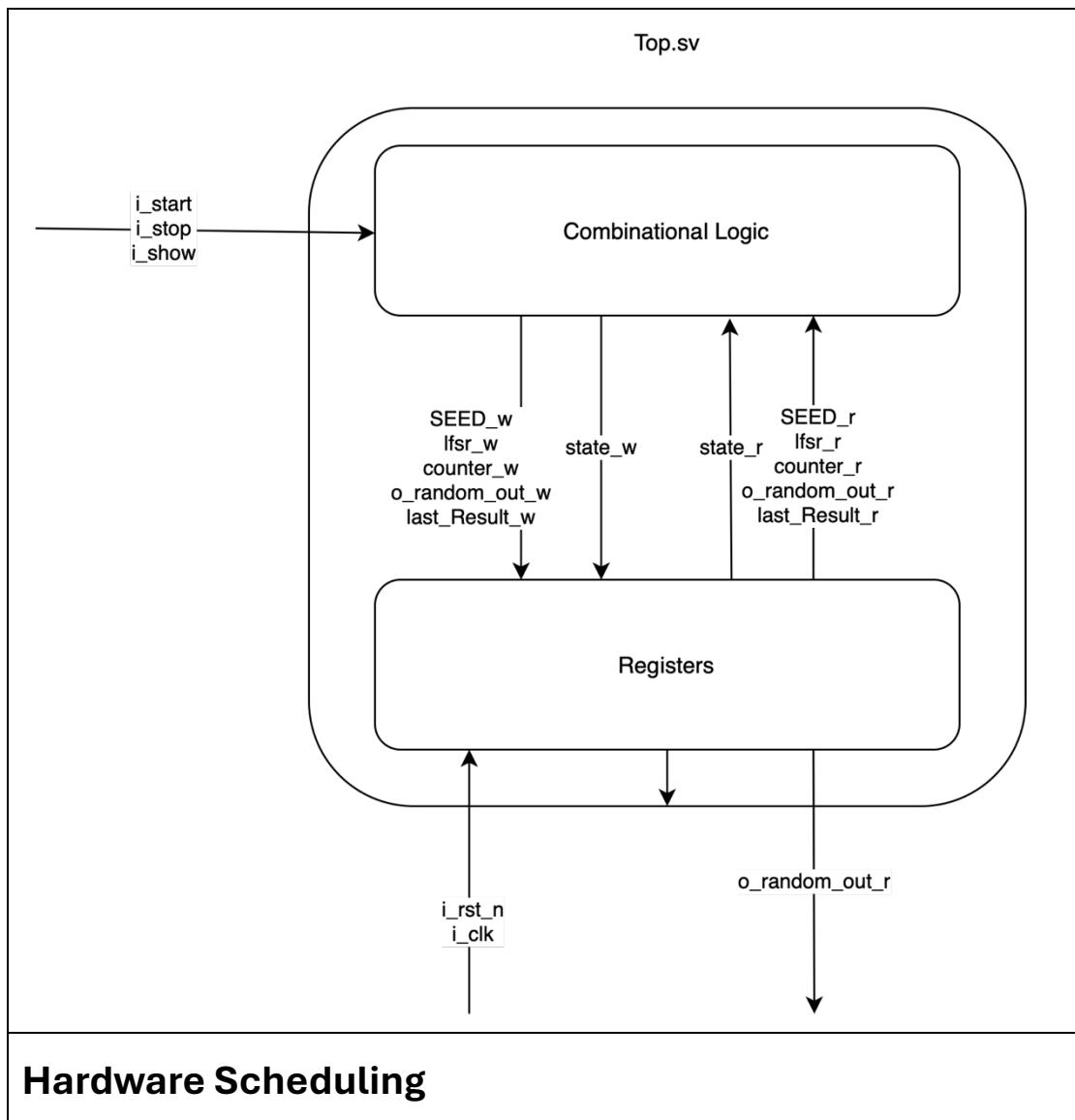
Team 04

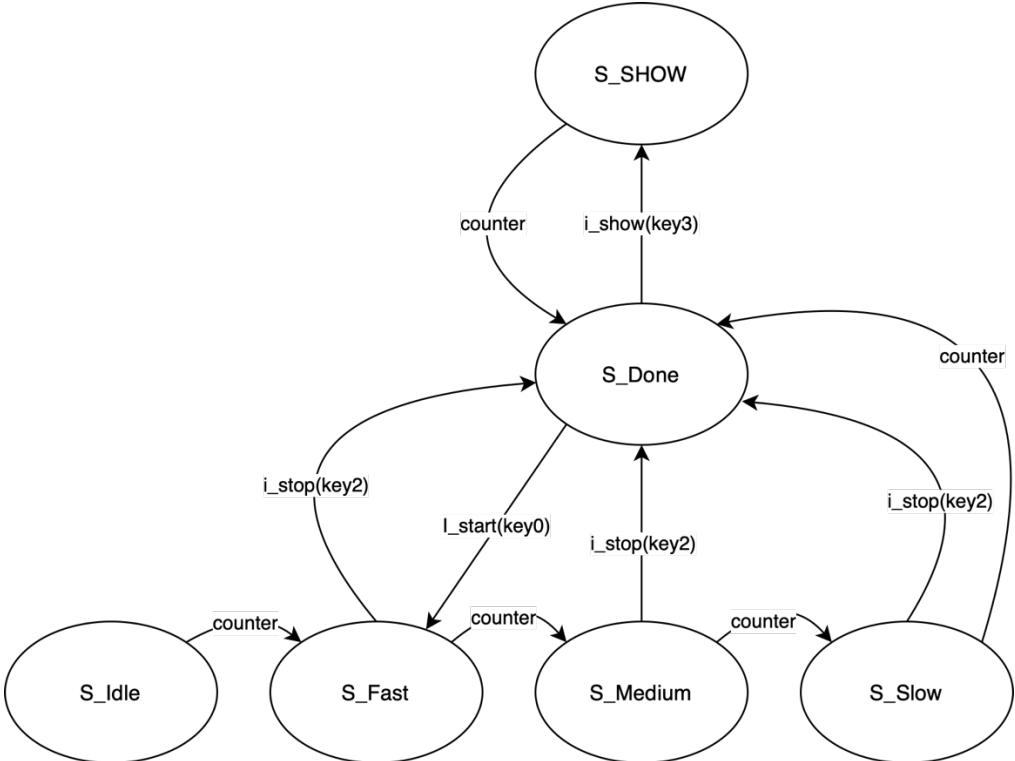
B10901163 張顥譽 B10901176 蔡弘祥 B10901179 鄭承瑞

File Structure

- team04_lab1
 - team04_lab1_report
 - src
 - Top.sv
 - DE2_115.qsf
 - DE2_115.sdc
 - DE2_115.sv
 - SevenHexDecoder.sv
 - Debounce.sv

System Architecture





Signal and Button Explanation

Button	Signal	Description
None	i_clk	Clock signal
key1	i_RST_N	Reset the machine
key0	i_start	Start the machine
key2	i_stop	Freeze the current result
key3	i_show	Display the last result
None	o_random_out	Output signal

State Transition Explanation

The machine operates with several states. The initial state is S_IDLE, and pressing the key0 (i_start) will move it into the S_FAST state. The machine goes through different processing states such as S_FAST, S_MEDIUM, and S_SLOW. If key2 (i_stop) is pressed in any of these states, the machine transitions to S_DONE, freezing the result. After the result is frozen, pressing key3 (i_show)

will transition the machine to S_SHOW, where the last result is displayed. To start the next operation, pressing key0 will take the machine back to S_FAST.

The machine's state transitions automatically based on the clock cycle counts. These transitions are:

- S_FAST to S_MEDIUM after 2^{25} cycles.
- S_MEDIUM to S_SLOW after 2^{25} cycles.
- S_SLOW to S_DONE after 2^{25} cycles.
- S_SHOW to S_DONE after 2^{24} cycles.

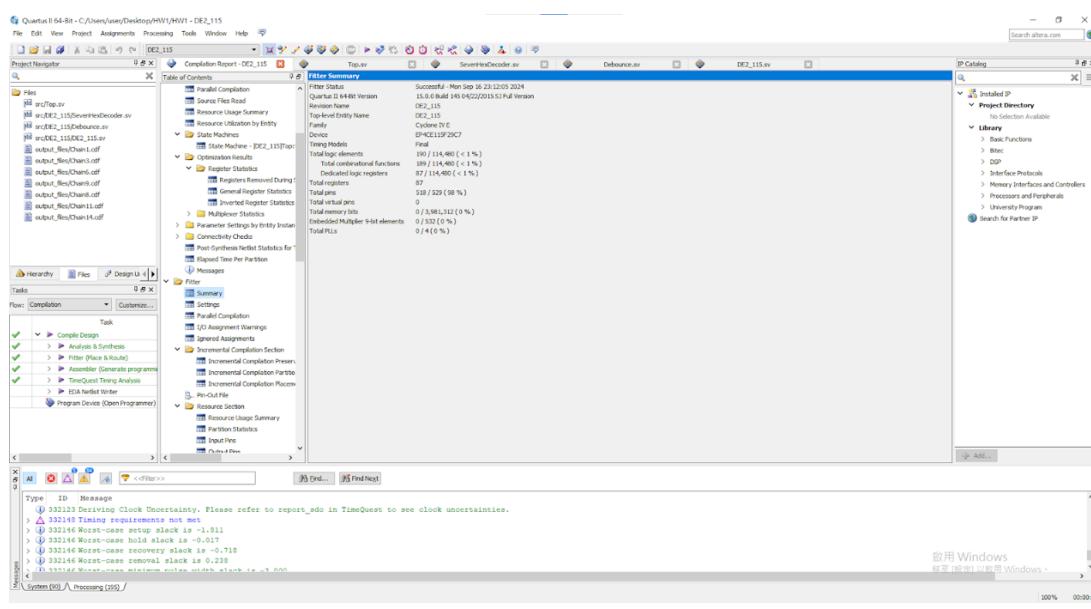
Additionally, pressing key1 (i_RST_N) will reset the machine to the initial state S_IDLE.

Display Change Rate Explanation

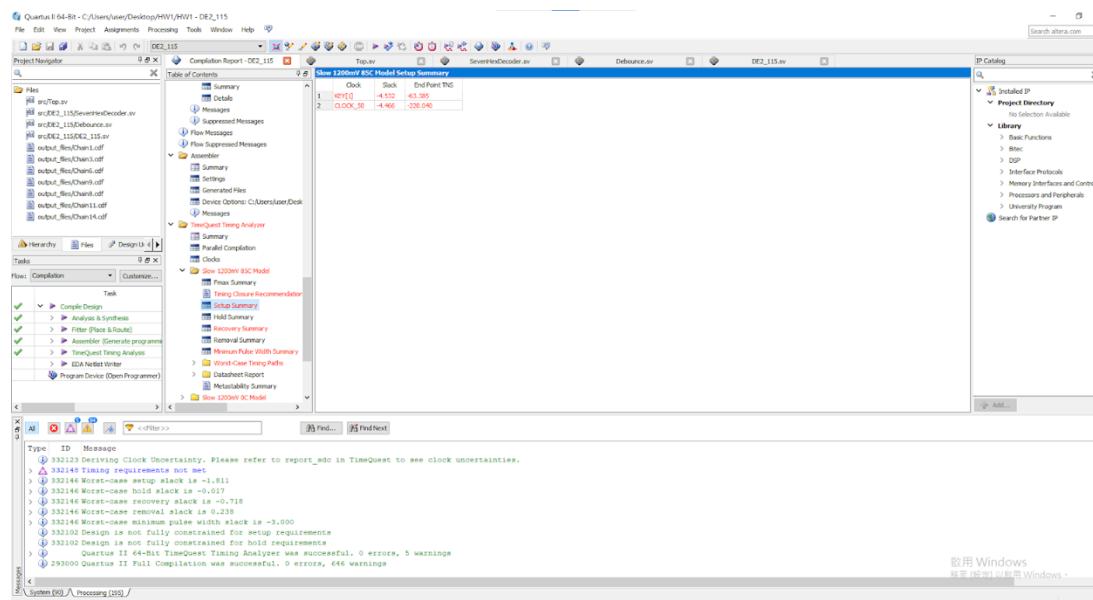
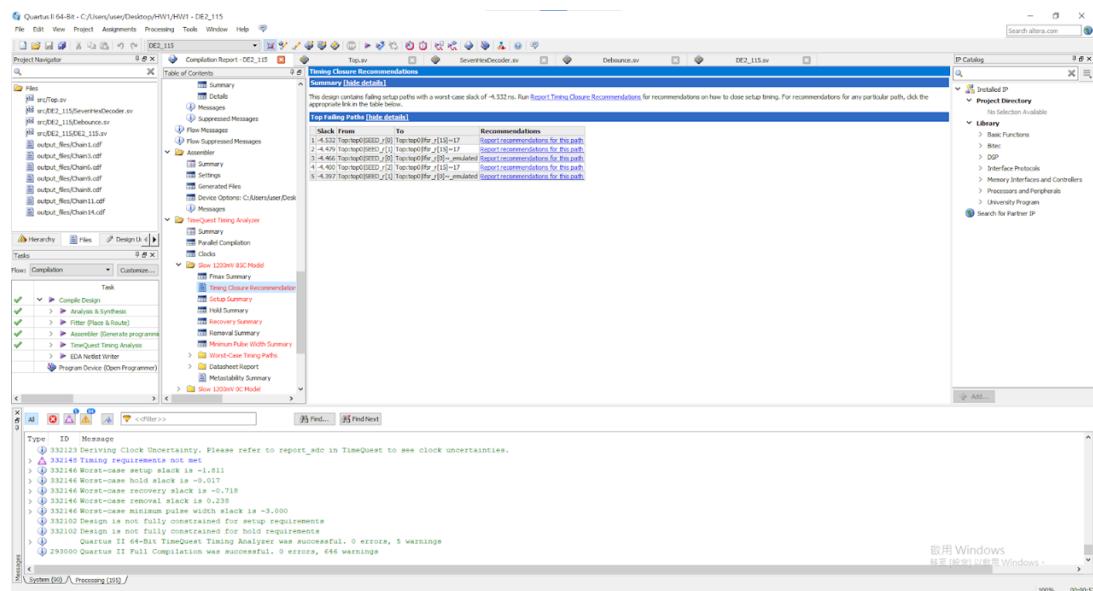
The machine changes its display output at different rates depending on the state it is in:

State	Change Period
S_FAST	2^{19} clock cycles
S_MEDIUM	2^{21} clock cycles
S_SLOW	2^{23} clock cycles

fitter analyzer



timing analyze



setup clock50

Quartus II 64-Bit - C:/Users/USER/Desktop/HW1/HW1 - DE2_115

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Project Navigator 0 # x DE2_115

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File Summary Messages Suppressed Messages Flow Messages Flow Suppressed Messages

Flow Summary Settings Generated Files Device Options: C:/Users/USER/Desktop/HW1/HW1

TimeQuest Timing Analyzer

Summary Parallel Completion Clocks

Show 1200mV I_C Model

Timing Closure Recommender Hold Summary Recovery Summary Removable 'CLOCK_SF' Removal Pulse Width Summary Worst-Case Timing Paths Datasheet Report Metability Summary Show 1200mV I_C Model

Tasks

Compilation 0 # x

Flow: Compilation Customer...

Tasks

Compile Design Analysis & Synthesis Filter (Place & Route) Assembler (Generate program) TimeQuest Timing Analysis EDNA Netlist Writer Program Device (Open Programmer)

All Find... Find Next

Type ID Message

332123 Deriving Clock Uncertainty. Please refer to report_adc in TimeQuest to see clock uncertainties.

332145 Timing requirements not met

332146 Worst-case setup slack is -0.011

332146 Worst-case hold slack is -0.017

332146 Worst-case recovery slack is -0.718

332146 Worst-case removal slack is 0.238

332146 Worst-case minimum pulse width slack is -3.000

332102 Design is not fully constrained for setup requirements

332102 Design is not fully constrained for hold requirements

Quartus II 64-bit TimeQuest Timing Analyzer was successful. 0 errors, 5 warnings

293000 Quartus II Full Compilation was successful. 0 errors, 446 warnings

Messages

System (65) Processing (195) /

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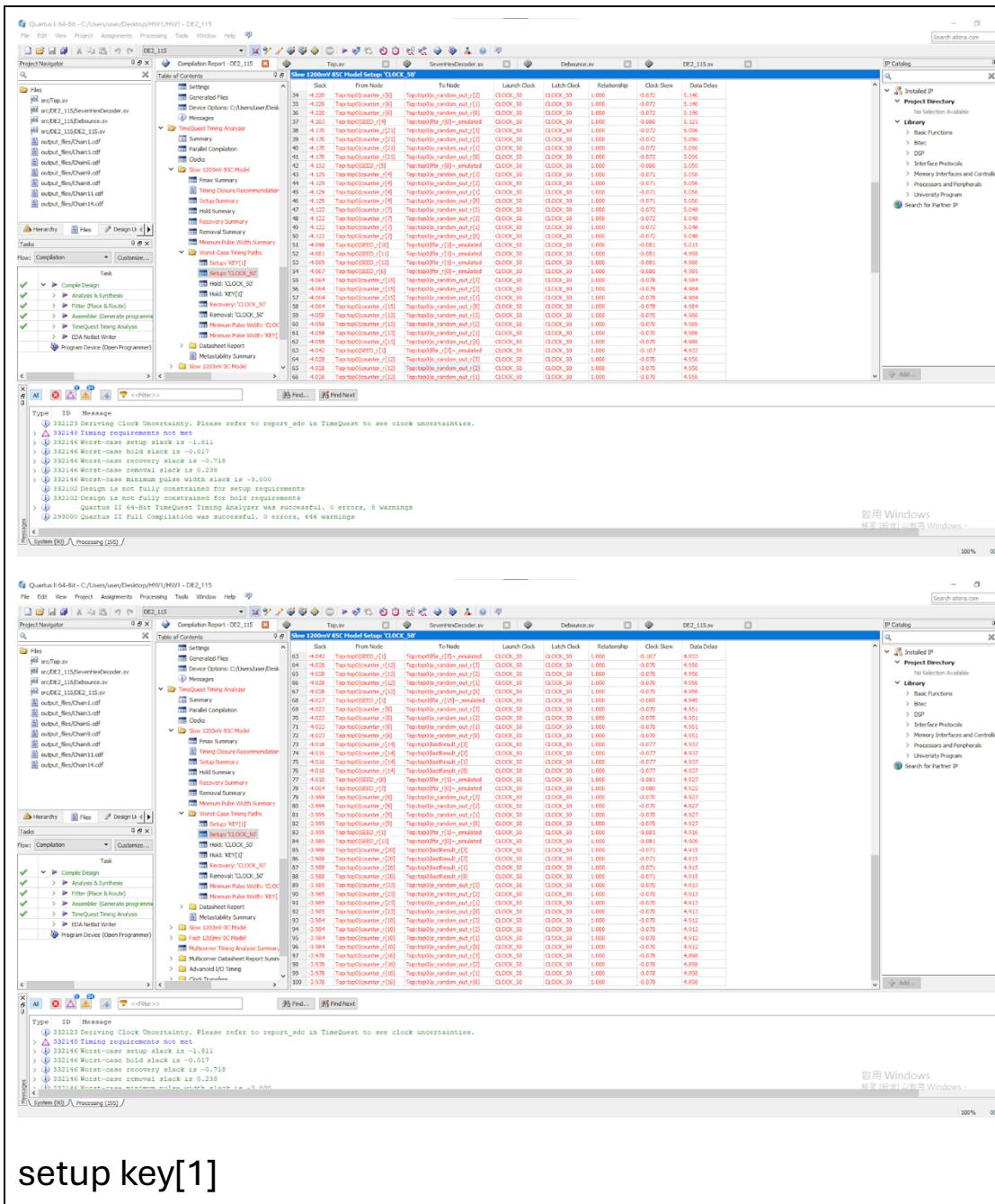
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Task List

Messages

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File Hierarchy

Task

Flow: Compilation

Session: System (65) \ Processing (199) /

Type ID Message

- 332123 Deriving Clock Uncertainty. Please refer to report_mdc in TimeQuest to see clock uncertainties.
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- > 332146 Worst-case removal slack is 0.238
- < 332146 Worst-case minimum cycles width slack is -0.400

Session: System (65) \ Processing (199) /

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File Hierarchy

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Slow 120MHz I2C Model

Sock From Node To Node Launch Clock Latency Clock Relationship Clock Skew Data Delay

Timing Closure Analyzer

Summary Parallel Compilation Clocks

Worst-Case Timing Path Hold CLOCK_SF Hold KEY_SF Recovery CLOCK_SF Recovery Pulse Width CLOCK_SF

Database Report Metability Summary Slow 120MHz I2C Model Fast 120MHz I2C Model Multicore Timing Analysis Advanced I/O Timing Clock Transfers

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minimum pulse width clock50

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Slow 120MHz I2C Model Maximum Pulse Width 'CLOCK_SF'

Sock Actual Width Required Width Type Clock Clock Edge Target

Timing Closure Analyzer

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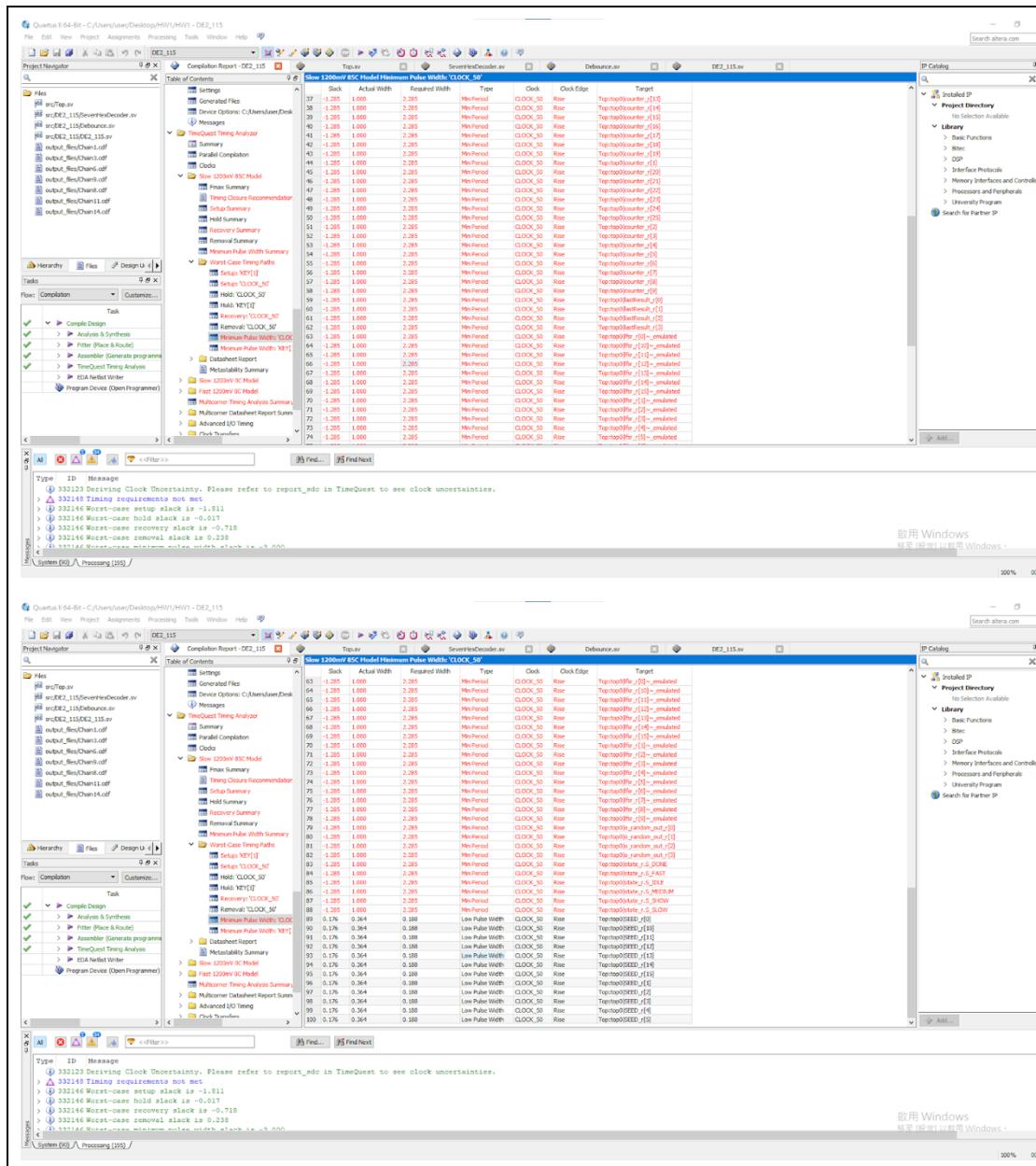
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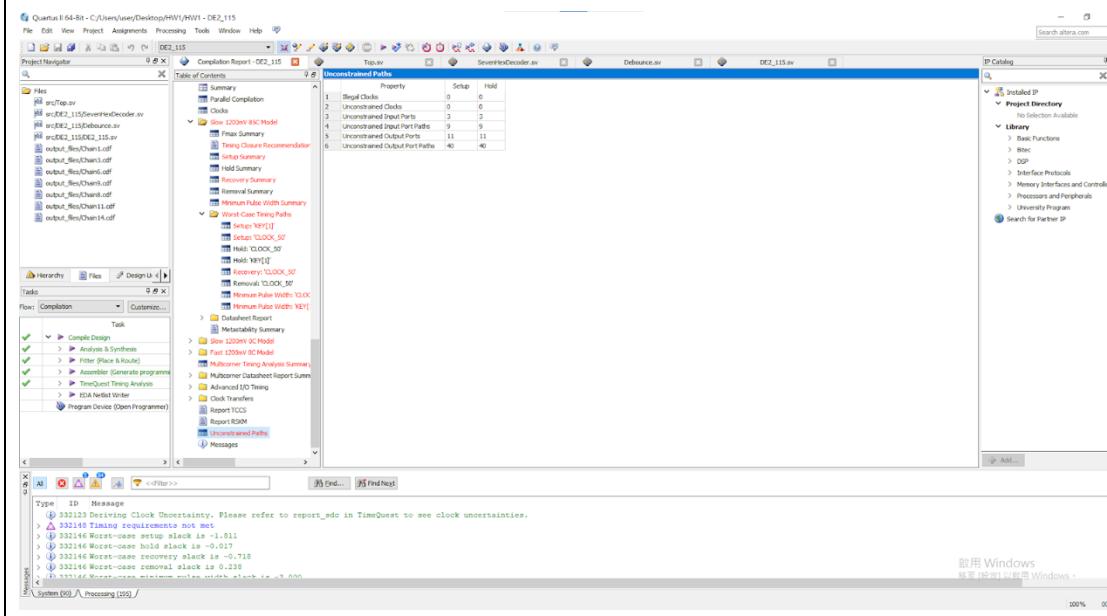
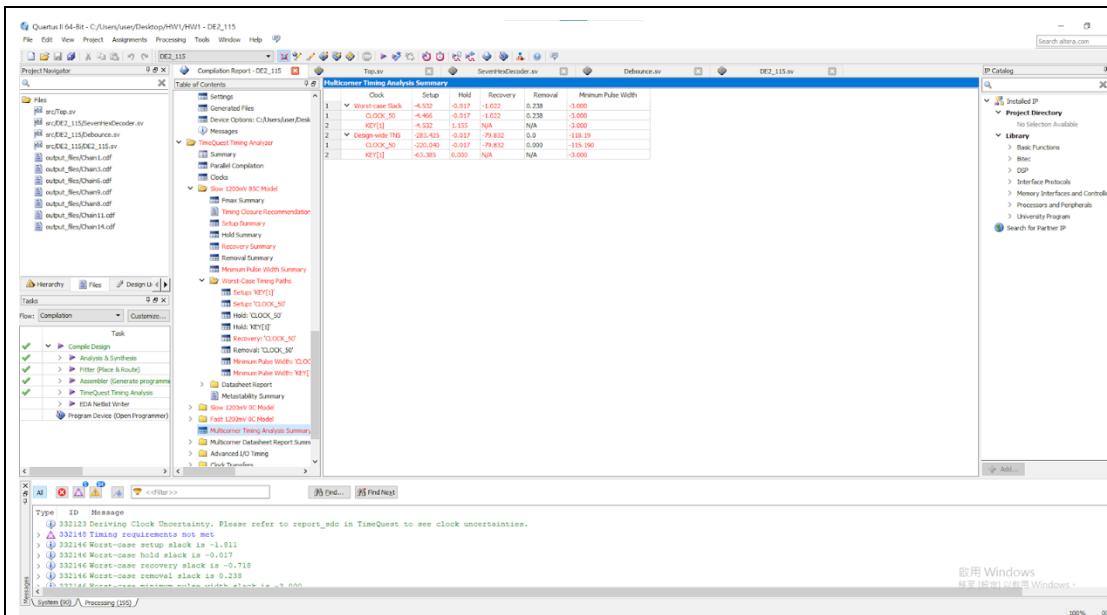
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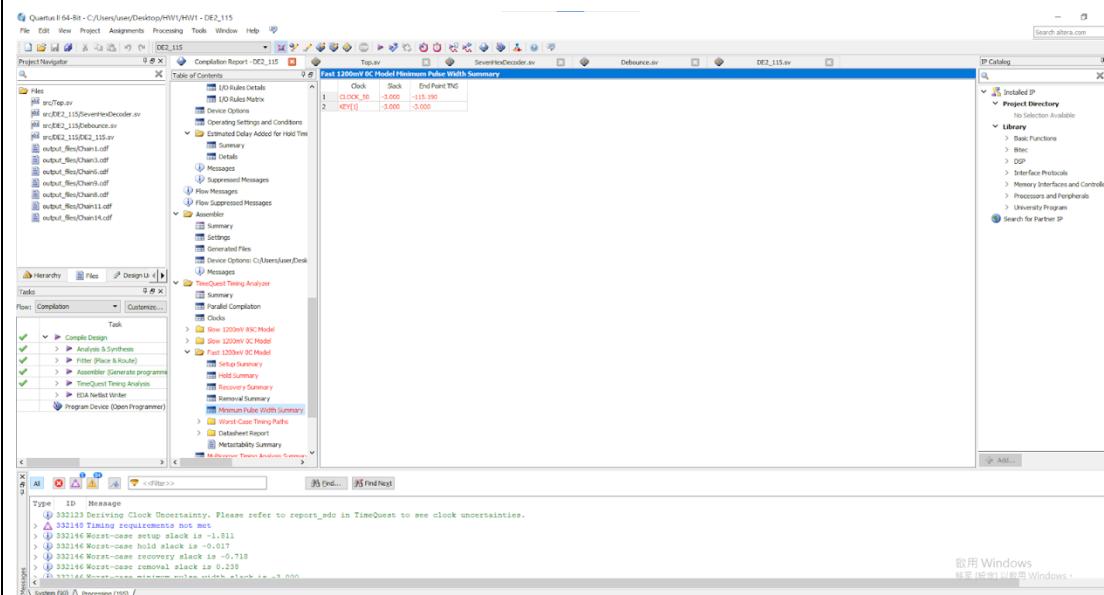
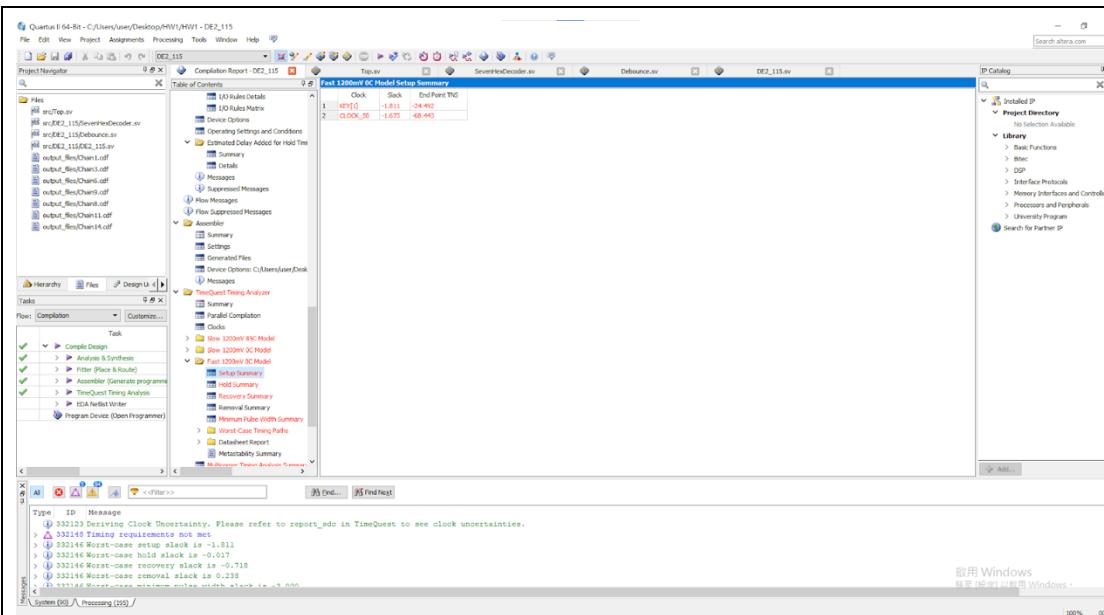
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問題解決

時間長度不合適

因為一開始沒有抓好 clock timing，因此一開始以為有

bug，把很多正確邏輯改的很怪，但是後來調整到一個適

合的時間後，七段顯示器看起來就正常多了

心得

這是第一次用 **FPGA**，真的是非常難用，原本寫好 **verilog**
以為寫好就直接燒上去就很 **arduino** 一樣簡單，沒想到還是出了一堆 **bug**