
NTUEE DCLAB

Introduction to SpyGlass

Presenter: Jeng-Bang Wang

Graduate Institute of Electronics Engineering, National Taiwan University



DCSL



Introduction to SpyGlass Lint

- ❖ The SpyGlass platform provides designers with insight about their design, early in the process at RTL
- ❖ SpyGlass Lint is a comprehensive HDL design rule checker
- ❖ We can use SpyGlass Lint to check the **coding style** of our design and if it is **synthesizable**



Before Using SpyGlass

- ❖ Source the environment settings of CAD tools.

```
source /usr/cad/synopsys/CIC/license.csh
```

```
source /usr/cad/synopsys/CIC/spyglass.cshrc
```



Start SpyGlass

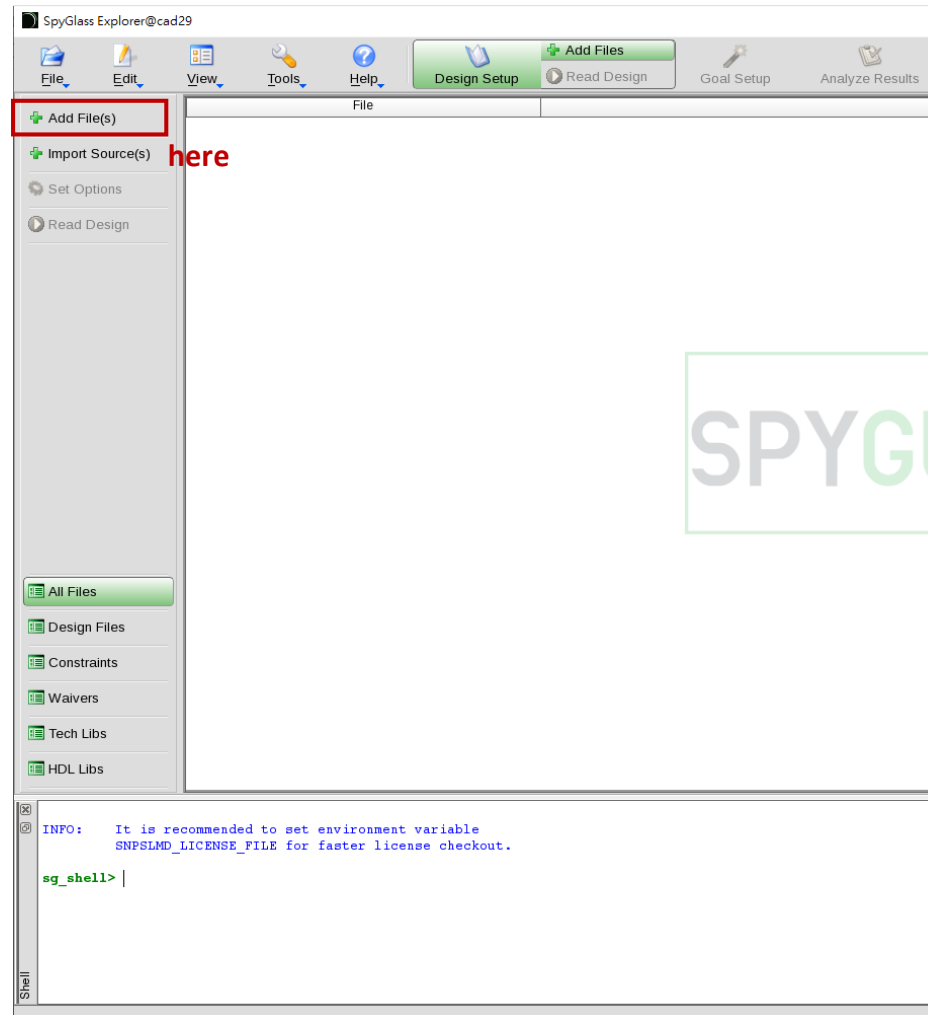
- ❖ Type the following command

```
spyglass &
```

- ❖ The token “&” enable you to use the terminal while Verdi is running in the background.

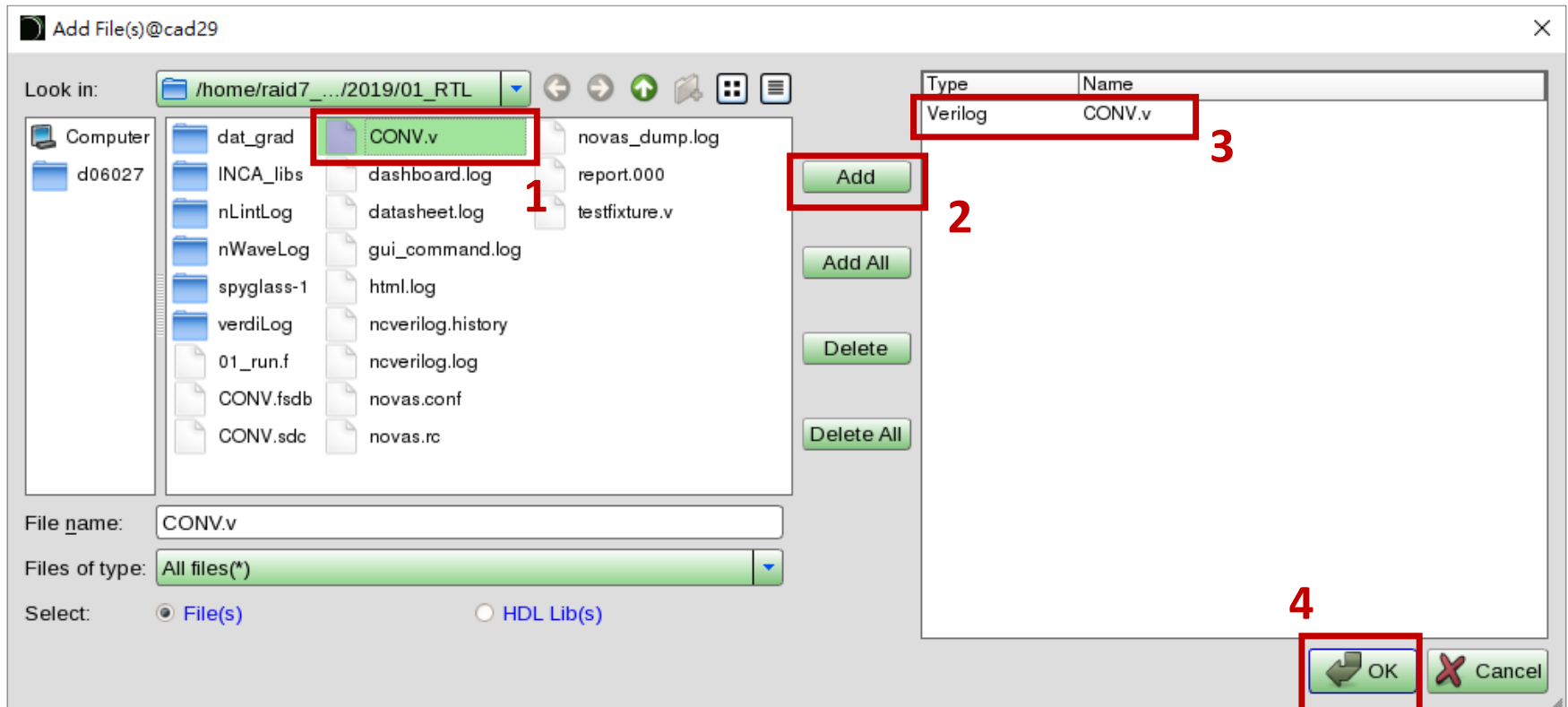


Specify the Design File



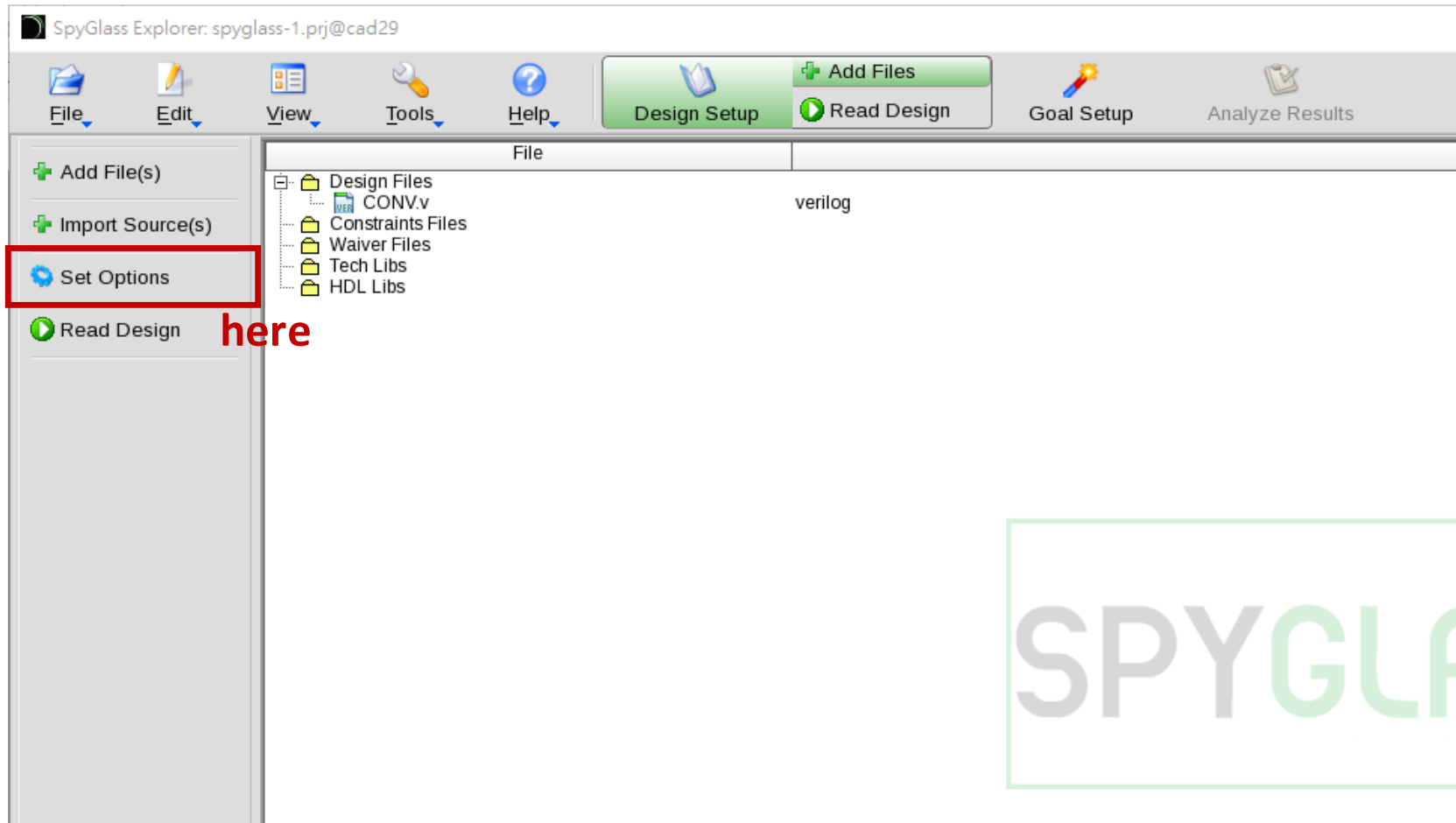


Specify the Design File





Specify Top Module Name





Specify Top Module Name

SpyGlass Explorer: spyglass-1.prj@cad29

File Edit View Tools Help Design Setup Add Files Read Design Goal Setup Analyze Results

+ Add File(s)
+ Import Source(s)
Set Options
Read Design

☐ Advanced Options

Option	Value
Top Level Design Unit	CONV
Stop Design Unit(s)	
Ignore Design Unit(s)	
Diveable Block Abstracted Design Unit(s)	
Interpret Pragma(s)	
Ignore VHDL code within pragma block 'translate'	<input type="checkbox"/>
Ignore VHDL code within pragma block 'synthesis'	<input type="checkbox"/>
Enter Macros for Analysis	
Set HDL Parameter(s) Value	
Searches the specified paths for include files	
Specify the library files in the source design	
Specify the library directories containing libraries	
Specify library file extensions	
Enable System Verilog Processing	<input type="checkbox"/>
Enable auto-compilation of gateslib into sglib	<input type="checkbox"/>
Allow Duplicate Module Names in Verilog Designs	<input type="checkbox"/>
Disable Verilog 2k Processing	<input type="checkbox"/>
Run in VHDL87 Compatibility Mode	<input type="checkbox"/>
Automatically Sort VHDL File(s)	



Read Design

SpyGlass Explorer: spyglass-1.prj@cad29

File Edit View Tools Help Design Setup Add Files Read Design Goal Setup Analyze Results

+ Add File(s)
+ Import Source(s)
Set Options
Read Design

☐ Advanced Options

Option	Value
Top Level Design Unit	CONV
Stop Design Unit(s)	
Ignore Design Unit(s)	
Diveable Block Abstracted Design Unit(s)	
Interpret Pragma(s)	
Ignore VHDL code within pragma block 'translate'	<input type="checkbox"/>
Ignore VHDL code within pragma block 'synthesis'	<input type="checkbox"/>
Enter Macros for Analysis	
Set HDL Parameter(s) Value	
Searches the specified paths for include files	
Specify the library files in the source design	
Specify the library directories containing libraries	
Specify library file extensions	
Enable System Verilog Processing	<input type="checkbox"/>
Enable auto-compilation of gateslib into sglib	<input type="checkbox"/>
Allow Duplicate Module Names in Verilog Designs	<input type="checkbox"/>
Disable Verilog 2k Processing	<input type="checkbox"/>
Run in VHDL87 Compatibility Mode	<input type="checkbox"/>
Automatically Sort VHDL File(s)	



Read Design

SpyGlass Explorer: spyglass-1.prj@cad29

File Edit View Tools Help Design Setup Read Design Add Files Goal Setup Analyze Results

Run Design Read ☐ Synthesize Netlist ☐ Incremental Mode

Click on the 'Run Design Read' button to start the design read.
After the design read is completed, review the results and resolve critical design issues.
The results are displayed as list of messages that can be selected to show additional debug information and features.



Goal Setup

SpyGlass Explorer: spyglass-1.prj@cad29

File Edit View Tools Help Design Setup **Goal Setup** Select Setup Analyze Results

Run Goal(s): 1/49 **3** **1**

Methodology : GuideWare Reference Methodology for rtl_handoff stage of New RTL Block development

Goal	Run Status
GuideWare/latest/block/rtl_handoff	
lint	
lint_rtl	Run Complete (F:0, E:3,...)
lint_turbo_rtl	Not Run Yet
lint_functional_rtl	Not Run Yet
lint_abstract	Not Run Yet
adv_lint	
constraints	
txv_verification	
cdc	
rdc	
dft	
power	
power_verification	
physical	
physical_aware_power	
rtl2netlist	
connectivity_verify	

2



Message Window

SpyGlass Explorer: spyglass-1.prj@cad29

File Edit View Tools Help Design Setup Goal Setup Analyze Results Reports

Run Goal: lint/lint_rtl Incremental Mode MS IS Waiver Design

Instance

CONV

```
1 `timescale 1ns/10ps
2
3
4 module CONV
5     input          clk,
6     input          reset,
7     output reg busy,
8     input          ready,
9
10    output reg [11:0] iaddr,
11    input  [19:0] idata,
12
13    output cwr,
14    output [11:0] caddr_wr,
15    output reg [19:0] cdata_wr,
16
17    output crd,
18    output reg [11:0] caddr_rd,
19    input  [19:0] cdata_rd,
20
21    output [2:0] csel
22 );
23
24
25 //*****
26 // Parameters
27 //*****
28
29
30 CONV_v
```

Modules Instances Files Constraints

Group By: Goal by Rule

Message Tree (Total: 9, Displayed: 9, Waived: 0)

- Design Read (2)
- lintLint_rtl (7)
 - W123 (2): A signal or variable has been read but is not set
 - UndrivenInTerm-ML (1): Undriven but loaded input terminal of an instance detected
 - W528 (4): A signal or variable is set but never read

Violations

Shell Violations Waiver Tree

Not all the warnings or errors are valuable