

DC Lab3 Report

Team 04

B10901163 張顯譽 B10901176 蔡弘祥 B10901179 鄭承瑞

File Structure

team04_lab3

|- src

 |- DE2_115

 |- DE2_115.sv

 |- FastSlow.sv

 |- SevenHexDecoder.sv

 |- Debounce.sv

 |- AudPlayer.sv

 |- AudDSP.sv

 |- AudRecorder.sv

 |- I2cInitializer.sv

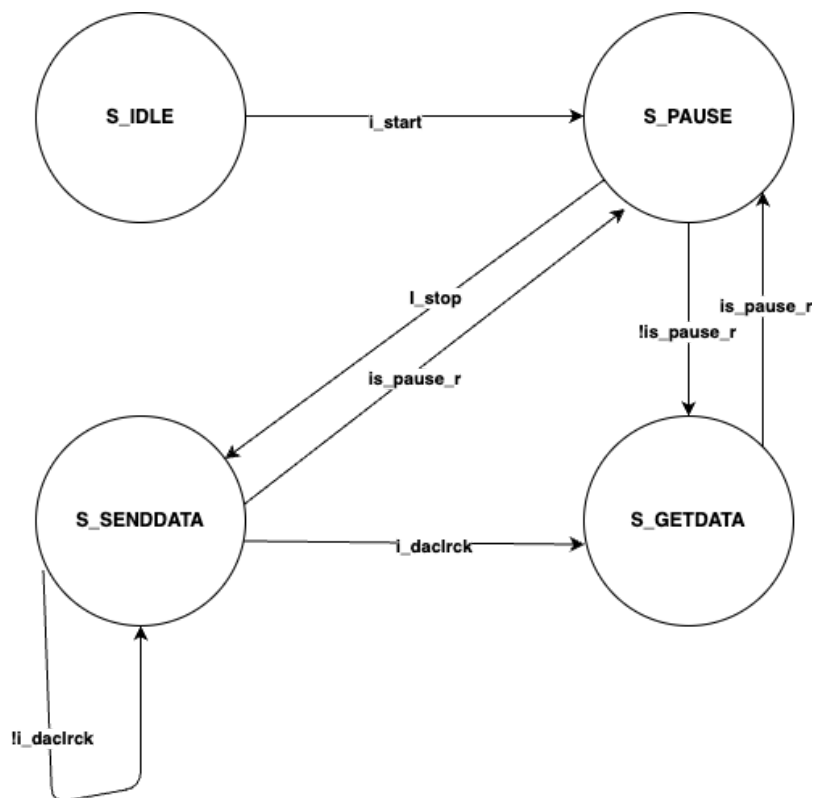
 |- Top.sv

team04_lab3_report

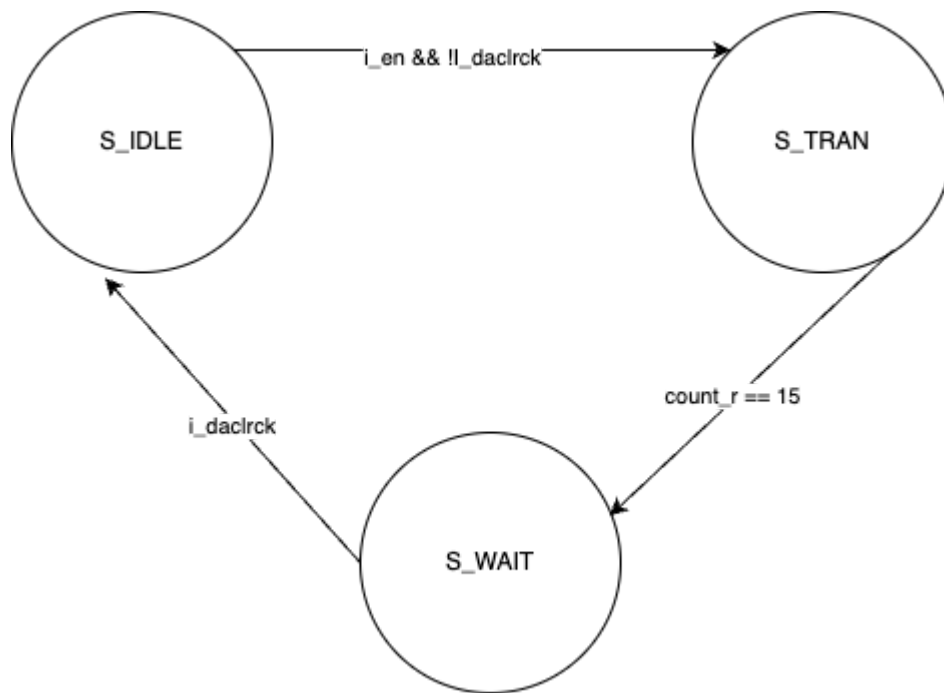
Hardware Scheduling

Modules / Submodules

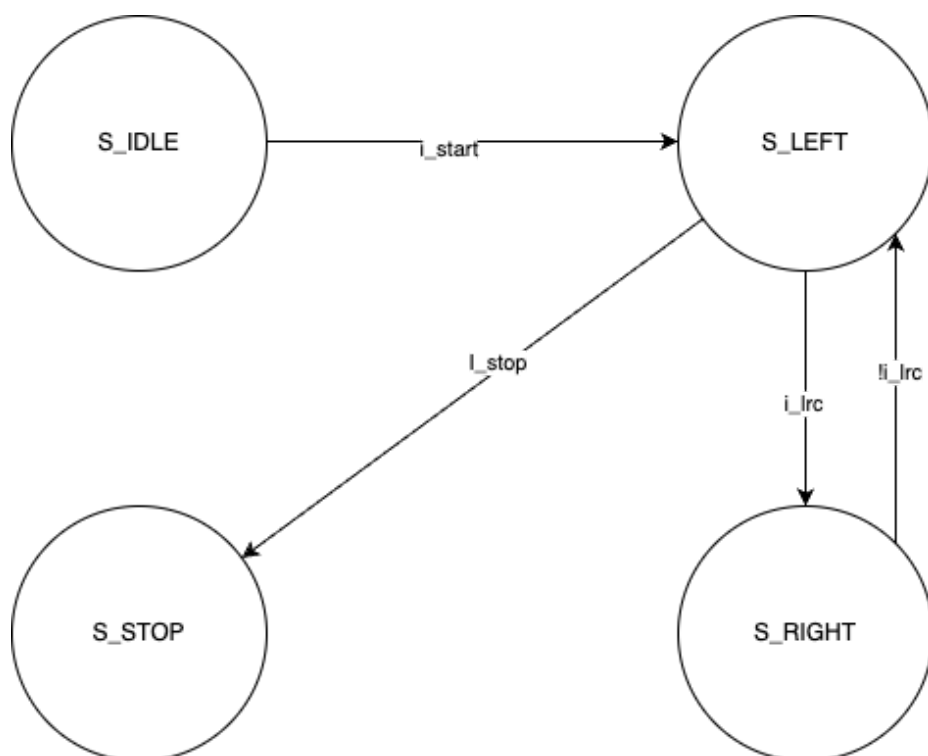
| - AudDSP sv



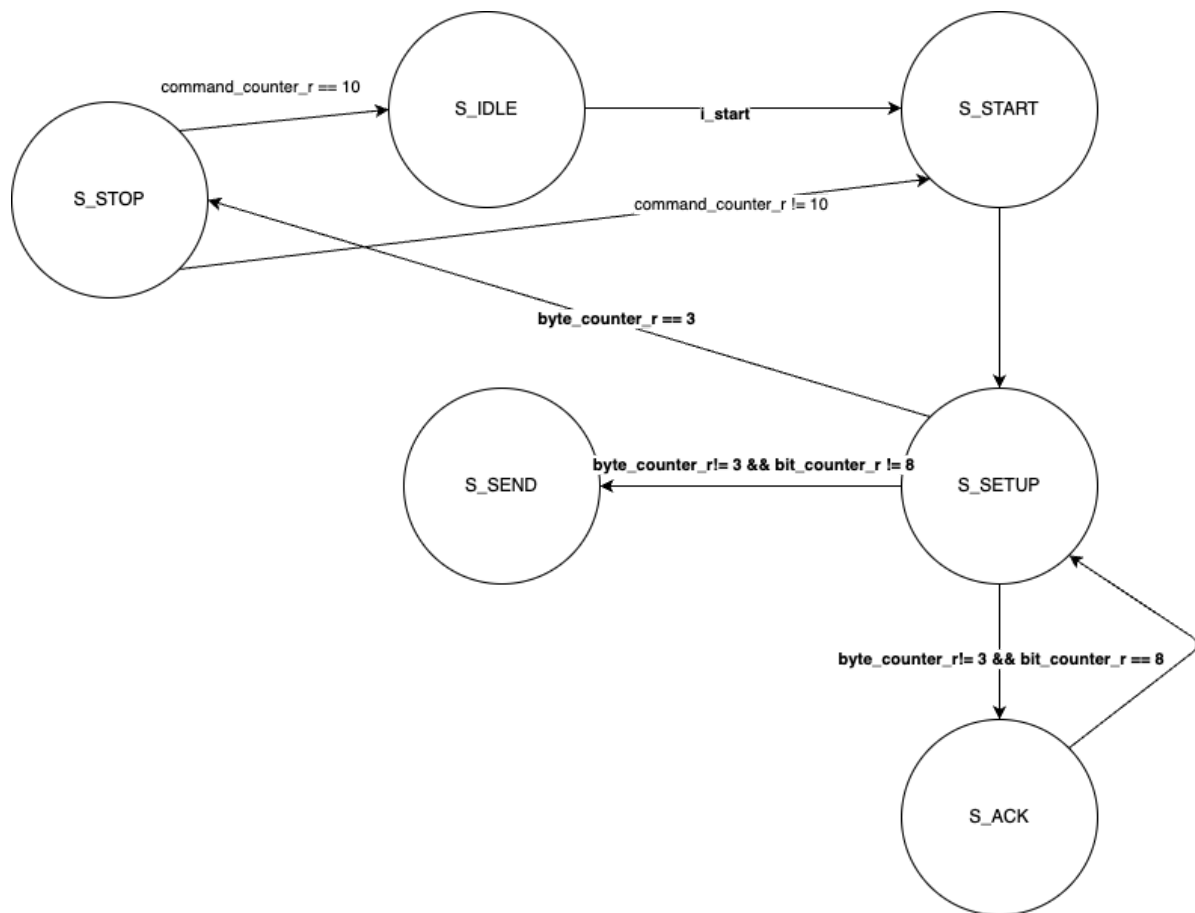
|- AudPlayer.sv



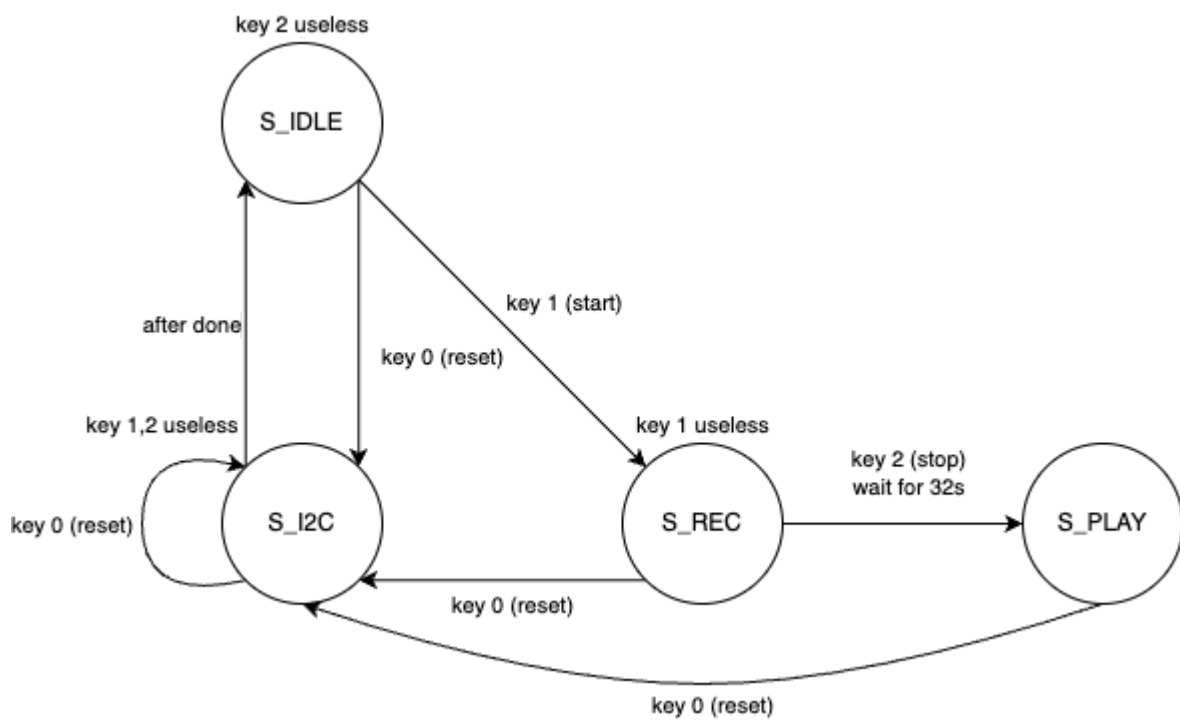
|- AudRecorder.sv



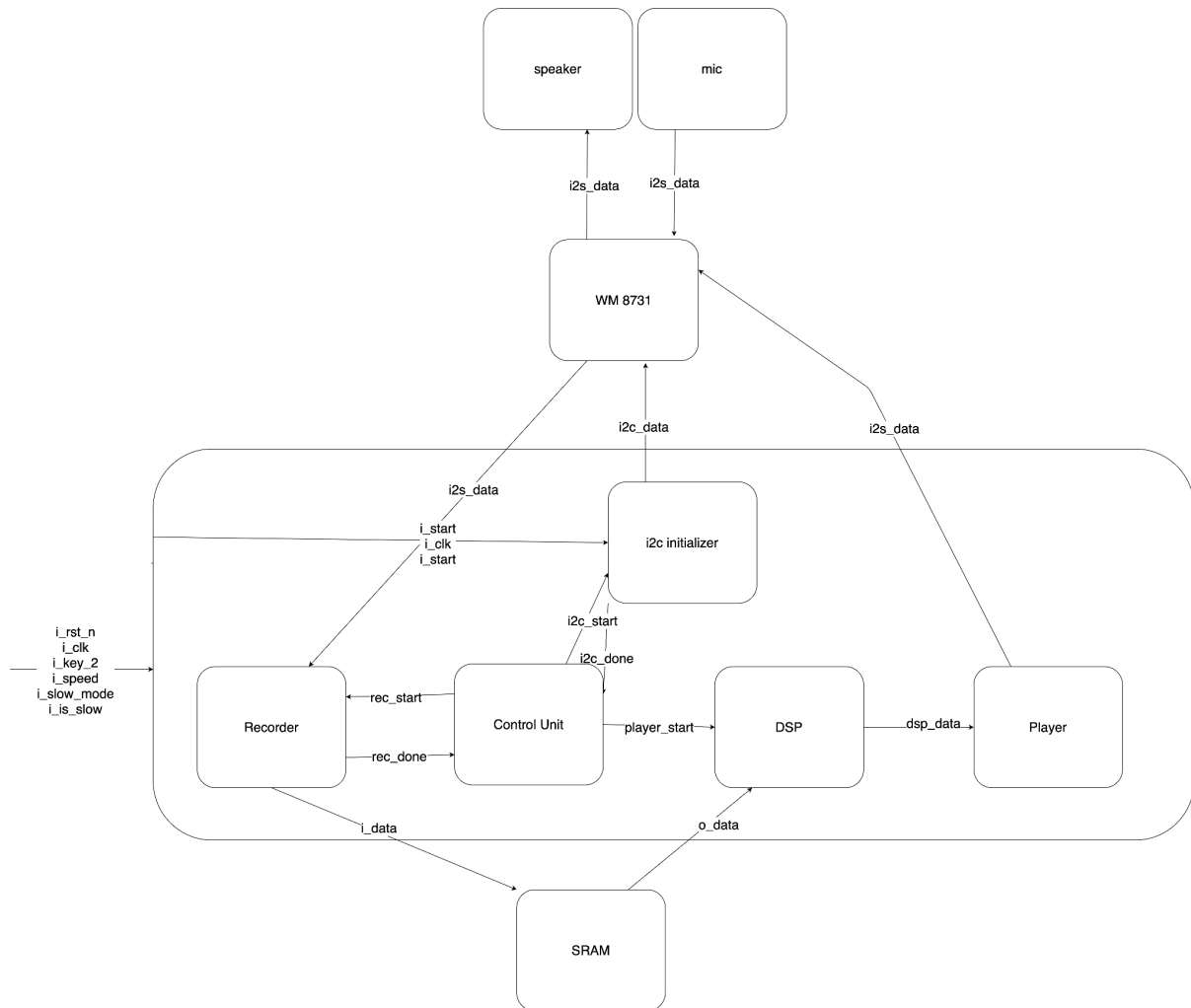
|- I2cInitializer.sv



|- Top.sv



System Architecture



Fitter summary

Quantus II 64-Bit - C:/Users/user/Desktop/Lab3_1/Lab3_1 - DE2_115

File Edit View Project Assignments Processing Tools Window Help

DE2_115

Project Navigator Table of Contents Compiler Report - DE2_115

Analysis & Synthesis

Summary

Settings

Parallel Compilation

I/O Assignment Warnings

Heldset Optimizations

Ignored Assignments

Incremental Compilation Section

Pin-Out File

Resource Section

I/O Rules Section

Device Options

Operating Settings and Conditions

Estimated Delay Added for Hold Times

Messages

Suppressed Messages

New Messages

Flow Suppressed Messages

Assembler

TimeQuest Timing Analyzer

Summary

Parallel Compilation

SDC File List

Clocks

Slow 1200nm BSC Model

Fmax Summary

Timing Closure Recommendations

Setup Summary

Hold Summary

Recovery Summary

Removal Summary

Filter Summary

Filter Status

Quantus II 64-Bit Version

Revision Name

Top-Level Entity Name

Family

Device

Timing Models

Final

Total logic elements

3,124 / 114,480 (3 %)

Total combinational functions

1,712 / 114,480 (2 %)

Dedicated logic registers

2,306 / 114,480 (2 %)

Total registers

2307

Total pins

480 / 529 (91 %)

Total virtual pins

0

Total memory bits

71,968 / 3,981,312 (2 %)

Embedded Multiplier 9-bit elements

2 / 332 (< 1 %)

Total PLBs

1 / 4 (25 %)

IP Catalog

Installed IP

Project Directory

System

Library

Basic Functions

Block

DSP

Interface Protocols

Memory Interfaces and Controllers

Processors and Peripherals

University Program

Search for Partner IP

System (68) / Processing (38) /

在搜尋欄輸入文字來搜尋

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下午 08:55

2024/10/25

TIMING SUMMARY

Quantus II 64-Bit - C:/Users/user/Desktop/LAB3_REF/LAB3_REF - DE2_115

File Edit View Project Assignments Processing Tools Window Help

DE2_115

Project Navigator Table of Contents Compiler Report - DE2_115

Timing Closure Recommendations

Summary [Hide Details]

This design contains failing setup paths with a worst-case slack of -43.598 ns. Run Report Timing Closure Recommendations for recommendations on how to close setup timing. For recommendations for any particular path, click the appropriate link in the table below.

Top Failing Paths [Hide Details]

Slack	From	To	Recommendations
-43.598	Top:top[State]_S_PLAY	Top:top[AuxPlay...ayer0]diff_j14	Report recommendations for this path
-43.577	Top:top[State]_S_PLAY	Top:top[AuxPlay...ayer0]diff_j14	Report recommendations for this path
-43.560	Top:top[State]_S_PLAY	Top:top[AuxPlay...ayer0]diff_j14	Report recommendations for this path
-43.553	Top:top[State]_S_PLAY	Top:top[AuxPlay...ayer0]diff_j14	Report recommendations for this path
-43.553	Top:top[State]_S_PLAY	Top:top[AuxPlay...ayer0]diff_j14	Report recommendations for this path

Slow 1200nm BSC Model

Fmax Summary

Timing Closure Recommendations

Setup Summary

Hold Summary

Recovery Summary

Removal Summary

Minimum Pulse Width Summary

Worst-Case Timing Paths

Datasheet Report

Metastability Summary

Slow 1200nm IC Model

Slow 1700nm IC Model

Filter Summary

Filter Status

Quantus II 64-Bit Version

Revision Name

Top-Level Entity Name

Family

Device

Timing Models

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University Program

Search for Partner IP

System (26) / Processing (225) /

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Quantus II 64-Bit - C:/Users/user/Desktop/LAB3_REF/LAB3_REF - DE2_115

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Project Navigator

Entity

Cyclone IV E: EP4KCE119P25C7

DE2_115

Table of Contents

Slow 1200mV BSC Model Setup Summary

Flow Summary

Flow Settings

Flow Non-Default Global Settings

Flow Elapsed Time

Flow OS Summary

Flow Log

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Flow Messages

Flow Suppressed Messages

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Hold Summary

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Removal Summary

Minimum Pulse Width Summary

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Datasheet Report

Metastability Summary

Slow 1200mV OC Model

Fast 1700mV OC Model

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Processors and Peripherals

University Program

Search for Partner IP

Messages

Type ID Message

332146 Worst-case removal slack is 0.488

332146 Worst-case minimum pulse width slack is 9.400

332009 The launch and latch times for the relationship between source clock: pll0altpll0_0adilpl17clk[0] and destination clock: AUD_BCLK are outside of the legal time range. The relationship difference is correct, however the 1

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332102 Design is not fully constrained for setup requirements

332102 Design is not fully constrained for hold requirements

Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 20 warnings

293000 Quartus II Full Compilation was successful. 0 errors, 603 warnings

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Quantus II 64-Bit - C:/Users/user/Desktop/LAB3_REF/LAB3_REF - DE2_115

File Edit View Project Assignments Processing Tools Window Help

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Project Navigator

Entity

Cyclone IV E: EP4KCE119P25C7

DE2_115

Table of Contents

Slow 1200mV BSC Model Hold Summary

Flow Summary

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Flow Non-Default Global Settings

Flow Elapsed Time

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Slow 1200mV OC Model

Fast 1700mV OC Model

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The screenshot shows the Quartus II 64-bit IDE interface. The top menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The main window is divided into several panes:

- Project Navigator:** Shows the project hierarchy for DE2_115, including the Entity (Cyclone IV EP4C115P2C7) and various files like DE2_115.qsf.
- Table of Contents:** Lists the contents of the project, including the Minimum Pulse Width Summary, Worst-Case Timing Paths, and various setup/hold time reports.
- Completion Report - DE2_115:** Displays the timing and setup/hold times for various components. The report is organized into sections for different components and their timing parameters.
- IP Catalog:** Shows the installed IP components, including Project Directory, System, Library, Basic Functions, Block, DSP, Interface Protocol, Memory Interface and Controllers, Processors and Peripherals, and University Program.

The Completion Report - DE2_115 pane shows the following data:

Component	Minimum Pulse Width Summary	Worst-Case Timing Paths	Setup	Hold	Recovery	Removal
ALU	39.445	-440.295	-6.132	-273.265	-	-
altera_reserved_sck	43.208	0.000	-	-	-	-
altera_reserved_b	81.218	0.000	-	-	-	-

[illegible][illegible]

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File Edit View Project Assignments Processing Tools Window Help

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Project Navigator DE2_115 Table of Contents DE2_115

Entity
Cyclone IV E: EP4KCE119P25C7
DE2_115

Tasks
Flow: Completion
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate program)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)

Table of Contents
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Slow 1200nm OC Model
Free Summary
Setup Summary
Hold Summary
Recovery Summary
Removal Summary
Minimum Pulse Width Summary
Worst-Case Timing Paths
Setup: 'ALD_BCLK'
Setup: 'p0(altpd_0)pd1(p07)ck[0]'
Setup: 'altera_reserved_is'
Setup: 'p0(altpd_0)pd1(p07)ck[0]'
Hold: 'p0(altpd_0)pd1(p07)ck[0]'
Hold: 'altera_reserved_is'
Hold: 'p0(altpd_0)pd1(p07)ck[0]'
Hold: 'ALD_BCLK'
Recovery: 'altera_reserved'
Removal: 'altera_reserved'
Minimum Pulse Width: 'VLC'
Minimum Pulse Width: 'VLC'
Minimum Pulse Width: 'VLC'
Minimum Pulse Width: 'ALC'
Minimum Pulse Width: 'p0'
Minimum Pulse Width: 'altera_reserved'
Minimum Pulse Width: 'p0'
DataSheet Report
Metastability Summary
Fast 1200nm OC Model
Setup Summary
Hold Summary
Recovery Summary
Removal Summary
Minimum Pulse Width Summary
Worst-Case Timing Paths
DataSheet Report
Metastability Summary

Fast 1200nm OC Model Setup Summary

	Clock	Slack	End Point TNS
1	ALD_BCLK	21.620	-461.902
2	p0(altpd_0)pd1(p07)ck[0]	-2.909	-157.371
3	altera_reserved_is	46.476	0.000
4	p0(altpd_0)pd1(p07)ck[0]	62.136	0.000

IP Catalog
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Basic Functions
Blac
DSP
Interface Protocols
Memory Interfaces and Controllers
Processors and Peripherals
University Program
Search for Partner IP

Message
Type ID Message
332146 Worst-case removal slack is 0.488
332146 Worst-case minimum pulse width slack is 9.400
System (26) / Processing (25)

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File Edit View Project Assignments Processing Tools Window Help

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Project Navigator DE2_115 Table of Contents DE2_115

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Hold: 'p0(altpd_0)pd1(p07)ck[0]'
Hold: 'altera_reserved_is'
Hold: 'p0(altpd_0)pd1(p07)ck[0]'
Hold: 'ALD_BCLK'
Recovery: 'altera_reserved'
Removal: 'altera_reserved'
Minimum Pulse Width: 'VLC'
Minimum Pulse Width: 'VLC'
Minimum Pulse Width: 'VLC'
Minimum Pulse Width: 'ALC'
Minimum Pulse Width: 'p0'
Minimum Pulse Width: 'altera_reserved'
Minimum Pulse Width: 'p0'
DataSheet Report
Metastability Summary
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Removal Summary
Minimum Pulse Width Summary
Worst-Case Timing Paths
DataSheet Report
Metastability Summary
Multicorner Timing Analysis Summary
Multicorner DataSheet Report Summary
Advanced I/O Timing
Clock Transfers
Report TCCS
Report RSM

Fast 1200nm OC Model Setup Summary

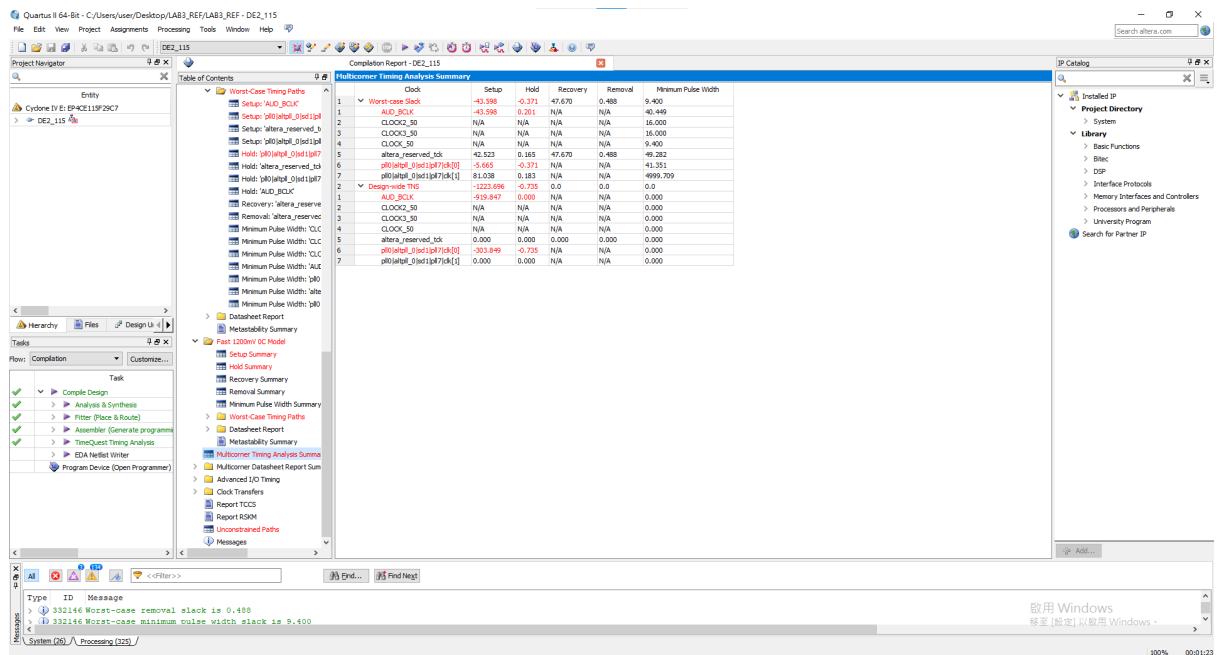
	Clock	Slack	End Point TNS
1	p0(altpd_0)pd1(p07)ck[0]	-0.175	-0.345
2	altera_reserved_is	0.165	0.000
3	p0(altpd_0)pd1(p07)ck[0]	0.163	0.000
4	ALD_BCLK	0.201	0.000

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System (26) / Processing (25)

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遇到問題的解決方法

debug一開始沒有很好的方式，後來發現軟體內建有示波器signal tab，所以可以直接透過軟體的示波器去看。不然坑很多會很易出事。另外一個問題是pll module沒有特別說他的名字，所以定義pll的時候名字要按照那個或是自己手動改，否則clock會無法出來。坑太多，族繁不及備載。

心得：

這次作業真的太狠了，放出來的瞬間就是心情的最高點了。