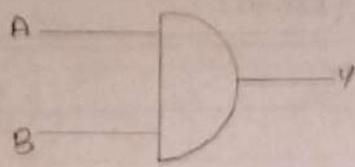


Particulars of the Experiments Performed

CONTENTS

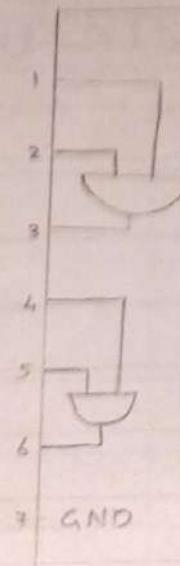
Sl. No.	Date	TITLE OF THE EXPERIMENTS	Page No.		Marks	Initial of Staff
			From	To		
1	26/07/2019	Realization of Basic Gates	01	03		
2	02/08/2019	Realization of AND, OR, & NOT	04	06		
3	09/08/2019	Realization of half adder & subtractor	07	08		
4	16/08/2019	Realization of full adder.	09	11		
5	23/08/2019	Realization of 4 bit adder/subtractor	12	13		
6	30/08/2019	Realization of BCD Adder	14	15		
7	06/09/2019	Realization of JK Flip Flop	16	17		
8	06/09/2019	Realization of T & D Flip Flop	18	19		
9	13/09/2019	Implementation of odd/even parity	23	24		
10	20/09/2019	Implementation of PISO Shift Register	20	22		
11	27/09/2019	Realization of Boolean Expression	25	—		
12	27/09/2019	Realization of half adder	26	27		
13	04/10/2019	Realization of half subtractor	28	29		
14	04/10/2019	Realization of 3 bit binary to Gray code	30	31		
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17	18/10/2019	Realization of RS flip flop	36	37		
18	18/10/2019	Implementation of PIPO Shift reg.	38	39		
19	25/10/2019	Implementation of SISO Using JK	40	41		
20	08/11/2019	Implementation of PISO shift reg.	42	43		
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22						
23						
24						
25						

1. AND Gate

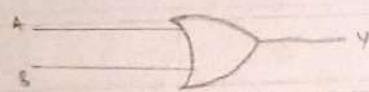


DIP Diagrams

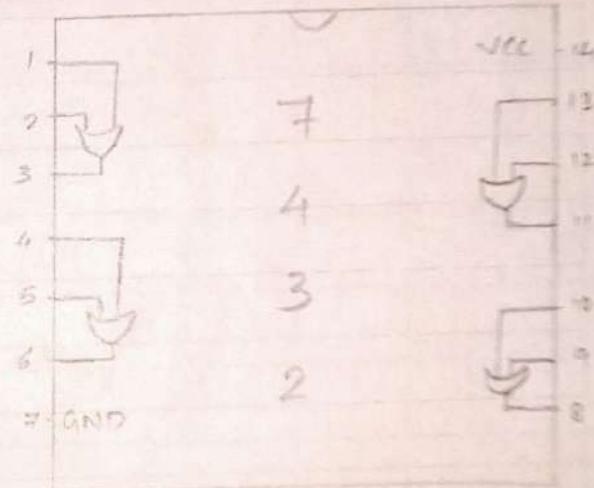
Input	Output	
A	B	$Y = AB$
0	0	0
0	1	0
1	0	0
1	1	1



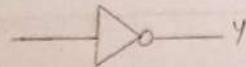
OR Gate



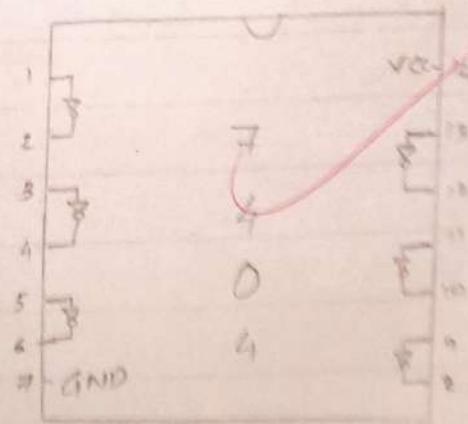
Input	Output	
A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1



NOT GATE



Input	Output
A	$Y = \bar{A}$
0	1
1	0



1

Realisation of Basic Gates

AND OR NOT NAND NOR XOR

Aim :- To Study the operations of basic logic gates

Components Required :

AND → IC 7408

OR → IC 7432

NOT → IC 7404

NAND → IC 7400

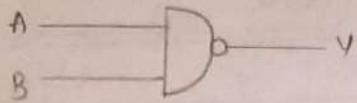
NOR → IC 7402

XOR → IC 7483

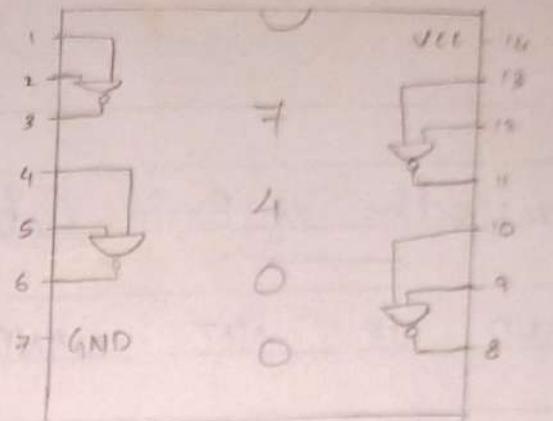
Equipments Required :

Digital IC trainer kit, patch cards

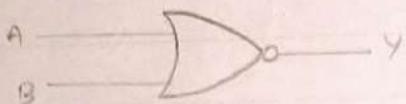
NAND GATE



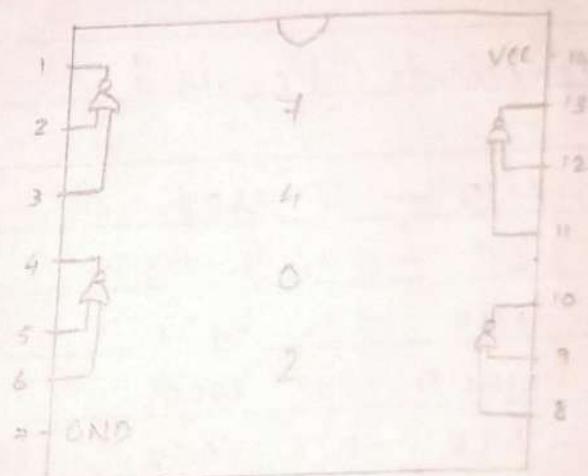
Input		Output
A	B	$Y = \bar{A}\bar{B}$
0	0	1
0	1	1
1	0	1
1	1	0



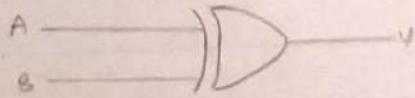
NOR GATE



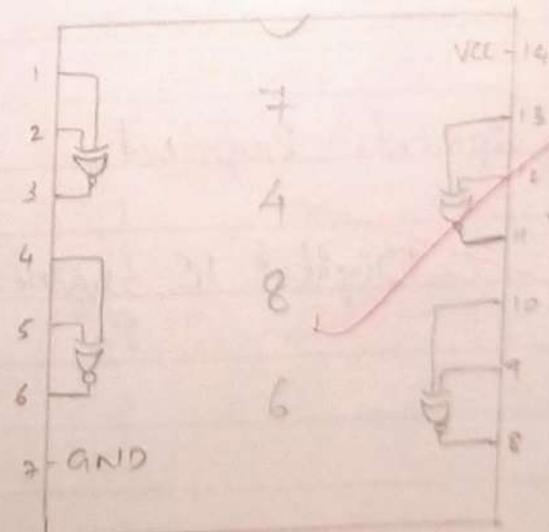
Input		Output
A	B	$Y = A+B$
0	0	1
0	1	0
1	0	0
1	1	0



XOR GATE



Input		Output
A	B	$Y = AB$
0	0	0
0	1	1
1	0	1
1	1	0



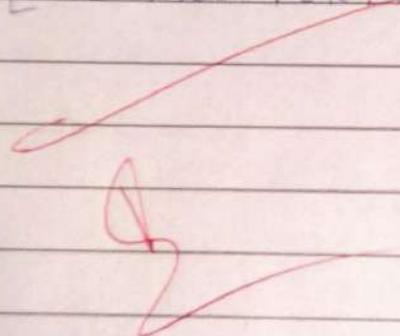
Procedure :-

- * All components and patch cards are test for good working condition.
- * To Study the operation of each logic gates. The appropriate IC's is inserted into socket IC base and is lock by moving the lever downwards.
- * Connections are made by using patch cards according to the details shown in pin pin diagram.
- * The Circuit connections are verify thoroughly
- * Power Supply is given to the trainer kit.
- * ~~Truth table~~ input conditions are set up.
- * Output are observed for all cases of input conditions.

Result :-

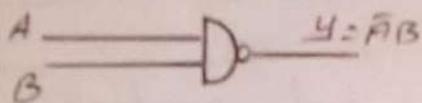
Verify the truth table and realize
the Logic gates.

[AND, NOT, OR, ~~ANAND~~, NOR, XOR]

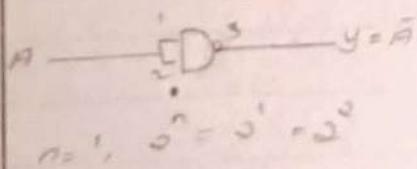
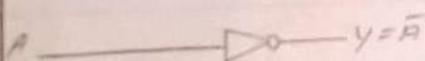


NAND gati or universal gati

Nand gati



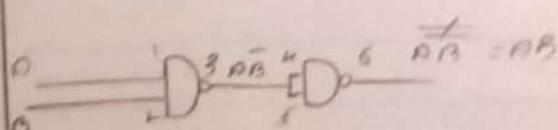
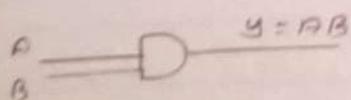
NAND gati as NOT gate :-



Truth table

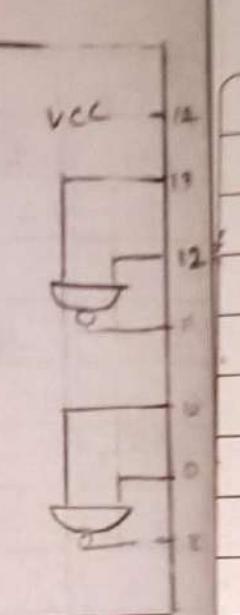
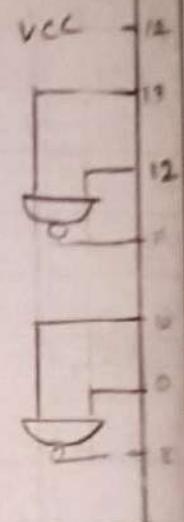
Input	Output
1	$Y = \bar{A} = 0$
0	1
1	0

> NAND Gate 175 And Gate



Truth table

Input	Output
0 0	0
0 1	0
1 0	0
1 1	1



2 Realisation of AND OR NOT Gates Using Universal Gates :-

* Aim :- To realize AND, OR, NOT Gate using Universal Gates NAND & NOR

* Components Required :-

1, IC 7400 NAND Gate

2, IC 7402 NOR Gate

* Equipments Required :-

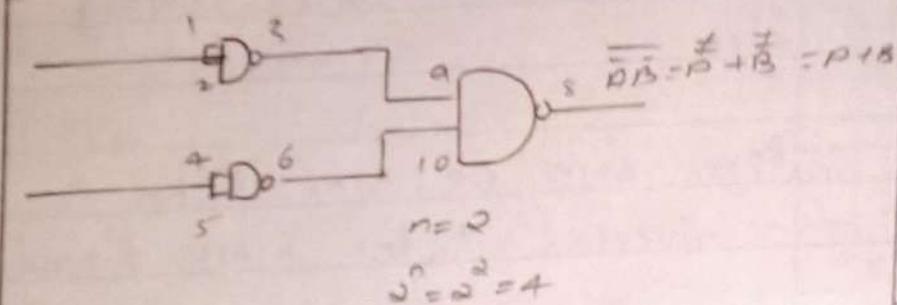
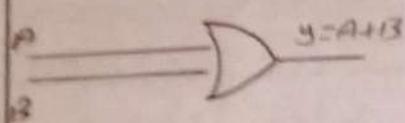
Digital IC trainer kit and patch cards

~~* Procedure :-~~

1, All Components and patch cards are tested for good working Condition.

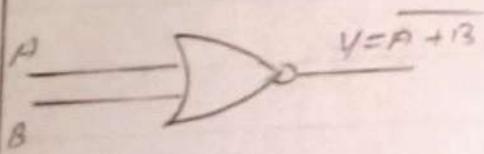
2, Appropriate IC's are Inserted into

NAND gate as OR gate :-

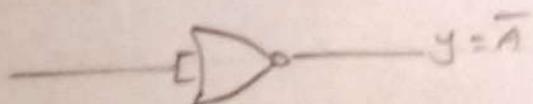
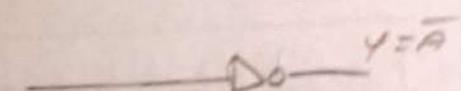


Input	Output
A B	$Y = A + B$
0 0	0
0 1	1
1 0	1
1 1	1

NOR gate as universal gate



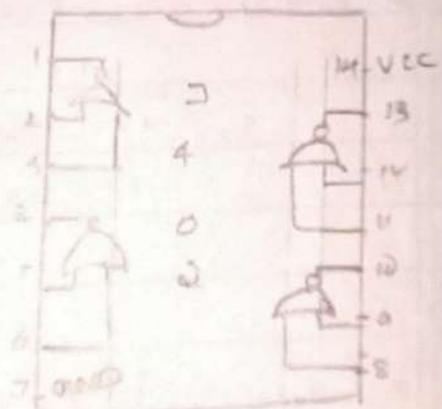
> NOR gate as NOT gate



$$n = 1$$

$$S = \omega L Q_H$$

Input	Output
0	$Y = 1$
1	0



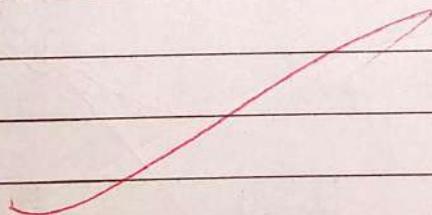
the socket IC based and are located
out by moving level downwards.

3. Connections are made as shown
circuit diagram.

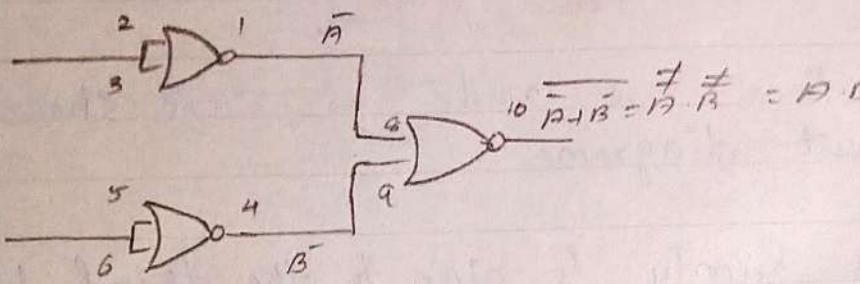
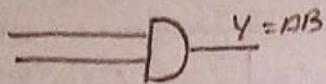
4. Power Supply is given to the trial kit.

5. The input suitable are used to
set up the input condition to the
circuit.

6. The truth table is verified and the
output are observed.

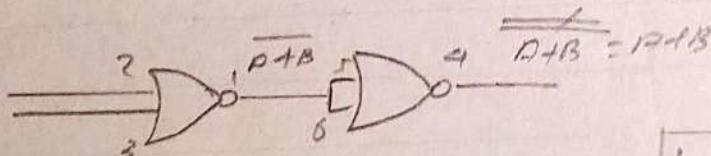
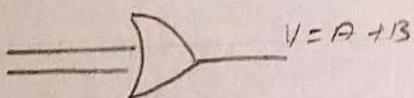


NOR gate as AND gate



Input	Output
A B	$Y = \overline{A \cdot B}$
0 0	0
0 1	0
1 0	0
1 1	1

NOR gate as OR gate



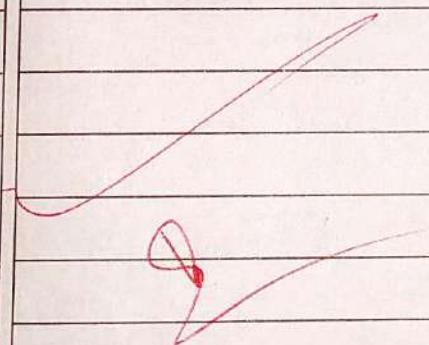
$$2^n = 2^2 = 4$$

$$2^n = 2^2 = 4$$

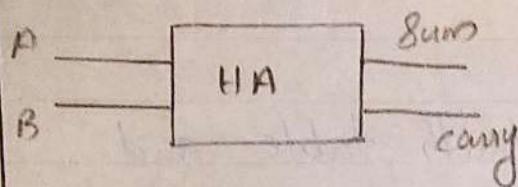
Input	Output
A B	$Y = \overline{A+B}$
0 0	0
1 0	1
0 1	1
1 1	1

* Result :-

Verified the truth table and
realized the gates (NAND as Universal
gate & NOR as Universal Gate)



Half Adder



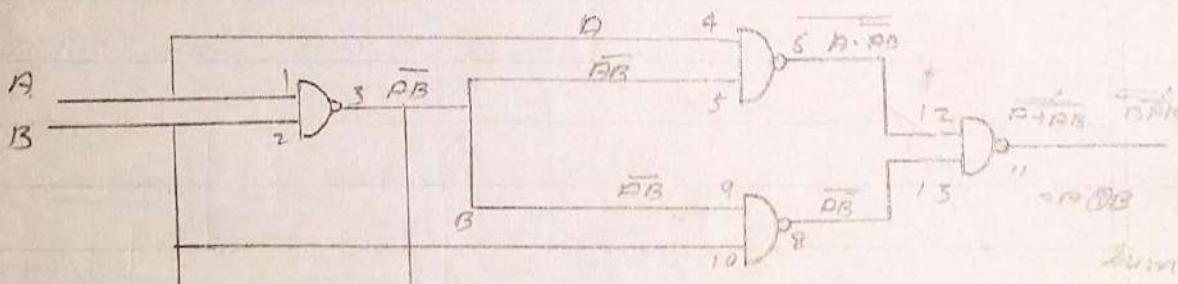
$$Sum = \bar{A}B + A\bar{B}$$

$$= A \oplus B$$

$$Carry = A \cdot B$$

Input-		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

NAND gate



$$= \overline{A \cdot AB} \cdot \overline{B \cdot AB}$$

$$= \overline{A \cdot \overline{AB}} + \overline{B \cdot \overline{AB}}$$

$$= \overline{A \cdot \overline{AB}} \rightarrow A \cdot \overline{AB}$$

$$= (\overline{A} + B) + (\overline{A} \cdot B)$$

$$= A \overline{B} + B \overline{A} + A \overline{B} \cdot B \overline{A}$$

$$= A \overline{B} + B \overline{A} + A \overline{B} \cdot B \overline{A} = A \oplus B$$

3

Design & Realization of half adder
half subtractor using NAND Gates

Aim:- To design and realize half adder
and half subtractor using NAND
Gates.

Components Required :-

i, IC 7400

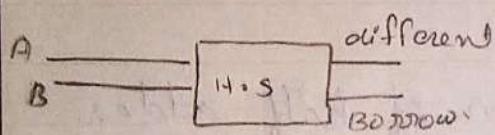
Equipments Required :-

Digital ic trainer kit and patch
cards

Procedure :-

1. All Components and Patch Cards are tested for good working Condition.
2. Connections are made as shown in the circuit diagram.

> half subtraction :-

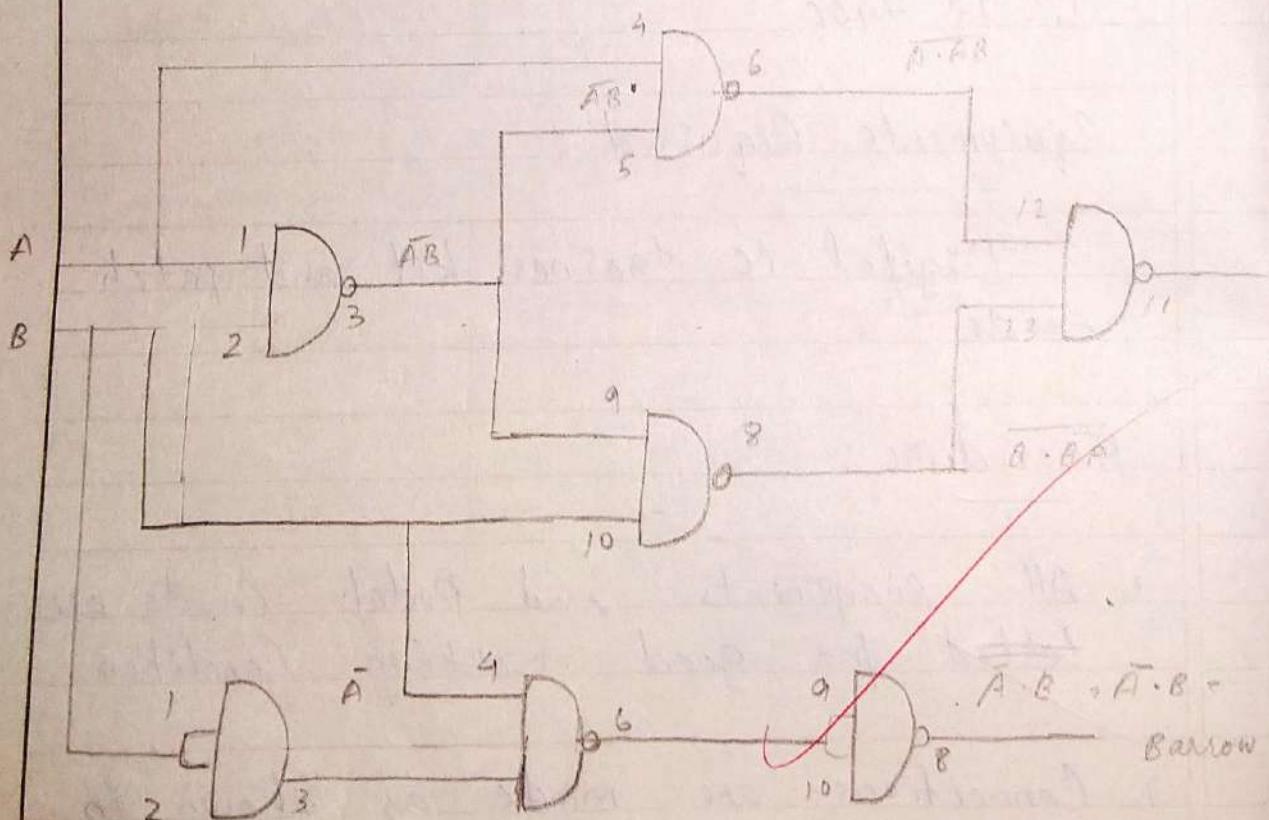


$$\text{different} : \bar{A}B + A\bar{B}$$

$$= A \oplus B$$

$$\text{Borrow} = \bar{A}B$$

INPUT		OUTPUT	
A	B	diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0



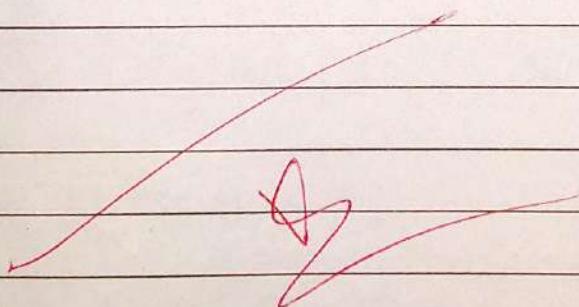
3. Power Supply is given to the kit.

4. Input data are provided by using switches.

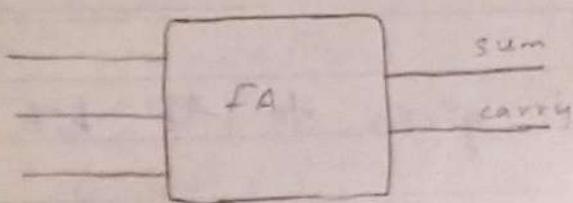
5. Truth table Sequence is verify and output are observe with LED display.

* Result :-

Verify the truth table and realized half adder & half subtractor using NAND Gates.



full adder :



Logical expression

$$\text{sum} = AB\bar{C} + \bar{A}BC + ABC + A\bar{B}\bar{C}$$

$$= \bar{A}(B\bar{C} + BC) + A(\bar{B}\bar{C} + BC)$$

$$= \bar{A}\bar{B} + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + ABC$$

$$+ A\bar{B}C$$

$$\text{sum} = A\bar{B}C + \bar{A}BC$$

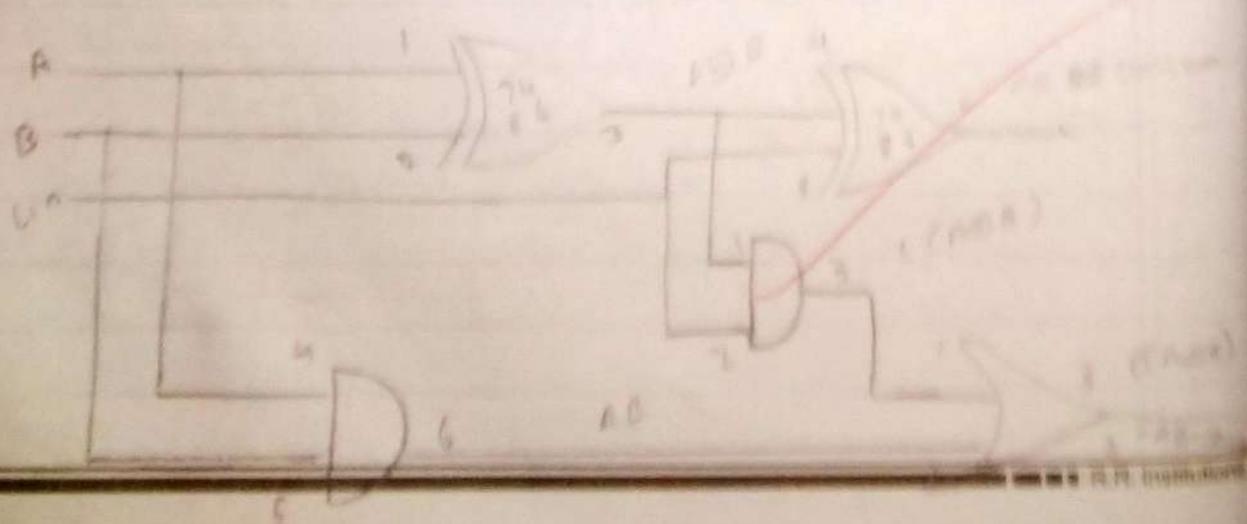
$$\text{carry} = ABC + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C}$$

$$+ \bar{A}(A\bar{B} + A\bar{B}) + A\bar{B} + A\bar{B}$$

$$\text{carry} = ((A\bar{B}) + A\bar{B}) + A\bar{B}$$

$$O = 3 \cdot n^2 + 2^3 + 1$$

INPUT			OUTPUT	
A	B	Cin	sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



4

Design and Realisation of full adder using logic Gates :-

* Aim :- To design and realize full adder using logic gates.

* Components Required :-

- i, IC 7486
- ii, IC 7408
- iii, IC 7432

* Equipments Required :-

Digital IC trainer kit and patch cards.

* Procedure :-

i) All Components and patch cards are tested for good working conditions.

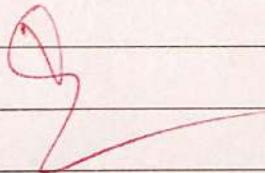
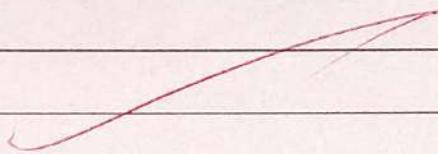
ii) Connections are made as shown in

circuit program.

iii, Power Supply is given to trainer kit.

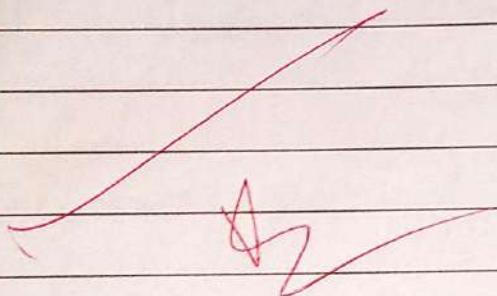
iv, Input data are provided by Using Input
Switches

v, truth table Sequence is verified and
output are observe with LED Supply

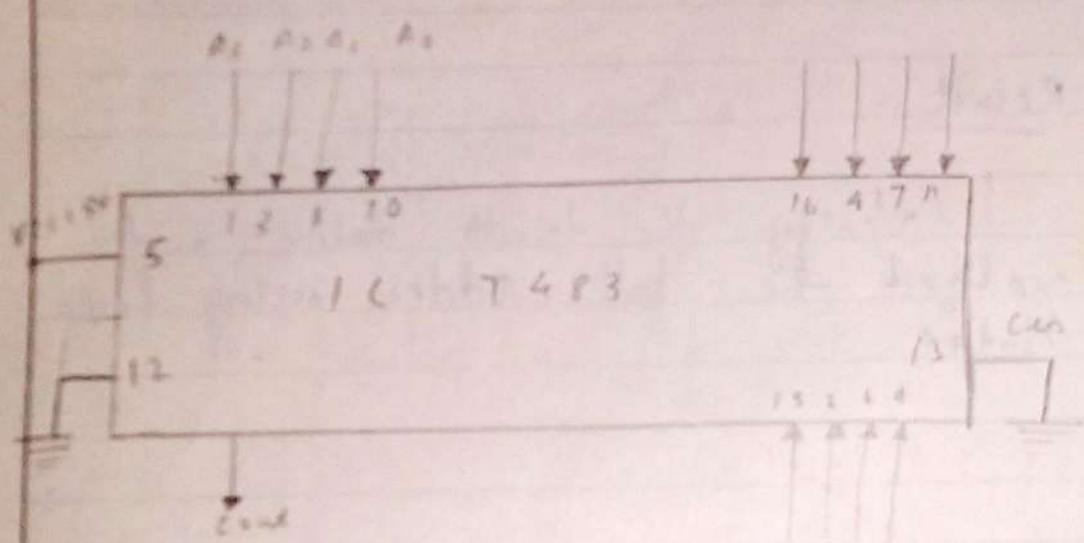


* Result :-

Verify the truth table and
realized the full adder using logic
Gates.



pin diagram of 7483



5

Design and Realisation of 4 bit adder Subtraction Using IC 7483.

* Aim :- using 4 bit Binary adder IC 7473
to design

(i) 4 bit Binary Adder Circuit

(ii) 4 bit Adder / Subtractor Circuit

* Components Required :-

IC 7483 (4 bit Binary Adder)

IC 7486 (EX-OR Gates)

* Equipments Required :-

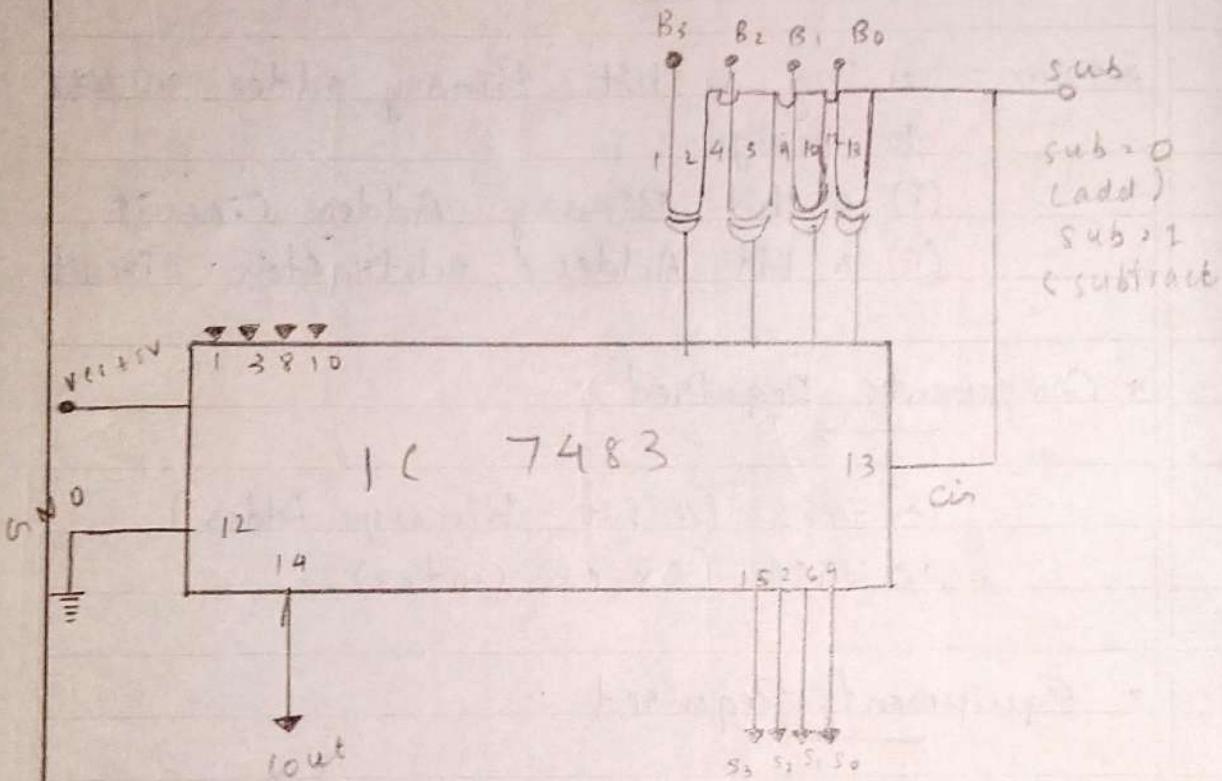
Digital IC Trainer kit , Patch Cards

* Procedure :-

1. All Components and patch cards are tested for good working Condition.

Pin Diagram of a bit

Adder / Subtractor circuit



Truth table

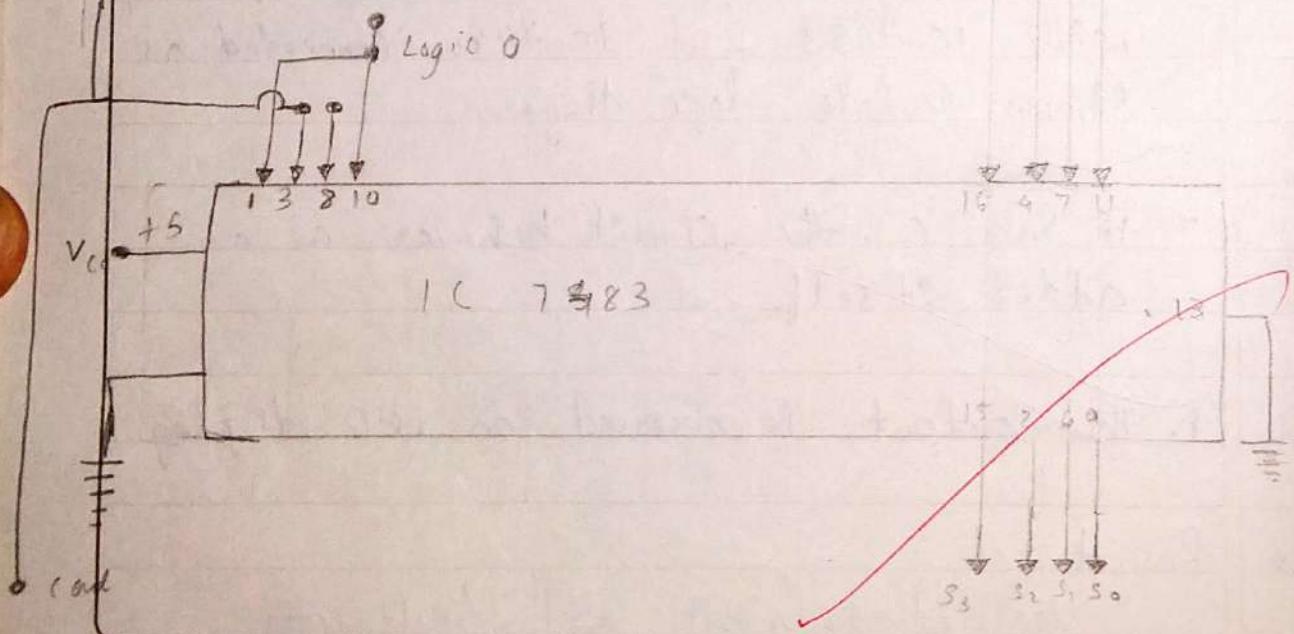
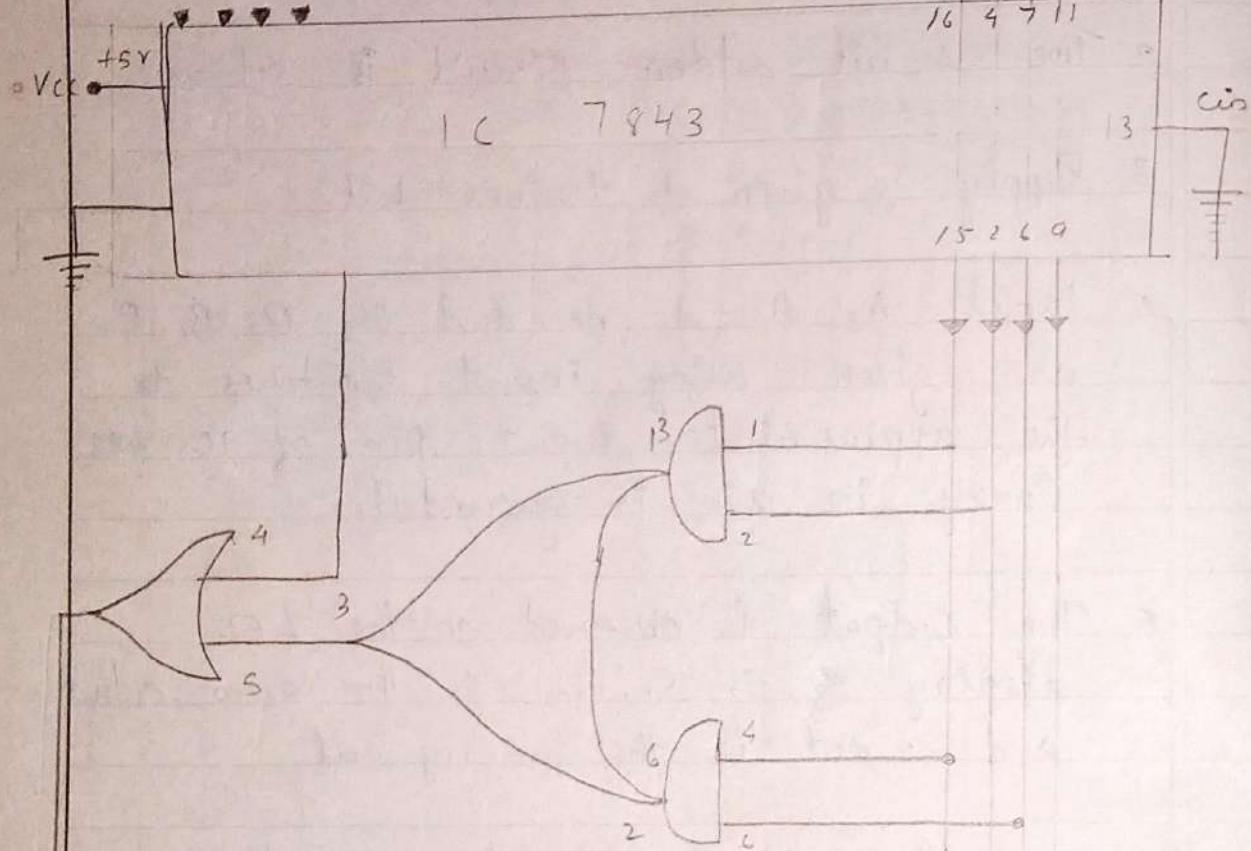
	INPUT								Output					
	Cin	A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	Out	S ₃	S ₂	S ₁	S ₀
Adder	0	1	0	1	0	1	0	1	0	1	0	1	0	0
Subtractor	1	1	0	1	0	1	0	1	0	0	0	0	0	0

2. The 4 bit adder circuit is set up.
3. Supply is given to trainer kit.
4. Input A_3, A_2, A_1, A_0 and B_3, B_2, B_1, B_0 are given using input switches to the appropriate input pin of IC 7483. Carry in pin is grounded.
5. The Output is observed on the LED display. S_3, S_2, S_1, S_0 is the sum output and C_{out} is the carry out.
6. Then the adder/subtractor circuit is setup with IC 7483 and IC 7486 connected as shown in the logic diagram.
7. If $Sub = 0$, the circuit behaves as an adder itself.
8. The output is observed on LED display.

* Result :-

Verified the 4 bit adder/subtractor

pin diagram



6 Design and Realisation of BCD adder
Using IC 7483

* Aim :- To design adder using IC 7483
and to study its operation.

* Components Required :-

IC 7483 (21Cs)

IC 7408 (AND Gate)

IC 7432 (OR Gate)

* Equipments Required :-

Digital IC trainer kit, patch Cards.

* procedure :-

1. All Components and patch cards are tested
using ~~multiplexers~~ and IC tester for
good working Condition.

2. The BCD Adder circuit is built using

Truth table

INPUTS									OUTPUTS			
A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	Count	S_3	S_2	S_1	S_0
0	0	1	0	0	1	0	0	0	0	1	1	0
1	0	1	0	0	1	0	1	0	1	1	1	1

ICs 7483 7408 and 7432

3. Power Supply is given to the trainer kit.

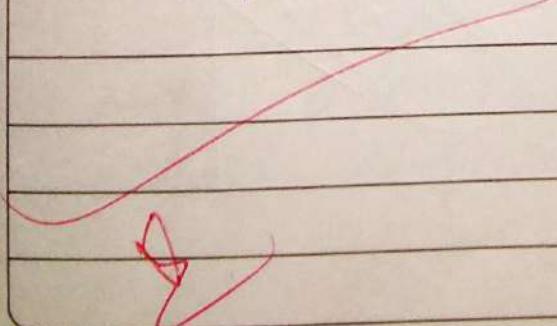
4. Input are given (BCD representation of two decimal digits) using Input switches for High(1) or Low(0).

5. The Output is Cout S_3 , S_2 , S_1 , S_0 are observed on the LED display out 3210

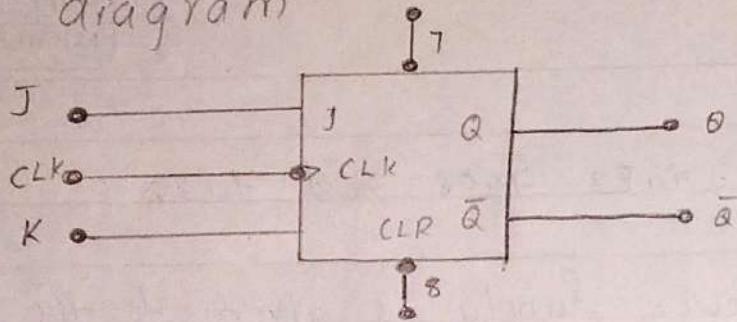
6. These outputs can also be connected to BCD to decimal decoder circuit to have the output on the 7-Segment display.

* Result :-

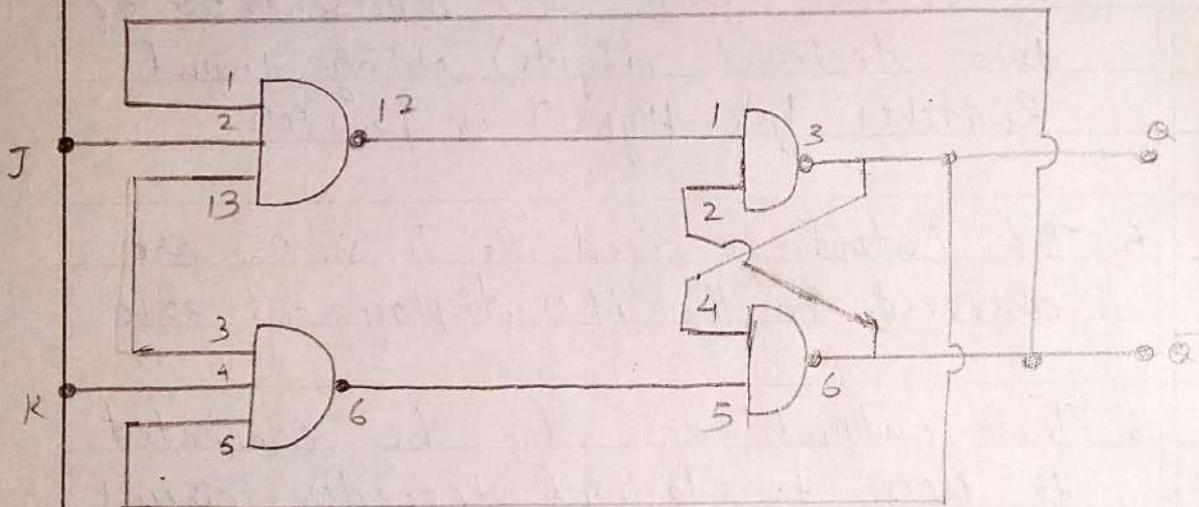
Verified BCD adder using IC 7483



Logic diagram



(i) JK flip flop using NAND gate



Truth table

INPUTS			OUTPUTS		Mode of Operation
CLK	J	K	Q	\bar{Q}	
0	0	0	Q	\bar{Q}	No change
0	1	0	0	1	Reset
1	0	1	1	0	Set
1	1	1	Invalid condition		Racing condition

7

Realisation of Flip flop

* Aim :- To realize the working of JK Flip Flop.

* Components Required :-

IC 7400 (2 Input NAND Gate)

IC 7410 (3 Input NAND Gate)

* Equipments Required :-

Digital IC Trainer kit, patch Cards.

* Procedure :-

1. Verify all components and patch Cards.
Whether they are in good Condition.

2. Make Sure Connection as shown in the circuit diagram.

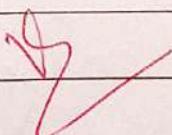
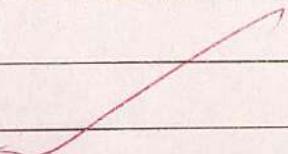
3. Give Supply to the trainer kit.

4. Set Input Conditions and apply input
Clock pulse.

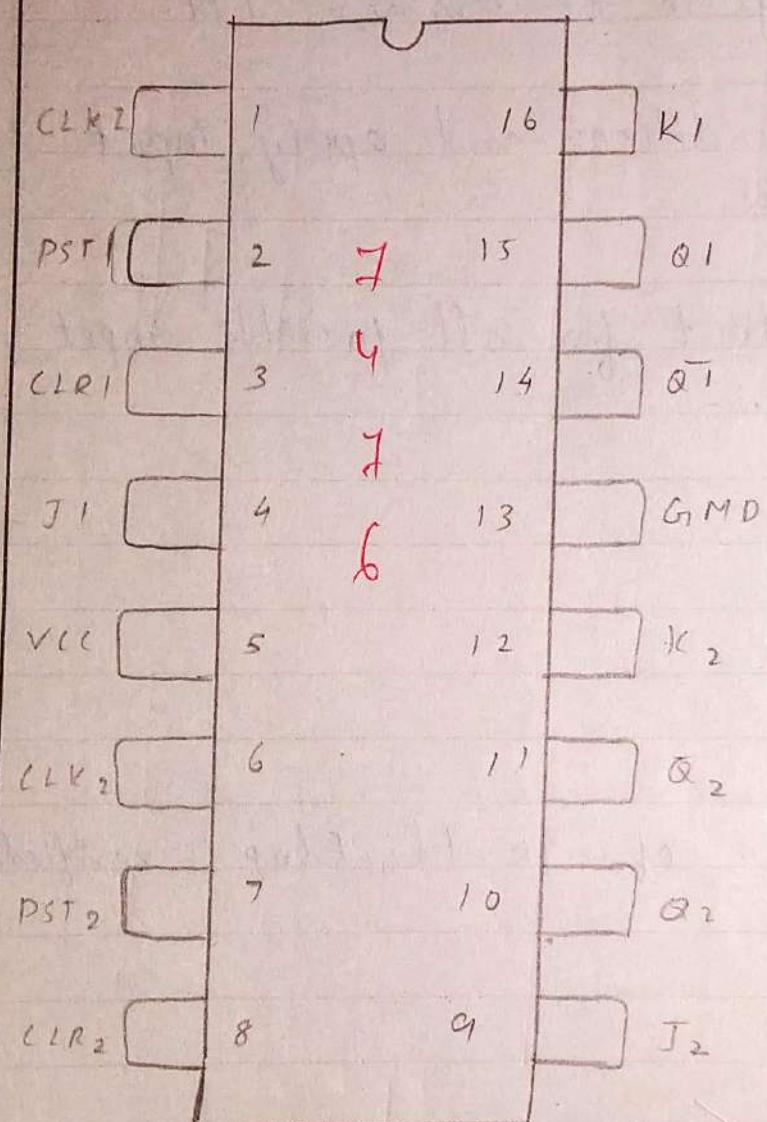
5. Observe output for all possible input
Combinations.

* Result :-

Realisation of JK Flip Flop is verified.



Pin program of IC 7476



✓

8

Realisation of T AND D Flip Flop.

* Aim :- To realize the following Circuits.

- (i) D Flip Flop using IC 7476
- (ii) T Flip Flop using IC 7476

* Components Required :-

IC 7476

* Equipments Required :-

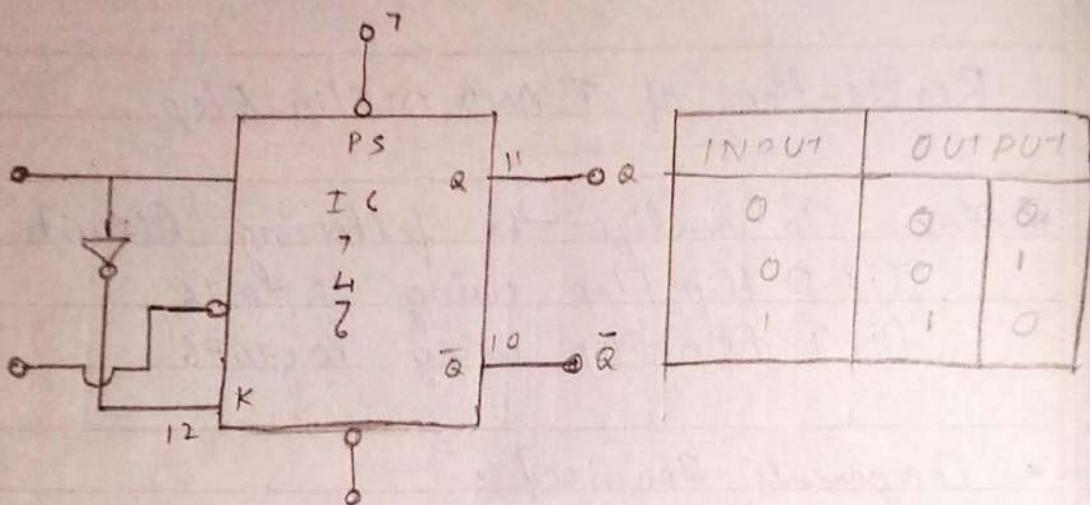
Digital IC Trainer kit, patch Cards

* Procedure :-

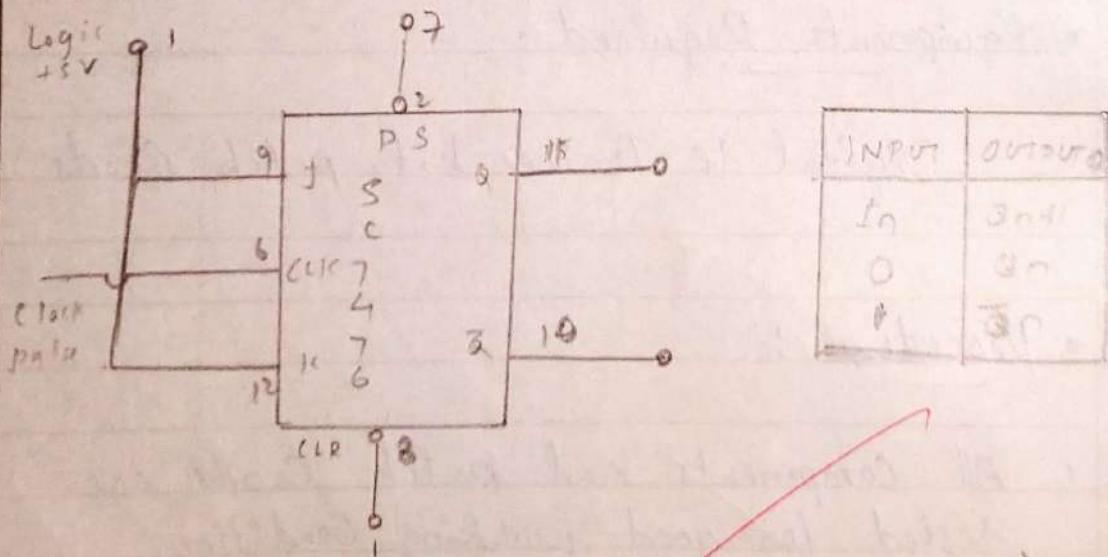
1. All components and patch Cards are tested for good working Condition.

2. Circuit Connections are made as shown in the diagrams for each case.

ii) D flip flop using JK flip flop (IC7476)



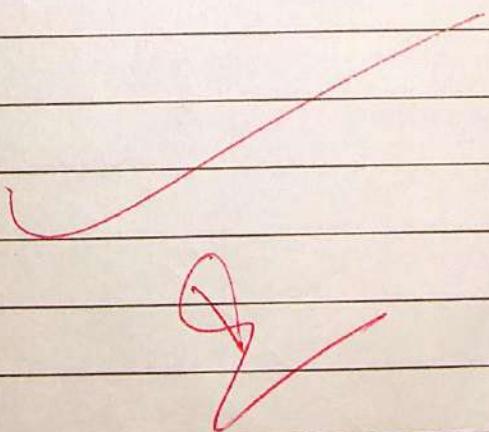
(iii) Q flip flop using JK flip flop (IC7476)



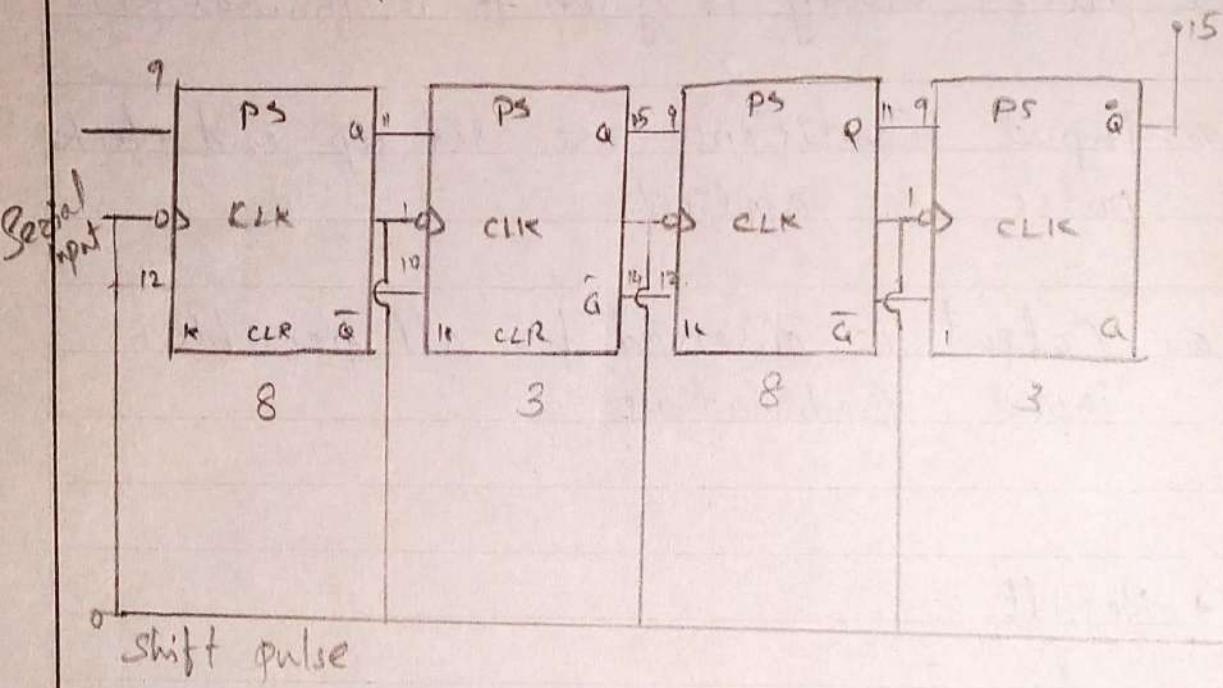
3. Power Supply is given to IC Trainers kit.
4. Input Conditions are set up and clock pulse are applied.
5. Output is observed for all possible input Combinations.

* Result :-

Verified the T & D flip flop



logic diagram



Truth Table

Parallel Input				Parallel Output			
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0
1	0	1	0	1	0	1	0

9

Implementation of Pipelined Shift Register Using Flip Flops.

* Aim :- To implement parallel-in parallel-out Shift Register using Flip Flop IC 7476.

* Components Required :-

IC 7476 JK Flip Flops

* Equipments Required :-

Digital IC trainer kit, patch Cords.

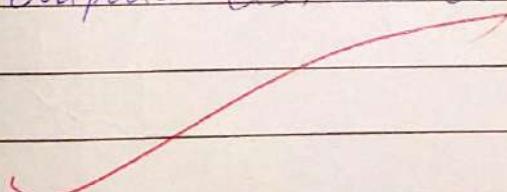
* Procedure :-

1. Components are tested for good working condition.

2. Circuit diagram for Pipelined Shift Register is constructed using D Flip-Flop ICs

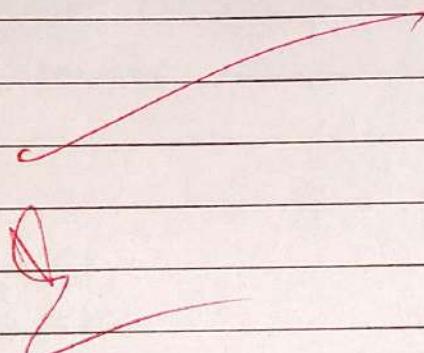
3. Supply is given to the trainer kit.
4. To Shift data in parallel in to the registers the Asynchronous inputs present (PS) and clear (CLR) are used.
5. To Shift a 0 onto the Flip-Flop, a Low level is given on clear (CLR) input.
6. To Shift a 1, into the Flip-Flop, a low level is given on present (PS) input
7. The Output can be obtained at the parallel outputs Q_3, Q_2, Q_1, Q_0 .

*

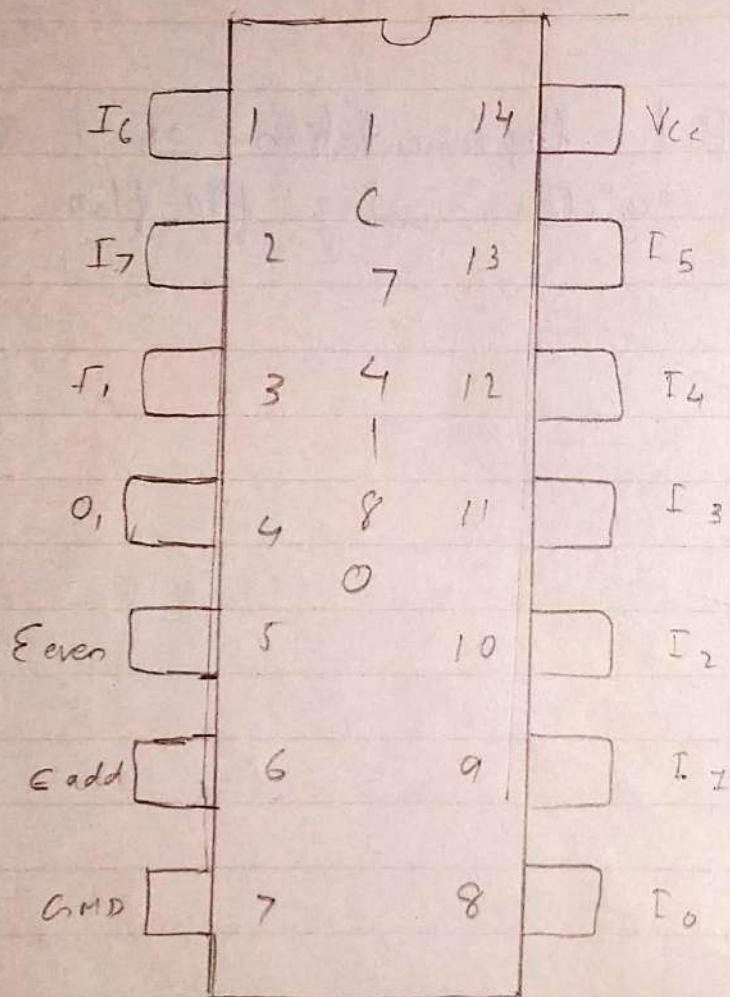


* Result :-

Verified implementation of P, P₀
Shift register using flip-flop.



Pin diagram



10

Design and implementation of add and even parity checker/Generator Using IC 74180

* Aim :- To design implement add and even parity checker/generator using IC 74180

* Components Required :-

IC 74180 (9 bit parity Generator/Checker
Consisting of 1 bit parity and 8 databil)

* Equipments Required :-

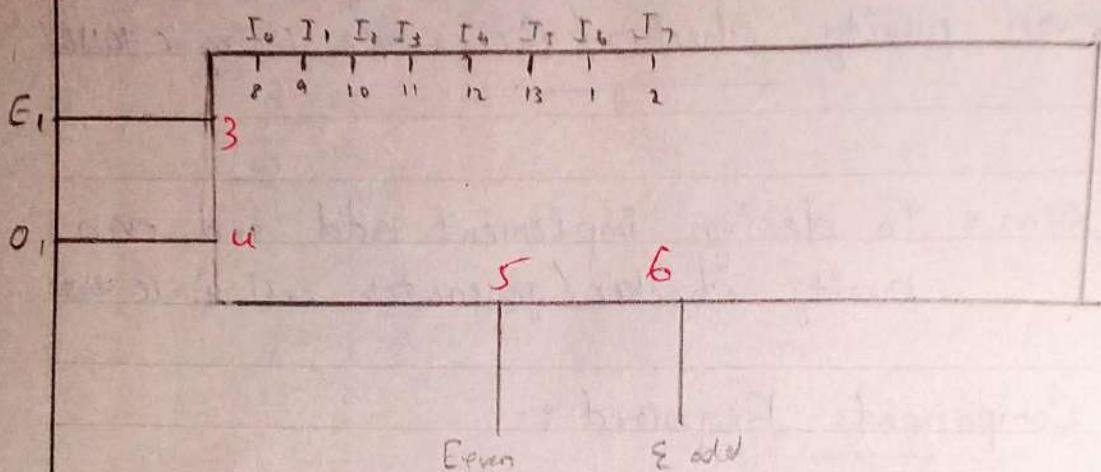
Digital IC trainer kit, patch Cards.

* Procedure :-

1. All components are tested for good working Condition.

2. IC is fixed in zif socket and locked

Logic diagram



Truth table

Number of inputs that are high	Outputs	
	Even	odd
0, 2, 4, 6, 8	4	2
1, 3, 5, 7, 9	2	4

3. Power Supply is given to the trainer kit

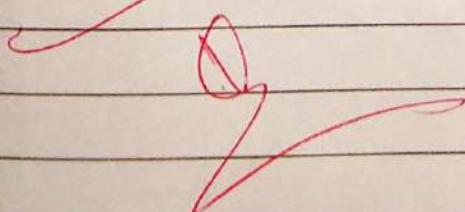
4. Appropriate data inputs are given.

5. The IC device can be used both as parity checker and parity generator.

6. When used as even parity checker the number of input bits should always be even.

* Result :-

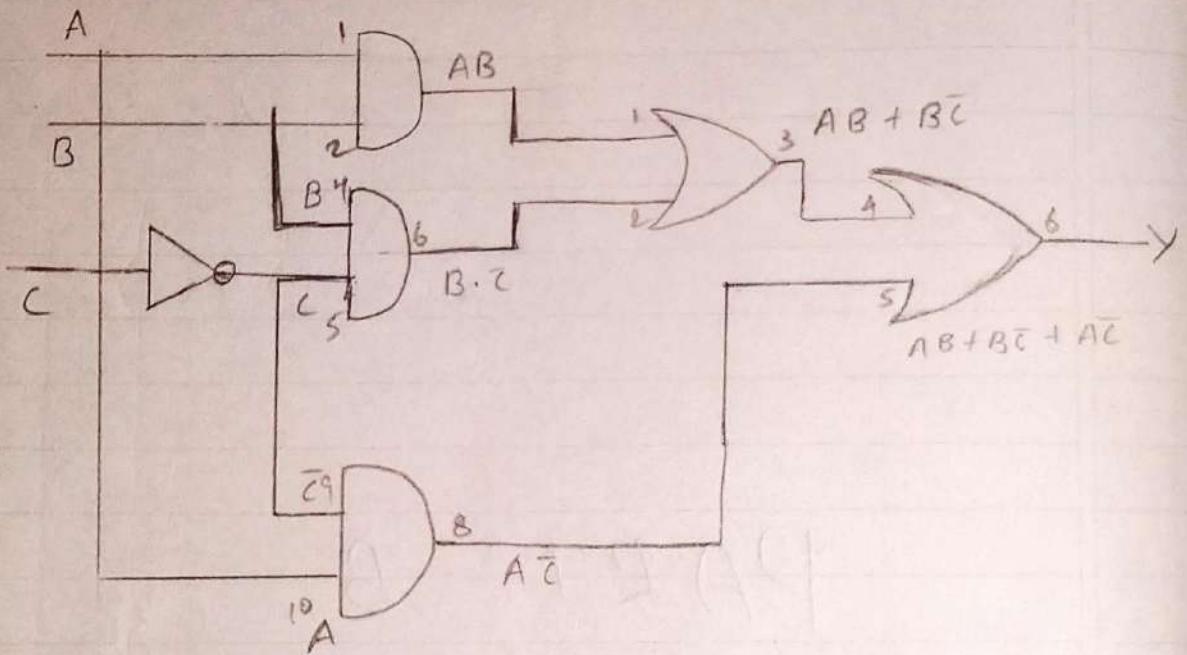
Design and implementation of odd & even parity checker /generator is verified.



DATE:

EXP.NO.:

PART - B



Truth table

inputs			output
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

11.

Realization of Boolean Expressions Using Logic Gates

* Aim:- To implement Boolean expressions using logic gates

* Components Required :-

IC 7408 AND Gate

IC 7432 OR Gate

IC 7404 NOT Gate

IC 7400 NAND Gate

IC 7402 NOR Gate

IC 7486 EX-OR Gate

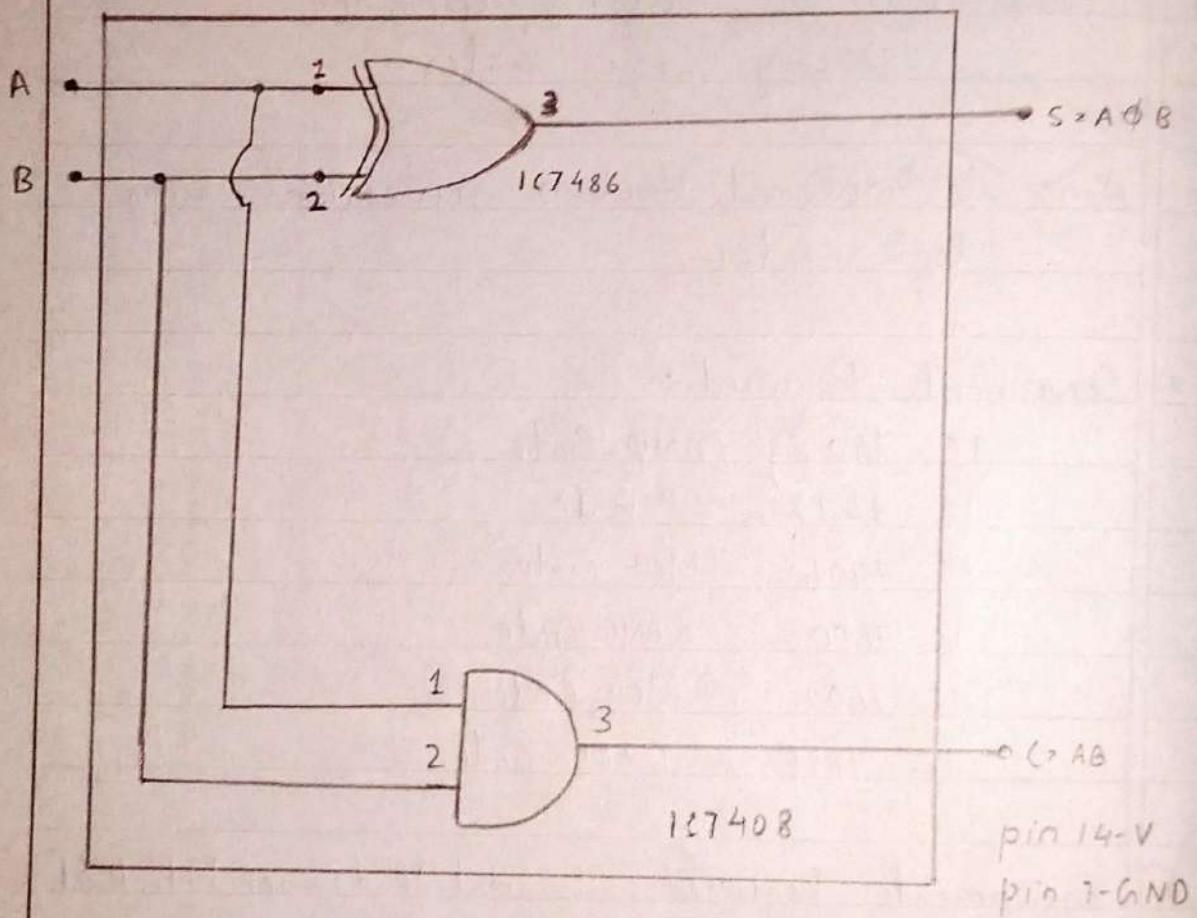
* Equipments Required :- Digital IC trainer kit Patch Cards.

(i) Implement logic circuit for boolean Expression

$$Y = AB + BC' + AC'$$

* Result : Realization of boolean expression using logic gates.

Logic diagram (using IC 7486, IC7408)



Truth table

INPUTS		OUTPUTS	
X	Y	S (sum)	C (carry)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Logical expression : S (sum) = X ⊕ Y

C (carry) = X · Y

12.

Design and Realization of Half-Adder Using Logic Gates

* Aim:- to design and realize Half Adder using Logic Gates

* Components Required :- IC 7408, IC 7486

* Equipment Required :- Digital IC trainer kit, Patch Cards

* Procedure :-

a) All Components and patch cards are tested for good working condition.

b) Connections are made as shown in circuit diagram.

c) power Supply is given to the trainer kit.

d) Input data are provided by using Input switches (HIGH OR LOW)

(e) Truth Table sequence is verified and outputs are observed with LED Display

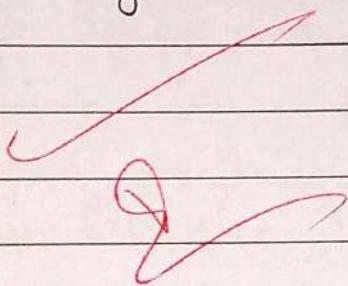
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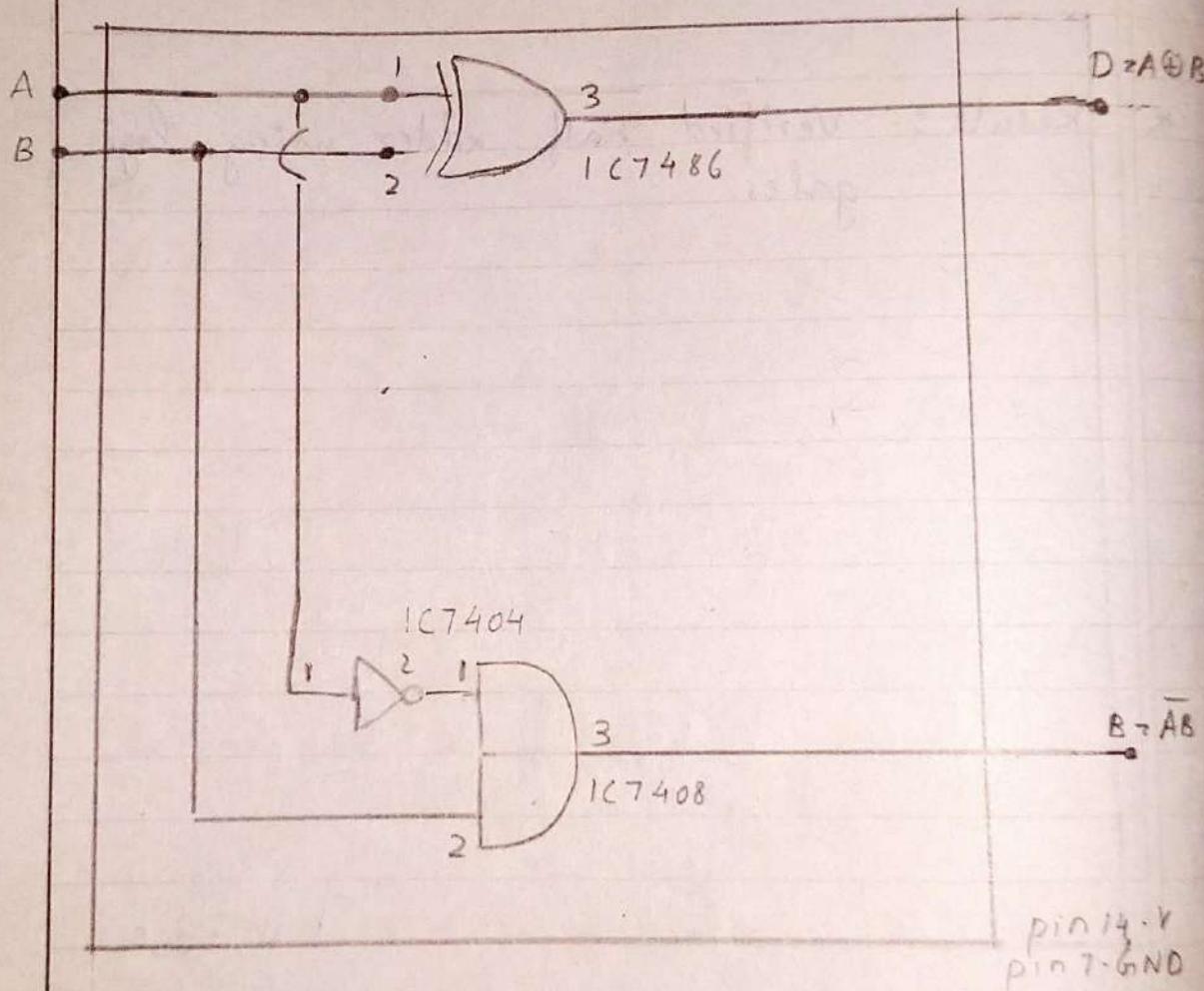
EXP.NO.:

*

Result :- Verified half adder using logic
gates.



Logic diagram (using IC 7486, IC 7408, IC 7404)



Truth table

INPUTS		OUTPUTS	
X	Y	D (difference)	B (borrow)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Logical expression: D (difference) $= X \oplus Y$

B (borrow) $= X \cdot Y$

Design and Realization of Half - Subtractor Using Logic gates.

* Aim :- To design and realize Half Subtractor using logic gates.

* Components Required :- IC 7408, IC 7486, IC 7404

* Equipments Required :- Digital IC Trainer kit, Patch cards

* Procedure :-

a) All components and patch cards are tested for good working condition.

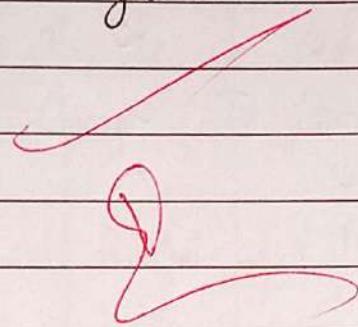
b) Connections are made as shown in circuit diagram.

c) Power supply is given to the trainer kit.

d) Input data are provided by using input switches (High or Low)

e) Truth Table Sequence is verified and outputs are observed with LED display.

* Result: Verified half subtractor using logic gates.



Truth Table :

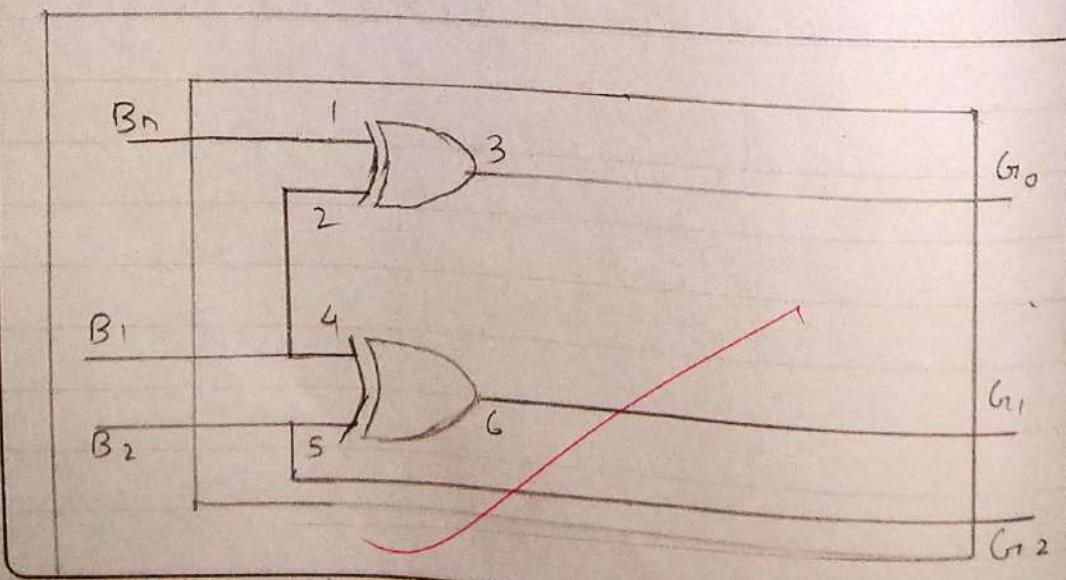
INPUTS			OUTPUTS			
BINARY			GRAY			
B ₂	B ₁	B ₀	G ₂	G ₁	G ₀	
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	0	1
0	1	1	0	1	0	0
1	0	0	1	1	0	0
1	0	1	1	0	1	1
1	1	0	1	0	0	1
1	1	1	1	0	0	0

Logical expression $G_0 = B_0 \oplus B_1$

$G_1 = B_1 \oplus B_2$

$G_2 = B_2$

Logic diagram



14

Design and Implementation of 3 Bit Binary to Gray Code Converter Circuit

Aim :- To design and implement 3 bit binary to Gray Code Converter.

* Components Required : IC 7486 EX-OR Gate

* Equipment Required :- Digital IC Trainer kit, Patch Cards

* Procedure :-

a) All components and patch cards are tested for good working condition.

b) Connections are made as shown in circuit diagram.

c) Power Supply is given to the trainer kit.

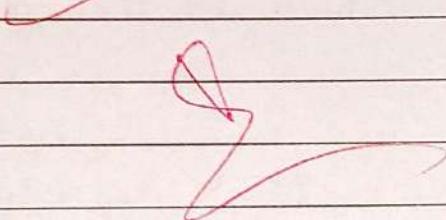
d) Input data are provided by using input switches (HIGH OR LOW)

e, Truth table sequence is verified and outputs are observed with LED Display.

*

Result:-

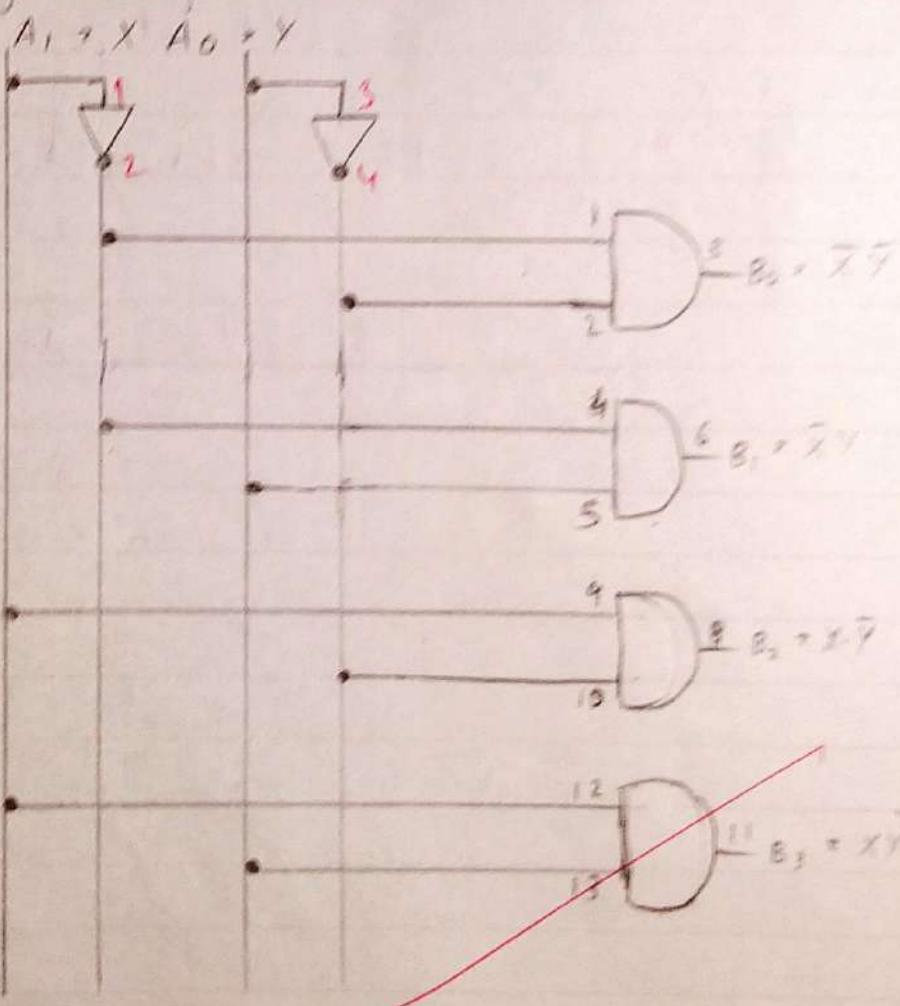
Design and implementation of 3
bit binary & code to gray code
converter circuit.



Truth table

INPUTS		OUTPUTS			
X	Y	B_3	B_2	B_1	B_0
0	0				HIGH
0	1			HIGH	
1	0		HIGH		
1	1	HIGH			

Logic diagram



Result: The logic circuit for 1 of 4 decoder

Circuit is implemented and truth table is verified

15.

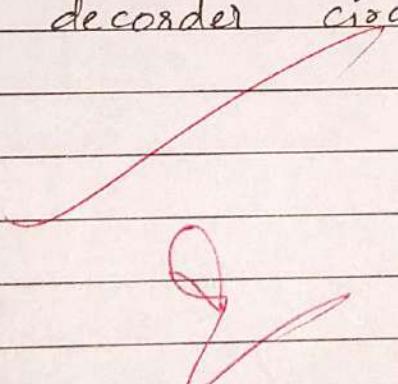
Design and Implementation of 1 of 4 Decoder Circuit.

- * Aim :- To design and implement 1 of 4 Decoder Circuit (2 Bit Decoder).
- * Components Required :- IC 7408 AND Gate, IC 7404 NOR Gate
- * Equipment Required :- Digital IC trainer kit, Patch Cards.
- * Procedure :-
 - a) All components and patch cards are tested for good working condition.
 - b) Connections are made as shown in circuit diagram
 - c) power Supply is given to the trainer kit.
 - d) Input data are provided by using Input

Switches (HIGH OR LOW)

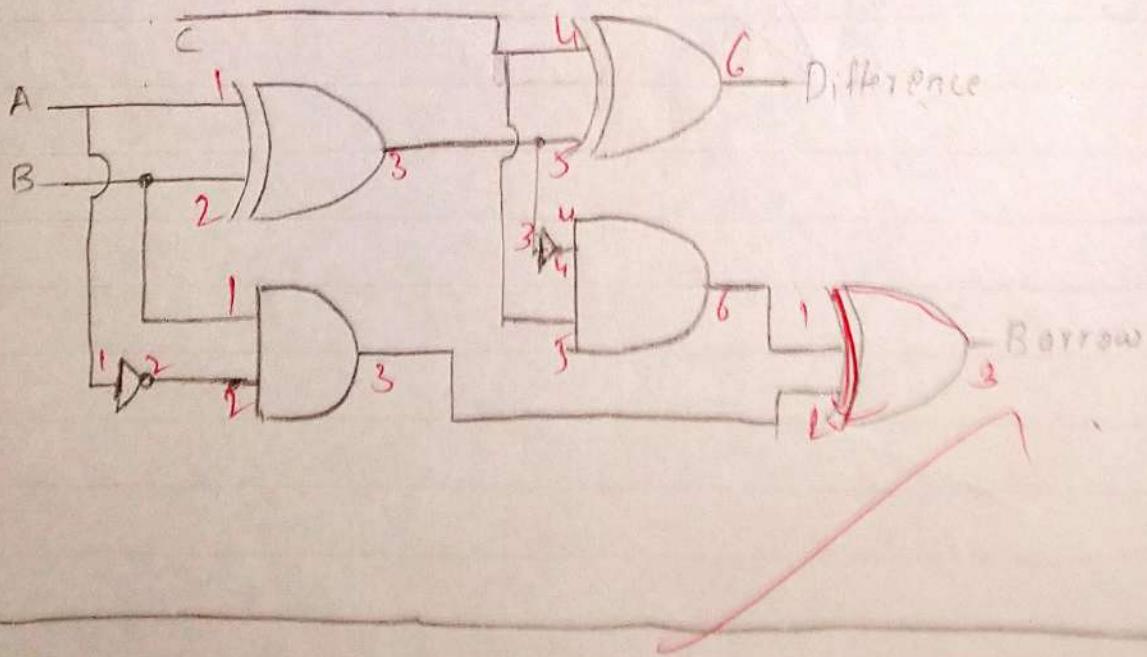
e) Truth Table Sequence is verified and outputs are observed with LED display.

* Result : Design and implementation of a decoder circuit.



Truth Table

INPUTS			OUTPUTS	
X	Y	B_{IN}	D	B_{OUT}
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



16.

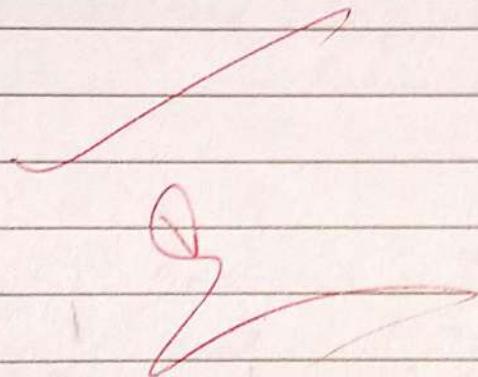
Design and Realization of full-Subtraction Using Logic Gates

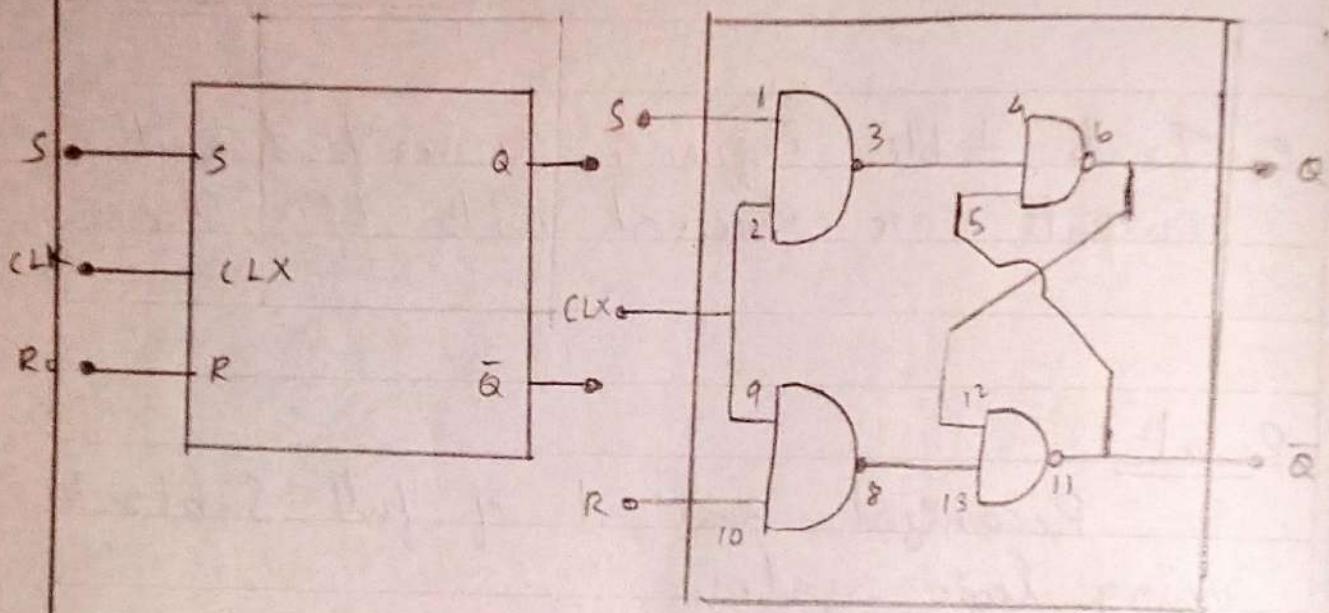
- * Aim :- To design and realize full Subtractor using Logic Gates.
- * Components Required : IC 7486, IC 7408, IC 7432, IC 7404.
- * Equipment Required :- Digital IC Trainer kit, Patch Cords.
- * Procedure :-
 - a) All Components and patch cords are tested for good working condition
 - b) Connections are made as shown in the Circuit diagram.
 - c) Power Supply is given to the Trainer kit.
 - d) Input data are provided by using Input Switches (High or Low)

e, Truth table sequence is verified and outputs are observed with LED Display.

* Result:-

Recognized realized of full Subtractor using logic gates.





Truth table

INPUTS			OUTPUTS		MODE OF OPERATION
CLX	S	R	Q	Q̄	
high	0	0	Q	Q̄	Hold state
high	0	1	0	1	RESET
high	1	0	1	0	SET
high	1	1	Invalid condition		Prohibited

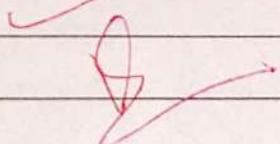
17.

Realization of RS Flip-Flop Using NAND Gates.

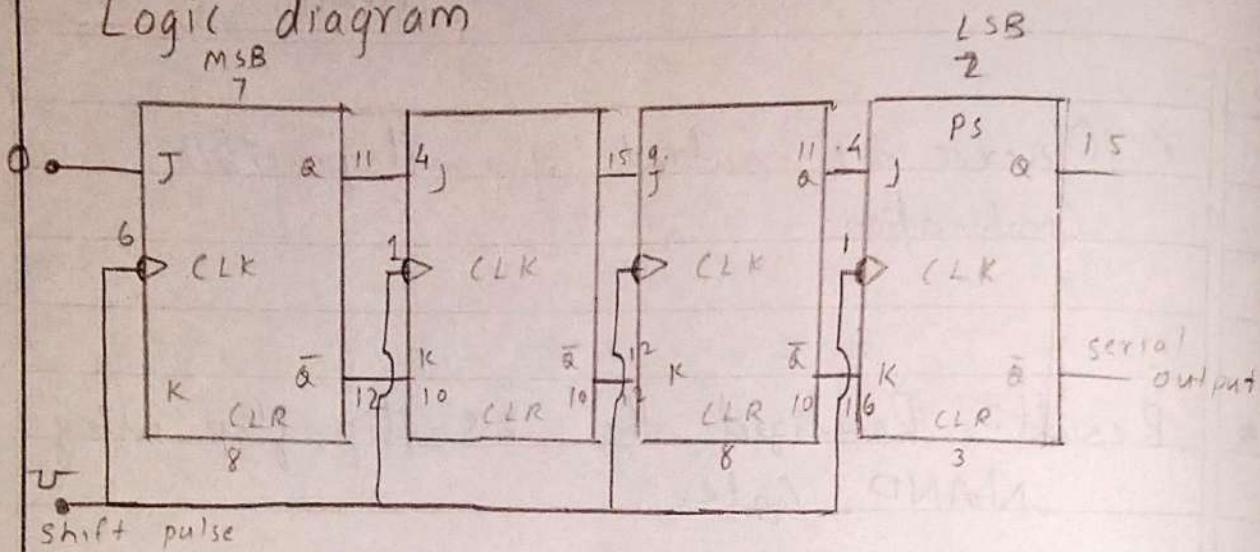
- * Aim :- To realize a suitable circuit of RS Flip Flop using NAND Gates
- * Components Required :- IC 7400
- * Equipment Required :- Digital IC Trainer Kit,
Patch Lead
- * Procedure :-
 - a) Verify the components and patch cords for working in good condition.
 - b) Make connections as shown in the circuit diagram.
 - c) Give power supply to the Trainer kit.
 - d) Set the input conditions and apply clock pulse (monopulse) to the clock input

e, Observe the output for all possible Combinations.

* Result:- Realized the RS-flip flop using NAND Gate.



Logic diagram



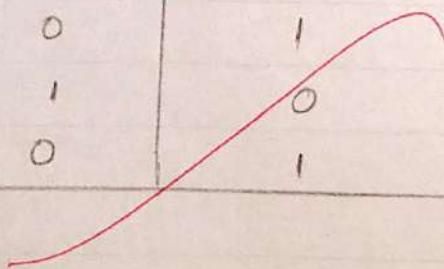
For 4 bit Shift register, 2 ICs 7476 are required

Set Inputs $J=0 \ K=1$ to Shift a 0 bit into the flipflop

Set Inputs $J=1 \ K=0$ to Shift a 1 into the flipflop.

Truth table

INPUTS		OUTPUTS
1	0	1
1	0	1
0	1	0
1	0	1



18.

Implementation of 8150 Shift Register Using Flip - Flops IC 7476.

* Aim :- To implement serial - In .serial out Shift Register using Flip Flops.

* Components Required : IC 7476

* Equipments Required : Digital IC Trainer kit,
Patch Cords.

* Procedure :-

a) Components are tested for good working condition.

b) Circuit diagram for 8150 shift Register is constructed using PK Flip Flop ICs.

c) Power Supply is given to Trainer kit

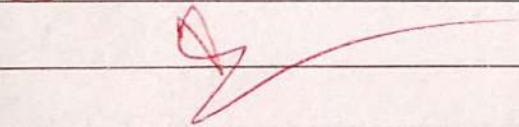
d) Serial Input is given and every clock pulse applied.

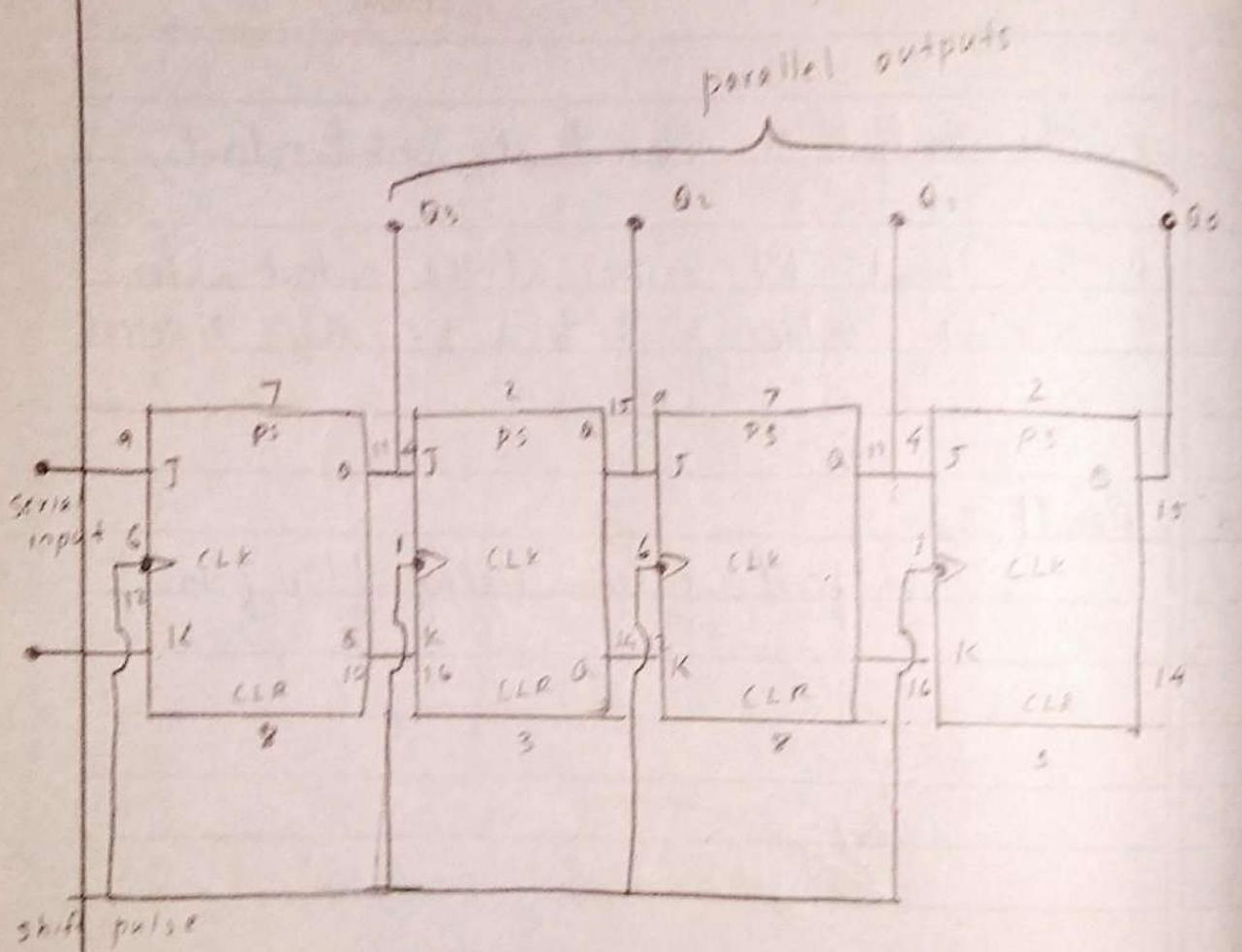
e. The output is observed at serial output.

f. The input bit arrives at the output after 4 clock pulses in a b8 4 bit shift Register.

* Result :-

Verified PISO Using flip flop.





For a 4 bit Shift Register, two IC's 7476 are required.

Set Inputs J=0 and K=1 to Shift a 0 into the Flip Flop

Set Inputs J=1 and K=0 to Shift a 1 into the Flip Flop

After 4 shift pulses output Q₃, Q₂, Q₁, Q₀ can be obtained as the parallel data in the shift Register

19.

Implementation of SIPO Shift Register Using Flip-Flops

* Aim :- To implement Serial in parallel out Shift Register using Flip Flops.

* Components Required : IC 7476 5 k flip flop

* Equipment Required : Digital IC Trainer kit.
Patch Cords.

* Procedure :-

a) Components are tested for good working condition.

b) Circuit diagram for SIPO shift Register is constructed using D flip

c) Supply is given to Trainer kit.

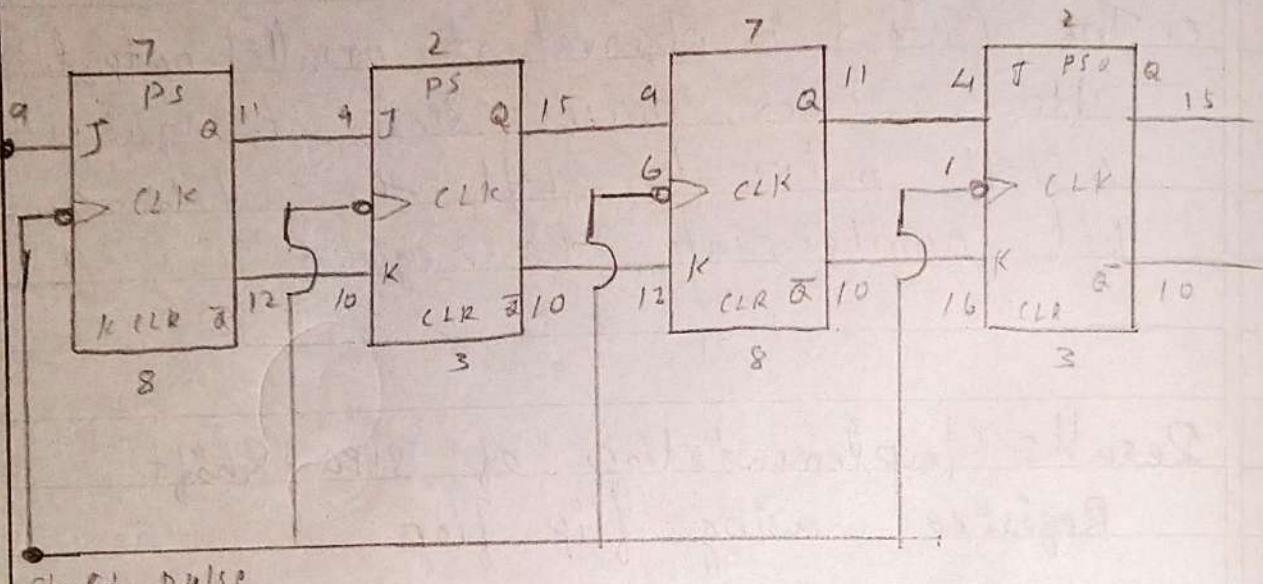
d) Serial input is given with LSB First and MSB last then clock pulse is applied

e. The Output is observed at parallel output after 4 clock pulses, since it requires 4 shift pulses to shift the whole 4 bit number into the register.

* Result:- Implementation of SIPO Shift Register using flip flop



Logic diagram



Shift pulse

To shift data bit pattern 1001 into shift register as parallel input

$PS_{T3} \# PS_{T0}$ must be given a low signal $CLR_2 \# CLR_1$ must be given a low signal

shift type	parallel Input				serial output
	Q ₃	Q ₂	Q ₁	Q ₀	
HIGH	1	0	0	1	1
HIGH	0	1	0	0	0
HIGH	0	0	1	0	0
HIGH	0	0	0	1	1

20.

Implementation of PISO Shift Register Using Flip-Flops.

* Aim :- To implement parallel in serial out Shift Register using Flip Flops.

* Components Required :- IC 7476 D Flip Flops.

* Equipment's Required :- Digital IC Trainer kit,
Patch Cords.

* Procedure :-

a) Components are tested for good working condition.

b) Circuit diagram for PISO shift Register is constructed using D flip flop ICs.

c) Supply is given to the Trainer kit.

d) To Shift data in parallel into the register the Asynchronous Inputs preset (Ps) and clear (Cir) are used.

e. To Shift a 0 into the Flip Flop, a low level is given on preset (Ps) input.

f. For a 4 bit shift register, using this a certain data can be moved into the shift register in parallel.

g. On application of every shift pulse, one input bit can be obtained at the serial output (LSB First)

h. It takes four shift pulses to obtain all the four bits of data input.

* Result :-

Parallel in serial out Shift register is implemented using.