NBTI Impact on Transistor & Circuit: Models, Mechanisms & Scaling Effects

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Abstract

We describe a quantitative relationship between I_D and V_T driven NBTI specifications. Mobility degradation is shown to be a significant (~40%) contributor to I_D degradation. We report for the first time, **degradation** in gate-drain *capacitance* (C_{GD}) *due to NBTI. The impact of this* C_{GD} degradation on circuit performance is quantified for both digital and analog circuits. We find that C_{GD} degradation has a greater impact on the analog circuit studied than the digital circuit. We demonstrate that there is an **optimum operating voltage** that balances NBTI degradation against transistor voltage headroom. Further, a **numerical model** based on the reaction-diffusion theory has been **developed**, which is found to satisfactorily describe degradation, recovery and post-recovery response to stress.

Introduction

Negative bias temperature instability (NBTI) has become one of the dominant reliability concerns in advanced CMOS processes. Therefore, accurate NBTI lifetime models are needed to ensure product reliability. Typically, a % change in parameters such as I_{DSAT} or I_{DLIN}, or a change in V_{TLIN} has been used as a NBTI lifetime metric. The multiplicity of parameters used has made comparisons challenging. In addition, NBTI impact on several critical parameters has been ignored. The impact of NBTI on mobility has not been quantified, while its impact on C_{GD} has not been reported.

In this report, we use analytical expressions to derive the relationship between transistor and circuit degradation, using the ring oscillator frequency as a figure of merit (FOM). Mobility, C_{GD} and circuit (digital and analog) degradation are quantified. The transistors used in this study were manufactured in the 130nm node with dual gate oxides (2.7nm SiO_2 operated at 1.5V and 7nm SiO_2 operated at 3.3V) and 5 levels of dual damascene Cu.

Results and Discussion

I. Current Degradation

Fig. 1 shows the channel length dependence of V_T shift and I_{DSAT} shift. The V_T shift shows no channel length dependence, while the I_{DSAT} degradation shows the long channel device **degrading more** than the short channel device. The I_D degradation as a function of stress time is plotted in Fig. 2, indicating that **I_{DSAT} degradation is more** than I_{DLIN} degradation.

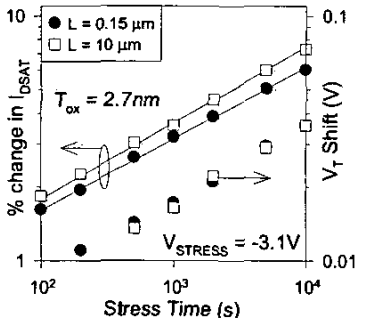

Fig. 1. % change in I_{DSAT} vs. stress time for two different channel lengths (L), showing that the V_T degradation is identical, but I_{DSAT} degradation **increases with L.**

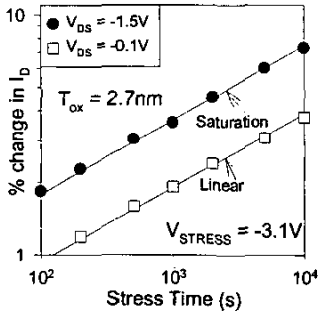

Fig. 2. % change in I_D vs. stress time for two drain biases, showing that **I_{DSAT} degradation is more than I_{DLIN} degradation.**

$$I_{DLIN} = \left[\frac{\left(\frac{\mu C_{ox} W}{L}\right)}{\left(1+\frac{V_{DS}}{E_{SAT}L}\right)}\right]\left((V_G - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right) \quad \text{Eq. 1}$$

$$\boxed{\frac{\delta I_{DLIN}}{I_{DLIN}} \propto \frac{(-\delta V_T)}{(V_G - V_T)}} \quad \text{Eq. 2}$$

$$I_{DSAT} = W v_{SAT} C_{ox} \frac{(V_G - V_T)^2}{(V_G - V_T) + E_{SAT}L} \propto (V_G - V_T)^{\theta} \quad \text{Eq. 3}$$

$$\boxed{\frac{\delta I_{DSAT}}{I_{DSAT}} \propto \theta \frac{(-\delta V_T)}{(V_G - V_T)}} \quad \text{Eq. 4}$$

Fig. 3. Relationship between change in I_{DLIN}, I_{DSAT}, and V_T. These relations indicate that I_{DSAT} degradation is more than I_{DLIN} degradation **because $1<\theta<2$**, and I_{DSAT} degradation increases with L because **θ increases with L.**

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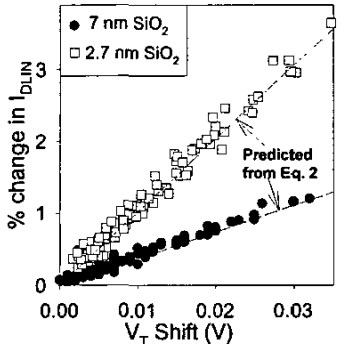

Fig. 4. % change in I_{DLIN} vs. V_T shift, with the dotted lines showing the values predicted by Eq. 2. **Higher I_{DLIN}** degradation is observed for the same V_T shift for thinner dielectric, due to smaller voltage headroom (V_G-V_T).

A relation between the NBTI-induced V_T degradation and I_D degradation is needed to explain these observations. Such a relation can be obtained by differentiating the Level-1 SPICE model equation[1] for I_{DLIN} (Eq. 1) and attributing all the change in drain current to a change in V_T (assumption, validity shown in Section II). Similarly, a relationship between V_T degradation and I_{DSAT} degradation (Eq. 4) is obtained from Eq. 3[2].

Eqs. 2 & 4 can now be used to relate interface trap creation and current degradation. (a). Short channel vs. long channel device: We note that in Eq. 4, θ=2 for long channel devices. As L decreases, velocity saturation results in a lower value of θ, causing less I_{DSAT} degradation. (b). I_{DLIN} vs. I_{DSAT} degradation: I_{DSAT} degradation has been reported to be larger than I_{DLIN} degradation[3]. This can be understood by comparing Eqs. 2 & 4. Since $1<\theta<2$ (Eq. 4), the I_{DSAT} degradation is always larger than I_{DLIN} degradation. (c). Thin vs. Thick dielectric I_{DSAT} degradation: The voltage headroom (V_G-V_T) is smaller for the 2.7nm SiO_2 than the 7nm SiO_2. Smaller headroom[4] causes **the same extent** of V_T degradation to result in a **larger** I_{DSAT} degradation for the 2.7nm dielectric. Fig. 4 shows that the predicted value using Eq. 2 (dotted line) is in excellent agreement with data, establishing a quantitative relationship between I_D and V_T driven specifications.

II. Mobility Degradation

The mobility degradation was neglected in the Eqs. 1 through 4. A plot of effective mobility (μ_{eff}) obtained from split C-V measurements as a function of silicon electric field, (E_{eff}) for 2.7nm SiO_2 (Fig. 5) indicates that mobility degradation is **large close to V_T, but decreases at high V_{GS}**. Since I_{DLIN} and I_{DSAT} are measured at high V_{GS}, neglecting the mobility degradation (as done in Section I) results in <5% error in relating I_D and V_T degradation. However, because mobility degradation at low V_{GS} is significant, the I_D vs. V_{GS} plots before and after stress become significantly different.

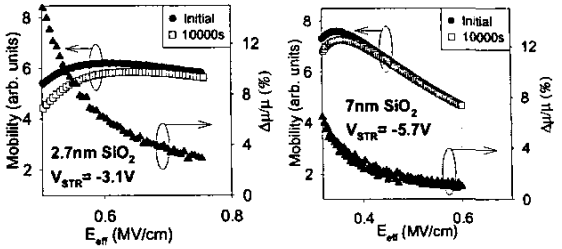

Fig. 5. μ_{eff} vs. E_{eff}, showing that mobility degradation is large at low E_{eff}, but decreases with increasing E_{eff}. The large degradation in mobility at low fields is due to **Coulomb scattering by interface traps**, and decreases at higher fields because of screening by inversion charge. The smaller mobility degradation in 7nm SiO_2 is due to **fewer interface traps** causing the same level of V_T shift ($\Delta V_T \approx q.D_{IT}/C_{OX}$).

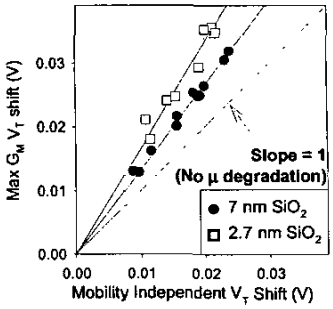

Fig. 6. Mobility-independent V_T shift vs. V_T shift extracted using the Max. G_m technique, showing that the mobility contribution **increases with decreasing dielectric thickness.**

The % change in mobility is smaller for 7nm SiO_2 than for 2.7nm SiO_2, even though the V_T degradation is ~30mV in both cases. The higher specific capacitance of the 2.7nm dielectric results in a larger number of interface traps causing the same V_T degradation ($\Delta V_T \approx qD_{IT}/C_{OX}$). This larger number of interface traps leads to a larger increase in Coulomb scattering due to interface traps. A linear relationship exists between the mobility-independent V_T [5] and V_T extracted using maximum G_M technique (Fig. 6), which incorporates mobility degradation. It is clear that impact of mobility degradation on V_T shift is higher for the 2.7nm dielectric, consistent with Fig. 5. Consequently, SPICE models for NBTI that involve VTHO shift only become **increasingly inaccurate with technology scaling**, as low V_{GS} mobility degradation is not incorporated (impact demonstrated in section IV).

III. Gate-Drain Capacitance (C_{GD}) Change

The normalized C_{GD} before and after NBTI stress is plotted in Fig. 7. The inset shows that the **C_{GD} increases** at ~0V, and shows a lateral shift at negative voltages (due to the V_T shift). The normalized ΔC_{GD} (Fig. 8) shows a peak at ~0V. Fig. 8 shows the results of TCAD simulations with varying levels of donor interface traps. The estimated C_{GD} change agrees remarkably well with the experimental results.

The normalized ΔC_{GD} **obeys a power law** with time, similar to V_T shift (Fig. 9).

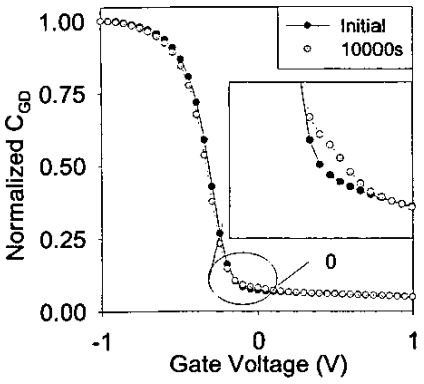

Fig. 7. Normalized C_{GD} vs. Gate Voltage, showing an **increase in C_{GD}** near 0V due to the interface trap capacitance.

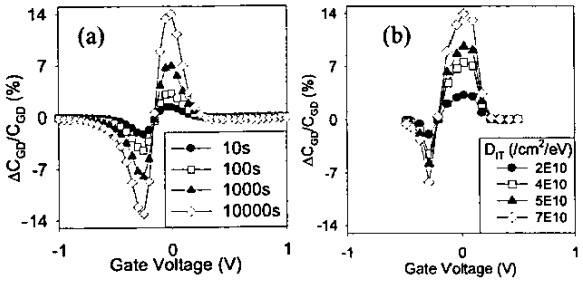

Fig. 8. Experimental (a) and Simulated (b) (TCAD) normalized ΔC_{GD} vs. Gate Voltage. Hence, **donor interface traps** used in the TCAD model accurately capture the experimentally observed C_{GD} trends.

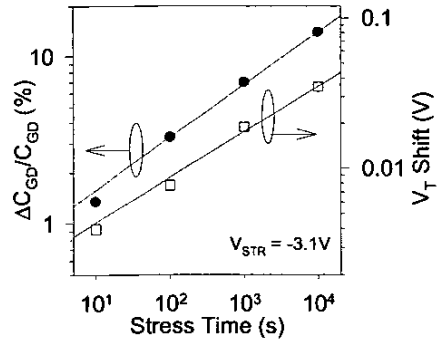

Fig. 9. Normalized C_{GD} change vs. time, showing that the **C_{GD} peak follows a power law**, similar to the V_T shift. The linear relationship between C_{GD} peak and V_T shift enables prediction of C_{GD} peak for any V_T shift.

The gate length and V_{DS} dependence are important, as circuits incorporate transistors with various gate lengths and operate over a range of V_{DS}. The C_{GD} change **increases** with increasing gate length (Fig. 10), due to greater contribution from the interface trap capacitance (C_{IT}). The C_{GD} change as a function of V_{DS} for different V_{GS} (Fig. 11) indicates that maximum change occurs for low V_{GS}. The peak moves to higher V_{DS} for higher gate voltages because V_{DS} causes the entire C_{GD} vs. V_{GS} curve to shift to a higher V_{GS}.

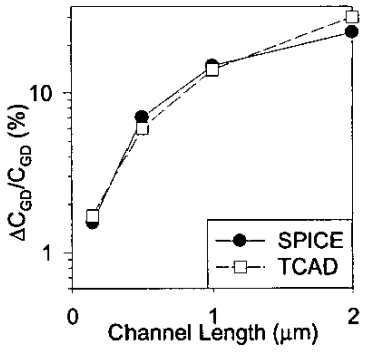

Fig. 10. Simulated normalized ΔC_{GD} peak vs. gate length. The TCAD & SPICE models were calibrated to match the experimental data at L=1μm. Very good agreement is seen at other gate lengths between TCAD and SPICE predictions.

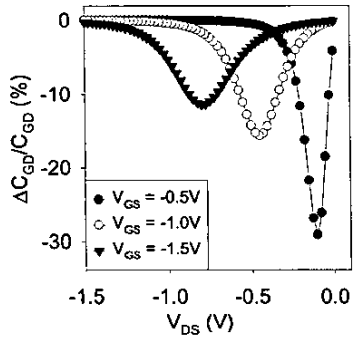

Fig. 11. Simulated normalized C_{GD} change as a function of drain voltage for different gate voltages, showing peak in C_{GD} change moving to **higher V_{DS}** with increasing V_{GS}.

IV. Circuit Impact of NBTI Degradation

The impact of I_{DSAT} and C_{GD} change on inverter ring oscillator (RO) frequency is illustrated by Eq. 7 (Fig. 12). 2% I_{DSAT} degradation causes 1% reduction in RO frequency, but 1% change in C_L directly translates to a 1% reduction in RO frequency. The change in C_{GD} results in degradation of digital and analog circuit performance because of the Miller Effect. Digital circuit performance degradation is evident from Table. 1, which shows that the VTHO shifted SPICE model (ignoring mobility degradation) captures only ~60% of the degradation, while a model incorporating I-V degradation but ignoring C_{GD} change due to NBTI captures ~90% of the frequency degradation. In contrast to the digital circuit, the C_{GD} change is the dominant contributor (70%) to the degradation in unity current gain frequency response of a 2-stage operational amplifier (op-amp) with PMOS input pair, a commonly used analog circuit.

$$\tau_{Delay} = \frac{C_L V_{DD}}{k}\left[\frac{1}{I_N} + \frac{1}{I_P}\right] \quad \text{Eq.5}$$

$$F_{osc} = \frac{1}{kN\tau_D} \quad \text{Eq. 6}$$

$$\frac{\delta F_{osc}}{F_{osc}} = \frac{\delta I_P}{2I_P} - \frac{\delta C_L}{C_L} \quad \text{Eq. 7}$$

C_L = Load Capacitance
I_N, I_P = NMOS and PMOS Drive currents respectively
K = Constant
τ = Ring oscillator delay
F_{OSC} = Ring oscillator frequency

Fig. 12. Relationship between inverter delay, drive current degradation and capacitance change, showing the large impact of change in load capacitance.

Model	RO Frequency Degradation (DIGITAL) (%)	Change in Unity Gain Bandwidth (ANALOG) (%)
VTHO Shifted Model	-3.2	-1.0
Degraded I-V only	-4.5	-1.3
Including C_{GD} Degradation	-4.9	-4.4

Table 1. RO Frequency degradation (change in unity gain bandwidth) due to NBTI. The VTHO shifted SPICE model captures **only ~60% (20%)** of the degradation, while a model incorporating mobility degradation but ignoring C_{GD} change due to NBTI captures ~90% (only 30%) of the frequency degradation.

V. Increased Headroom vs. Increased Degradation

The increase in operating voltage V_{op} (for a specific T_{OX}) has two consequences: (a) increase in headroom (V_{op}-V_T) [4], which results in reduced impact on I_D, and (b) increased degradation due to higher stress voltage. Using analytical expressions, we have quantified the competition between these two trends, and we find that there is an optimum V_{op} at which there is a **minimum in I_D shift** (Fig.13). If V_{op} is below this value, the I_D shift will increase due to reduced headroom.

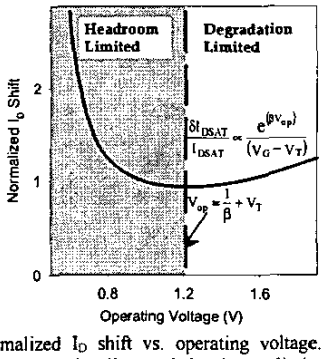

Fig. 13. Normalized I_D shift vs. operating voltage. Two regimes of operating voltage can be discerned, headroom limited and degradation limited. The competition between these two regimes results in a **minimum in normalized I_D shift**.

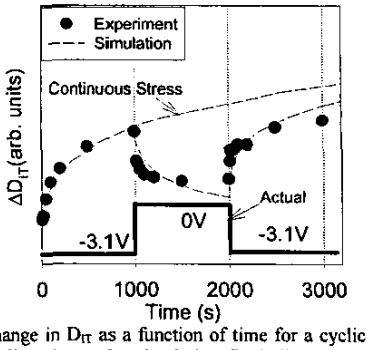

Fig. 14. Change in D_{IT} as a function of time for a cyclic (ON/OFF/ON) stress. The line shows the simulation fit, indicating that **degradation, recovery, and post-stress behavior can be explained** using the reaction-diffusion theory.

VI. Numerical Model for NBTI Degradation

The NBTI reverse reaction has been postulated as the reason for the observed recovery in transistor characteristics [6,7]. The post-recovery response to stress is crucial, as continuous DC stress is seldom seen in circuits. A numerical model based on the reaction-diffusion theory [6] has been developed and the predictions of this model are overlaid on the experimental data (Fig. 14). Application of DC stress following recovery results in a rapid increase in interface state density in the initial period and subsequently slows down to an envelope similar to that of the DC characteristic. It is clear that the model is able to **capture the observed experimental trends accurately**.

Conclusions

A quantitative relationship between the V_T and I_D driven NBTI specifications has been established. Mobility degradation becomes increasingly significant with oxide scaling. Degradation in C_{GD} and its impact on digital and analog circuits has been demonstrated. An optimum operating voltage that balances NBTI degradation against transistor voltage headroom is shown to exist. The reaction-diffusion theory has been used to accurately model NBTI degradation, as well as recovery and post-stress behavior.

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