Compact Modeling and Simulation of Circuit Reliability for 65-nm CMOS Technology

Wenping Wang, *Student Member, IEEE*, Vijay Reddy, Anand T. Krishnan, Rakesh Vattikonda, Srikanth Krishnan, and Yu Cao, *Member, IEEE*

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***Abstract*—Negative bias temperature instability (NBTI) and channel hot carrier (CHC) are the leading reliability concerns for nanoscale transistors. The *de facto* modeling method to analyze CHC is based on substrate current $I_{\rm sub}$, which becomes increasingly problematic with technology scaling as various leakage components dominate $I_{\rm sub}$. In this paper, we present a unified approach that directly predicts the change of key transistor parameters under various process and design conditions for both NBTI and CHC effects. Using the general reaction–diffusion model and the concept of surface potential, the proposed method continuously captures the performance degradation across subthreshold and strong inversion regions. Models are comprehensively verified with an industrial 65-nm technology. By benchmarking the prediction of circuit performance degradation with the measured ring oscillator data and simulations of an amplifier, we demonstrate that the proposed method very well predicts the degradation. For 65-nm technology, NBTI is the dominant reliability concern, and the impact of CHC on circuit performance is relatively small.**

***Index Terms*—Channel hot carrier (CHC), circuit, interface traps, negative bias temperature instability (NBTI), performance, reaction–diffusion (R–D) model, simulation.**

I. Introduction

THE RELENTLESS scaling of CMOS technology inevitably leads to multiple reliability concerns such as negative bias temperature instability (NBTI), which is prominent in PMOS devices [4], [7], [24], [25], [29], and channel hot carrier (CHC), which is prominent in NMOS devices [10], [13], [21], [22]. NBTI occurs due to the generation of the interface traps at the Si/SiO_2 interface when a negative gate bias is applied to the PMOS. It manifests itself as an increase in the threshold voltage $V_{\rm th}$ of the PMOS transistor [4], [7], [16], [25], [29]. Removal of the stress can anneal some of the interface traps, resulting in partial recovery [29], i.e., reduced $V_{\rm th}$ degradation. CHC causes the generation of the interface traps at the Si/SiO_2 interface near the drain end when the gate of NMOS switches. It also results in $V_{\rm th}$ degradation, and this degradation cannot be recovered. Due to the $V_{\rm th}$ degradation, these reliability effects result in poor drive current, lower noise margin, and shorter device and circuit lifetime [17], [23].

To date, research work on NBTI and CHC has been active only within the communities of device and reliability physics [2]–[4], [8], [17]. This is partially due to its complexity, emerging status, and lack of design knowledge and computer-aided design (CAD) tools for managing the NBTI and CHC degradation [1], [11]. Leading industrial companies develop their own models and tools to handle this effect. These tools, however, are usually proprietary and customized to a specific technology. In this case, a generic and Simulation Program with Integrated Circuit Emphasis (SPICE)-compatible model that can accurately predict the degradation would be extremely useful.

In this paper, a predictive NBTI model is presented. It bridges the gap between the technological community and CAD tool developers. The proposed model can be used to predict the effect of dynamic NBTI for any given time. It has two features: 1) the diffusion of hydrogen in poly-Si is considered in this model, instead assuming poly-Si as a reflector or absorber [4], [17], [29]; and 2) the new model captures the dependence of NBTI on the oxide thickness $t_{\rm ox}$ and a variety of diffusing species (H or H_2). Furthermore, due to its compactness, this model is conveniently customized and implemented into the circuit simulation environment, such as SPICE, to predict the degradation of circuit performance.

In addition, this paper proposes a modeling framework that integrates both NBTI and CHC. Traditionally, CHC is characterized by $I_{\rm sub}$ that is induced by hot carriers [13]. However, in the nanoscale region, the $I_{\rm sub}$-based method is not effective since the amount of $I_{\rm sub}$ is dominated by other leakage components such as gate leakage, junction current, and gate-induced drain leakage. Fig. 1 shows the measured $I_{\rm sub}$ in 65-nm technology [9]. It exhibits a significant deviation from the traditional hot-carrier model [13], particularly when the drain voltage is smaller than 1 V. This phenomenon suggests that continuous usage of $I_{\rm sub}$ would overestimate the degradation and result in an overly pessimistic design.

Instead of resorting to $I_{\rm sub}$, we unify the understanding of both NBTI and CHC based on the general reaction–diffusion (R–D) mechanism and directly develop degradation models for key transistor parameters that are affected by the stress,

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W. Wang and Y. Cao are with the Department of Electrical Engineering, Arizona State University, Tempe, AZ 85287 USA (e-mail: wwang39@asu.edu).

V. Reddy, A. T. Krishnan, and S. Krishnan are with the Silicon Technology Development, Texas Instruments, Dallas, TX 75243 USA.

R. Vattikonda is with Broadcom Corporation, Tempe, AZ 85284 USA.

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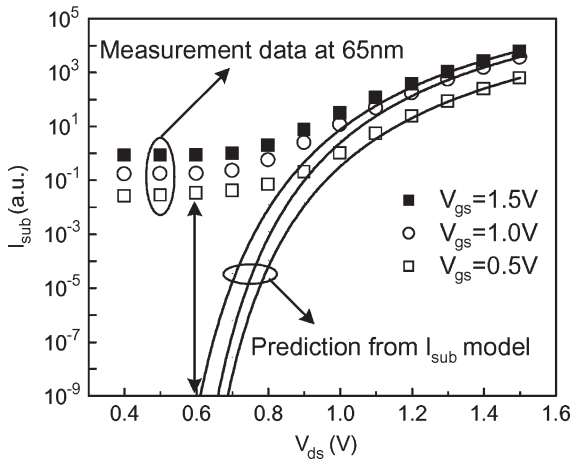


Fig. 1. Deviation of the traditional CHC model of $I_{\rm sub}$.

including threshold voltage degradation $\Delta V_{\rm th}$ and mobility μ. These integrated models are comprehensively verified with an industrial 65-nm technology. This model can capture its dependence on the key process and design parameters (e.g., $V_{\rm th}$, $V_{\rm dd}$, and duty cycle). Due to the introduction of high-k dielectrics, recent experimental data show that the power-law exponent is 0.07–0.10 [26]. Since the high-k gate stack actually consists of two layers, namely a high-k dielectric layer and an interfacial SiO_2 layer [19], the fast stress and recovery component most likely associates with the defects in the SiO_2 interfacial layer induced by the overlaying high-k film. Thus, stress-induced changes in the threshold voltage, i.e., $\Delta V_{\rm th}$, should be modeled by both the R–D theory and hole trapping/detrapping mechanism. Fast stress and recovery can be modeled by using the hole trapping theory, whereas slow stress and recovery can be explained by the R–D model. For 65-nm technology without the introduction of high-k gate stack, we did not observe the hole trapping/detrapping phenomenon from our experimental data. R–D is still the dominant mechanism that can very well explain our data. In addition, transition metal oxides have been shown to contain a high density of preexisting structural defects, which gives rise to the fast transient charging phenomenon [6], [15]. With the improvement of the process, these defects will be gradually reduced, and correspondingly, the fast transient phenomenon can be minimized.

Overall, the predictive models of NBTI and CHC enable efficient design examinations within the standard CAD environment. The outline of the rest of the paper is as follows: The development of the models for $V_{\rm th}$ and μ degradation is described in Section II for both NBTI and CHC. These integrated models are comprehensively verified with an industrial 65-nm technology in Section III. By using the predictive models, both digital and analog circuit performance degradation characterization is discussed in Section IV.

II. Integrated Modeling Paradigm

A. R–D Mechanism

NBTI and CHC can be physically described as the generation of charges in the region close to the Si/SiO_2 interface. Therefore, a common theoretical framework, i.e., the R–D model, is proposed to explain both effects. Fig. 2 shows the cross section of a transistor to illustrate the R–D model.

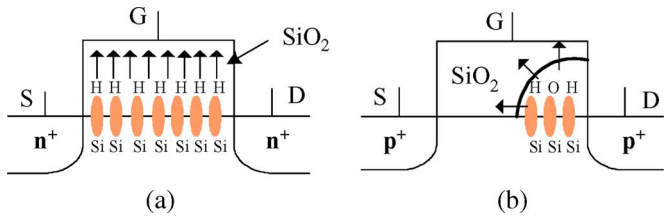


Fig. 2. R–D mechanism. (a) NBTI: 1-D hydrogen species diffusion. (b) CHC: 2-D hot-carrier trapping.

There are two critical steps that happen in the process of NBTI and CHC.

1) *Reaction:* This is where some Si–H or Si–O bonds at the substrate/gate oxide interface are broken under the electrical stress [4], [7], [29]. The species that trigger such reactions can be positive holes in NBTI or hot electrons in CHC [21]. Consequently, interface charges are induced, which cause the increase of $V_{\rm th}$. Given the initial concentration of the Si–H bonds, i.e., N_o, and the concentration of the inversion carriers, i.e., P, the generation rate of the interface traps, i.e., $N_{\rm IT}$, is given by [4]

$$\frac{dN_{\rm IT}}{dt} = k_F(N_o - N_{\rm IT})P - k_R N_{\rm H} N_{\rm IT} \tag{1}$$

where k_F and k_R are the reaction rates of the forward and reverse reactions. Akin to other reactions, the generation rate is an exponential function of the electrical field and temperature. It is also proportional to the density of reaction species, namely holes or hot electrons [4], [7], [29].

2) *Diffusion:* This is where reaction-generated species diffuse away from the interface toward the gate, driven by the gradient of the density. While NBTI happens uniformly in the channel, CHC impacts primarily the drain end, as shown in Fig. 2. This process influences the balance of the reaction and is governed by

$$\frac{dN_{\rm H}}{dt} = D_{\rm H}\frac{d^2 N_{\rm H}}{dx^2}. \tag{2}$$

The solution of (2) exhibits a power-law dependence on time [4], [7], [29]. The exact value of the power-law index indicates the type of diffusion species [7].

B. Model Development

During the initial period of the stress phase, trap generation is slow [2]. Hence, $dN_{\rm IT}/dt \approx 0$ and $N_{\rm IT} \ll N_o$. Thus, (1) reduces to

$$N_{\rm H} N_{\rm IT} \approx \frac{k_F}{k_R} P \cdot N_o. \tag{3}$$

With continued forward reaction, H is produced, and two H atoms combine to generate a H_2 molecule. The concentration of H_2, i.e., N_{H_2}, is related to the concentration of H, i.e., $N_{\rm H}$, using

$$N_{H_2} = k_{\rm H} N_{\rm H}^2. \tag{4}$$

Driven by the gradient of the generated H_2 density, the H_2 current diffuses into oxide and then into poly-Si. This process is governed by (2). The diffusion front $x_{\rm DF}(t) = \sqrt{D_{\rm H_2} t}$. Let t_0 be the time taken by H_2 to reach the SiO_2/poly interface. Once in poly-Si, the diffusion front moves forward in poly-Si as $\sqrt{D_{\rm H_2}(t-t_0)}$. Since the diffusion rate of H_2 in oxide is much larger than its diffusion rate in poly-Si [16], the amount of time t_0 taken by H_2 to reach the SiO_2/poly interface is very small, or $t \gg t_0$. Thus, after time t, the diffusion front is at a distance of $\sqrt{D_{\rm H_2} t} + t_{\rm ox}$ from the Si/SiO_2 interface. The total number of interface charges produced after time t is twice the number of H_2 molecules generated during that time since there are two hydrogen atoms in a hydrogen molecule. Thus

$$N_{\rm IT} = 2 \int_0^{x_{\rm DF}(t)} N_{\rm H_2}(x)dx. \tag{5}$$

The total hydrogen can be divided into two parts: 1) hydrogen in the oxide and 2) hydrogen in the poly-Si. The fast diffusion rate of H_2 in the oxide [16], along with the small thickness of the oxide, leads to a very small difference between the H_2 concentration at the Si/SiO_2 interface and the SiO_2/poly interface. For example, in sub-90-nm technology, the oxide thickness is only 1.2 nm. We introduce a fitting parameter δ to indicate the fractional drop in the concentration of H_2 at the SiO_2/poly interface. Hence, (5) can be rewritten as

$$N_{\rm IT} = 2 \int_0^{t_{\rm ox}} N_{\rm H_2}(x)dx + 2 \int_{t_{\rm ox}}^{\sqrt{D_{\rm H_2} t}+t_{\rm ox}} N_{\rm H_2}(x)dx \tag{6}$$

$$\approx 2\left(\frac{1}{2}(1+\delta)\cdot N_{\rm H_2}(0)\ \cdot\ t_{\rm ox} + \frac{1}{2} N_{\rm H_2}(0)\cdot\sqrt{D_{\rm H_2} t}\right) \tag{7}$$

where $N_{\rm H_2}(0)$ is the concentration of H_2 at the Si/SiO_2 interface, and $\delta N_{\rm H_2}(0)$ represents the density of $N_{\rm H_2}$ at the SiO_2/poly interface. Replacing $N_{\rm H_2}(0)$ from (4) in terms of $N_{\rm H}(0)$, we obtain

$$N_{\rm H}(0) = \left(\frac{N_{\rm IT}}{k_{\rm H}\left((1+\delta)t_{\rm ox} + \sqrt{D_{\rm H_2} t}\right)}\right)^{1/2}. \tag{8}$$

Using (3) and (8), we can represent $N_{\rm IT}$ as

$$N_{\rm IT} = \left(\frac{\sqrt{k_{\rm H}} k_F N_o P}{k_R}\right)^{2/3} \left((1+\delta)t_{\rm ox} + \sqrt{D_{\rm H_2} t}\right)^{1/3} \tag{9}$$

where $k_F N_o / k_R$ is proportional to the vertical electrical field, the inversion hole density $P = C_{\rm ox}(V_{\rm gs} - V_{\rm th})$ for the saturation region, and the diffusion constant $D_{\rm H_2}$ depends on the activation energy and temperature. Substituting (9) in $\Delta V_{\rm th} = qN_{\rm IT}/C_{\rm ox}$, we can obtain the general form of $V_{\rm th}$ degradation as

$$\Delta V_{\rm th}(t) = A\left((1+\delta)t_{\rm ox} + \sqrt{Ct}\right)^{2n} \tag{10}$$

where

$$A = \left(\frac{q t_{\rm ox}}{\epsilon_{\rm ox}}\right)^{1/2n} \sqrt{K^2 C_{\rm ox}(V_{\rm gs} - V_{\rm th})\left(\exp\left(\frac{E_{\rm ox}}{E_0}\right)\right)^2}. \tag{11}$$

C has a temperature dependence as $C = T_o^{-1}\exp(-E_a/kT)$ [20], k being the Boltzmann's constant and T_o being another constant. Although the aforementioned result was derived assuming H_2 as the diffusing species, a similar dependence can be obtained if the diffusing species is assumed to be H. For a H_2 diffusion-based model, $n = 1/6$, and for a H-based model, $n = 1/4$. In addition, the diffusion constant will correspond to H, and the multiplication factor can also be modified accordingly.

In the recovery phase, due to the absence of holes, there is no net generation of interface traps. The hydrogen species that were generated during the stress phase continue to diffuse away from the interface toward the poly-Si. At the same time, some of the hydrogen species that are closer to the interface diffuse back and repassivate the broken Si^+ bonds. This results in the reduction of the H_2 density $N^A_{\rm H_2}$. This is because the H/H_2 diffusion is faster in the oxide, and it very quickly anneals the broken Si–H bonds [16]. The H/H_2 density is much higher in the poly-Si than in the oxide. Let t_1 be the time for the recovery to be applied after stress and $N_{\rm IT}(t_1)$ be the number of interface charges at the end of the stress cycle. Let $N^A_{\rm IT}(t)$ be the number of charges annealed at time t. Therefore, the number of interface charges at time t is given by

$$N_{\rm IT}(t) = N_{\rm IT}(t_1) - N^A_{\rm IT}(t). \tag{12}$$

From the stress phase, using (7), the number of interface charges at time t is given by

$$N_{\rm IT}(t) = \left((1+\delta)\cdot t_{\rm ox} + \sqrt{Ct}\right)\cdot N_{\rm H_2}(0). \tag{13}$$

Due to the widely different diffusivity of H_2 in the oxide and poly-Si, the recovery becomes a two-step process, with fast recovery driven by H_2 in the oxide, followed by slow recovery of H_2 by backdiffusion from the poly-Si. The number of annealed traps can be due to two parts: 1) recombination of H_2 in the oxide and 2) backdiffusion of H_2 in the poly-Si [2]. Thus

$$N^A_{\rm IT}(t) = 2\left(\xi_1 t_e + \frac{1}{2}\sqrt{\xi_2 C(t-t_1)}\right)\cdot N_{\rm H_2}(0) \tag{14}$$

where ξ_1 and ξ_2 are the backdiffusion constants. Depending on the duration $t - t_1$ of the recovery, the effective oxide thickness t_e either equals $t_{\rm ox}$ or the diffusion distance of hydrogen in the initial stage of recovery. Here, we define the time when all the hydrogen species in the oxide are recombined with the interface traps as t'. This corresponds to the time taken by the diffusing species to diffuse to a distance of $t_{\rm ox}$. For example, for a 1.2-nm oxide, the typical value of t' is about 2.5 ms for H_2 and 0.14 μs for H, based on their diffusion constants [16]. If $t - t_1 \geq t'$, t_e equals $t_{\rm ox}$; otherwise, t_e equals

TABLE I
MODELS OF THE DEGRADED PARAMETERS $\Delta V_{\rm th}$ AND μ

ΔV_{th}	NBTI	Stress	$\left(K_v(t-t_0)^{0.5} + \sqrt[2n]{\Delta V_{th0}}\right)^{2n}$
		Recovery	$\Delta V_{th0}\left(1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(t-t_0)}}{2t_{ox} + \sqrt{Ct}}\right)$
	CHC		$\frac{q}{C_{ox}} K_2 \sqrt{Q_i} exp(\frac{E_{ox}}{E_{o2}}) exp(-\frac{\varphi_{it}}{q\lambda E_m}) t^{n'}$
μ	$\mu_{eff}/(1+\alpha N_{IT})^m$		

TABLE II
MODEL PARAMETERS FOR DIFFERENT OPERATION REGIONS

	Strong Inversion	Subthreshold region
Q_i	$C_{ox}(V_{gs}-V_{th})$	$\sqrt{\frac{\epsilon_0\epsilon_{Si}qN_b}{2\phi_s}} V_t exp((\phi_s - 2\phi_f)/V_t)$
E_{ox}	$(V_{gs}-V_{th})/t_{ox}$	$\epsilon_{Si}E_{Si}/\epsilon_{ox}$
V_{dsat}	$\frac{(V_{gs}-V_{theff}+2V_t)L_{eff}E_{sat}}{V_{gs}-V_{theff}+2V_t+A_{bulk}L_{eff}E_{sat}}$	
K_v	$(\frac{qt_{ox}}{\epsilon_{ox}})^3 {K_1}^2 C_{ox}(V_{gs}-V_{th})\sqrt{C} exp(\frac{2E_{ox}}{E_{o1}})$	
ϕ_s	$V_{gs}-V_{fb}+\gamma^2/2-\gamma\sqrt{V_{gs}-V_{fb}+\gamma^4/2}$	
E_{Si}	$(\frac{2qN_b}{\epsilon_0\epsilon_{Si}}(\phi_s + V_t exp(-\frac{2\phi_f}{V_t})(exp(\frac{\phi_s}{V_t})-1)))^{0.5}$	
E_m	$(V_{ds}-V_{dsat})/l$	C $\quad exp(-E_a/kT)/T_0$
γ	$\sqrt{2\epsilon qN_b}/C_{ox}$	ϕ_f $\quad V_t log(N_b/n_i)$

$K_1(C^{-0.5}nm^{-2.5})$	7.5			$T_0(s/nm^2)$	10^{-8}
δ	0.5	$E_a(eV)$	0.49	$E_{01}(V/nm)$	0.08
ξ_1	0.9	ξ_2	0.5	$E_{02}(V/nm)$	0.8
$K_2(nmC^{-0.5})$	1.7×10^8			$E_{sat}(V/nm)$	0.011
$\varphi_{it}(eV)$	3.7	$l(nm)$	17	$\lambda(nm)$	7.8
$V_t(V)$	0.0259	A_{bulk}	0.005	α	5
$V_{fb}(V)$	-1.05	m	1.6		

the diffusion distance of hydrogen in the oxide. From (13) and (14)

$$N_{\rm IT}^{A}(t) = N_{\rm IT}(t)\left(\frac{2\xi_1 t_e + \sqrt{\xi_2 C(t-t_1)}}{(1+\delta)\cdot t_{\rm ox} + \sqrt{Ct}}\right). \quad (15)$$

Substituting $N_{\rm IT}^{A}(t)$ from (15) into (12), simplifying, and using $\Delta V_{\rm th} = qN_{\rm IT}/C_{\rm ox}$, we obtain

$$\Delta V_{\rm th}(t) = \Delta V_{\rm th}(t_1)\left(1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(t-t_1)}}{(1+\delta)\cdot t_{\rm ox} + \sqrt{Ct}}\right) \quad (16)$$

where $V_{\rm th}(t_1)$ is the threshold voltage at the end of the stress phase.

For a dynamic operation, the PMOS transistor undergoes alternate stress ($V_{\rm gs} = -V_{\rm dd}$) and recovery ($V_{\rm gs} = 0$) periods. Using (10) and (16), we can obtain

Stress :

$$\Delta V_{\rm th}(t) = \left(K_v(t-t_0)^{1/2} + \sqrt[2n]{\Delta V_{\rm th}(t_0)}\right)^{2n}. \quad (17)$$

Recovery :

$$\Delta V_{\rm th}(t) = \Delta V_{\rm th}(t_1)\left(1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(t-t_1)}}{(1+\delta)t_{\rm ox} + \sqrt{Ct}}\right). \quad (18)$$

The times t_0 and t_1 correspond to the time at which the stress and recovery phases begin, respectively.

In addition to the change of $V_{\rm th}$, the increase in interface charges also results in the degradation of carrier mobility [12], [13], [27]. The mobility degradation as a function of interface trap density can be expressed by the empirical relationship [12], [27]

$$\mu = \mu_{\rm eff}/(1+\alpha N_{\rm IT})^m \quad (19)$$

where $N_{\rm IT} = \Delta V_{\rm th} C_{\rm ox}/q$.

Consequently, we derive the models for $\Delta V_{\rm th}$ and μ, as shown in Table I. For the degradation of $V_{\rm th}$ in NBTI, both stress and recovery phases are significant, whereas the recovery phase is negligible in CHC. The power-law dependence of NBTI, i.e., n, equals 0.16 if H_2 is the diffusion species, and n equals 0.25 for H diffusion. In CHC, the time exponential constant n' is 0.45.

The key parameters that determine the degradation rate include the inversion charge Q_i, electrical field $E_{\rm ox}$, and temperature (Table I). In the strong inversion region, $Q_i = C_{\rm ox}(V_{\rm gs} - V_{\rm th})$ and $E_{\rm ox} = (V_{\rm gs} - V_{\rm th})/t_{\rm ox}$. While traditionally the reliability degradation is only a concern in the strong inversion region, the degradation in the subthreshold region becomes more pronounced since the advanced design stays longer in the standby mode. To physically predict Q_i and $E_{\rm ox}$ across various operation regions, i.e., subthreshold and strong inversion, we formulate our model based on the concept of the surface potential ϕ_s. In the subthreshold region, Q_i can be expressed as [28]

$$Q_i = \sqrt{\frac{\epsilon_0\epsilon_{\rm Si}qN_b}{2\phi_s}} V_t \exp\left((\phi_s - 2\phi_f)/V_t\right) \quad (20)$$

and $E_{\rm ox}$ can be expressed as [5]

$$E_{\rm ox} = \epsilon_{\rm Si}E_{\rm Si}/\epsilon_{\rm ox} \quad (21)$$

where

$$E_{\rm Si} = \sqrt{\frac{2qN_b}{\epsilon_0\epsilon_{\rm Si}}\left(\phi_s + V_t\exp\left(-\frac{2\phi_f}{V_t}\right)\left(\exp\left(\frac{\phi_s}{V_t}\right) - 1\right)\right)}. \quad (22)$$

In (20) and (22), V_t is the thermal voltage for room temperature, N_b is the substrate doping concentration, ϕ_f is the Fermi potential, and ϕ_s is the surface potential, which is given by [28]

$$\phi_s = V_{\rm gs} - V_{\rm fb} + \frac{\gamma^2}{2} - \gamma\sqrt{V_{\rm gs} - V_{\rm fb} + \frac{\gamma^4}{2}} \quad (23)$$

where γ is body effect coefficient, and $V_{\rm fb}$ is the flatband voltage.

In summary, the complete set of the model parameters for different operation regions are listed in Table II. The compact

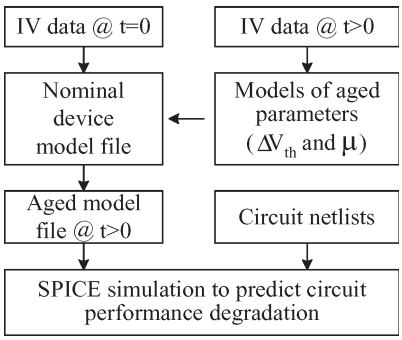


Fig. 3. Data flow and structure for the prediction of circuit performance degradation.

model shown in Table I can be easily characterized for a given technology and implemented in a circuit simulation environment, such as SPICE. In the following section, we validate the various dependences of NBTI and CHC on channel length L, gate–source voltage $V_{\rm gs}$, and drain–source voltage $V_{\rm ds}$, as well as the subthreshold behaviors.

III. Model Verification

A. Extraction of Model Parameters

In the nanoscale regime, both process variation and reliability degradation are pronounced. While the effect of process variation is static after the fabrication, reliability degradation is dynamically dependent on circuit operations. To extract model parameters for reliability degradation, the first step is to decouple static variation and time-dependent degradation. Fig. 3 presents the flow diagram to extract related parameters and predict circuit performance degradation. By examining the measurement data at different times, it effectively decouples the change caused by process variation from that caused by the aging effects (i.e., NBTI of PMOS and CHC of NMOS).

We begin with the current–voltage $(I$–$V)$ data at $t = 0$ to prepare the nominal model file and identify process variations from one device to another. The value of threshold voltage is extracted from the subthreshold current using the constant-current method, whereas the mobility is from the linear region [30]. For process variations, the main parameters include effective channel length $L_{\rm eff}$ and $V_{\rm th}$. Thereafter, we extract the degraded parameters $\Delta V_{\rm th}$ and μ from the I–V data at $t > 0$. There are four fitting parameters in the newly developed model, including K_1, E_a, T_0, and E_{01}. E_a and T_0 are responsible for the degradation under various temperatures. The value of E_{01} is adjusted by fitting different bias conditions. Finally, K_1 is tuned to minimize the overall error against the measurement.

The fitting parameters in the reliability model may change from one technology to another, but they are relatively insensitive to local process variations at the transistor level. This observation is confirmed in Table III, which validates the difference in threshold voltage induced by process variation and NBTI. Although these devices suffer from a large amount of process variations at $t = 0$, their temporal $V_{\rm th}$ degradation can be accurately predicted by the same set of reliability parameters. Therefore, during the preparation of reliability models, we only need to focus on the data from one device. The difference among devices is taken care by process variations at $t = 0$. Combining the nominal transistor model file with aged parameters, we can predict the degradation of transistor and circuit performance at any time.

TABLE III
Model Prediction Error for Different Devices

Device	ΔV_{th}^{*} (%) t=0 s	ΔV_{th} @ $t = 10^5 s$		
		$Data^{*}$ (%)	$Model^{*}$ (%)	$Error$ (%)
1	12.03	5.43	5.50	1.29
2	2.85	3.51	3.66	4.27
3	-6.75	8.02	8.23	2.62
4	-8.14	18.26	18.37	0.60

$*$: Normalized to the mean value of V_{th} (t=0) for the four devices.

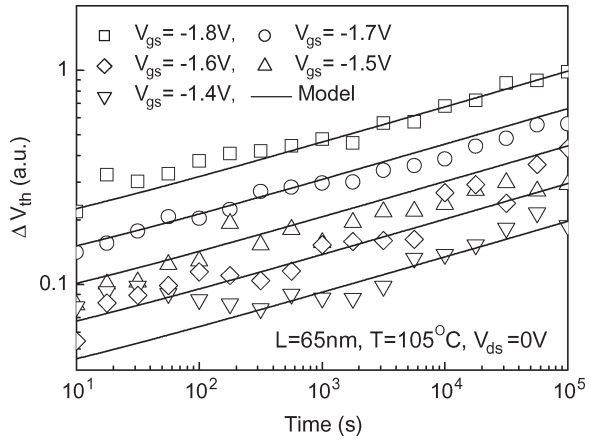


Fig. 4. V_{gs} dependence of NBTI.

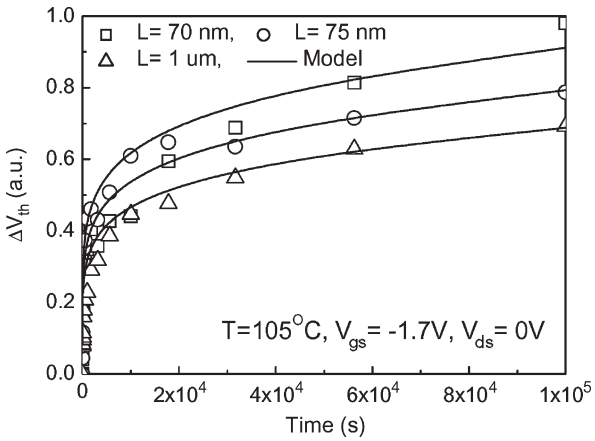
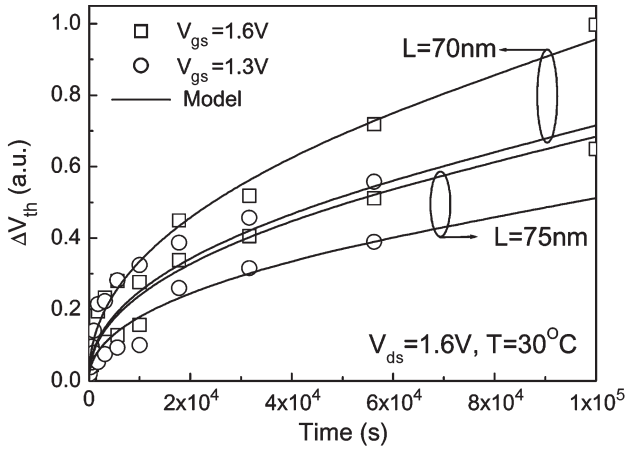


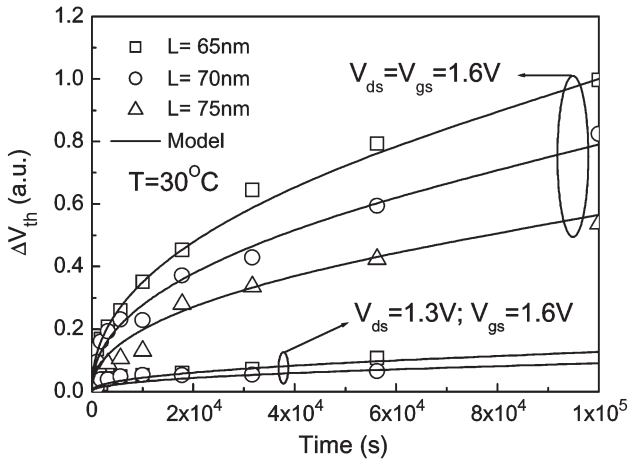
Fig. 5. L dependence of NBTI.

B. Comprehensive Model Verification

Comprehensive degradation data are collected for 65-nm CMOS technology under various temperatures T and bias conditions [9]. Fig. 4 validates the increase in $V_{\rm th}$ under NBTI at different electrical stress. NBTI is strongly affected by the vertical electrical field, which is proportional to $V_{\rm gs}$. With the increase of $V_{\rm gs}$, $\Delta V_{\rm th}$ exponentially increases as a result of the reaction process. For a small range of L tuning, NBTI is relatively independent (Fig. 5), except that the



(a)



(b)

Fig. 6. CHC of NMOS under various L and bias conditions. (a) $V_{\rm gs}$ and L dependence. (b) $V_{\rm ds}$ and L dependence.

nominal $V_{\rm th}$ needs to be adjusted based on the DIBL effect (Table I).

Fig. 6 systematically verifies the $V_{\rm th}$ change in NMOS devices due to CHC under various L and bias conditions. Without using $I_{\rm sub}$ as the monitor, the proposed model in Table I accurately predicts $\Delta V_{\rm th}$ under various gate and drain voltages. Compared with NBTI, CHC is affected by both vertical and lateral electrical fields.

Contrary to NBTI, CHC has a strong dependence on the channel length of the NMOS. With the increase in L, the damage region when compared with L decreases, and thus, there is a reduction in $V_{\rm th}$ degradation under CHC [18]. Fig. 7 further demonstrates that CHC is pronounced even in the subthreshold region.

With the degradation models for $\Delta V_{\rm th}$ and μ being available, we directly predict the performance of transistors and circuits under NBTI and CHC effects according to the paradigm shown in Fig. 3. By integrating the degraded parameters $\Delta V_{\rm th}$ and μ, which are function of degraded time with the nominal model file, an aged model file is obtained. The aged model file can be used to predict the performance of transistors and circuits. Fig. 8 shows a complete set of I–V curves of a single transistor after the degradation, where the root-mean-square error is 0.8%.

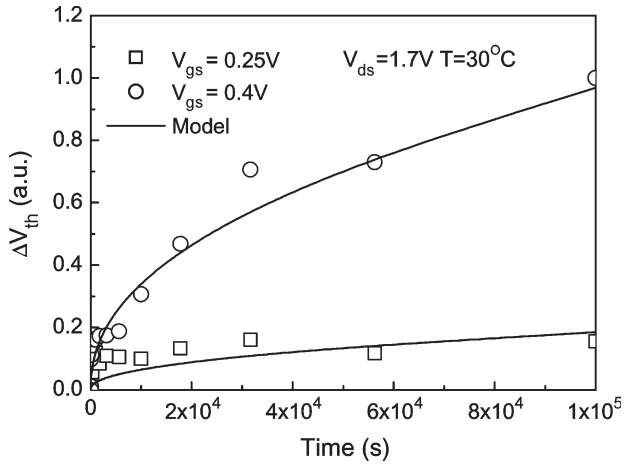


Fig. 7. Subthreshold region for CHC.

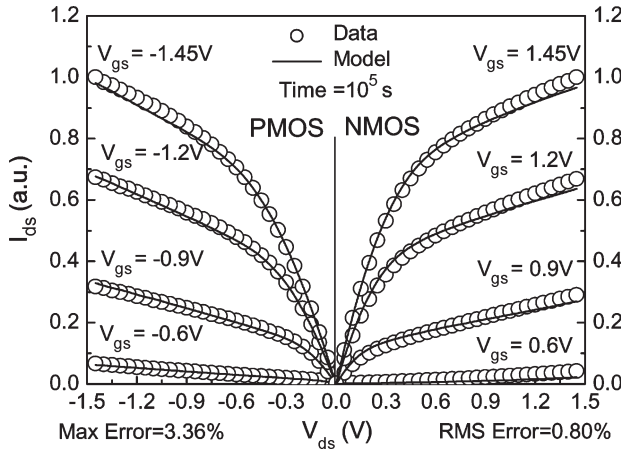


Fig. 8. I–V verification for NBTI of PMOS and CHC of NMOS.

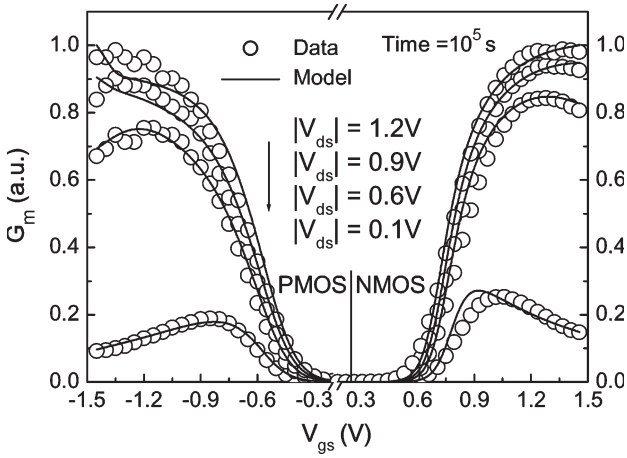


Fig. 9. G_m verification for NBTI of PMOS and CHC of NMOS.

In addition to the degradation of drive current, the development of interface charges also results in the degradation of important metrics for analog circuit design, such as transconductance G_m and drain conductance $G_{\rm ds}$ [18]. Fig. 9 evaluates G_m for both NBTI and CHC after a stress of 10^5 s under various biasing conditions. The proposed model well predicts the degradation.

TABLE IV
GAIN FOR NMOS AND PMOS

G_m/G_{ds}	NMOS		PMOS	
	Data	Model	Data	Model
$\|V_{gs}\| = 1.2V, \|V_{ds}\| = 1.2V$	7.03	6.51	5.55	5.75
$\|V_{gs}\| = 1.2V, \|V_{ds}\| = 0.9V$	5.59	5.56	4.62	4.20
$\|V_{gs}\| = 1.2V, \|V_{ds}\| = 0.6V$	3.44	3.66	2.79	3.00
$\|V_{gs}\| = 1.2V, \|V_{ds}\| = 0.1V$	0.20	0.19	0.12	0.13
Max error	9.09%		7.39%	

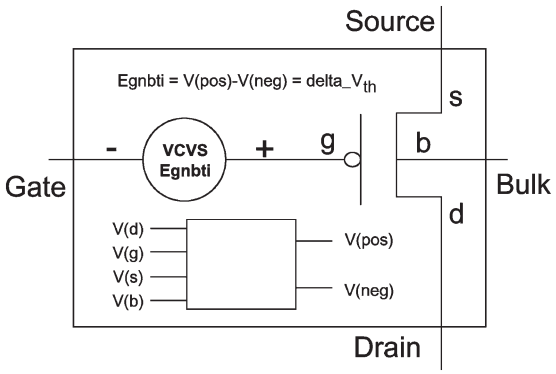


Fig. 10. Subcircuit model for the PMOS NBTI effect.

Gain degradation of a single NMOS and a single PMOS with dc stress is further shown in Table IV, where the gain is given by Gain $= G_m/G_{\rm ds}$. G_m and $G_{\rm ds}$ are separately measured at four operating points, i.e., $|V_{\rm gs}| = 1.2$ V and $|V_{\rm ds}| = 1.2$, 0.9, 0.6, and 0.1 V. These important analog metrics are well predicted with maximum errors of 9.09% and 7.39% for CHC and NBTI, respectively.

IV. CIRCUIT RELIABILITY SIMULATION

With the scaling of CMOS technology, the impact of reliability degradation on circuit performance becomes more pronounced. In this section, we apply the aged model file in SPICE and investigate the performance degradation for representative digital and analog circuits.

A. Subcircuit Model

The new model is compatible with the standard MOSFET model, such as BSIM, and the surface-potential-based compact MOSFET model, such as PSP. It can be conveniently customized and implemented into the circuit simulation environment, such as SPICE, to predict the degradation of circuit performance. Fig. 10 shows the subcircuit module for the PMOS transistor that is used for SPICE. The increase in $V_{\rm th}$ was modeled as a voltage-controlled voltage source (VCVS: Egnbti). The VCVS leads to a decrease in $V_{\rm gs}$ (compared with $V_{\rm GS}$) and subsequently reduces the drain current. The decrease in $V_{\rm gs}$ emulates the increase in $V_{\rm th}$ that is induced by the NBTI effect. The instantaneous increase in $V_{\rm th}$ is equal to the voltage difference between the VCVS nodes [Egnbti $= \Delta V_{\rm th}(t)$].

In complex circuits with a large number of PMOS transistors, a subcircuit model can be used to accurately estimate the degradation in threshold voltage. The degradation in threshold voltage for a particular PMOS transistor will depend on the circuit topology and the bias conditions during the operation. Since the model is calibrated for various bias conditions and temperatures (Section III), the subcircuit model accurately captures the NBTI degradation. Similarly, the degradation of $V_{\rm th}$ caused by CHC is calculated by using a subcircuit module for NMOS.

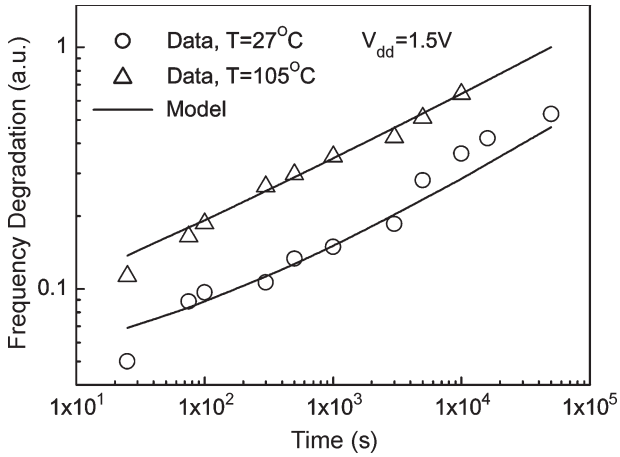


Fig. 11. Ring oscillator frequency degradation.

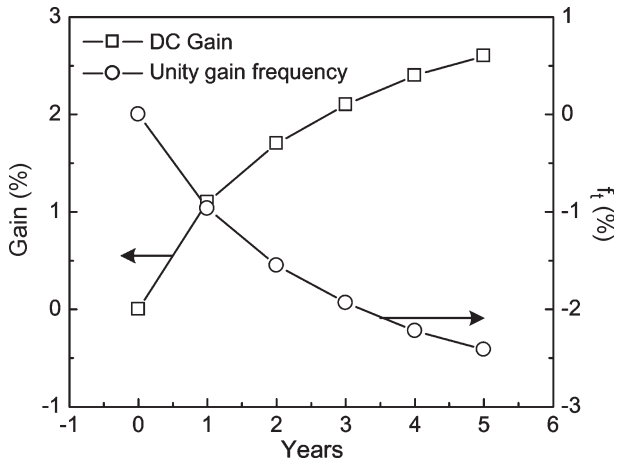


Fig. 12. Op-Amp dc gain and unity gain frequency degradation.

B. Circuit Performance Prediction

The ring oscillator is selected as the representation for digital circuit since it is widely used as a performance metric. Fig. 11 shows the frequency change of a ring oscillator with 11 stages of inverters at 65-nm technology over the period of 10^5 s, and the switching frequency of such a digital oscillator degrades more than 1%. It is readily observed from Fig. 11 that frequency degradation increases significantly as T increases.

Fig. 12 further studies the degradation of a two-stage CMOS operational amplifier (Op-Amp) [14]. To reduce the flicker noise, PMOS transistors are usually used as input terminals. Hence, the NBTI effect can have a dramatic effect on Op-Amp performance metrics. Fig. 12 shows the trend followed by the dc gain and the unity gain frequency f_t as a function of time. As the NBTI effect decreases the bias current in the Op-Amp, the overall dc gain increases, which results in the degradation of f_t. A decrease of about 2.5% is observed in f_t over a span of five

years. This degradation is lesser than the typical degradation of various metrics in digital circuits, just as stress voltages in analog circuits are usually not rail to rail.

Unlike CHC that occurs only during dynamic switching, NBTI is caused during static stress on the oxide even without current flow. Consequently, the threshold voltage change caused by NBTI for the PMOS transistor has become the dominant factor to limit the lifetime, which is much shorter than that defined by the hot-carrier-induced degradation of the NMOS transistor.

V. Conclusion

The proposed models integrate NBTI and CHC into the general R–D mechanism. The degradation of the key parameters $\Delta V_{\rm th}$ and μ is directly captured by analytical models, without using $I_{\rm sub}$. Model accuracy and efficiency were comprehensively verified with 65-nm experimental data. This new approach enables efficient and convenient reliability modeling. It is fully compatible with standard transistor models. A new transistor and circuit performance prediction paradigm is proposed. It can effectively decouple the process variation between different devices and accurately predict the performance degradation of circuits caused by the aging effects (NBTI and CHC). These results can be easily incorporated into design tools to diagnose and mitigate the degradation. We further investigate the impact of NBTI and CHC on digital and analog benchmark circuits.

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Wenping Wang (S'06) received the B.S. and M.S. degrees from the Changchun University of Science and Technology, Changchun, China, in 2000 and 2003, respectively. She did her Master research work at Peking University, Beijing, China, from 2001 to 2003. She is currently working toward the Ph.D. degree in the Department of Electrical Engineering, Arizona State University, Tempe.

Her research interests include modeling of transistor and circuit reliability degradation, particularly negative bias temperature instability (NBTI) and channel hot carrier (CHC) effects, simulation method and design solutions for circuit aging, and CMOS low-power and reliable design.

Vijay Reddy received the Ph.D. degree in electrical engineering from the University of Texas at Austin in 1994.

He joined Texas Instruments, Dallas, in 1994 and has worked on several topics concerning transistor and circuit reliability and product qualification methodologies. He is currently a Senior Member of Technical Staff with Texas Instruments. He has authored or coauthored more than 20 papers published in conference proceedings of the International Reliability Physics Symposium (IRPS), the International Electron Device Meeting (IEDM), and the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium. He is the holder of nine patents with several pending.

Dr. Reddy has served on the program committees for the IRPS and the IEDM and has presented invited tutorials on CMOS Reliability at the IRPS in 2002–2004 and at the International Conference on Microelectronic Test Structures in 2006. He was the recipient of the 2002 IRPS Outstanding Paper Award for his work on the circuit impact of NBTI and was a corecipient of the 2004 IRPS Outstanding Paper Award and the 2002 EOS/ESD Symposium Best Paper/Best Presentation Awards.

Anand T. Krishnan received the B.Tech. degree in metallurgical engineering from Banaras Hindu University, Varanasi, India, in 1994 and the M.S. and Ph.D. degrees in materials from The Pennsylvania State University, University Park, in 1997 and 2000, respectively.

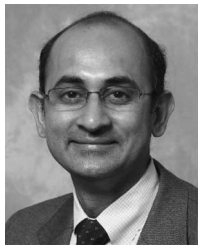
In 2000, he joined the Silicon Technology Development Group, Texas Instruments, Dallas, where he is currently a Reliability Engineer. He has authored or coauthored 42 papers. He is the holder of ten patents. His interests and activities are in the areas of negative bias temperature instability, dielectric breakdown physics, and plasma-charging damage.

Dr. Krishnan has served on the Technical Program Committees for the International Reliability Physics Symposium, the Integrated Reliability Workshop, and the Plasma Process-Induced Damage (P2ID) Symposium.

Rakesh Vattikonda received the B.Tech. degree from Indian Institute of Technology, Guwahati, India, and the M.Tech. degree from Arizona State University, Tempe.

He is currently with Broadcom Corporation, Tempe, as a Memory Design Engineer. His research interests are in circuit design and modeling in nanometer technologies.

Mr. Vattikonda was the recipient of the Best Paper in Session Award at the 2006 Semiconductor Research Corporation Student Symposium in modeling and simulation session.



Srikanth Krishnan received the B.Tech. degree in electrical engineering from the Indian Institute of Technology Madras, Chennai, India, in 1985, the M.S. and Ph.D. degrees in engineering science from The Pennsylvania State University, University Park, in 1988 and 1992, respectively, and the M.B.A. degree from Southern Methodist University, Dallas, TX, in 2000.

He joined the Plasma Etch Group, Semiconductor Process and Design Center, Texas Instruments, Dallas, where he worked on plasma damage effects on transistor performance. In 1998, he joined the Reliability Group, Texas Instruments, and subsequently led the 130-nm component reliability effort. He is currently the Device Reliability Manager with Texas Instruments, where he is responsible for component reliability of CMOS technology nodes. During his 15-year career at Texas Instruments, he has authored 30 papers (six invited) and one trade secret. He is the holder of 20 patents.

Dr. Krishnan served on the Technical Program Committee for the International Reliability Physics Symposium (IRPS) in 1999. He was appointed to the Management Committee of the IRPS in 2003. He served on the Program Committee for the Plasma Process-Induced Damage Symposium (P2ID) and was the Vice-Chairman and Chairman for the P2ID in 2003 and 2004, respectively.

Yu Cao (S'99–M'02) received the B.S. degree in physics from Peking University, Beijing, China, in 1996 and the M.A. degree in biophysics and the Ph.D. degree in electrical engineering from University of California, Berkeley, in 1999 and 2002, respectively.

He worked as a Summer Intern with Hewlett-Packard Laboratories, Palo Alto, CA, in 2000 and with the Microelectronics Division, IBM, East Fishkill, NY, in 2001. After working as a Postdoctoral Researcher with the Berkeley Wireless Research Center, he is currently an Assistant Professor of electrical engineering with Arizona State University, Tempe. He has published numerous articles and coauthored one book on nano-CMOS physical and circuit design. His research interests include modeling and analysis of nanoscale CMOS circuits, physical-level design and tools for variability and reliability, reliable integration of postsilicon technologies, and low-power design solutions.

Dr. Cao currently serves on the Technical Program Committee for numerous design automation and circuit design conferences. He was a recipient of the 2007 Best Paper Award at the International Symposium on Low Power Electronics and Design, the 2006 National Science Foundation CAREER Award, the 2006 and 2007 IBM Faculty Award, the 2004 Best Paper Award at the International Symposium on Quality Electronic Design, and the 2000 Beatrice Winner Award at the International Solid-State Circuits Conference.