Impact of Negative Bias Temperature Instability on Digital Circuit Reliability

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ABSTRACT

We have examined the impact of NBTI degradation on digital circuits through the stressing of ring oscillator circuits. By subjecting the circuit to pMOS NBTI stress, we have unambiguously determined the circuit reliability impact of NBTI. We demonstrate that the relative frequency degradation of the NBTI stressed ring oscillator increases as the voltage at operation decreases. This behavior can be explained by reduced transistor gate overdrive and reduced voltage headroom at the circuit level. We present evidence that donor interface state generation during NBTI stress is a significant component of the transistor degradation. Furthermore, we show that the Static Noise Margin of a SRAM memory cell is degraded by NBTI and the relative degradation increases as the operating voltage decreases.

INTRODUCTION

There has been a recent escalation in interest on the reliability impact of pMOS negative bias temperature instability (NBTI) [1,2]. The parametric manifestation of NBTI damage is a decrease in the drive current and an increase in the threshold voltage. To date, the focus of the NBTI literature [3] has been on discrete transistor parameter drift, rather than on circuit performance drift. Recent work has explored the NBTI impact on analog circuit reliability through the study of NBTI drift on long-channel pMOS transistors, suitable for use in sensitive analog circuits such as operational amplifiers [4,5]. For digital circuits, an indirect correlation of NBTI drift to circuit performance drift has been reported [6]. We will show unambiguously the digital circuit reliability impact of NBTI. The experiments described here were performed on a 0.13μm CMOS process with a nominal operating voltage of 1.5V and gate oxide thickness of 26Å [7].

In this paper, we will show that the dominant degradation mode that occurs during static CMOS operation is pMOS NBTI. The circuit impact of pMOS NBTI is demonstrated through the static stress of a ring oscillator. We then present evidence that donor interface state generation during NBTI stress is a significant component of the transistor degradation. Circuit simulation using degraded SPICE models is also performed to corroborate the experimental ring oscillator data. Finally, we present additional circuit simulations illustrating the NBTI induced degradation of the Static Noise Margin (SNM) of a 6-T SRAM memory cell.

EXPERIMENTAL APPROACH

A. Static CMOS Inverter Degradation Modes

If one considers the operation of a CMOS inverter, shown below in Figure 1, the impact of steady-state degradation must be considered due to the fact that an inverter is in this mode for the majority of a clock duty cycle. This is the case, in particular, for high-speed, short rise time signals where the capacitive load the inverter is driving has been charged to the supply rails.

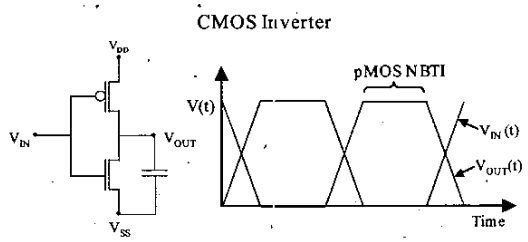

Figure 1. Circuit schematic of a CMOS inverter driving a capacative load. Steady-state degradation should be considered since the inverter is in this mode for the majority of a clock duty cycle. Also shown is the portion of the waveform where pMOS NBTI can occur.

The degradation modes, tabulated in Table 1, during steady-state inverter operation are pMOS NBTI, Off-state pMOS, nMOS PBTI (positive bias temperature instability), and Off-State nMOS.

Inverter Biasing Configuration	V_{IN}	V_{OUT}	nMOS Stress Mode	pMOS Stress Mode
1	V_{DD}	0V	PBTI	Off-State
2	0V	V_{DD}	Off-State	NBTI

Table 1. Degradation modes present in a CMOS inverter during steady state operation.

A pictorial representation of the various degradation modes tabulated in Table 1 is shown in Figure 2, where V_{DD} is the supply voltage.

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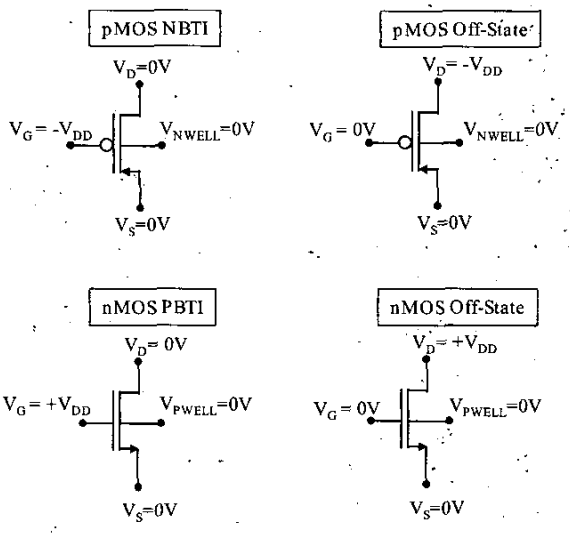

Figure 2. Degradation modes present during steady-state CMOS inverter operation.

To understand the relative impact of the various stress modes, discrete nMOS and pMOS transistors were stressed in the configurations shown in Figure 2. The threshold voltage, V_{TH}, drift evolution versus stress (V_{DD}=2.8V and T=105°C) time is shown in Figure 3 and clearly indicates that pMOS NBTI degradation is much more significant than the other three degradation modes. The stress voltage and temperature conditions were chosen to accelerate the transistor degradation. A similar trend is also observed for the transistor drain current, I_D, drift evolution.

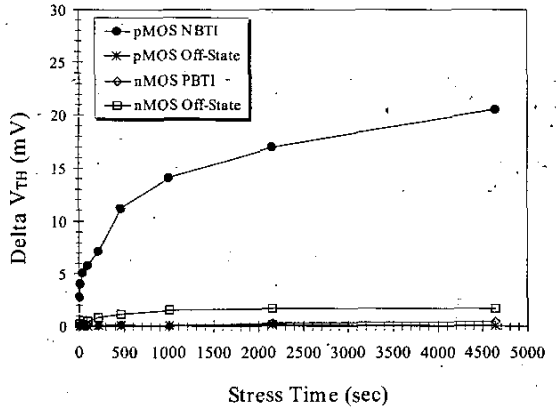

Figure 3. V_{TH} drift versus stress time (T=105°C) for the various stress modes observed in a CMOS inverter during steady state operation. The stress applied at the appropriate nodes was 2.8V. PMOS NBTI degradation is the dominant degradation mode.

Therefore, we can conclude that pMOS NBTI degradation is the dominant degradation mechanism during a static (or steady-state) stress of the CMOS inverter. Furthermore, we note that we can disregard channel hot-carrier (CHC) degradation since the static stress precludes any current flow [8].

B. NBTI Induced Ring Oscillator Degradation

To study the circuit impact of NBTI induced pMOS transistor degradation, an inverter ring oscillator circuit, shown in Figure 4, was statically stressed.

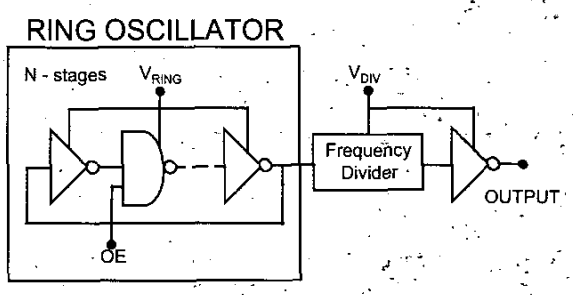

Figure 4. Simplified schematic of inverter ring oscillator circuit. The ring oscillator frequency of approximately 1. GHz is frequency divided down for observation with an oscilloscope. Oscillation is disabled by grounding the Oscillation Enable (OE) pin.

A ring oscillator was chosen as the prototypical circuit as it is widely used as a performance metric during process technology development. The channel length of the transistors in the ring oscillator is drawn at the minimum design rule. The ring oscillator was stressed statically by disabling oscillation and applying the stress voltage (V_{DD}=2.8V) at V_{RING}. The stress and measurements were performed at wafer-level with the wafer temperature held at 105°C for both stress and characterization. This static stress, based on the data in Section A, will only induce pMOS NBTI degradation and therefore any change in circuit performance can be directly attributed to this failure mechanism. The pre- and post-stress characterization phase consisted of measuring the frequency of the output waveform at different supply voltages. A plot of the percentage frequency shift (Post-stress–Pre-stress) versus the supply voltage, V_{DD}, for a thirty and sixty-minute stress is shown in Figure 5.

It is clearly observed from Figure 5 that the **frequency shift increases significantly as V_{DD} decreases**. For example, a sixty-minute stress results in 10% frequency reduction at V_{DD}=0.85V and only 1.5% frequency reduction at V_{DD}=1.5V. Furthermore, increasing the stress time from thirty minutes to sixty minutes results in larger degradation at a given V_{DD}.

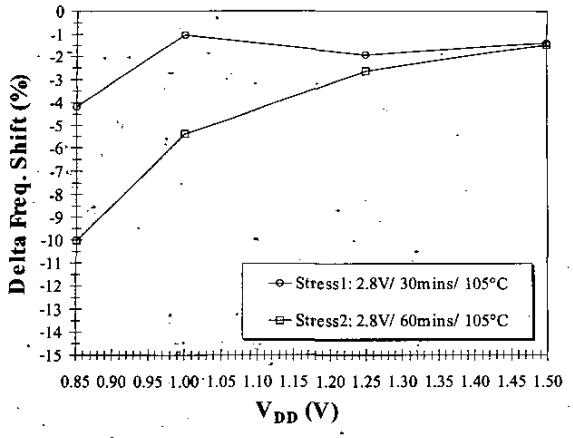

Figure 5. Percentage Frequency Reduction (Post-stress–Pre-Stress) of NBTI stressed ring oscillator versus V_{DD}, for a 30 and 60 minutes stress at 2.8V and 105°C. The magnitude of the frequency reduction increases as V_{DD} decreases.

C. pMOS NBTI Transistor Characterization

C1. V_{DD} Dependent I_{DSAT} Degradation

To understand the device level degradation, a pMOS transistor with similar dimensions to those used in the ring oscillator circuit (W/L=10/0.13μm) was stressed in the NBTI mode (V_G=-2.8V and T=105°C). The resultant transistor saturation drive current, I_{DSAT}, degradation is plotted versus V_{DD} for different stress intervals in Figure 6. We clearly see the dependence of transistor degradation on V_{DD}, with a lower characterization supply voltage exhibiting more degradation. In other words, the transistor parametric degradation is not constant with V_{DD} and increases as V_{DD} decreases.

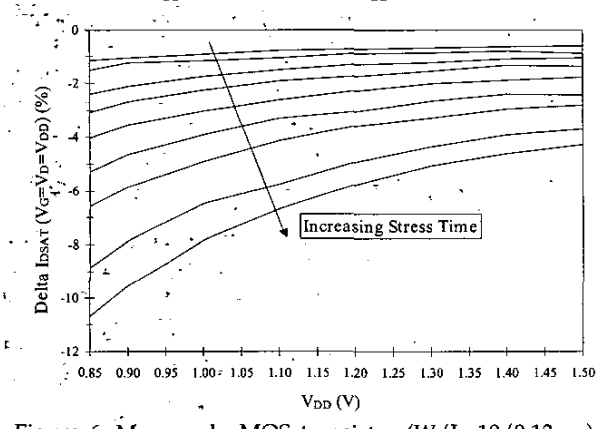

Figure 6. Measured pMOS transistor (W/L=10/0.13μm) drain saturation current, I_{DSAT}, degradation after NBTI stress. The stress condition (V_G = -2.8V and T=105°C) is identical to the static ring oscillator stress. The I_{DSAT} *degradation increases as the supply voltage decreases.* The total stress time was 4600 seconds.

The increased degradation at lower V_{DD} characterization voltages is due to a decreasing amount of gate *over-drive, which is equal to* (V_G – V_{TH}). *Since the gate voltage* is equal to V_{DD} during the I_{DSAT} measurement, the gate overdrive decreases as the V_{DD} decreases. Qualitatively, both the ring oscillator frequency degradation versus V_{DD} (Figure 5) and I_{DSAT} degradation versus V_{DD} (Figure 6) exhibit similar characteristics.

C2. pMOS NBTI Capacitance-Voltage Characteristics

To further understand the degradation mechanism, insight can be gained by considering the change in the gate capacitance-Voltage (C_G-V_G) characteristics after NBTI stress. A pMOS transistor in a gated diode configuration was stressed in an NBTI mode (V_G=-2.8V/T=105°C/10000sec), and a high frequency (10KHz) C_G-V_G sweep was taken at various stress intervals. The pre/post NBTI stress C-V curves, shown in Figure 7, exhibit the following characteristics: no flat-band voltage shift (V_G ~ 1V), increased capacitance in the region where the transistor goes into depletion, and then a lateral *shift in the curve as the silicon surface is inverted.*

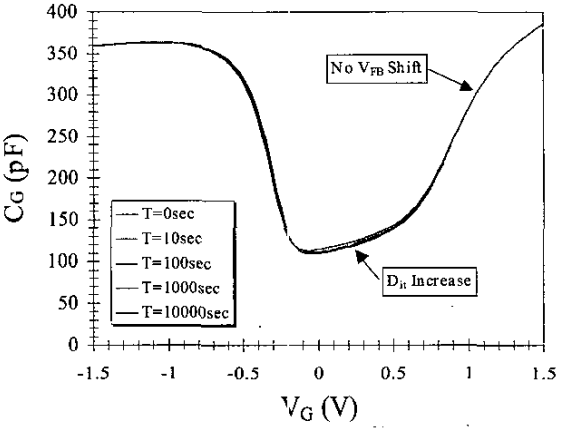

Figure 7. Time evolution of pMOS C_G-V_G characteristics during NBTI stress (V_G=-2.8V and T=105°C). The total stress time was 10000sec. While no flat-band voltage shift occurs, one can observe an increase in the interface trap density after the NBTI stress.

C3. pMOS NBTI Charge Pumping Characteristics

Charge-pumping characteristics were also measured simultaneously on the same structure used for the C-V characterization. Constant amplitude charge pumping measurements with f=100KHz, t_{rise}=t_{fall}=200nS, and a pulse amplitude of 1.5V were performed at various stress intervals. The peak charge pumping current, I_{cp}, was recorded and converted into an average interface state density, N_{it}, through the following relation [9].

$$N_{it} = I_{cp}/(q^*A^*f) \qquad \text{Eq. 1}$$

where q is the electronic charge, A is the gate oxide area, and f is the charge pumping frequency. The change in the average interface state density, Delta N_{it}, is plotted in Figure 8 and clearly shows a monotonic increase in the interface state

density as the NBTI stress progresses. Therefore, the charge pumping measurements confirm that the increase in capacitance, observed in Figure 7, is due to interface state generation.

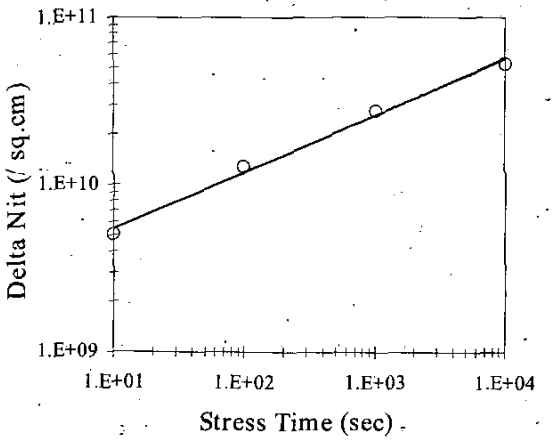

Figure 8. Time evolution of change in interface state density (measured through charge-pumping current, I_{CP}, characteristics) during pMOS NBTI stress (V_G=-2.8V and T=105°C). The I_{CP} characteristics were measured simultaneously on the same device as shown in Figure 7. The change in the average interface state density, Delta N_{it}, clearly shows a monotonic increase in the interface state density as the NBTI stress progresses.

DISCUSSION

A. Transistor Degradation Model

A mechanism that can explain the distortion in the C_G-V_G behavior that is occuring during the NBTI stress (see Figure 7) is the presence of donor interface traps created during the NBTI stress [10,11]. This distortion can be understood by considering SiO_2/N-Si energy band diagrams with donor interface traps as illustrated in Figure 9.

At flat-band (V_G ~ 1V), the Fermi level, E_F, is above the trap states and the states are neutral and do not contribute to the capacitance. As the transistor is biased into depletion and the trap states go above E_F, they become positively charged. The presence of the positively charged donor interface traps results in the lateral shift of the C-V curve when the transistor moves from depletion into inversion. Since the C_G-V_G characteristics show a rather subtle shift, a plot of the change in capacitance, Delta C_G, versus stress time, shown in Figure 10, more clearly shows the distortion in the C_G-V_G characteristics resulting from the NBTI stress. The increase in capacitance occurs in the region where the transistor is biased in depletion and the donor interface traps contribute additional capacitance. As the device goes into strong inversion the interface traps manifest themselves as a lateral shift of the C_G-V_G curve, or equivalently, a reduction in the capacitance at a given gate voltage.

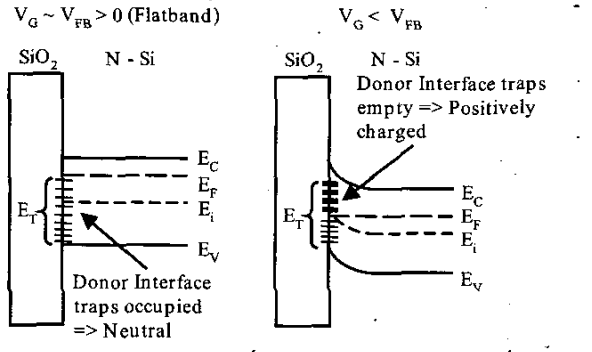

Figure 9. Energy band diagrams showing the impact of donor interface traps. At flatband, the trap states are occupied and therefore neutral. When the transistor is in depletion and/or inversion, some of the donor interface states are above the Fermi level and therefore are positively charged.

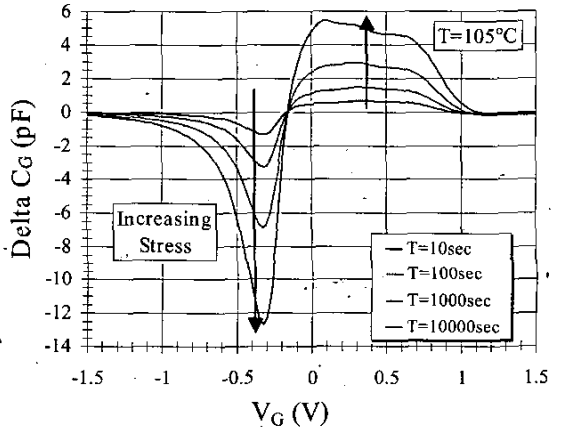

Figure 10. Experimental Delta C_G versus V_G characteristics during pMOS NBTI stress (V_G=-2.8V and T=105°C). The change in C_G is calculated with respect to the pre-stress C_G-V_G characteristics. The increase in capacitance occurs in the region where the transistor is biased in depletion and the donor interface traps contributed additional capacitance. As the device goes into strong inversion, the interface traps become positively charged and result in a lateral shift of the C_G-V_G curve, or equivalently, a reduction in the capacitance at a given gate voltage.

To confirm the donor interface trap model, 2-D TCAD simulations of a pMOS transistor were performed to simulate the impact of these types of traps on the C_G-V_G characteristics. A wide range of trap densities was simulated, including the trap levels extracted from the charge-pumping measurements. The modeling assumed that the distribution of donor interface states was equally spaced within the band-gap, located at the oxide/silicon interface, and placed uniformly across the length of the transistor channel region.

Figure 11 shows the simulated change in C_G-V_G characteristics for various donor interface trap densities. The simulations show very good agreement with the measured results, and provide validation of the device degradation model.

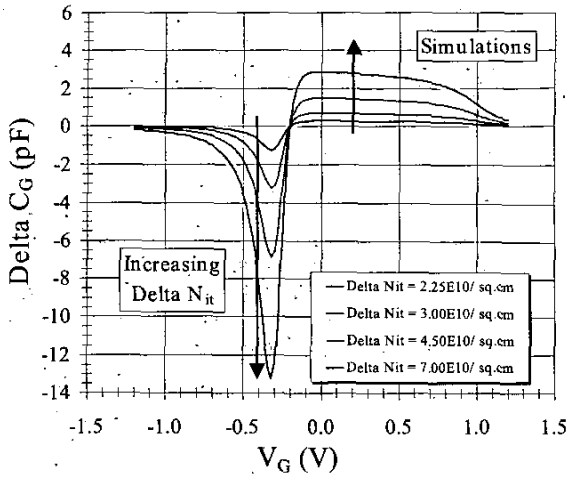

Figure 11. TCAD simulated Delta C_G versus V_G for various donor interface trap densities. A wide range of trap densities was simulated, including the trap levels extracted from the charge-pumping measurements. The simulations show very good agreement with the measured data of Figure 10. In fact, they capture the experimental Delta C_G-V_G characteristics, including the location of the negative peaks, the zero crossover point, and the plateau region in the positive gate voltage region.

The TCAD simulations capture the experimentally observed Delta C_G-V_G characteristics, including the location of the negative peaks, the zero crossover point, and the plateau region in the positive gate voltage region. To further compare the experimental and simulated Delta C_G-V_G behavior, the amplitude of the negative Delta C_G peaks is plotted versus the corresponding change in interface state density, as illustrated in Figure 12. The very good agreement between the simulations and experimental data further confirms that donor interface traps are responsible for the observed change in the C_G-V_G characteristics during NBTI stress.

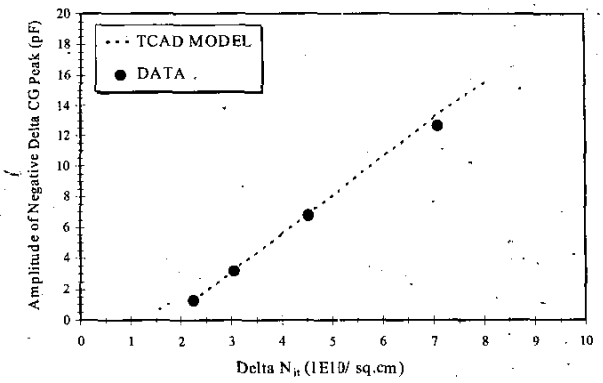

Figure 12. Comparison of measured and simulated amplitude of negative Delta C_G-V_G peaks versus Delta N_{it}. Very good agreement is seen between the TCAD simulations and the experimental data, further confirming the donor interface trap model.

B. NBTI Induced Circuit Degradation Model

To understand the first-order impact of the NBTI induced pMOS transistor degradation at a circuit level, an analytical calculation was performed to study the effect of a threshold voltage increase on inverter delay. A simple expression for the inverter propagation delay, τ, [12] is given below in Equation 2:

$$\tau = \frac{1}{2}\left(\frac{C*V_{DD}}{2*I_N} + \frac{C*V_{DD}}{2*I_P}\right) \qquad \text{Eq. 2}$$

where C is the load capacitance, I_N is the n-ch I_{DSAT}, and I_P is the p-ch I_{DSAT}. During the static ring-oscillator stress, only the p-ch transistor V_{TH} increases (see Figure 3). If we include the velocity-saturated expression for I_P, $I_{DSAT}=Wv_{sat}C_{ox}(V_{DD}-V_{TH})$ that is valid for deep sub-micron devices [13], then we can develop an expression, Equation 3, for the change in inverter propagation delay:

$$\Delta\tau = k*V_{DD}\left[\frac{1}{V_{DD}-V_{T0}-\Delta V_{TH}} - \frac{1}{V_{DD}-V_{T0}}\right] \qquad \text{Eq. 3}$$

where V_{T0} is the pre-stress V_{TH} and ΔV_{TH} is the degradation due to NBTI stress. The dependence of delay on decreasing V_{DD} with a ΔV_{TH} of 10mV is shown in Figure 13. This figure clearly supports the data in Figure 5, where the frequency decreases (or the delay increases) as the supply voltage is reduced.

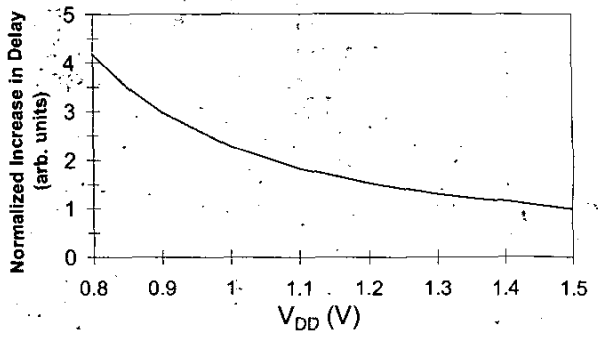

Figure 13. Analytical model for normalized inverter delay versus supply voltage for a NBTI degraded pMOS transistor with a ΔV_{TH}=10mV. The increasing delay, or equivalently, decreasing frequency corroborates the characteristics observed experimentally in Figure 5.

To further understand the circuit impact of NBTI induced transistor degradation, SPICE simulations of the ring oscillator circuit were performed with SPICE transistor models that shifted the SPICE model parameter VTHO by 10mV and 20mV. A plot of the simulated frequency shift versus V_{DD} for the two SPICE models, shown in Figure 14, also exhibits the strong dependence of frequency shift on supply voltage shown in the experimental results of Figure 5.

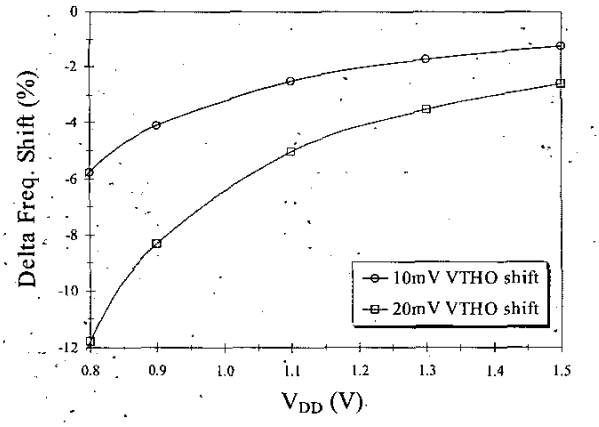

Figure 14. Simulated frequency degradation at T=105°C employing both constant VTHO shift of 10mVand 20mV. The SPICE simulations show that the frequency degradation increases as the supply voltage is lowered and corroborate the experimental data.

Impact of NBTI degradation on SRAM Cell Stability

With the rapid advances in system-on-a-chip integrated circuits and high-performance microprocessors, the amount of on-chip SRAM has increased considerably to the range of several megabits and typically constitutes the majority of the transistor count. This has elevated SRAM cell stability issues to the forefront. One of the most important cell stability metrics is the Static Noise Margin and refers to the ability of the cell to maintain stable data under parasitic noise and device mismatches in the SRAM cell [14]. During the process development and design rule selection phase, the SNM is a gating factor in determining a technology's performance versus cost tradeoff. Therefore, it is crucial to understand the impact of NBTI degradation on the SRAM cell transistors. The impact of NBTI degradation on SNM was modeled by incorporating NBTI degraded SPICE models in one of the pMOS load transistors of the SRAM 6-T memory cell. The percent degradation in SNM as a function of the supply voltage is shown in Fig. 15. One can see that the SNM degradation increases as the supply voltage decreases, a trend similar to that observed for both the ring oscillator and a discrete transistor

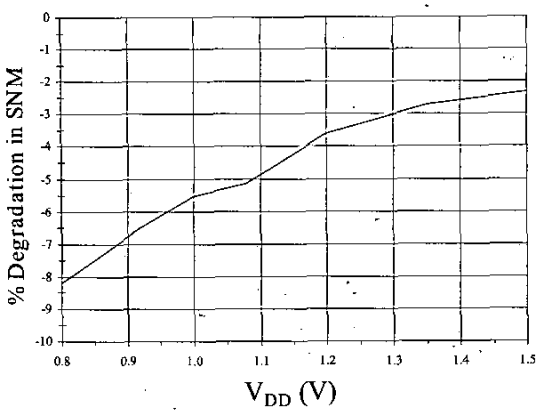

Figure 15. The static noise margin degradation increases as the supply voltage decreases; similar behavior to that observed with the ring oscillator frequency degradation and transistor parametric degradation.

SUMMARY

Through static NBTI stress of a ring oscillator circuit, we have unambiguously determined the circuit reliability impact of NBTI. The relative frequency degradation of the NBTI stressed ring oscillator increases as the operating voltage decreases. This behavior can be explained by reduced transistor gate overdrive and reduced voltage headroom at the circuit level. We present evidence that donor interface state generation during NBTI stress is a significant component of the transistor degradation. Further, NBTI stress can result in SRAM static noise margin degradation. These results indicate that the circuit impact of NBTI will become increasingly significant as we continue technology scaling.

ACKNOWLEDGMENTS

The authors would like to thank P. Nicollian, R. Baumann, and G. Boselli for useful discussions and J. Carulli and J. Ondrusek for their support of this work.

REFERENCES

[1] N. Kimizuka, K. Yamaguchi, K. Imai, T. Iizuka, C.T. Liu, R.C. Keller, and T. Horiuchi, "NBTI Enhancement by Nitrogen Incorporation into Ultrathin Gate Oxide for 0.10-μm gate CMOS generation," *Symposium on VLSI Technology Digest*, pp. 92-93, 2000.

[2] A. T. Krishnan, V. K. Reddy, and S. Krishnan, "Impact of Charging Damage on Negative Bias Temperature Instability," *IEDM Technical Digest*, pp. 865-868, 2001.

[3] G. La Rosa, S. Rauch, F. Guarin, "New Phenomena in Device Reliability Physics of Advanced CMOS Submicron Technologies," *International Reliability Physics Symposium Tutorial*, 2001.

[4] R. Thewes, R. Brederlow, C. Schlunder, P. Wieczorek, B. Ankele, A. Hesener, J. Holz, S. Kessel, and W. Weber, "Evaluation of MOSFET Reliability in Analog Applications," *European Solid-State Device Research Conference*, 2001.

[5] P. Chaparala, J. Shibley, and P. Lim, "Threshold Voltage Drift in PMOSFETS due to NBTI and HCI," *Integrated Reliability Workshop Digest*, pp. 95-97, 2000.

[6] F. Pagaduan, J. K. Lee, V. Vedagarbha, K. Lui, M. Hart, D. Gitlin, T. Takaso, S. Kamiyama, and K. Nakayama, "The Effects of Plasma-Induced Damage on Transistor Degradation and the Relationship to Field Programmable Gate Array Performance," *Proceedings of the International Reliability Physics Symposium*, pp. 315-318, 2001.

[7] A. Chatterjee, D. Mosher, S. Sridhar, Y. Kim, M. Nandakumar, S. W. Aur, Z. Chen, P. Madhani, S. Tang, R. Aggarwal, S. Ashburn, and H. Shichijo, "Analog Integration in a 0.35μm Cu Metal Pitch, 0.1um Gate Length, Low-Power Digital CMOS Technology," *IEDM Technical Digest*, pp.211-214, 2001.

[8] K. N. Quader, P. K. Ko, and C. Hu, "Projecting CMOS Circuit Hot-Carrier Reliability from DC Device Lifetime," *IEDM Technical Digest*, pp.511-514, 1993.

[9] J. S. Brugler and P. Jespers, "Charge Pumping in MOS Devices," *IEEE Transactions on Electron Devices*, ED-16, No. 3, pp.297-302, 1969.

[10] G. La Rosa, F. Guarin, S. Rauch, A. Acovic, J. Lukaitis, and E. Crabbe, "NBTI – Channel Hot Carrier Effects in PMOSFETs in Advanced CMOS Technologies," *Proceedings of the International Reliability Physics Symposium*, pp. 282-286, 1997.

[11] C. Schlunder, R. Brederlow, P. Wieczorek, C. Dahl, J. Holz, M. Rohner, S. Kessel, V. Herold, K. Goser, W. Weber, and R. Thewes, "Trapping Mechanisms in Negative Bias Temperature Stressed p-MOSFETs," *Microelectronics Reliability*, pp. 821-826, 1999.

[12] Y. Taur and T. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998.

[13] D. Sylvester and K. Keutzer, "Impact of Small Process Geometries on Microarchitectures in Systems on a Chip," *Proceedings of the IEEE*, Vol. 89, No. 4, pp: 467-489, 2001.

[14] A. Bhavnagarwala, X. Tang, and J.D. Meindl, "The Impact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability," *IEEE Journal of Solid State Circuits*, Vol. 36, no. 4, pp. 658-665, 2001.