The Annealing Behavior of Oxide Trapped Charges and Interface Traps in Fluorinated NMOSFETs

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Abstract **The gate bias annealing of threshold voltage, oxide trapped charges and interface traps in fluorinated n-channel MOSFETs has been investigated. The annealing rate of oxide trapped charge is correlated with the value of gate bias. The annealing of interface traps has a turnaround effect. Switching gate bias during anneal results in the creation and banishment of oxide trapped charges.The annealing saturation appear after long term anneal. The radiation damage can be restrained in fluorinated MOS oxides. Gate bias has a more significant influence on the build-up and annealing of oxide trapped charges in fluorinated NMOSFETs.**

I. INTRODUCTION

It is well known that annealing of radiation-induced oxide trapped charges and interface traps in MOS oxides are strongly dependent on the gate bias[1-2] . Recently,it has been reported by introducing minute amounts of fluorine into MOS gate oxide to suppress hot carrier damage and improve electrical characteristics[3-6]. However, little is known about the gate bias dependencies upon the annealing of oxide trapped charges and interface traps in fluorinated oxides thus far.

In this paper, we have investigated the effect of gate bias on post irradiation behavior of oxide trapped charges and interface traps in fluorinated NMOSFETs. The experimental results have shown that gate biases play an important role in the annealing of radiation-induced oxide trapped charges and interface traps after irradiation.

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II. EXPERIMENTAL

The control and fluorinated n-channel MOSFET used in this study were fabricated on p-type well of (100) n-type silicon substrate of 3-4.5 Ω.cm. The gate oxides were grown in H_2+O_2 at high temperature to thickness of 50nm,followed by annealing N_2 at 900℃ for 30 minutes. Channel length was 6 μ m with width 90 μ m.

For test sample 30kev F^+ ions (dose 1×10^{16} F/cm^2) were implanted into the upper layer of the polysilicon gate after 500nm polysilicon films was deposited on the oxide. Then 30 minutes annealing in N_2 with proper high temperature was followed.

Total dose test was performed at Co-60 γ source, dose rate 122 Gy(si)/min. The bias during irradiation is Vgs=5V and Vds=0V. After irradiation, Samples were left under bias in environmental chamber at 100 ℃ constant temperature between measurements.

After each annealing, the subthreshold characteristics (Ids-Vgs) measurements were completed within 20 minutes. From subthreshold

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characteristics measured by HP4140 and the "stretch out" principle[7] the threshold voltage (Vt) and the density of oxide trapped charges (△ Not) were obtained. The density of interface traps (Dit) was calculated by subthreshold method[8].

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. Dependence upon the value of gate bias

Fig.1 shows the threshold voltage shift(△ Vt)、 △ Not and △ Dit as a function of time during the irradiation(bias:Vgs=5V, Vds=0V) and the 100 ℃ anneal (bias:Vgs=0 ~ 15V, Vds=0V) in fluorinated NMOSFETs, respectively.Total dose are 5×10^3 Gy(si).

From figures we can clearly see bellow:

1)During irradiation △ Dit and △ Not are increased with time to lead to the decrease of Vt.

2)During annealing, △ Vt for all gate biases is increased with time, the faster increasing rate is corespondent to the larger gate bias. When annealing time is more than about 30 hours Vt may pass through preirradiation threshold voltage (△ Vt>0), behaving "Rebound" effect. △ Not decreased with time for all samples, the larger Vgs,the more immunity of radiation-induced oxide trapped charges. At Vgs=0V less oxide trapped charges are annealed. The annealing of interface traps has a "turnaround" effects for all samples.

3)The "saturation" effects of increase or decrease for all samples appear after longer term annealing.

From above discussed, we can conclude that radiation-induced oxide trapped charges and threshold voltage shifts may be gradually annealed. The value of gate bias play a very great role in the annealing rate of oxide trapped charges. The "turnaround" means that interface traps will be created after long term anneal. The "Rebound" effect of threshold voltage annealing should contribute to the interface traps generation.

B. Dependence upon the polarity of gate bias

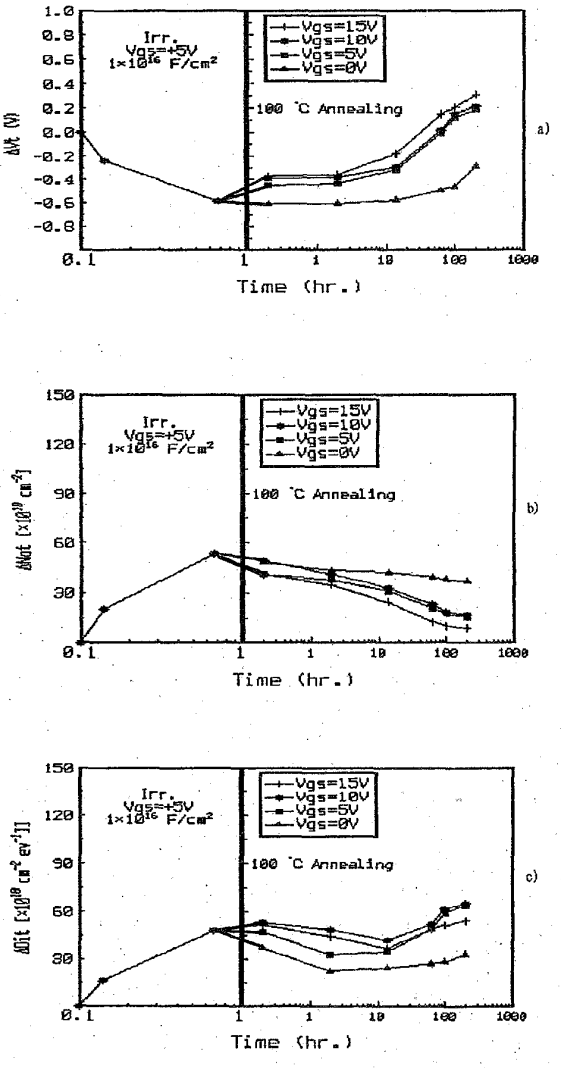

Fig.1 △Vt (a), △Not (b) and △Dit (c) versus time in fluorinated NMOSFET.

The effects of switch gate bias on △Vt and △ Not during annealing are shown in Fig.2 for control and fluorinated NMOSFETs. Radiation gate bias is Vgs=5V.Two gate bias line between

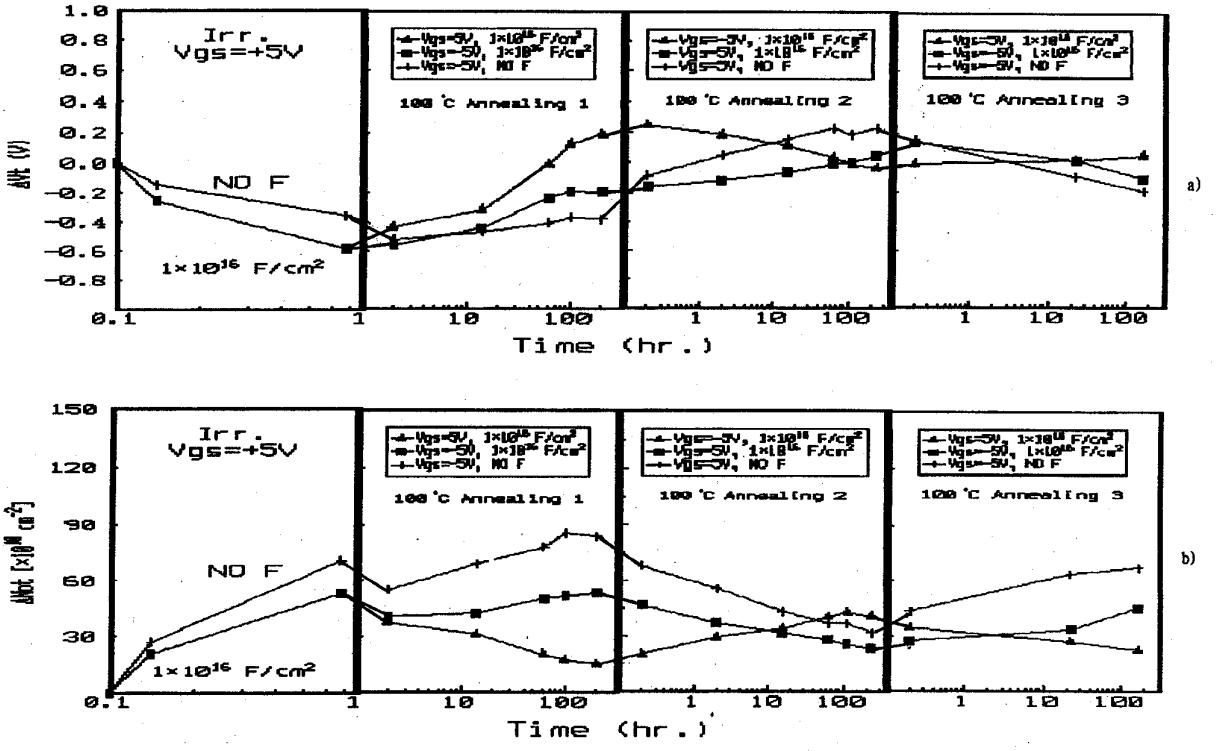

Fig.2 △Vt (a) and △Not (b) versus time in no F and fluorinated NMOSFET

annealing 1 to 3 are :1) Vgs=+5V → Vgs=-5V → Vgs=+5V; 2) Vgs=-5V → Vgs=+5V → Vgs=-5V, for one sample. Annealing temperature is 100 ℃. Radiation total doses are 5×10^3 Gy(si).

Experimental data have shown below:

1) △Not for fluorinated samples is less than that for control under total irradiation.

2) The time dependence of △ Not during annealing indicate a "switch" effect: when gate bias is reversed from negative (positive) to positive (negative) △ Not is changed from increase (decrease) to decrease (increase) with anneal time. The change rate of △ Not for fluorinated samples is smaller than that for control. It is opposite dependence for △ Vt except Vgs=-5V in Fig.2(a) because △ Vt is the combined shifts induced by △Not and interface traps generation.

3) when time increased enough the change in △ Vt and △Not will be saturate.

These experimental results have shown that the gate bias during annealing has an obvious "switch" effect on the build-up and annealing of oxide trapped charges. Properly incorporating minutes of fluorine in MOS gate oxide can suppress ionizing radiation damage. The saturation of annealing and creation of oxide trapped charges will appear after long term annealing.

After irradiation with a positive gate bias, electrons either from the silicon conduction band or from the silicon valence band tunnel into the oxide and neutralize the oxide trapped charge[2]. The number of electrons in the silicon conduction band will increase with gate bias. The tunneling rate increases with the number of surface electrons. In the case of tunneling from the silicon

valence band, decreasing bias causes an incomplete annealing of the oxide trapped charge. Regardless of the energy location of oxide traps the data is consistent with above gate bias annealing mechanism.

When we reverse the polarity of the gate bias from positive to negative the oxide trapped charges will be from disappearance to reappearance. This is because the weakly bound electrons which tunneled into oxide during positive gate bias annealing on the oxide trap can escape from the trap and tunnel back into the silicon. Recent "Border trap" model can also explain this "switch" effect and is similar to above discussions[9].

The annealing saturation of oxide trapped charges is the results induced by the equilibrium of escape and tunnel of electrons.

The "turnaround" effect of interface traps after long term anneal should contribute to the combined effects of the creation and banishment of interface traps at the same time. The creation of Dit after long term annealing is dominate to result in turnaround.

The replacement of Si-H and Si-OH weak bonds as well as Si-O strain bonds by Si-F bonds and the relaxation of Si/SiO_2 interface stress in fluorinated oxides will lead to the less generation of interface traps and oxide trapped charges during irradiation[4-6]. Weaker dependencies of oxide trapped charges annealing on switch gate bias should be responsible for higher Si-F bonds energy in fluorinated oxides.

IV. SUMMARY

The annealing rate of oxide trapped charges depends strongly on gate bias because of the gate-bias related electron tunneling from the silicon. The interface traps have a "turnaround" effect during different positive gate bias annealing because of the creation and banishment of Dit at the same time. The annealing of oxide trapped charges has a "switch" effect induced by the gate bias related motion of bound electron. The saturation of oxide trapped charges after long term anneal should be responsible for the equilibrium of annealing and creation of oxide traps. During irradiation the less oxide trapped charges are created in fluorinated oxides. Fluorinated oxides have a weaker dependency on switch gate bias.

V. REFERENCES

[1] R. E. Stahlbush, B. J. Mrstik and R. K. Lawrence, "Post-Irradiation Behavior of the interface state density and the trapped positive charge," *IEEE Trans., Nucl. Sci.*, vol.37,no.6, pp.1641,1990.

[2] J. R. Schwank, P. S. Winokur, P. J. Mcwhorter, F. W. Sexton, P. V. Dressendorfer," Physical Mechanism Contributing to Device 'Rebound'," *IEEE Trans., Nucl. Sci.*, vol.31,no.6,pp.1434,1984.

[3] N. Kasai, P. J. Wright, and K. C. Saraswat, "Hot-Carrier-Degradation Characteristics for Fluorine Incorporated nMOSFETs," *IEEE Trans., Electron Devices*, vol.37, pp.1426,1990.

[4] Y. Nishioka, Y. Ohji, K. Mukai, T. Sugano, Y. Wang and T. P. Ma, "Dielectric Characteristics of Fluorinated Ultra-dry SiO2," *Appl.Phys. Lett.*,vol. 54, pp.1127,1989.

[5] Zhang Guoqiang, Yan Rongliang, Yu xuefen, Ren Diyuan, Zhao Yuanfu, Hu Yuhong, and Wang Yinming,"Effects of Gate Oxidation on Radiation Effects of Fluorinated MOSFET," *Nucl. Tech. (China)*, vol.17,no.4,pp. 221,1994.

[6] Zhang Guoqiang, Yu xuefen, Gao Wenyu, Ren Diyuan, Yan Rongliang, Zhao Yuanfu, Hu Yuhong, and Wang Yinming, "Ionizing Radiation Responses of Fluorinated Dielectrics for Two Implantation Energy," *Chinese Journal of Semiconductors (China)*, vol. 15, no.1, pp. 64, 1994.

[7] P. S. Winokur, J. R. Schwank, P. J. Mcwhorter, P. V. Dressendorfer, and D. C. Turpin, "Correlation the Radiation Response of MOS Capacitors and Transistors," *IEEE Trans. , Nucl. Sci.* , vol. 31, no.6, pp. 1453, 1984.

[8] M. Gaitan, T. J. Russell, "Measurement of Radiation-Induced Interface Traps Using MOSFETs," *IEEE Trans. , Nucl. Sci.* , vol. 31, no. 6, pp. 1256, 1984.

[9] D. M. Fleetwood, M. R. Shaneyfelt, L. C. Riewe, P. S. Winokur, and R. A. Reber, Jr., "The Role of Border Traps in MOS High-Temperature Postirradiation Annealing Response," *IEEE Trans., Nucl. Sci.* , vol. 40, no. 6, pp. 1323, 1984.