Aging Analysis of Circuit Timing Considering NBTI and HCI

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***Abstract*—We present an aging analysis flow able to calculate the degraded circuit timing. To the best of our knowledge it is the first approach on gate level so far capable of analyzing the impact of the two dominant drift-related aging effects – NBTI and HCI – on complex digital circuits. The aging-aware gate model used to compute the aged circuit timing provides not just the cell delay degradation, but also the degradation of the output slope. To get more accurate results, the individual workload of a gate can be considered.**

I. Introduction

With the continued downscaling of feature sizes in integrated digital circuits, the variation of device parameters has become a major concern. During manufacturing, variations of process parameters are inevitable. Hence, performance parameters like power consumption or operating frequency differ from the values they were designed for. After manufacturing the circuit performance degrades over time due to several aging effects that cause a drift of device parameters. These effects must be considered during a timing analysis of an aged circuit.

Negative Bias Temperature Instability (NBTI) [1] and Hot Carrier Injection (HCI) [6] are considered to be the dominant drift-related aging effects in current technologies. NBTI degrades PMOS transistor characteristics and its impact can best be modeled by an increase in the magnitude of the threshold voltages. HCI degrades the drain current of both, PMOS and NMOS, transistor types.

The traditional approach in a digital design flow to handle reliability concerns, brought up by uncertainties of device parameters, is to introduce safety margins. Those safety margins tend to increase in newer technologies because the relative parameter variations caused by process variations are increasing. Furthermore, an increased impact of aging effects on circuit performance can be observed.

This increased impact of aging effects can be explained by the following two reasons: First, the degradation is dependent on the strength of the electric fields occurring in a device. For several technology generations, the feature sizes have been scaled more aggressively than the supply voltage, resulting in an increased drift due to higher electric fields. Second, the sensitivity of a logic gate's delay according to a drift of threshold voltage increases with lower supply voltage. Hence, newer technologies are more sensitive to a threshold voltage drift.

Timing sign-off for complex digital circuits can only be performed on gate level due to complexity reasons. But there is a lack of methods that can analyze the impact of process variation and aging effects on circuit performance. Therefore, safety margins must be set conservatively. A major drawback of conservative safety margins is that they can minimize or even eliminate the advantages of moving to a smaller technology node. Operating frequencies are not as high as they could be, chip area is wasted and power consumption is not reduced as much as possible. Hence, conservative safety margins make it hard to design competitive products.

More sophisticated analyzing methods are needed to tighten the safety margins again. Statistical static timing analyzers (SSTA) [2] are developed to consider the impact of process variations during timing sign-off. A similar approach to handle the impact of aging effects is crucial. In contrast to process variations, aging effects lead to a directed drift of device parameters dependent on operating conditions over lifetime. Hence, the impact of aging effects can be analyzed deterministically.

The approach presented here is a static timing analyzer considering aging (ASTA). It consists of an aging-aware gate model providing the degraded gate performances for given operating conditions over lifetime and an analysis flow to determine the degraded timing of an aged circuit. The aging-aware gate model not just provides an aged cell delay but also an aged output slope. ASTA is capable of handling combinatorial circuits on gate level. The impact of the two most dominant drift-related aging effects, NBTI and HCI, is analyzed. The proposed approach is able to either do a worst-case analysis or to consider the workload of individual gates for more realistic results. Our results indicate that by not considering the individual workload of the gates the critical path delay degradation was overestimated by at least 2.6 percentage points.

The remainder of the paper is structured as follows: Related work is presented in Section II, the proposed gate model and the ASTA flow are introduced in Sections III and IV, respectively, results are shown in Section V, and conclusions are drawn in Section VI.

II. Related work

Prior work on determining the degraded performance of an aged circuit is briefly reviewed in this section.

A. Transistor-level aging simulation

Aging simulators on transistor level have already been published [4], commercial tools are also available. For the analysis of aged circuit behavior, the following three steps are necessary:

1) The circuit is simulated and the relevant current and voltage waveforms are collected to determine the workload for each single transistor.

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2) An aged netlist is generated with degraded model cards for every single transistor dependent on the individual workload and the operating conditions over lifetime. Therefore, degraded transistor models or degradation equations are necessary.
3) The aged netlist is simulated again to obtain the aged circuit behavior.

These simulators are able to handle circuits with up to several thousand transistors. They are not capable of verifying the timing constraints of a complex digital circuit. The degradation of a transistor is dependent on its workload. Input vectors are needed to determine the workload of an individual transistor, but are usually not available. Nevertheless, the following approach demonstrates that those tools can be of use for the generation of aged gate models.

B. LUT-based aged gate model

A gate model provides gate performances Q (e.g., gate delay τ) as a function of input signals, output load C_L and operating conditions (temperature T, supply voltage V_{DD} and process P). In a look-up-table (LUT) based gate model the input signals are approximated by pulses with a constant slope. It uses 2-dimensional LUTs to store the dependence of a nominal gate performance Q_0 on input slope S_{IN} and C_L. In order to determine S_{IN}, the output slope S_{OUT} of a previous gate is needed. Hence, S_{OUT} is another gate performance of interest. The remaining dependencies are combined as a corner case (PVT):

$$Q_0 = f(S_{IN}, C_L)\big|_{PVT} \tag{1}$$

A LUT-based aged gate model provides aged gate performances Q_{Age} instead of Q_0. To obtain Q_{Age}, aged netlists are characterized. These netlists are generated for predefined operating conditions over lifetime so called stress factors $\mathbf{SF}$:

$$Q_{Age} = f(S_{IN}, C_L)\big|_{PVT,\mathbf{SF}} \tag{2}$$

A major advantage of such a gate model is that the existing analysis flow can be reused. However, re-characterized standard cell libraries are needed for every combination of stress factors of interest. If the individual workload of a gate should be considered, each gate has to be characterized for varying workload conditions.

The ratio based gate model [3] uses 3-dimensional LUTs to provide the ratio α between τ_{Age} and τ_0 for a degradation due to HCI:

$$\alpha(S_{IN}, C_L, N_{sw}) = \frac{\tau_{Age}}{\tau_0} \tag{3}$$

Besides the dependence on S_{IN} and C_L, the dependence on the number of effective switchings N_{sw} is needed, since a transistor is only degrading due to HCI during transition.

C. Estimation of aged gate delay

Another approach to determine the impact of aging effects (especially NBTI) on circuit performance is to estimate the aged gate delay τ_{Age} due to a threshold voltage drift ΔV_{th} [11]:

$$\tau_{Age} = \tau_0 + \frac{\partial \tau}{\partial V_{th}} \Delta V_{th} \text{ with } \frac{\partial \tau}{\partial V_{th}} = \frac{\alpha}{V_{gs} - V_{th}} \tau_0 \tag{4}$$

The equation is derived under the assumption that the gate delay is primarily caused by charging the output load. Sakurai's α-power-law MOSFET model [13] is used to express the charging current. ΔV_{th} is provided by a degradation equation. A lot of effort is made to equip those equations with new capabilities (e.g., [7], [5]).

This estimation method is rather inaccurate as only the drift of ΔV_{th} can be considered. Drifts will differ amongst transistors due to unequal workloads. However, only one value for ΔV_{th} per gate can be used in (4). Furthermore, the estimation only provides τ_{Age} but no equation for the aged output slope $S_{OUT,Age}$ can be formulated.

III. Proposed gate model

The proposed aging-aware gate model consists of the following three parts:

1) A canonical gate model
2) Technology specific degradation equations
3) Structural information about transistor sizes and internal gate structure

A canonical gate model provides the aged gate performance for parameter drifts of individual transistors. Those drifts are obtained by technology specific degradation equations. The transistor sizes are necessary for the calculation of the transistor drifts and information about the internal gate structure is needed to estimate the time the transistor is in a stress condition.

An example should clarify the importance of the gate structure. A transistor degrades due to NBTI if the source and drain terminals are negatively biased with respect to the gate terminal. Therefore, the degradation of transistor P_C in Fig. 1 is only dependent on the static signal probability of C. P_B is in the transistor stack underneath P_C. Hence, its degradation is dependent on the static signal probabilities of B and C [8].

A. Canonical gate model

Sensitivities express the impact a parameter drift of a single transistor has on gate performance Q_{Age}. The fundamental equation to calculate Q_{Age} is:

$$Q_{Age} = Q_0 + \sum_{n=1}^{N} \sum_{p=1}^{P} \chi^Q_{p,n} \Delta p_n \tag{5}$$

The impact of aging effects is added to the nominal gate performance Q_0. N is the number of transistors in the logic gate and P is the number of transistor parameters that drift due to aging effects. The impact the parameter degradation of a particular transistor has on Q_{Age} is the product of linear sensitivity coefficient $\chi^Q_{p,n}$ times drift of a transistor parameter Δp_n.

The sensitivity coefficients $\chi^Q_{p,n}$ are defined as follows:

$$\chi^Q_{p,n} = \frac{\partial Q}{\partial \Delta p_n}\Big|_{\Delta p_n = 0, PVT} \tag{6}$$

It is the partial derivative of Q with respect to a drift Δp_n of a transistor parameter p of transistor n for a given corner case PVT. The sensitivity is calculated for nominal transistor parameter values ($\Delta p_n = 0$).

B. Degradation equations

The parameter drift Δp_n is a function of operating conditions over lifetime referred to as stress factors $\mathbf{SF}$, the time t_{stress} and transistor sizes W and L:

$$\Delta p_n = f(\mathbf{SF}, t_{\text{stress}}, W, L) \tag{7}$$

Two examples for **SF** are the effective temperature over lifetime T_{eff} and the effective supply voltage over lifetime V_{eff}.

Transistors are only aging, if the stress conditions for a particular aging effect are fulfilled. This time t_{stress} is dependent on the gate input signals over lifetime, i.e., the gate's workload. Input signals are characterized by two statistical parameters. Static signal probability SP is defined as the average fraction of clock cycles in which the steady state value of a signal is at logic "1" and transition density TD is defined as the average number of "0"-to-"1" and "1"-to-"0" transitions of a signal per clock cycle [10]. To consider t_{stress}, the duty factor DF is defined as the ratio of t_{stress} to overall lifetime t_{life}:

$$DF = \frac{t_{\text{stress}}}{t_{\text{life}}} \tag{8}$$

In (7), time t_{stress} can be replaced by $DF \cdot t_{\text{life}}$. Time t_{stress} is dependent on the workload. Hence, also DF is dependent on the values of SP and TD at the gate inputs. The method to obtain DF during the aging analysis is described in Section III-C.

The empirical degradation equations yield a threshold voltage drift ΔV_{th} for NBTI (9) and a degradation of the saturation drain current ΔI_{on} in terms of percentage for HCI (10):

$$\Delta V_{th,n} = f(\mathbf{SF}, DF_{NBTI} \cdot t_{\text{life}}, W, L) \tag{9}$$

$$\Delta I_{on,n} = f(\mathbf{SF}, DF_{HCI} \cdot t_{\text{life}}, W, L) \tag{10}$$

C. Calculation of duty factors

To calculate the drifts of a transistor, the duty factors DF_{NBTI} and DF_{HCI} are needed. Duty factors are defined according to (8). The time t_{stress} is dependent on the signals at the transistor terminals over the transistor's lifetime. For ASTA, the challenge is to obtain the duty factors from the values of SP and TD at the logic gate inputs and the internal gate structure.

The following two stress conditions have to be fulfilled so that a PMOS transistor M (e.g., P_A in Fig. 1) is degraded due to NBTI:

- A: M in inversion
- B: gate terminal negatively biased with respect to source and drain

The probability that M is in inversion is $P(\text{"on"})$. Hence, the probability for condition A is:

$$P(A) = P(\text{"on"}) \tag{11}$$

For PMOS transistors $P(\text{"on"})$ equals $1 - SP$ and for NMOS transistors $P(\text{"on"})$ equals SP.

If condition A is fulfilled, it is sufficient that M's source is at the positive supply voltage V_{DD} for condition B to be fulfilled. Therefore all transistors in the transistor stack that are above M must be in inversion:

$$P(B|A) = P(\text{"}M\text{'s source at } V_{DD}\text{"}) \tag{12}$$
$$= \begin{cases} \prod\limits_{\text{transistors above } M} P(\text{"on"}) \text{ if sig. independent,} \\ \min\limits_{\text{transistors above } M} (P(\text{"on"})) \text{ else.} \end{cases}$$

For independent gate input signals, the probabilities have to be multiplied. If independent signals cannot be assumed, a worst-case assumption is that all transistors in the stack tend to conduct at the same time. Hence, one has to determine the minimum of the probabilities $P(\text{"on"})$ for all transistors in the stack above M for a conservative estimation.

The probability that both conditions A and B are fulfilled also depends on the correlation of the gate input signals:

$$P(A \wedge B) = \begin{cases} P(A) \cdot P(B|A) & \text{if sig. independent,} \\ \min\left(P(A), P(B|A)\right) & \text{else.} \end{cases}$$

Finally, DF_{NBTI} can be calculated as follows:

$$DF_{NBTI} = \frac{t_{\text{stress}}}{t_{\text{life}}} = \frac{P(A \wedge B) \cdot t_{\text{life}}}{t_{\text{life}}} = P(A \wedge B) \tag{13}$$

For a transistor M to be degraded due to HCI a considerable current must flow in the channel, because the transistor is demaged by accelerated carriers. Two stress conditions have to be fulfilled:

- C: transition from "off"- to "on"-state at transistor in stack
- D: all transistors in the transistor stack must be "on"

The sum of the transition densities TD of all transistors in the transistor stack is a measurement of the number of transitions (condition C). For condition D, all transistors in the transistor stack must be "on" to provide a conducting path from a supply line to the output load of the gate:

$$P(D) = P(\text{"all transistors on"}) \tag{14}$$
$$= \begin{cases} \prod\limits_{\text{all transistors}} P(\text{"on"}) \text{ if sig. independent,} \\ \min\limits_{\text{all transistors}} (P(\text{"on"})) \text{ else.} \end{cases}$$

For independent gate input signals the probabilities have to be multiplied. Otherwise, the minimum of the probabilities $P(\text{"on"})$ of all transistors in the stack is needed.

To obtain DF_{HCI}, time t_{stress} has to be expressed. The number of transitions from "off"- to "on"-state during the whole lifetime t_{life} are $TD/2 \cdot f \cdot t_{\text{life}}$, with f being the operating frequency. This number multiplied by $P(D)$ is the number of effective transitions with a considerable current flow. The number of effective transitions times the transition time S_{IN} is t_{stress}. Hence, DF_{HCI} is:

$$DF_{HCI} = \frac{t_{\text{stress}}}{t_{\text{life}}} = \frac{TD/2 \cdot f \cdot P(D) \cdot S_{IN} \cdot t_{\text{life}}}{t_{\text{life}}} \tag{15}$$

For calculating DF_{NBTI} and DF_{HCI}, the gate input signals are important. For independent signals, the probabilities $P(A \wedge B)$ and $P(D)$ will be smaller, resulting in smaller duty factors and smaller drifts. Hence, for a conservative timing analysis independent signals should not be assumed, unless specific information is available.

For illustration, the probability $P(A \wedge B)$ for transistor P_A in Fig. 1 is calculated. For independent signals $P(A \wedge B) = (1 - 0.5) \cdot (1 - 0.4) \cdot (1 - 0.3)$ is equal to 0.21. Otherwise, $P(A \wedge B)$ is the minimum of the three SP values of the transistors in the stack. Hence $P(A \wedge B) = \min(0.5, 0.6, 0.7) = 0.5$.

D. Gate model generation

The generation of the gate model is fully automated in our implementation. The sensitivities with respect to transistor parameters are efficiently computed through adjoint network analysis [12] while determining the nominal gate performance

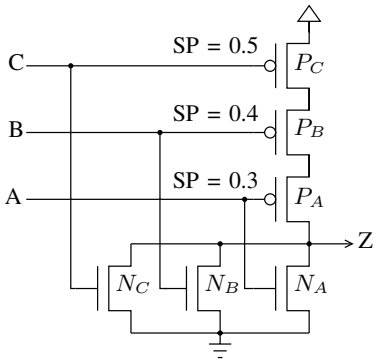

Fig. 1. NOR3 gate with static signal probability for inputs.

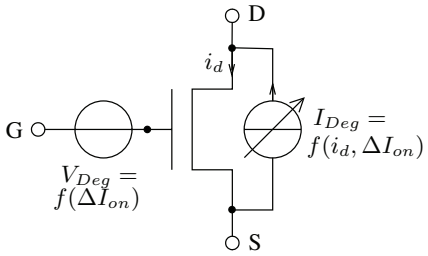

Fig. 2. HCI equivalent circuit for a degraded transistor. V_{Deg} and I_{Deg} are dependent on the degradation of the saturation current ΔI_{on}.

Q_0. Thereby, the sensitivities with respect to transistor parameters can be computed. For NBTI the sensitivity of Q with respect to ΔV_{th} must be obtained:

$$\chi^Q_{\Delta V_{th},n} = \frac{\partial Q}{\partial \Delta V_{th,n}} \tag{16}$$

The sensitivity of Q with respect to ΔI_{on} cannot be calculated directly by adjoint network analysis because ΔI_{on} is not a parameter of the transistor model card. Fortunately, an equivalent circuit for a degraded transistor (see Fig. 2) is provided to simulate the impact of HCI on circuit performance on transistor level. This equivalent circuit represents ΔI_{on} by a threshold voltage drift and a drift of the transistor mobility $\Delta\mu_0$. ΔV_{th} is realized by the voltage source V_{Deg} and $\Delta\mu_0$ is achieved by the current controlled current source I_{Deg}, which provides a current opposing the drain current. The sensitivity $\chi^Q_{\Delta I_{on},n}$ can be calculated by applying the chain rule:

$$\chi^Q_{\Delta I_{on},n} = \frac{\partial Q}{\partial V_{Deg,n}} \frac{\partial V_{Deg,n}}{\partial \Delta I_{on,n}} + \frac{\partial Q}{\partial I_{Deg,n}} \frac{\partial I_{Deg,n}}{\partial \Delta I_{on,n}} \tag{17}$$

For the determination of $\partial Q/\partial V_{Deg}$ and $\partial Q/\partial I_{Deg}$ all transistors of the logic gate are replaced by their equivalent circuit. The remaining partial derivatives can be derived from the equations for V_{Deg} and I_{Deg}. Fig. 3 shows how well the delay degradation of an inverter caused by a ΔI_{on} drift is approximated with the aid of $\chi^Q_{\Delta I_{on},n}$.

Like in a standard LUT-based gate model without aging, the dependencies of Q_0 and $\chi^Q_{p,n}$ on S_{IN} and C_L are stored in 2-dimensional LUTs. During aging analysis the actual values are determined by interpolation.

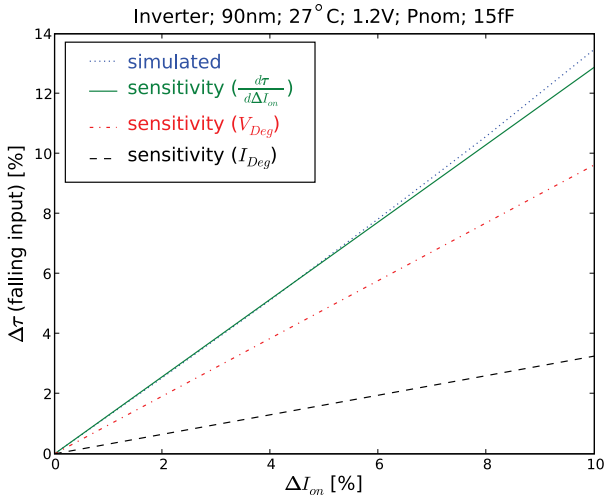

Fig. 3. Delay degradation $\Delta\tau$ of an inverter due to a drift ΔI_{on}. The solid line indicates how well the simulated delay degradation can be approximated with the aid of the computed sensitivity $\chi^Q_{\Delta I_{on},n}$. Also the approximations obtained with the two separate sensitivities V_{Deg} and I_{Deg} are given.

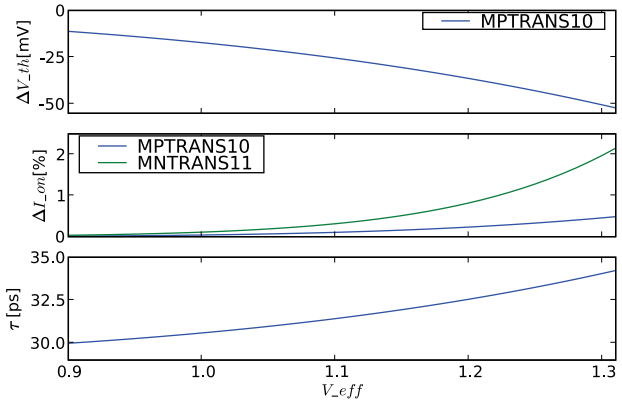

Fig. 4. Dependencies of V_{eff} on ΔV_{th}, ΔI_{on} and inverter delay τ. The dependencies are obtained from our aging-aware gate model. For ΔI_{on} the drifts for both transistors are listed separately.

E. Discussion

Fig. 4 shows the dependencies provided by our gate model of effective supply voltage over lifetime V_{eff} on ΔV_{th}, ΔI_{on} and inverter delay τ.

Major advantages of the new aging-aware gate model are its independence and flexibility. Only the drifts Δp_n in (5) are dependent on the stress factors **SF** and they are computed during the aging analysis. Hence, a standard cell library does not have to be re-characterized for varying **SF**. It is also very flexible, because the degradation equations can easily be replaced and new drift-related aging effects can be added. Improved equations taking the NBTI recovery phenomenon [16] into account would raise the accuracy of the analysis. All that is needed to add other aging effects is a corresponding degradation equation and new sensitivities if they are not already available. The way different aging effects mask or even

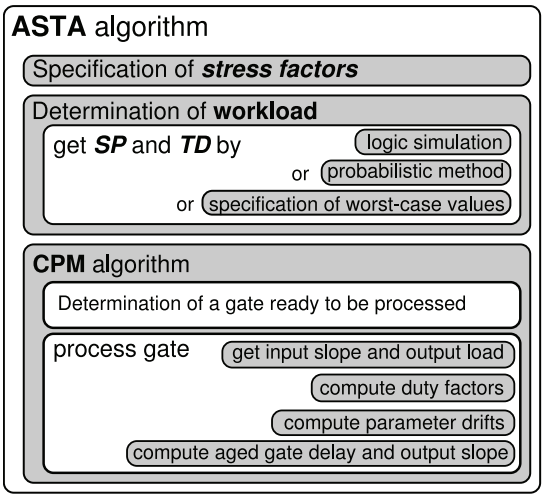

Fig. 5. Main steps of the aging analysis flow.

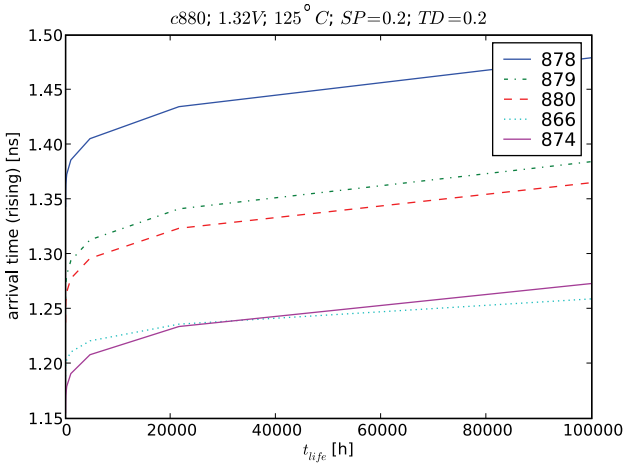

Fig. 6. The five slowest output arrival times over lifetime for ISCAS circuit c880. Individual workloads for the gates were obtained for $SP = 0.2$ and $TD = 0.2$ at primary inputs. The signals 866 and 874 change their order with time.

amplify each other is not well understood at the moment. In our approach, we assumed that NBTI and HCI do not influence each other.

IV. Aging analysis with proposed gate model

In this section we describe how the gate model is used to determine the degraded timing information of a combinatorial circuit. A static timing analyzer was implemented that can process our aging-aware gate model.

Most STA tools use the critical path method (CPM) [15] to determine the slowest timing path of a circuit. The algorithm traverses the circuit in topological order, from primary inputs to primary outputs. For every net the worst-case arrival times for a rising and a falling transition are determined. A gate is ready to be processed if the arrival times at all its inputs are available. The only step that is different in the CPM for ASTA compared to traditional STA is the treatment of a gate ready to be processed.

The first step is to specify the stress factors **SF** (see Fig. 5). Then, the individual workloads for the gates have to be obtained. Hence, values for SP and TD have to be determined for all nets. There are two methods to do that. Either a logic simulation can be used if primary input vectors for the circuit are available [14]. This method is strongly input pattern dependent. Otherwise probabilistic methods can be used to propagate SP and TD values from the primary inputs throughout the circuit. The second method is only weakly input pattern dependent but has a reduced accuracy. If no information about the primary input signals is available, a worst case analysis can be performed and values for SP and TD have to be predefined by the user. Those predefined values will then be used for every net of the circuit.

Thereafter, the CPM is performed. When a gate is processed, the first step is to determine the latest input signal. This signal triggers the transition of the gate output. Also the output load of the gate has to be obtained. Afterwards the duty factors DF_{NBTI} and DF_{HCI} for the degradation equations (13), (15) are calculated. The next step is to calculate the parameter drifts of all transistors by means of the degradation equations (9) and (10). Finally, the aged gate delay τ_{Age} and the aged output slope $S_{OUT,Age}$ can be computed with (5).

V. Results

For evaluation purposes, an industrial 90 nm standard cell library is characterized for the following corner case: nominal process P_{nom}, a temperature T of $27° C$ and $0.9 V$ supply voltage V_{DD}. A standard use profile for communication applications is used with a specified lifetime of 10 years, an effective temperature T_{eff} of $125° C$ and an effective supply voltage V_{eff} of $1.32 V$. Due to the low V_{DD}, the circuit is very sensitive to parameter changes and the demanding use profile results in a high parameter drift. Hence, a large circuit performance degradation will be observed. Such a combination of high V_{eff} and low V_{DD} is possible if the circuit is operating in a high performance mode for a long time and is than switched to a low power mode.

Modified ISCAS85 benchmark circuits are used as test circuits, where complex gates are replaced by a combination of single stage gates. Single stage gates do not have any internal nets connected to the gate terminals of transistors inside the gate. That is due to two reasons. For the internal nets of a gate no SP and TD values can be obtained and for the calculation of DF_{HCI} the transition time S_{IN} for internal nets would be needed. Extending our gate model that complex gates can be analyzed directly is a subject of current work.

Fig. 6 shows how the arrival times at the primary outputs of circuit c880 increase over lifetime. SP and TD values are determined by the probabilistic method in [9] for $SP = 0.2$ and $TD = 0.2$ at the primary inputs. The figure indicates that it is not enough just to consider the most critical nominal path during aging analysis because the order of the arrival times can change over lifetime (signals 866 and 874).

In Table I the path delay degradation $\Delta delay$ of the critical paths are depicted for a worst-case analysis. The fresh path delays without aging (FRESH) are shown as a reference. Either the degradation due to both effects (BOTH) or just due to one effect (NBTI, HCI) is analyzed. When both effects are considered, the degradation of the critical path delay is between 12.3 % and 19.5 %. The dominant aging effect in our case is NBTI, with a performance degradation of up to

TABLE I
DEGRADATION OF CRITICAL PATH DELAYS FOR DIFFERENT ASTA SETTINGS. EITHER BOTH OR JUST ONE AGING EFFECT WERE CONSIDERED. FOR BOTH AGING EFFECTS ALSO THE RUN TIME IS GIVEN.

	FRESH [ns]	HCI [%]	NBTI [%]	BOTH [%]	BOTH ([s])	NO_SLP [1] [%]
c17	0.18	4.7	8.4	13.0	(2.57)	9.8
c432	2.30	4.0	10.9	15.4	(4.06)	11.1
c499	1.49	5.0	11.7	17.3	(6.52)	12.2
c880	1.88	3.3	8.4	11.9	(6.97)	9.4
c1355	1.84	4.0	8.7	13.2	(7.56)	9.8
c1908	2.51	3.2	10.3	14.1	(17.07)	10.1
c2670	2.89	2.4	10.1	12.8	(15.65)	9.1
c3540	3.47	2.4	10.6	13.2	(19.11)	9.8
c5315	3.10	2.5	9.4	12.3	(28.32)	9.1
c6288	8.88	1.7	12.3	14.2	(29.82)	9.0
c7552	2.66	2.7	9.6	12.6	(34.90)	9.3
MEAN	2.84	3.3	10.1	13.6	(15.69)	9.9

[1] both aging effects but without considering an aged output slope

14.6 %. In the last column values for $\Delta delay$ are given if no aged output slope $S_{OUT,Age}$ is computed. Not considering $S_{OUT,Age}$ will underestimate the degradation by 12.7 % in average.

For BOTH also the run time on an Opteron 2.4 GHz, 2 GB RAM is given. In contrast to traditional STA several additional calculations have to be performed when a gate is processed in ASTA. Nevertheless, our block based approach processes each gate after another and shows good scalability.

The degradation of a circuit is dependent on circuit structure and the individual workload of the gates. Fig. 7 quantifies the advantage of considering the individual workloads. The bars represent the range of the degradation if the values for SP and TD at the primary inputs are varied between 0.0 and 1.0. The lines depict the worst-case degradation as listed in Table I. When just the worst-case degradation is considered, the degradation is overestimated by at least 2.6 percentage points.

VI. CONCLUSION

We introduced an aging analysis method on gate level capable of determining the impact of the two dominant drift-related aging effects on circuit timing. A canonical gate model is used to obtain the impact of parameter drifts on gate delay and output slope. The degradation of the critical path was underestimated by mean of 12.7 % in our test cases when the degraded output slope was not considered. The drifts are calculated by the use of duty factor based degradation equations. In order to calculate the drift of single transistors as accurately as possible, the internal gate structure and the gate's workload are employed to identify the amount of time the transistor is in a stress condition. When the individual workloads of the gates were not considered, we observed an overestimation of the degradation by at least 2.6 percentage points.

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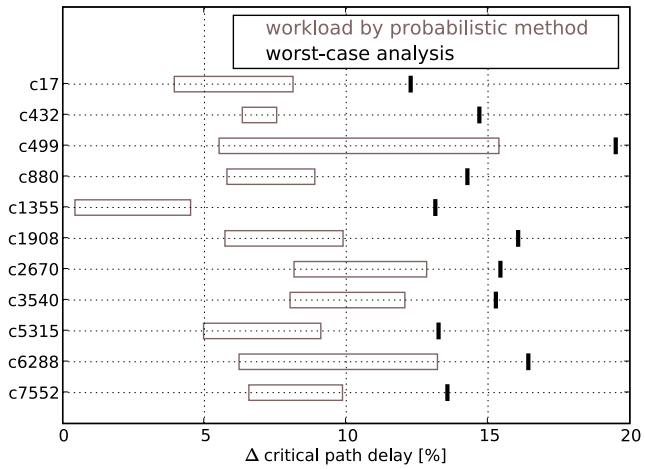

Fig. 7. Comparison of critical path delay degradation due to individual workloads and worst-case degradation. The bars represent the interval for the critical path degradation if SP values are in $\{0.0, 0.1, 0.2, \ldots, 1.0\}$ and TD values are in $\{0.0, 0.33, 0.67, 1.0\}$ for the primary inputs.

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