
Report : timing

-path full

-delay max

-max_paths 1

Design : s35932_bench

Version: K-2015.06-SP3

Date : Sat Nov 21 16:47:31 2015

* Some/all delay information is back-annotated.

Operating Conditions: tt1p05v25c Library: saed32rvt_tt1p05v25c

Parasitic source : LPE

Parasitic mode : RealRC

Extraction mode : MIN_MAX

Extraction derating : 25/25/25

Information: Percent of Arnoldi-based delays = 5.36%

Startpoint: TM1 (input port clocked by blif_clk_net)

Endpoint: DATA_9_30 (output port clocked by blif_clk_net)

Path Group: blif_clk_net

Path Type: max

Point	Incr	Path

clock blif_clk_net (rise edge)	0.00	0.00
clock network delay (ideal)	0.20	0.20
input external delay	1.00	1.20 f
TM1 (in)	0.00 @	1.20 f
U155/Y (NBUFFX2)	0.04 @	1.24 f
U159/Y (NBUFFX2)	0.05 &	1.29 f
U181/Y (NBUFFX2)	0.04 &	1.32 f
U182/Y (INVX2)	0.03 &	1.35 r
U9483/Y (XNOR3X1)	0.15 &	1.50 r
U9524/Y (XNOR2X1)	0.10 &	1.60 r
U698/Y (NBUFFX2)	0.05 @	1.65 r
DATA_9_30 (out)	0.00 @	1.65 r
data arrival time		1.65
clock blif_clk_net (rise edge)	5.00	5.00
clock network delay (ideal)	0.20	5.20
clock uncertainty	-0.30	4.90
output external delay	-1.00	3.90
data required time		3.90

data required time		3.90
data arrival time		-1.65

slack (MET)		2.25