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##########################################################################
####                Script for Placement and Routing                  ####
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# Root Directory = test_dir

# Run the following script in the "work" directory.

# Open Synopsys IC Compiler = icc_shell -gui

# Command: source ../scripts/icc_scripts.tcl > icc_run.txt

# *** Before Running, Change These Variables Based on Your Design ***
set Top_Name s35932_bench

# Set the Link and Target Library
set link_library {* ../models/saed32rvt_tt1p05v25c.db}

set target_library {../models/saed32rvt_tt1p05v25c.db}

# Create the Milkyway Library (Location of Placed and Routed Design)
create_mw_lib  -technology ../ref/tech/saed32nm_1p9m_mw_new.tf \
        -mw_reference_library {../ref/saed32nm_svt_1p9m} \
        -bus_naming_style {[%d]} -hier_separator {/} \
        -open  ../design_lib/test_lib

# Setup TLU+ Environment (Table of RC Coefficients)
set_tlu_plus_files -max_tluplus ../ref/tlup/saed32nm_1p9m_Cmax.tluplus \
        -min_tluplus ../ref/tlup/saed32nm_1p9m_Cmin.tluplus \
        -tech2itf_map  ../ref/tlup/saed32nm_tf_itf_tluplus.map

# Read the Design Netlist File
read_verilog {../output/netlist.v}

# Read the Design Constraint File
read_sdc  -version Latest "../output/design.sdc"

# Create Floorplan
create_floorplan \
        -core_utilization 0.70 \
        -start_first_row \
        -flip_first_row \
        -left_io2core 10 \
        -bottom_io2core 10 \
        -right_io2core 10 \
        -top_io2core 10

# Create PG Connection
foreach net {VDD} { derive_pg_connection -power_net $net \
        -power_pin $net -create_ports top}

foreach net {VSS} { derive_pg_connection -ground_net $net \
        -ground_pin $net -create_ports top}

derive_pg_connection -tie

# Create Power and Ground Rings
create_rectangular_rings  -nets  {VDD VSS}  -left_offset 1 -left_segment_layer M4 \
        -left_segment_width 3 -right_offset 1 -right_segment_layer M4 -right_segment_width 3 \
        -bottom_offset 1 -bottom_segment_layer M5 -bottom_segment_width 3 -top_offset 1 \
        -top_segment_layer M5 -top_segment_width 3

# Create Power and Ground Straps
create_power_straps  -direction horizontal  -nets  {VDD VSS}  -layer M5 \
        -width 0.16 -configure groups_and_step  -num_groups 130 -step 2

# Placement of Design
place_opt

# Preroute Standard Cells
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preroute_standard_cells -connect horizontal -extend_to_boundaries_and_generate_pins \
        -remove_floating_pieces -fill_empty_rows \
        -port_filter_mode off -cell_master_filter_mode off \
        -cell_instance_filter_mode off -voltage_area_filter_mode off \
        -route_type {P/G Std. Cell Pin Conn}

# Preroute Instances
preroute_instances

# Clock Optimization
clock_opt -fix_hold_all_clocks

# Route of Design
route_opt

# Insert Filler Cells
insert_stdcell_filler \
        -cell_without_metal "SHFILL128 SHFILL64 SHFILL3 SHFILL2 SHFILL1" \
        -connect_to_power {VDD} \
        -connect_to_ground {VSS}

# Write Parasitics
write_parasitics -output {../layout/parasitics.spef}

# Write Verilog File
write_verilog ../layout/layout.v

# Save the Design File in Milkyway Format
save_mw_cel -as design_mw

# Write the Fabrication File
write_stream -cells $Top_Name ../layout/design.gdsii

# Check Design
check_design > ../layout/check_design.txt
check_timing > ../layout/check_timing.txt

# Generate Reports
report_area > ../layout/area_report.txt
report_timing > ../layout/timing_report.txt
report_power > ../layout/power_report.txt
report_constraint -all_violators > ../layout/violator_report.txt

# Save Screenshot in Here !
```