Lab 2: Current Mirrors — Part I

Objectives

- To compare the accuracy, dynamic range, output resistance and voltage limitations of CMOS current mirror configurations, including basic current mirrors, cascodes and modified cascodes.

This is a simulation lab that should be completed within one week from the assigned date.

Reading

You are recommended to read the following sections from the text book:

- 7.4.1 : The basic MOSFET Current Source
- 7.5.1 : Cascode MOS Mirrors
- 7.5.4 : The Wilson MOS Mirror

1 Prelab

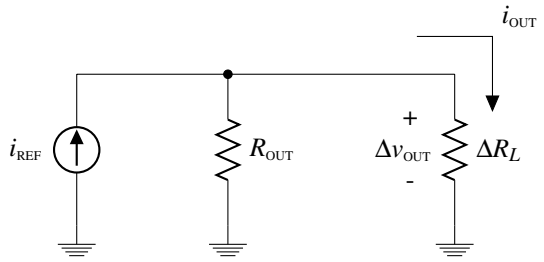
Exercise 1. Consider each of the four circuits shown in Fig. 1. Obtain an expression for the output resistance (looking to the drain of M_{out} for each circuit.

Exercise 2. Based on the predicted output resistance, state which of the circuits in Fig. 1 will have the best and worst accuracy.

Exercise 3. Each of the current mirror circuits in Fig. 1 requires all devices to be in *saturation*. Assuming the square-law model of the MOSFET, derive an expression for the minimum output voltage for each circuit in terms of v_{GS} and v_{OV}.

Exercise 4. Suppose $R_L = R_{\text{ref}}$ for each circuit in Fig. 1, and all devices are perfectly matched. In this case, prove that $i_{\text{OUT}} = i_{\text{REF}}$ and $v_{\text{OUT}} = v_{\text{REF}}$.

Exercise 5. If R_L is not equal to R_{ref}, then i_{OUT} is not necessarily equal to i_{REF}. To predict the *output error*, we may utilize a specialized type of small-signal model:



where $\Delta R_L = R_L - R_{\text{OUT}}$ and i_{OUT} is the estimated output current. Note that if $\Delta R_L = 0$, then the load is perfectly matched and $i_{\text{OUT}} = i_{\text{REF}}$. From this model, derive an expression for the *relative error* $E_R = \Delta i_{\text{OUT}}/i_{\text{REF}}$ in terms of R_{ref} and ΔR_L.

Exercise 6. In a SPICE simulation, we can obtain measurements for i_{REF}, i_{OUT}, R_{ref} and R_L. From these we can obtain Δi_{OUT} and ΔR_L. Derive an expression for R_{OUT} as a function of E_R and ΔR_L.

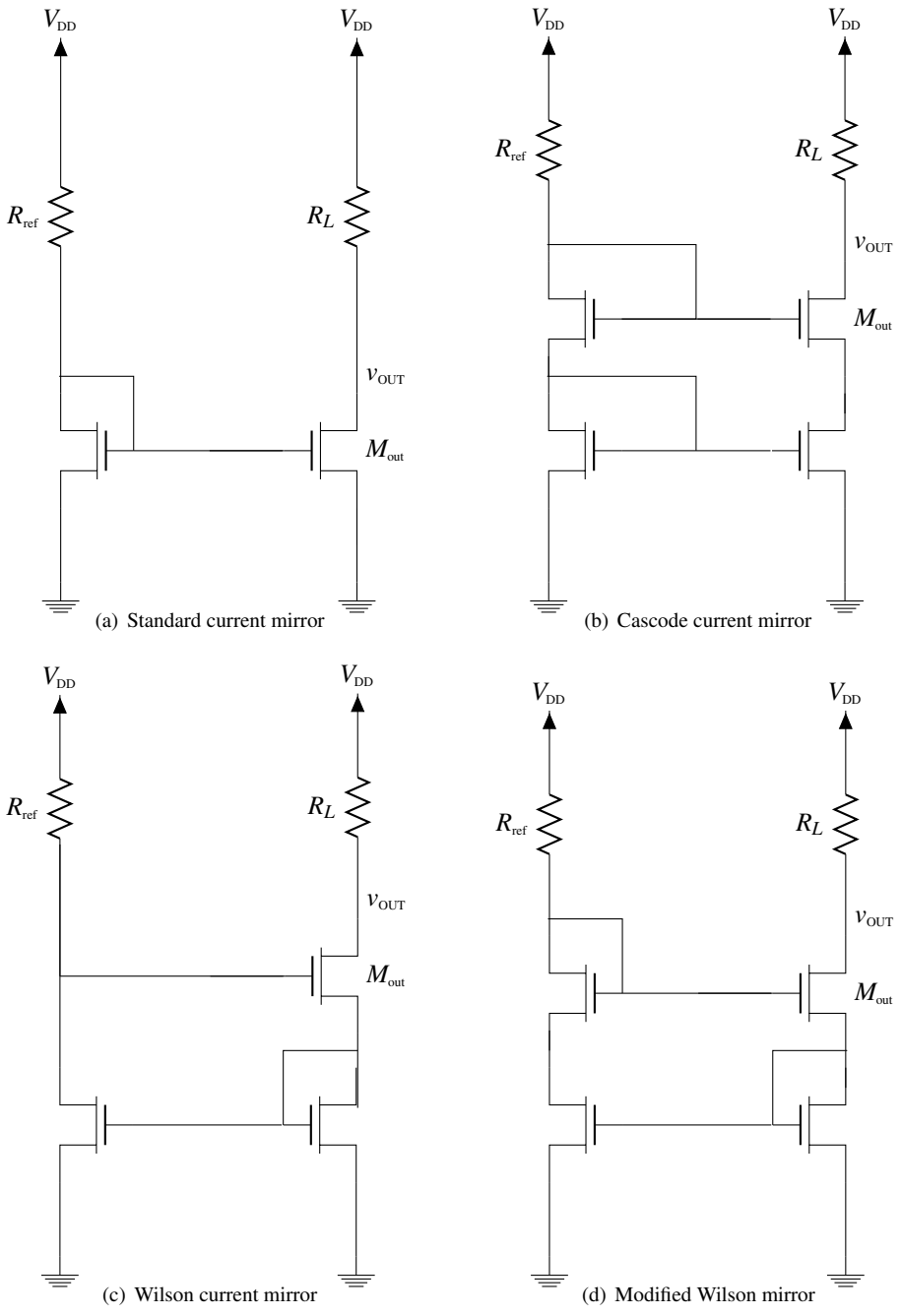


Figure 1: Several current-mirror configurations.

2 Modeling and Simulation

In this part of the lab you will construct circuit models and perform simulations using CAD tools, and then analyze the results using Matlab.

Procedure 1. Construct SPICE models of the four current mirror circuits shown in Fig. 1. Use these parameters for the circuits:

- $R_{\text{ref}} = 1\text{k}\Omega$.
- $R_L = 1\text{k}\Omega$.
- $V_{\text{DD}} = 5\text{V}$ for the basic current mirror.
- $V_{\text{DD}} = 10\text{V}$ for the cascode, Wilson and modified Wilson mirrors.
- All MOSFET devices use the "ncg" model from the `lab_parts.md` model file.

If using NGSpice: To simulate these circuits, obtain the "lab_parts.md" file from the course web page and reference it in your SPICE files by using an **include** statement. When creating instances for the NMOS devices, you need to provide the devices' geometry information, like this:

```
.include lab_parts.md

...

M1 <drain> <gate> <source> <substrate> ncg L=7.8e-6 W=138e-6
```

This tells the simulator to use the "ncg" technology model for an NMOS device of length $L = 7.8\mu\text{m}$ and width $W = 138\mu\text{m}$. Alternatively, you can use the **subcircuits** aldn and aldp which are already defined in lab_parts.md. These subcircuits already contain the geometry definitions so that you don't have to keep re-typing them. To instance an NMOS device using the subcircuit method, the device should be named with an 'X' label like this:

```
XM1 <drain> <gate> <source> <substrate> aldn
```

Note: You may use a different CAD tool, such as PSpice, if you prefer. The instructor and TA will provide support only for NGSpice.

Procedure 2. Verify each of your models by performing an *operating point* simulation using the .OP command in SPICE. For each of your circuits, the input current should equal the output current, which should be on the order of 2mA.

Procedure 3. Now perform a DC sweep simulation varying R_L from $1.1\text{k}\Omega$ to $2\text{k}\Omega$ for each circuit. In SPICE, you

may accomplish this using the DC sweep command:

```
.DC RL 1.1k 2k 10
```

This command tells the simulator to solve the operating point repeatedly for different values of R_L, which will be swept from 1.1kΩ up to 2kΩ in steps of 10Ω.

For each circuit perform the following tasks:

(a) Measure i_{REF} and i_{OUT} and transfer the associated simulation data to Octave (or Matlab) for analysis.

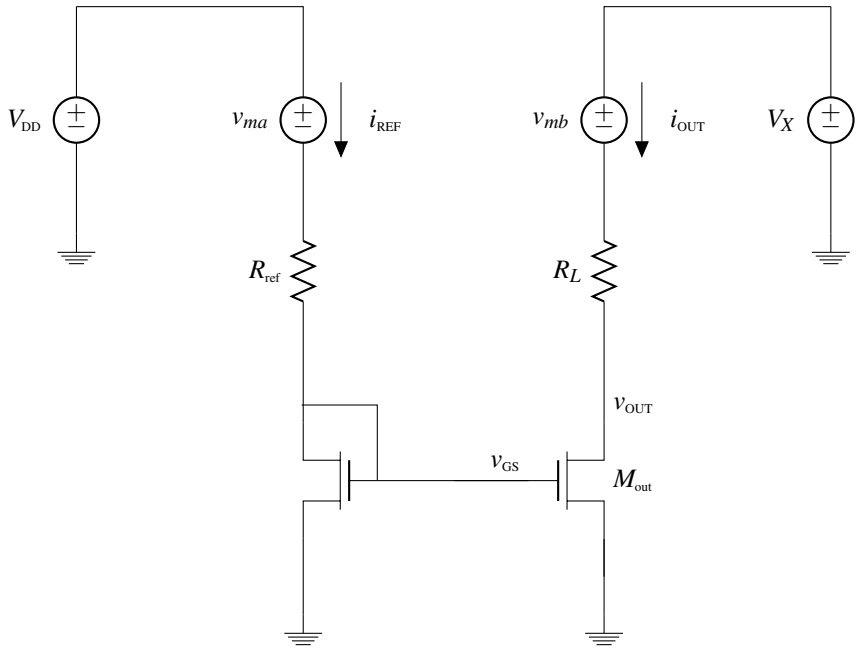
(b) In Octave, plot Δi_{OUT} as a function of ΔR_L. Note the linear appearance.

(c) Using the expression you derived for the mirror's output resistance, compute R_{OUT} using the simulated results for Δi_{OUT}, i_{REF} and ΔR_L.

(d) Plot R_{OUT} as a function of ΔR_L. It will not be perfectly constant, but you should notice that the variation is small compared to the magnitude of R_{OUT}. Based on this plot, estimate a numerical value for R_{OUT} to two significant figures.

After completing these simulations for all circuits, compare R_{OUT} for each of the mirror circuits. Does the trend match your prediction?

Procedure 4. Next you will perform a DC sweep of the supply voltage on the circuit's output branch, while leaving the supply voltage unchanged on the reference branch, like this:



where V_X is the power supply on the output branch. Perform a DC sweep of V_X, varying it from 0V up

to 10V in steps of 0.1V. For each circuit, perform these steps:

(a) Plot a trace showing i_{OUT} and i_{REF} as functions of v_{OUT} (note that v_{OUT} is the potential at the *drain terminal* of M_{out} in each circuit). Estimate the minimum value of v_{OUT} required for correct operation.

(b) Probe the value of v_{GS} as indicated in the figure above (this will always be the gate potential for the *bottom devices* in the cascode circuits). If the threshold voltage for our MOSFETs is 0.7V, calculate a value for v_{OV}. What is the expected minimum output voltage? How well does it compare to the observed minimum?