

Loading db file '/home/shayan/test_dir/models/saed32rvt_tt1p05v25c.db'
 Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)
 Warning: Design has unannotated primary inputs. (PWR-414)
 Warning: Design has unannotated sequential cell outputs. (PWR-415)

Report : power
 -analysis_effort low
 Design : s35932_bench
 Version: H-2013.03-SP5-3
 Date : Sat Nov 21 16:44:38 2015

Library(s) Used:

saed32rvt_tt1p05v25c (File: /home/shayan/test_dir/models/saed32rvt_tt1p05v25c.db)

Operating Conditions: tt1p05v25c Library: saed32rvt_tt1p05v25c
 Wire Load Model Mode: enclosed

Design	Wire Load Model	Library
s35932_bench	35000	saed32rvt_tt1p05v25c

Global Operating Voltage = 1.05
 Power-specific unit information :
 Voltage Units = 1V
 Capacitance Units = 1.000000ff
 Time Units = 1ns
 Dynamic Power Units = 1uW (derived from V,C,T units)
 Leakage Power Units = 1pW

Cell Internal Power = 7.6786 mW (98%)
 Net Switching Power = 188.6687 uW (2%)

 Total Dynamic Power = 7.8673 mW (100%)

Cell Leakage Power = 4.3481 mW

Power Group	Internal Power	Switching Power	Leakage Power	Total Power (%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000 (0.00%)	
memory	0.0000	0.0000	0.0000	0.0000 (0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000 (0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000 (0.00%)	
register	7.2372e+03	50.8725	1.6483e+09	8.9364e+03 (73.16%)	
sequential	0.0000	0.0000	0.0000	0.0000 (0.00%)	
combinational	441.3361	137.7969	2.6999e+09	3.2790e+03 (26.84%)	
Total	7.6786e+03 uW	188.6695 uW	4.3481e+09 pW	1.2215e+04 uW	