ECE 5420 – Microelectronics II
SPICE Handout VI

BJTs

Like MOSFETs and diodes, every BJT device requires a model to describe its behavior. The most basic BJT model is based on the Ebbers-Moll model. The model specifies beta factors, diode parameters and capacitance parameters for the forward and reverse PN junctions. For example, the model for a 2N3904 NPN device looks like this:

```
.model Q3904 NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=74.03 Bf=416.4 Ne=1.259
+      Ise=6.734f Ikf=66.78m Xtb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1
+      Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75
+      Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)
```

Some important parameters here include BF (forward beta), BR (reverse beta), Cjc (collector zero-bias junction-capacitance), Cje (emitter zero-bias junction capacitance), Vjc and Vje (the built-in potential of the collector and emitter, respectively), and Mjc and Mje (the denominator exponent in the collector and emitter junction capacitance formulas, respectively).

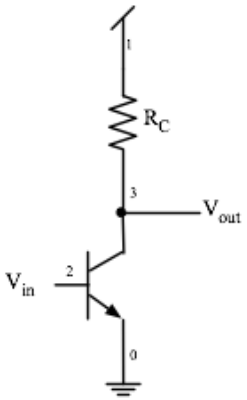
The instance syntax for a BJT device is:

```
Q1 collector base emitter [substrate] model_name [area]
```

The [substrate] and [area] parameters are optional. They should be included when simulating integrated BJT circuits, but are not necessary for discrete components.

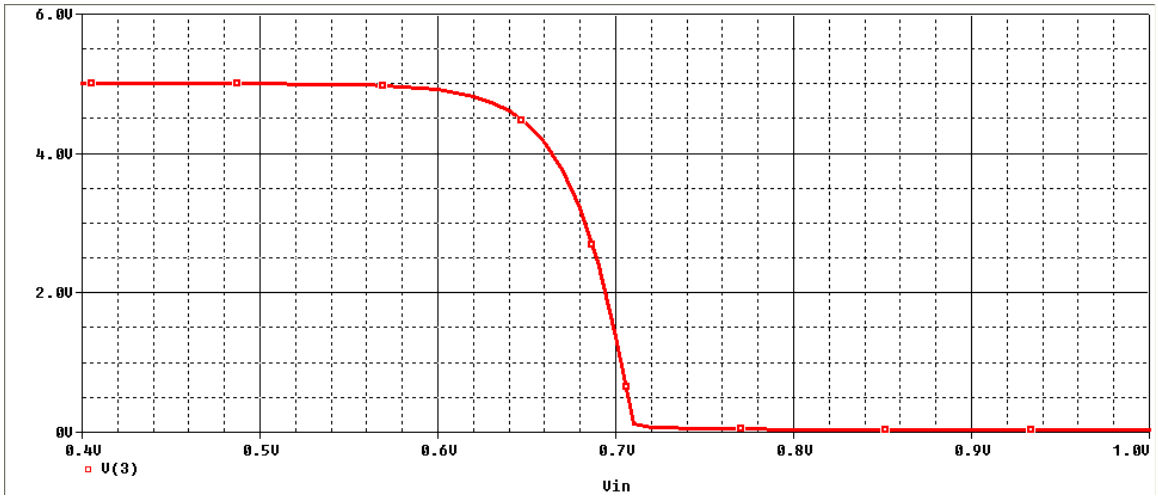
Example:

Let's perform a DC sweep simulation on the Common Emitter amplifier shown below.

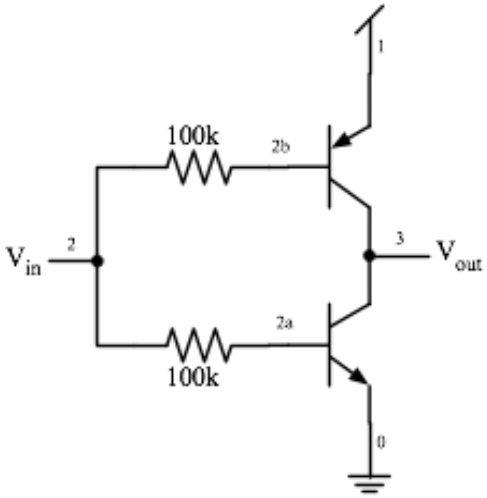



```
* Common Emitter simulation
.include BJT.lib
.probe

Vdd 1 0 DC 5V
Vin 2 0 DC 0V

Q1 3 2 0 Q3904
RC 1 3 1k

.DC Vin 0 5 .1

.end
```

This simulation should produce the output shown below at node 3.

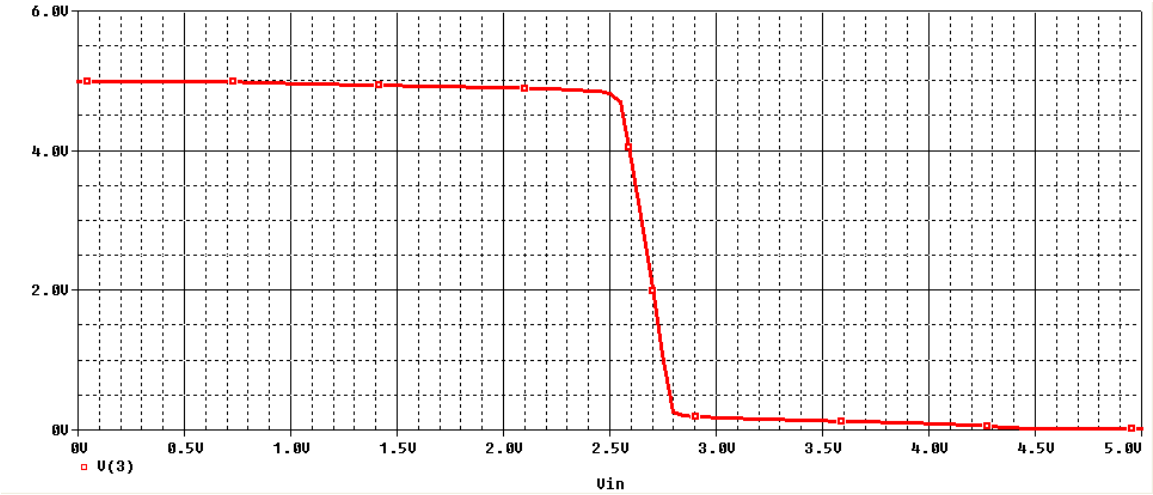


Next let's simulate a complementary BJT inverter circuit:



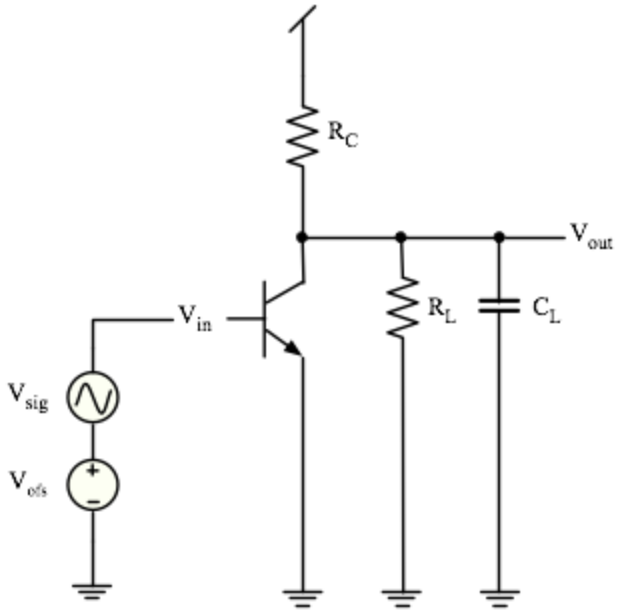

```
* BJT Inverter Simulation
.probe
.include BJT.lib

Vdd 1 0 DC 5
Vin 2 0 DC 0

R1 2 2a 100k
R2 2 2b 100k

* NPN transistor, 2N3904:
Q1 3 2a 0 Q3904
* PNP transistor, 2N3906:
Q2 3 2b 1 Q3906

.dc Vin 0 5 .05

.end
```

This circuit produces the output shown below at node 3.



Exercises:

1. Simulate a common emitter stage (shown below) with R_L=100kΩ, R_C=1kΩ, C_L=1μF, V_{ofs}=0.65V and VCC = 5V. Predict the 3dB cutoff frequency and perform an AC simulation to confirm your prediction. You may ignore any internal BJT capacitance and the Early-effect resistance when calculating the cutoff frequency. For the AC analysis, declare V_{sig} as a 1mV AC source. Perform the sweep from 1Hz to 100Hz. Turn in your analysis, SPICE file and a Bode plot of the simulation output. Use the cursors to carefully measure the simulated cutoff frequency, and record the result.



2. Simulate the Emitter Follower stage shown below. Use R_E=10kΩ and VCC=5V, and let Vin be a sine wave with a frequency of 1kHz, an amplitude of 100mV, and an offset of 3V. Perform a transient simulation that includes two periods of the input signal. Turn in your SPICE file and a transient probe plot showing the input and output signals on the same chart. Using the probe cursors, measure the

small-signal gain of the circuit and the DC offset difference between the input and output signals. Turn in your SPICE file, the probe waveforms and your measurements.