ECE 3410 – Microelectronics I
SPICE Handout V

MOSFETs

The real reason behind the existence of SPICE is to simulate integrated transistor circuits, including MOSFETs and BJTs. Transistors are considerably more complex than other devices. A typical SPICE package is able to simulate a variety of MOSFET models which differ in their degree of physical precision. The most common models are the BSIM family, which require a multitude of parameters to describe each transistor's behavior. Internally, each model has its own set of non-linear equations which are solved simultaneously by SPICE during simulation. The results can be quite accurate if the right models are used. Model parameters must usually be obtained from the device's manufacturer or measured in a highly specialized lab environment.

The various MOSFET models are distinguished by different *levels* within the model declaration. A partial model example is the statement below. This statement declares parameters for a BSIM3 model (indicated by the "level=49" parameter), specifying version 3.1 of the model.

```
.model model_name NMOS( level=49 version=3.1 tox=4e-9 vth0=0.41 ... )
```

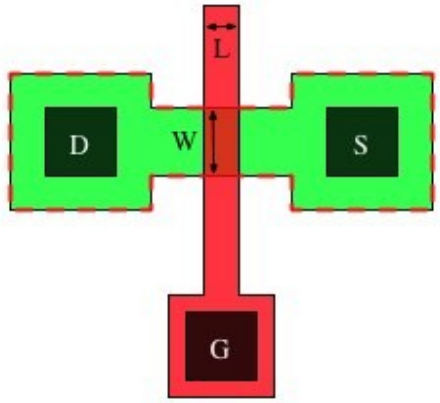
This particular model indicates N-Type devices in which the oxide thickness is 4nm, the nominal threshold voltage is 0.41V, along with a host of other parameters which are not shown.

Note: When reporting simulation results in a lab book, class report, or published paper, it is customary to identify the model used for the simulation. In this case we would say "the circuit is simulated using the BSIM3v3.1 MOS model."

In an integrated circuit, the designer has control over the geometry of the device. A MOSFET declaration must define the device's terminal connections, the model name and the device's dimensions. The dimensions include the length and width, as well as the area and perimeter of the source and drain regions.

```
M1 drain gate source substrate model_name L= W= AD= PD= AS= PS=
```

The geometry parameters are illustrated in the Figure shown below, which represents a typical transistor layout. In this Figure, the red region represents the gate material, and the green represents the N-type diffusion region. The black squares are metal contacts.



The drain/source perimeter is calculated by summing the distance around the dashed red line on the drain/source side of the gate. Note that the dashed red line excludes the gate edge. The drain/source area is calculated in the usual way. A possible declaration for this transistor is as follows.

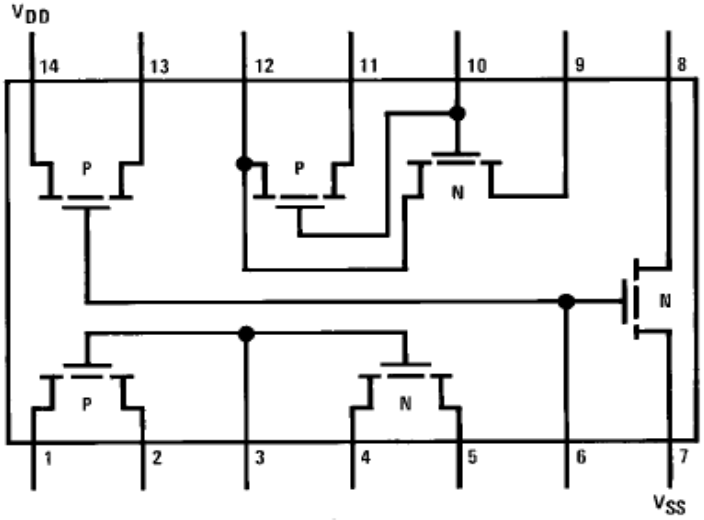
```
M1 1 2 0 0 NMOS L=.5u W=1u AD=64p PD=8u AS=64p PS=8u
```

The AD, AS, PD and PS parameters can be omitted, but your simulation will be more accurate if you include these values. These parameters are also unnecessary when simulating discrete off-the-shelf components.

CD4007

For use in discrete circuits, MOSFETs come in a variety of packages. One useful package is the CD4007 CMOS array, which is an integrated circuit containing two NMOS and two PMOS devices, along with a CMOS inverter configuration. For our lab and simulation exercises, we will use the CD4007 array.

A pinout of the CD4007 is shown below. Note that one NMOS has its source always connected to Vss, and one PMOS always has its source connected to Vdd. The substrate connections are all made internally, and each gate is shared between one NMOS and one PMOS device.



For breadboard circuits, very simple SPICE models often suffice. A low-complexity model for the CD4007 MOSFETs is given below.

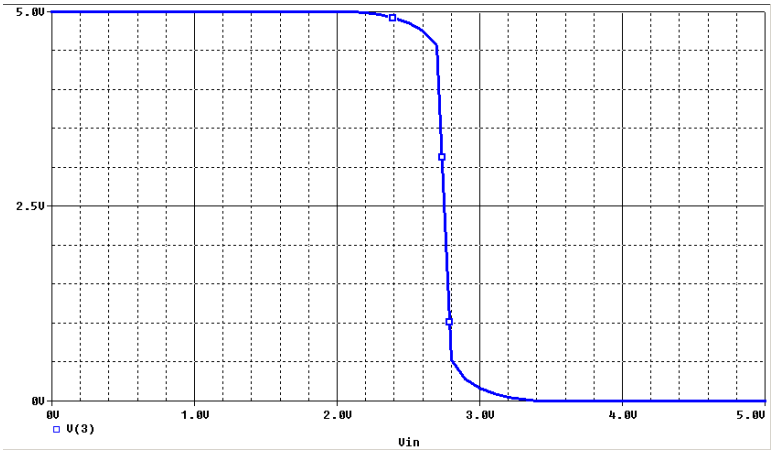
```
* CD4007 NMOS and PMOS SPICE models

.model NMOS NMOS
+ Level=1    Gamma= 0   Xj=0
+ Tox=1200n  Phi=.6     Rs=0      Kp=111u  Vto=2.0    Lambda=0.01
+ Rd=0       Cbd=2.0p   Cbs=2.0p  Pb=.8    Cgso=0.1p
+ Cgdo=0.1p  Is=16.64p  N=1

*The default W and L is 30 and 10 um respectively and AD and AS
*should not be included.


.model PMOS PMOS
+ Level=1    Gamma= 0   Xj=0
+ Tox=1200n  Phi=.6     Rs=0      Kp=55u  Vto=-1.5   Lambda=0.04
+ Rd=0       Cbd=4.0p   Cbs=4.0p  Pb=.8   Cgso=0.2p
+ Cgdo=0.2p  Is=16.64p  N=1

*The default W and L is 60 and 10 um respectively and AD and AS
*should not be included.
```

In the above models, Kp is equal to $\mu_n C_{ox}$, there is no body effect, $\lambda=0.1V^{-1}$, and the oxide thickness is 1200nm. The other parameters represent parasitic capacitance and leakage current phenomena. These models should be entered into a file called “cd4007.lib” and placed within your simulation directory. To make use of the models, you must include them within your SPICE file.

Example:

```
* Inverter simulation
.include cd4007.lib
.probe

Vdd 1 0 DC 5V
Vin 2 0 DC 0V

M1 3 2 1 1 PMOS W=60u L=10u
M2 3 2 0 0 NMOS W=30u L=10u

.DC Vin 0 5 .1

.end
```

This simulation should produce the output shown below.



Exercises:

1. Simulate a circuit with three parallel inverters, in which the PMOS device width is 20um, 60um and 100um. Let all the inverters be connected to the same input. Perform a DC sweep on the input voltage, just as in the example, and plot the outputs of the three inverters together on the same axes. Describe what happens. Can you explain the results using your knowledge of MOSFET devices?
2. Using the CD4007 models, simulate a single NMOS device in saturation, performing a DC sweep on the gate voltage from 0V to Vdd, where Vdd is 5V. Connect the MOSFET drain to Vdd and the source and substrate to ground. Plot the drain current of the device, which is listed in the trace menu as ID(M1). On another set of axes, plot sqrt(ID(M1)). You should see a straight line. Using the cursors, measure the slope of this line. The slope is equal to $\text{sqrt}\{\frac{1}{2}\mu_n C_{ox}(W/L)\}$. Report your measured value of $\mu_n C_{ox}$. How closely does your measurement match the model parameter Kp?
3. Repeat exercise 2 using a PMOS device.
4. Repeat exercises 2 and 3, adding a 10kΩ load resistor to the drain of each device. Instead of plotting sqrt(ID), plot $\text{sqrt}(5 - V_D)$ (NMOS) and $\text{sqrt}(V_D)$ (PMOS), where V_D refers to the voltage at the drain of the MOSFET. Explain the shape of these curves. Specify a method for measuring Kp based on the drain voltage. Report your choice of data points, your formula(s) and your results.

5. Using the available model data, design a PMOS current-mirror circuit to provide a bias of 0.5mA. Use a fixed load resistor at the drain of the diode-connected transistor. Determine the resistance needed to obtain 0.5mA. Verify your result by performing an operating-point analaysis on the current-mirror circuit. After a .op simulation, detailed results for each transistor will be placed at the end of the SPICE output file. The drain current is indicated as "ID".

6. Now use the current-mirror circuit from exercise 4 as a bias source for a common-source amplifier stage. As an input, provide a sinusoid with a 3.5V offset, 0.01V amplitude and 1kHz frequency. Analyze this circuit and predict the transconductance, output resistance and voltage gain. Perform a transient simulation with a 3ms duration. Turn in a plot showing the input and output waveforms, and measure the gain of this amplifier stage. How closely does it match your prediction?

7. Analyze the common-source circuit and determine the minimum and maximum values for v_{IN} and v_{OUT}. In SPICE, perform a DC sweep of the input voltage, from 3 to 4 volts in steps of 0.001V. Plot the waveform of v_{OUT}. Using the cursors, mark off a box in which v_{OUT} is nearly a straight line. The boundaries of this box are the maximum and minimum values for v_{IN} and v_{OUT}. Also measure the slope within the straight-line region. How closely does this slope match the gain that you reported in exercise 6?