

Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

Report : power
-analysis_effort low
Design : s35932_bench
Version: K-2015.06-SP3
Date : Sat Nov 21 16:47:32 2015

Library(s) Used:

saed32rvt_tt1p05v25c (File: /lhome/shayan/test_dir/models/saed32rvt_tt1p05v25c.db)

Operating Conditions: tt1p05v25c Library: saed32rvt_tt1p05v25c
Wire Load Model Mode: enclosed

Design	Wire Load Model	Library
s35932_bench	ForQA	saed32rvt_tt1p05v25c

Global Operating Voltage = 1.05
Power-specific unit information :
Voltage Units = 1V
Capacitance Units = 1.000000ff
Time Units = 1ns
Dynamic Power Units = 1uW (derived from V,C,T units)
Leakage Power Units = 1pW

Cell Internal Power = 3.2079 mW (79%)
Net Switching Power = 839.3428 uW (21%)

Total Dynamic Power = 4.0472 mW (100%)

Cell Leakage Power = 4.9515 mW

Power Group	Internal Power	Switching Power	Leakage Power	Total Power (%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000 (0.00%)	
memory	0.0000	0.0000	0.0000	0.0000 (0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000 (0.00%)	
clock_network	99.7256	528.2640	4.3864e+07	671.8532 (7.47%)	
register	2.4840e+03	66.4653	1.6515e+09	4.2019e+03 (46.69%)	
sequential	0.0000	0.0000	0.0000	0.0000 (0.00%)	
combinational	624.1705	244.6132	3.2562e+09	4.1250e+03 (45.84%)	
Total	3.2079e+03 uW	839.3425 uW	4.9515e+09 pW	8.9988e+03 uW	

1