Lab 4: OTAs and Op Amp Circuits

Objectives

- To design and analyze a MOSFET Operational Transconductance Amplifier (OTA) circuit.
- To analyze tradeoffs among key design parameters: gain, bandwidth, output resistance, power consumption.
- To implement a two-stage MOSFET operational amplifier suitable for standard feedback configurations.

Reading

You are recommended to read the following sections from the text book:

- 8.1–8.2 : MOSFET differential pair circuits
- 8.5 : Active-loaded MOS differential pair
- 8.6.1 : A two-stage CMOS op amp
- Problem 8.108 (page 682)
- 9.8 : High-frequency response of differential amplifiers
- 12.1 : The two-stage CMOS op amp (there is some repetition from 8.6.1)

Model Parameters

The circuits in this lab are constructed using devices from the ALD1105 MOSFET array chip. The parameters for these devices are

$$\begin{array}{ll} K_n = 0.7\,\mathrm{mA/V^2} & K_p = 0.19\,\mathrm{mA/V^2} \\ \lambda_n = 0.042\,\mathrm{V^{-1}} & \lambda_p = 0.017\,\mathrm{V^{-1}} \\ V_{\text{ThN}} = 0.75\,\mathrm{V} & V_{\text{ThP}} = -0.74\,\mathrm{V} \end{array}$$

In addition, a single-ended supply voltage is used with $V_{\text{DD}} = 5\,\mathrm{V}$.

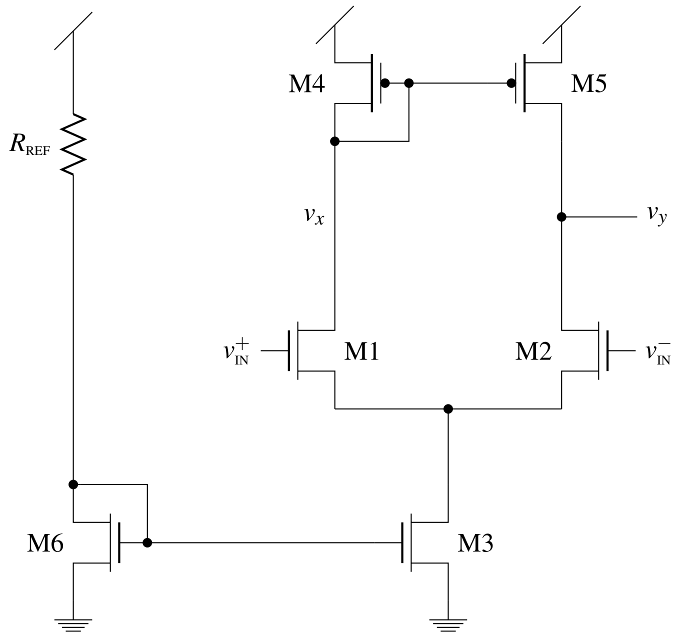

Figure 1: An OTA circuit, also known as a CMOS differential amplifier with active current mirror load.

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Exercise 1. Study the OTA circuit shown in Fig. 1. Suppose $R_{\text{REF}} = 10\,\text{k}\Omega$. Solve for the circuit's bias current i_{REF}. Then solve g_m and r_o for the PMOS and NMOS devices. Finally, predict the circuit's gain, $A_{vo} = \frac{v_y}{v_{\text{IN}}}$, the output resistance, the minimum and maximum common-mode voltages, and the minimum and maximum output voltages.

Exercise 2. Repeat Ex. 1 with $R_{\text{REF}} = 5\,\text{k}\Omega$.

Exercise 3. Open the file `ex3.sp` and study its contents. This file contains a *testbench* — a set of automated test and measurement commands — which evaluate a circuit described in seperate file. The actual circuit is described in the file `OTA.sp`. The testbench contains power supplies, signal sources and analysis statements.

This testbench performs numerous test functions while sweeping the input common mode voltage, v_{ICM}. In the testbench file, set R_{REF} to $10\,\text{k}\Omega$ (defined by the `.param` statement near the top of the file) and run the simulation. It will generate a series of transient simulation plots, one plot for each value of v_{ICM}. You should notice that the output amplitude — and hence the amplifier's gain — varies considerably for different values of v_{ICM}. When the simulation is finished, it prints out a table of data in the NGSpice terminal. Then copy the output data into Matlab or Octave and produce the following plots (I recommend using an m-file script to automate these plots):

- A plot of A_{vo} vs v_{ICM}.
- A plot of BW vs v_{ICM}.

- A plot of i_{REF} vs v_{ICM}.

Overall, how close does the measured gain match your prediction? You should see that the gain increases at low values of v_{ICM}. Can you explain this? Describe the relationship between gain and bandwidth as v_{ICM} is varied. From the graphs, determine the minimum input common mode voltage and compare it to your predicted value.

Exercise 4. Repeat Ex. 3 with $R_{\text{REF}} = 5\,\text{k}\Omega$. You may see a large discrepancy between the SPICE results and your predictions from Ex. 2. Can you identify the most likely cause of this discrepancy? (Hint: look at the values of i_{REF} calculated by NGSpice).

Exercise 5. Now open the file `ex5.sp` and study its contents. This file executes a simple transient simulation with FFT analysis. The input amplitude is set by a parameter named `Vin` at the top of the file. Set `Vin` to 1mV with $R_{\text{REF}} = 10\,\text{k}\Omega$ and run the simulation. Note the output peak-to-peak amplitude `Vopp` (this is measured using the `meas` command and reported to the console in NGSpice). Does the transient output waveform appear distorted? To measure the actual distortion, record the height (in dB) of the fundamental lobe in the FFT spectrum, and also the height of the first harmonic.

Exercise 6. Repeat Ex. 5 with `Vin` set to 10mV. Again, note the output peak-to-peak amplitude and describe any evidence of distortion. Record the heights of the fundamental and first harmonic lobes. How do these results compare with Ex. 5?

Exercise 7. In order to support feedback configurations, you will now add a second common-source stage to the OTA. Modify the `OTA.sp` file so that it implements the simple two-stage op amp design shown in Fig. 2, with $R_D = 10\,\text{k}\Omega$, and save the modified file as `opamp.sp`. Keep the input and output node names the same, i.e. they should be named `nplus`, `nminus` and `nout`, respectively.

Exercise 8. Calculate the expected gain and output resistance of the new common-source stage. Assume that the DC value of V_Y is equal to the minum allowed value for the OTA's output swing.

Exercise 9. Consider the feedback circuit shown in Fig. 3. This circuit implements a standard inverting op amp configuration, with $R_2 = 10\,\text{k}\Omega$ and $R_1 = 1\,\text{k}\Omega$. Note that R_2 acts as a load on the common-source stage. Predict how this load will affect the op amp's open-loop gain. Finally, predict the expected closed-loop gain for the configuration shown in Fig. 3.

Exercise 10. Now open the file `ex10.sp` and examine its contents. This file implements the same kind of test as the one from Ex. 3, only this time it will implement the test circuit shown in Fig. 3. Run the file in NGSpice, and repeat the data analysis from Ex. 3. How do these results compare with your predictions from Ex. 9? How do they compare with the results from Ex. 3?

Exercise 11. The last test is located in `ex11.sp`. This test repeats the FFT analysis from Ex. 5, applied to the feedback test circuit. Run the simulation in NGSpice and record the value of `Vopp`, and the heights (in dB) of the fundamental and first harmonic lobes. Then, change the input amplitude to 100 mV and repeat the measurements. Your results should have approximately the same output amplitudes as the ones observed in Ex. 5 and Ex. 6. How does the distortion in the feedback circuit compare to the original open-loop circuit? Can you explain the difference?

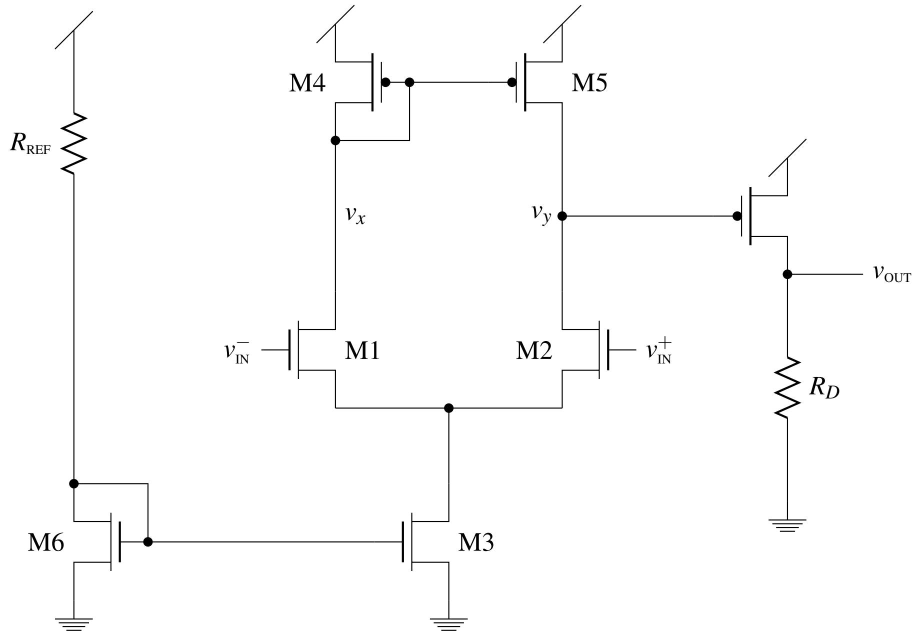

Figure 2: A simple two-stage op amp circuit. This circuit does not use a compensating capacitor because the bandwidth is already low enough to provide stable feedback behavior. Note that the differential input polarity is reversed because the common-source stage inverts the output signal.

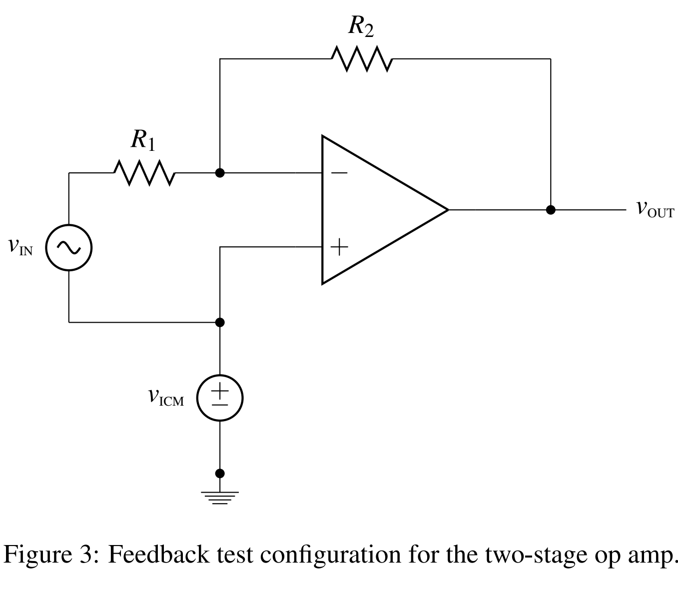

Figure 3: Feedback test configuration for the two-stage op amp.