Lab 1
Due 01/28/2014 1:30pm

Introduction to Design Data/Flow and CAD Tools

In this document we will introduce you to the CAD tools that we will be using for the design implementation of an example benchmark using ASIC design flow. The design implementation means taking an input design description (along with design constraints) provided by logic designers at a higher level of abstraction and refining it to the form that can actually be implemented into silicon. The input design functionality will be given in RTL form described in Verilog. The CAD tools used for the complete design flow will include Synopsys Design Compiler and Cadence SoC Encounter.

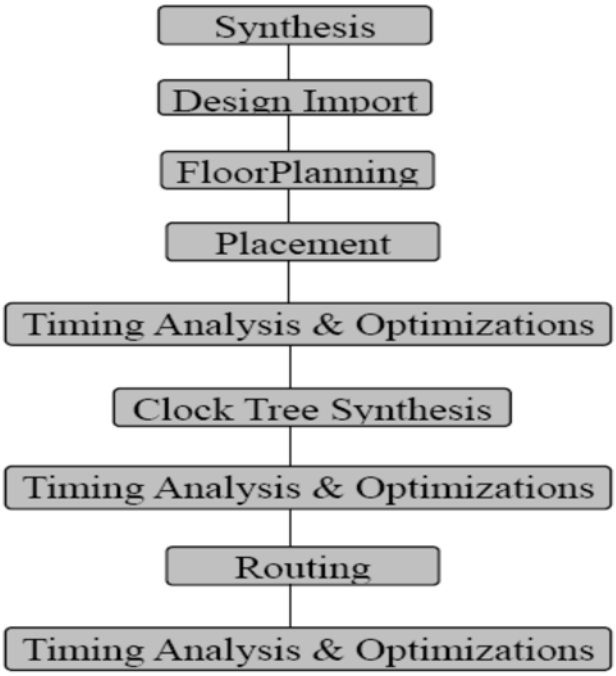
First the input design will be synthesized to a gate level netlist mapped using a general purpose standard cell library. This gate level netlist will then be placed and routed using Cadence SoC Encounter which is a "back-end" design tool. The timing closure and optimization flow will also be covered in the design implementation.

- **Setting up your run directory:**

1. Log on to a LINUX machine using your account.
2. Make a directory "5470_tutorial" at your choice of location and enter this directory.
   > mkdir 5470_tutorial
   > cd 5470_tutorial

- **Design Flow:**

Here is the design flow that we will cover over multiple sessions during this course.



In this design flow, we will do synthesis using Synopsys Design Compiler and the remaining flow steps will be performed inside Cadence SoC Encounter tool. The output of synthesis will be a gate-level mapped netlist that will be placed and routed later down in the flow.

- **The LINUX initial file (.bashrc)**

  - Each LINUX user has an initialization file in their home directory. This directory is called ***.bashrc***. It is hidden.
  - To open the file, first go to your home directory and then type: ***kedit .bashrc***
  - Your .bashrc file will look something like this:

```
# .bashrc

# User specific aliases and functions

# Source global definitions
if [ -f /etc/bashrc ]; then
    . /etc/bashrc
fi
```

  - Add the following at the bottom of the .bashrc file:

```
Export
LM_LICENSE_FILE=/opt/software/elicense.dat:/opt/software/qe
dlicense.dat

export
PATH=$PATH:/opt/software/mentor/modeltech/bin:/opt/software
/cadence/edi110/bin:/opt/software/synopsys/synthesis/bin:/o
pt/software/synopsys/coretools/bin:/opt/software/synopsys/h
spice/bin
export MODELSIM=/opt/software/mentor/modeltech/modelsim.ini
```

  - Save the file.
  - Make sure there are no line breaks in the PATH and LICENSE commands
  - Type the command: **source *.bashrc*** or restart the computer so that the new .bashrc will take into effect.

For this lab, you will make sure that you can run three tools: Synopsis Design Compiler, Synopsys Design Compiler GUI (Design Vision), and Cadence SoC Encounter Tool.

- **How to run Synopsys Design Compiler Tool**

Log on to a LINUX machine using your account. Then you can run Synopsys Design Compiler using the following command on command prompt.

- To start the Synopsys Design Compiler type: ***dc_shell***
- To exit the ***dc_shell*** type ***quit***

- **How to run Synopsys Design Compiler GUI (Design Vision)**

Log on to a LINUX machine using your account. Then you can run Synopsys Design Compiler GUI using the following command on command prompt.

- To start the Synopsys Design Compiler GUI from Linux prompt type: ***design_vision***

Or

- To start the GUI from dc_shell type ***gui_start*** in the dc_shell prompt.
- To stop the GUI type ***gui_stop*** in the dc_shell prompt.

- **How to run Cadence SoC Encounter Tool**

Currently Cadence SoC Encounter only runs on Linux Machines!

Log on to a Linux machine using your account.
You may run the tool using the following on the command prompt:
> encounter
It will run the tool in the GUI mode. You will also notice that encounter command prompt is accessible on the terminal. [Sometimes you may have to press 'enter' key after GUI pops up.]
The encounter command prompt will look like
encounter 1>
For using the tool itself, we will cover the details in the later section.

Things to turn in for this lab: Snapshots of Design Compiler, Design Vision, and Encounter