```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : s35932_bench
Version: H-2013.03-SP5-3
Date   : Sat Nov 21 16:44:36 2015
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: tt1p05v25c   Library: saed32rvt_tt1p05v25c
Wire Load Model Mode: enclosed

  Startpoint: TM0 (input port clocked by blif_clk_net)
  Endpoint: DATA_9_0 (output port clocked by blif_clk_net)
  Path Group: blif_clk_net
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  s35932_bench       35000                 saed32rvt_tt1p05v25c

  Point                                   Incr       Path
  --------------------------------------------------------------
  clock blif_clk_net (rise edge)          0.00       0.00
  clock network delay (ideal)             0.20       0.20
  input external delay                    1.00       1.20 r
  TM0 (in)                                0.00       1.20 r
  U9230/Y (INVX2)                         0.13       1.33 f
  U9487/Y (XNOR3X1)                       0.18       1.51 r
  U9526/Y (XNOR2X1)                       0.09       1.61 r
  DATA_9_0 (out)                          0.00       1.61 r
  data arrival time                                  1.61

  clock blif_clk_net (rise edge)          5.00       5.00
  clock network delay (ideal)             0.20       5.20
  clock uncertainty                      -0.30       4.90
  output external delay                  -1.00       3.90
  data required time                                 3.90
  --------------------------------------------------------------
  data required time                                 3.90
  data arrival time                                 -1.61
  --------------------------------------------------------------
  slack (MET)                                        2.29


1
```