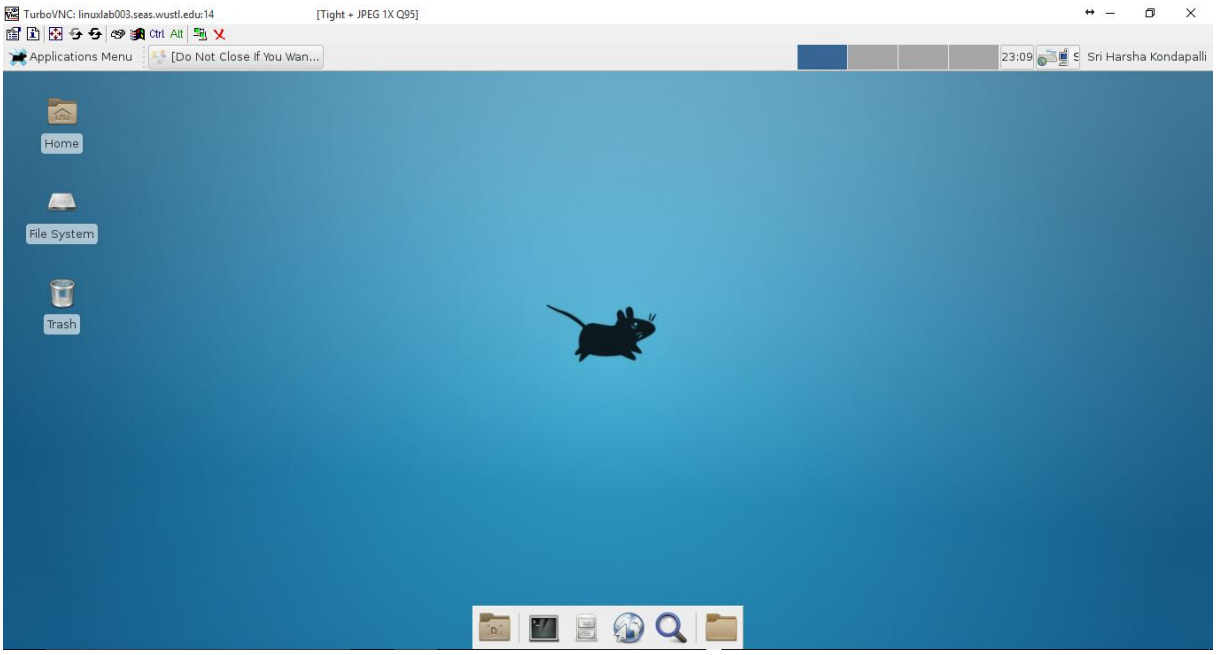
Tutorial for VCS

Note: Ignore the symbol "$" and type the italicized commands in the terminal

Once you login to your linux system.



STEP 1: Getting started with Verilog

Creating your model file –

- Create a new folder and start wring your Verilog script in a new file (.v file).
- Example code for modeling an Inverter is here.(https://wustl.box.com/Invertermodelcode)

Creating your Test Bench file –

- In addition to model code Test Bench script has to be given in order to verify the functionality of your model. (.v file)
- Example code of test bench for Inverter is here. (https://wustl.box.com/Invertertestbenchcode)

STEP 2: Setting up the environment for simulation

Download ".bashrc.cadence" file from http://aimlab.seas.wustl.edu/courses/.bashrc.cadence :

Note:

- Create an empty file in your home directory.
- Copy the content from above link
- Paste it to the empty file you created
- Rename the empty file to ".bashrc.cadence", once you rename, the file gets invisible don't mind.

STEP 3: Running your simulation

Running your files using vcs:

- Open Terminal (Default Directory will be Home)
- Type: $ *source .bashrc.cadence*
- Will see a message “Cadence environment loaded”
- Change to the directory (better if you have these files in a specific folder) where your model and test bench files(Inverter.v and Inverter_tb.v) are present by using this command: $ *cd /<path>/*
- Compile the files by typing $ *vcs <file>.v <file_tb>.v*
- This should generate an executable file named “simv” in the same folder where your codes are present
- Run this executable file $ *./simv*

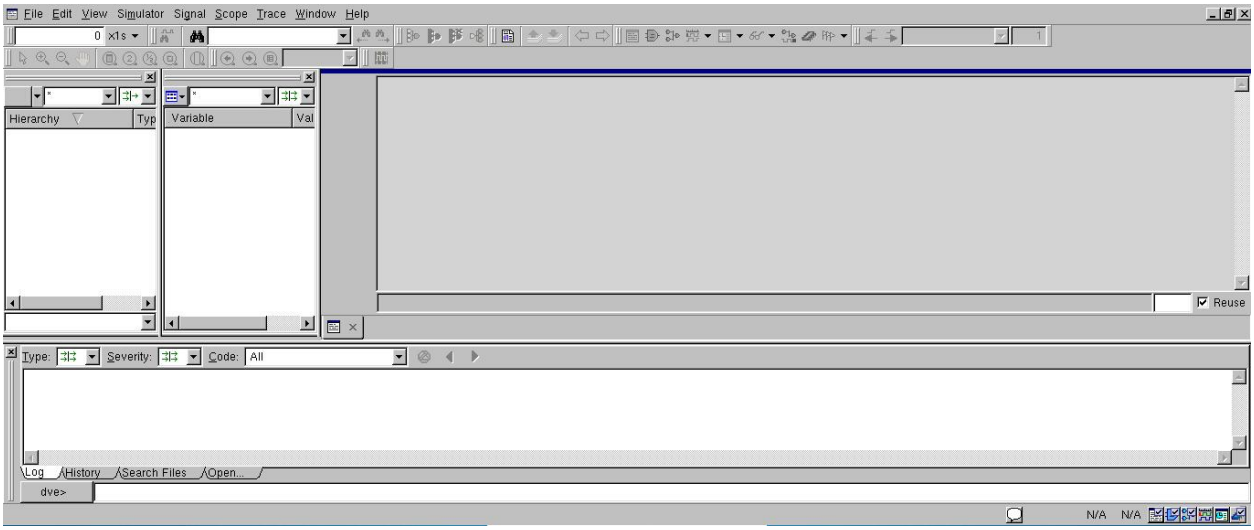
Example model and test bench codes are present in the following link

https://github.com/bangonkali/electronics/tree/master/verilog/adder

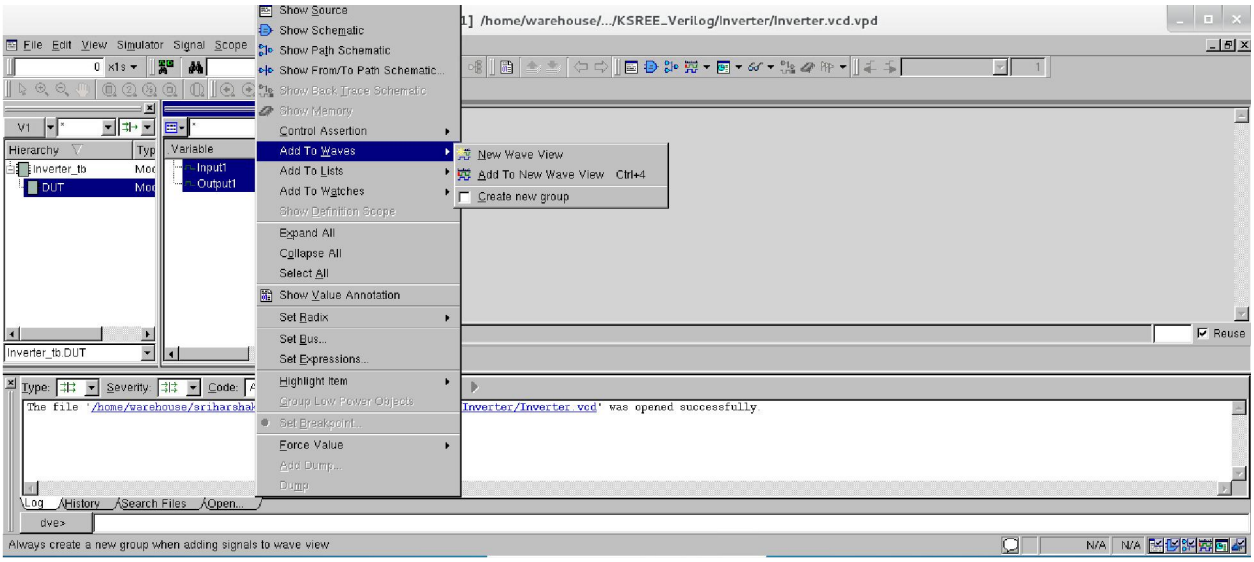
Reference for test bench syntax can be found here. (https://wustl.box.com/verilogtbref)

STEP 4: Displaying your Results

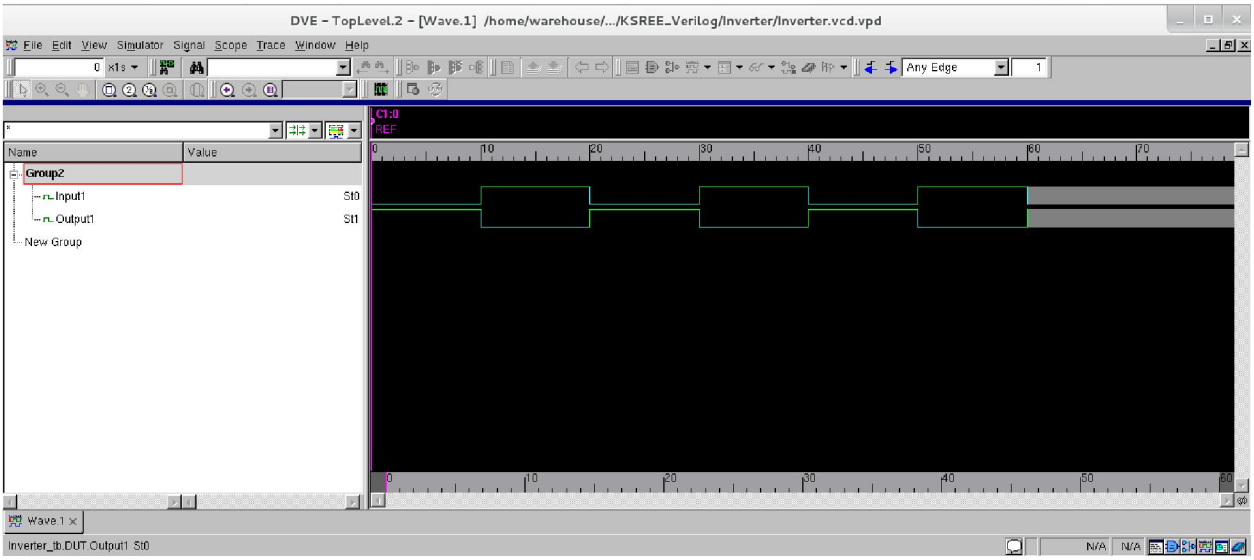
- Once you run the simulation, a file named “Inverter.vcd” is generated in the same folder.
- This is the dump file we specified in the testbench code.
- Now type the following command in the terminal $ *dve*



- This is a viewer to plot and verify your results
- Go to *File/Open Database* and select the “.vcd” file from the project folder
- You will find the name of your test banch model in the Hierarchy box (Inverter_tb). Expand it so that you can find DUT in the options.
- If you click on DUT and select the Input1 and Output1 and right click you will find an option “Add to Waves”.
- Click on “Add to New Wave View” to see the waveforms of your Inputs and Outputs.



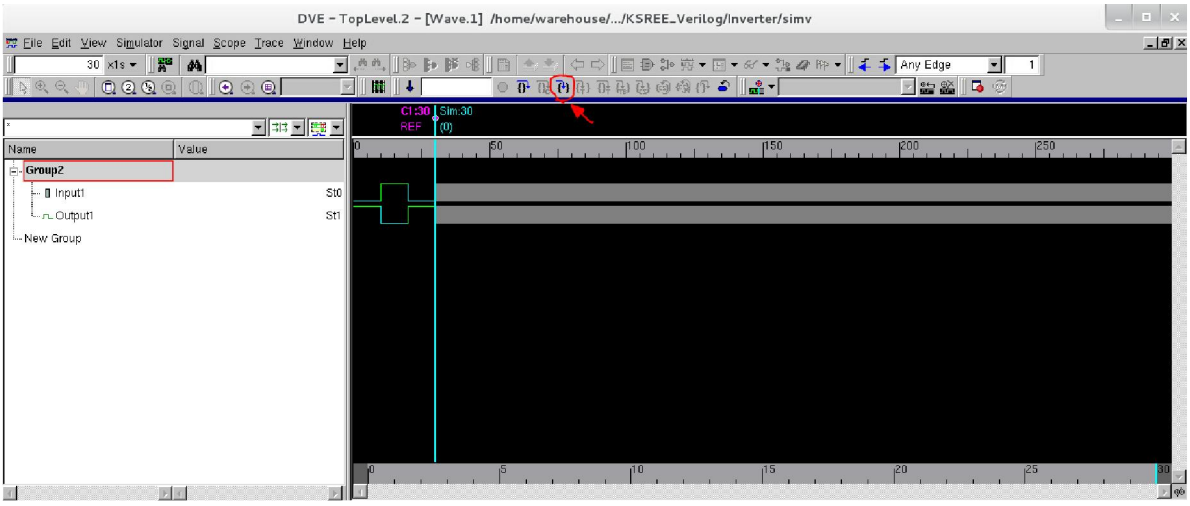
- You should see your results in a new window.



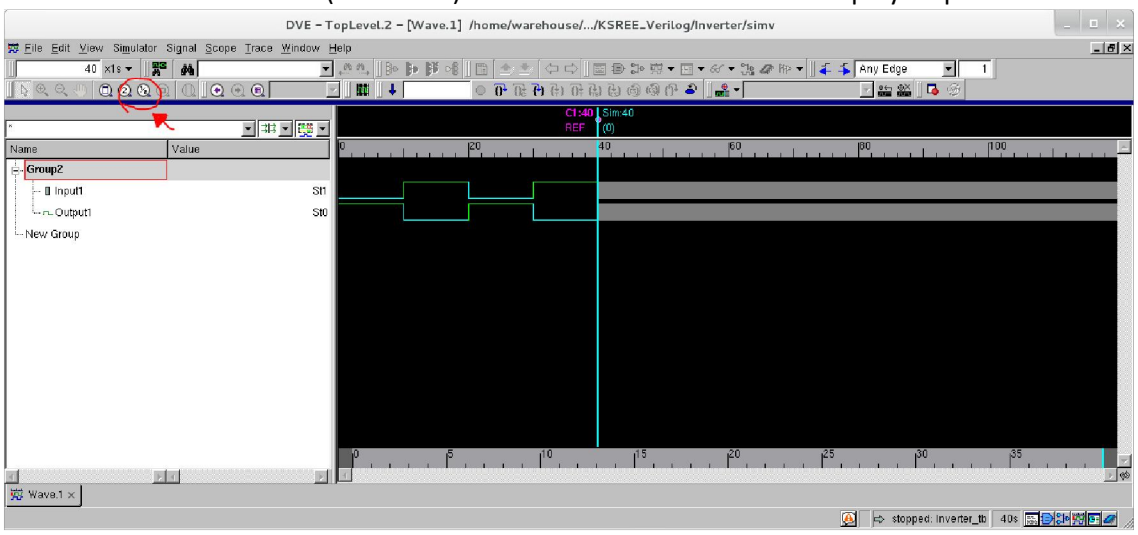
- Explore other options aswell.

Additional Option to run in Debug mode:

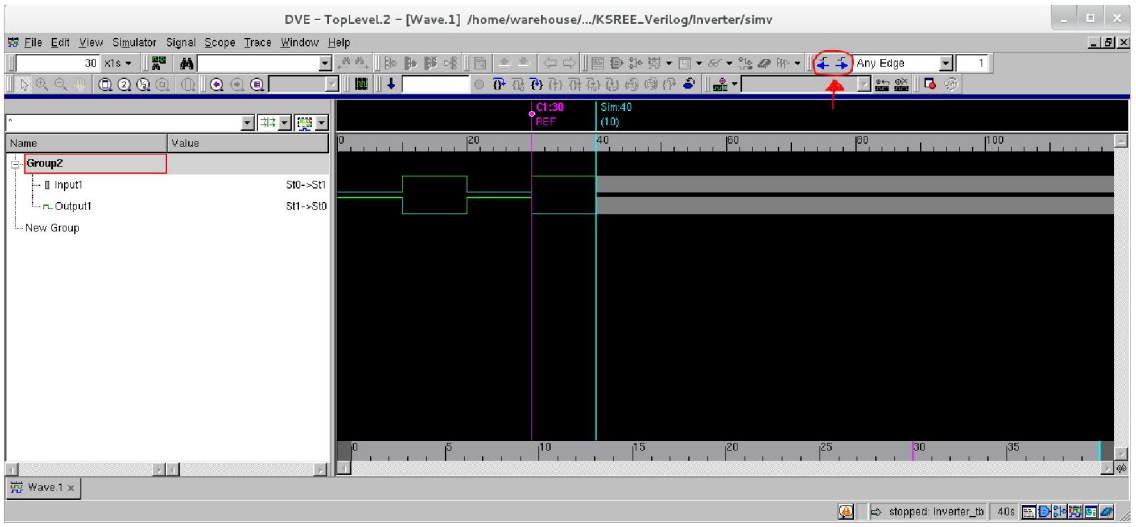
- Instead of compiling the files directly as before, we can enable a debug flag during compilation by using following command $ *vcs -lca –debug_access+all Inverter.v Inverter_tb.v*
- Now run the code $ ./simv -gui &
- This should open the dve tool automatically and you can debug your test bench step by step.
- To do this first select Input1 and Output1 from variable window and right click “Add to the Waves” as before this should open the following window as shown in the figure.
- Then start pressing the blue arrow tool button pointed in the image below to run your test bench step by step. Other tool options are also available just explore them.



Tool button (red arrow) is used to run the test bench step by step



Tool button (red arrow) is used to zoom in and zoom out



Tool button (red arrow) is used to move between step cycles front and back