ECE XX/XX (TBD) Syllabus

VLSI Testing and Verification

1. **Description**: The physical challenges incurred by the rapidly shrinking feature size and reduced power supply voltage of deep sub-micron semiconductor fabrication technologies continue to give rise to various design robustness concerns. Due to the trend of increasing test costs, and the fact that test costs have started to dominate the overall production costs, low-cost testing techniques and design-for-testability strategies have gained wide attention. This course aims to educate the students to understand the fundamentals of Very Large-Scale Integration (VLSI) testing strategies, importance of "test, diagnosis, and reliability", modeling and analysis of faults, testing "processes, methods, tools, and equipment", design-for-testability techniques that are currently used in high-technology industries. The objective is realized through hands-on discussion sections as well as theoretical, computer-aided, and programming assignments for students to apply their learned principles and gained skills in real applications. In overall, the course helps to gain the required knowledge and skills for testing of a given circuit using the most effective theories, techniques, and software.

2. **Number of Credits**: Three.

3. **Instructor**: Dr. Shayan (Sean) Taheri.

4. **Instructor University Role**: TBD in the Department of Electrical and Computer Engineering at the Gannon University.

5. **Office**: TBD.

6. **Phone**: TBD.

7. **Email**: TBD.

8. **Lecture and Laboratory Date and Time**: TBD.

9. **Lecture Location**: TBD.

10. **Laboratory Location**: TBD.

11. **Office Hours**: TBD (or by appointment).

12. **Teacher Assistant(s)**: TBD.

13. **Prerequisites**: Familiarity with digital circuit design and hardware description languages. Knowledge of C/C++ programming languages, algorithms, and data structures.

14. **Textbook**: Bushnell, M. and Agrawal, V., 2004. ***Essentials of electronic testing for digital, memory and mixed-signal VLSI circuits*** (Vol. 17). Springer Science & Business Media.

15. **Class Requirements**: Please bring a paper notebook or a laptop to your lectures for taking notes as well as working on short in-class exercises.

16. **References (Optional)**:

A. Jha, N.K. and Gupta, S., 2003. ***Testing of digital systems***. Cambridge University Press.

B. Abramovici, M., Breuer, M.A. and Friedman, A.D., 1990. ***Digital systems testing and testable design*** (Vol. 2, pp. 1015-1028). New York: Computer science press.

C. Wang, L.T., Wu, C.W. and Wen, X., 2006. ***VLSI test principles and architectures: design for testability***. Elsevier.

D. Lala, P.K., 1997. ***Digital circuit testing and testability***. Academic press.

E. Fujiwara, H., 1985. ***Logic testing and design for testability*** (pp. 57-58). Cambridge, MA: MIT press.

F. Crouch, A.L., 1999. ***Design-for-test for Digital IC's and Embedded Core Systems***. The Rosen Publishing Group.

G. Selected material from recent publications.

17. **Learning Objectives**: By the end of the course, you should be able to do the following functions:

A. Investigate failure mechanisms and reliability issues of VLSI circuits and characterize failures at various levels of circuit hierarchy.

B. Utilize logic and fault simulation to develop test vector generation algorithms for combinational and sequential circuits.

C. Design and develop testing methodologies for digital, analog, and mixed-signal chips.

D. Coordinate different testing tasks (such as combinational testing, sequential testing, memory testing, built-in-self-test, and scan testing) so that a chip is tested as a whole entity.

E. Utilize data structures and theoretical knowledge about algorithms in C++ programs that are used to implement testing software tools.

F. Utilize Very High-Speed Integrated Circuit Hardware Description Language (VHDL) and Verilog Hardware Description Language (HDL) to specify digital circuit structure and behavior to be implemented on Field-Programmable Gate Array (FPGA) development boards for testing.

G. Conduct literature survey on specific and demanding research topics in VLSI testing, identify current challenges, and develop solutions.

H. Prepare informative and organized project reports and presentations that describe the methodologies employed, the performance parameters used, the results obtained, and the conclusions made in simulation experiments.

18. **Course Webpage**: "TBD" (in "**https://my.gannon.edu**").

19. **Assignments**: The assignments are provided (approximately) on a biweekly basis to improve the learning process. A number of assignments involve computer-aided tools and/or programming.

20. **Computer Usage**: This course involves sufficient utilization of computer-aided tools from Cadence/Synopsys software companies (e.g., Synopsys TetraMAX) and/or programming in C/C++ languages.

21. **Exams and Quizzes**: There are a midterm and a final exam for overall evaluations. Unannounced quizzes may be considered for certain assessments. Access to books and/or notes along with simple calculators "might" be allowed.

22. **Grading Policy**: The following weights are used:

A. Assignments: 45%.

B. Midterm Exam: 25%.

C. Final Exam: 25%.

D. Lecture Class Participation: 5%. Laboratory Class Participation is "Mandatory".

Grading is based on a conventional fixed scale, and grades are "**A**": 90-100%; "**A-**": 85-89%; "**B+**": 80-84%; "**B**": 70-79%; "**B-**": 65-69%; "**C+**": 60-64%; "**C**": 55-59%; "**C-**": 50-54%; "**D+**": 47-49%; "**D**": 44-46%; "**D-**": 40-43%; and "**F**": 0-39%.

The instructor reserves the right to curve up the final scores.

23. **Late Policy**: Late submissions are not accepted without prior approval by the instructor.

24. **Disabilities**: In cooperation with the designated centers, reasonable accommodation is provided for qualified students with disabilities. Please meet with the instructor during the first week of semester to discuss possible arrangements.

25. **Cheating and Plagiarism**: Cheating and plagiarism are not permitted in any form and cause certain penalties. The instructor reserves the right to fail culprits.

26. **Course Outline**: The following topics are covered with certain variations:

A. ***Introduction***: Testing Philosophy, Role of Testing, Digital and Analog Circuits, Digital and Analog VLSI Testing, and Testing-Based VLSI Technologies.

B. ***VLSI Testing Process and Test Equipment***: Testing Chips, Automatic Test Equipment, and Electrical Parametric Testing.

C. ***Test Economics and Product Quality***: Test Economics, Yield, and Defect Level for Quality Measure.

D. ***Fault Modeling***: "Defects, Errors, and Faults", Functional Versus Structural Testing, Fault Models, and Single Stuck-at-Fault.

E. ***Logic and Fault Simulation***: Simulation for Design Verification, Simulation for Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-Value Simulation, Algorithms for Fault Simulation, and Statistical Methods for Fault Simulation.

F. ***Testability Measures***: Sandia Controllability/Observability Analysis Program (SCOAP), Controllability and Observability, and High-Level Testability Measures.

G. ***Combinational Circuit Test Generation***: Algorithms and Representations, Redundancy Identification (RID), Global Testing Problem, Significant Combination Automatic Test-Pattern Generator (ATPG) Algorithms, Test Generation Systems, and Test Compaction.

H. ***Sequential Circuit Test Generation***: ATPG for Single-Clock Synchronous Circuits, Time-Frame Expansion Method, and Simulation-Based Sequential Circuit ATPG.

I. ***Memory Test***: Memory Density and Defect Trends, Memory Faults, Memory Test Levels, March Test Notation, Fault Modeling, and Memory Testing.

J. ***Digital Signal Processing (DSP)-Based Mixed Signal Test***: Mixed-Signal Circuit Trends, Functional DSP-Based Testing, Static Analog to Digital Converter (ADC) and Digital to Analog (DAC) Testing Methods, Realizing Emulated Instruments, Compression/Decompression (CODEC) Testing, and Dynamic Flash ADC Testing Fast Fourier Transform (FFT) Technique.

K. ***Model-Based Mixed-Signal Test***: Testing Challenges, Fault Models, Abstraction Levels, Types of Testing, Fault Simulation, and ATPG.

L. ***Delay Test***: Test Problem, Path-Delay Test, Transition Faults, Delay Test Methodologies, and Practical Considerations.

M. ***Direct Drain Quiescent Current (IDDQ) Test***: Motivation, Detected Faults, Testing Methods, Testing Effectiveness, Limitations, Delta IDDQ Testing, IDDQ Built-In Current Testing, and IDDQ Design for Testability.

N. ***Digital Design for Testability (DFT) and Scan Design***: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, and Variations of Scan.

O. ***Built-In-Self-Test (BIST)***: Economic Case, Random Logic BIST, Memory BIST, and Delay Fault BIST.

P. ***Boundary Scan Standard***: Motivation, System Configuration with Boundary Scan, and Boundary Scan Description Language.

Q. ***Analog Test Bus Standard***: Analog Circuit Design for Testability and Analog Test Bus (ATB).

R. ***System Test and Core-Based Design***: System Test Problem, Functional Test, Diagnostic Test, Testable System Design, Core-Based Design and Test-Wrapper, System-on-a-Chip (SoC) Test Architecture, and Integrated Design and Test Approach.

S. ***The Future of Testing***.

Meanwhile, all the mentioned topics along with more complementary and advanced subjects will be covered if time permits.