Department of Electrical and Computer Engineering
Utah State University

ECE 5930/6930: VLSI Testing and Verification

Created By: Shayan (Sean) Taheri

Homework 03

Assigned Date: Month/Day/Year

Due Date: Month/Day/Year

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1. D-Algorithm. Use Roth's D-Algorithm to perform ATPG for the stuck-at-1 fault on the fan-out branch **h** on the circuit shown in Figure 1.

Note: For more information about this circuit, refer to the following paper:

P.R. Schneider, "On the Necessity to Examine D-Chains in Diagnostic Test Generation".

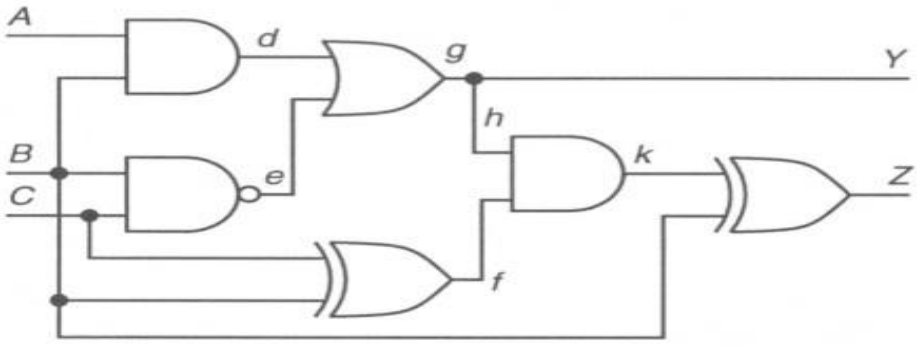

Figure 1

2. PODEM. Perform ATPG for the fault line **h** (stuck-at-1) on the circuit shown in Figure 1 using PODEM and SCOAP measures.

3. D-Algorithm. Perform ATPG on the circuit shown in Figure 2, using D-Algorithm to test the fault **h1** (stuck-at-1).

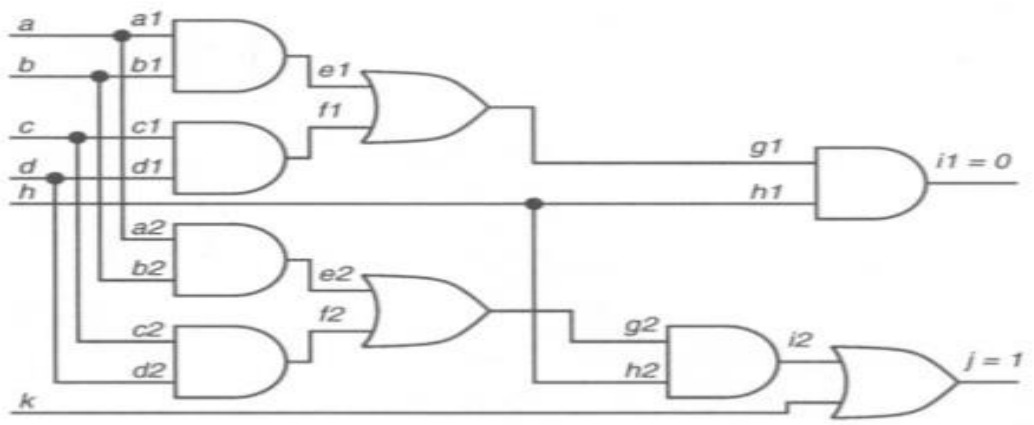

Figure 2

You can prepare a table like the one below while preparing your answer to this problem.

Step	Action	Impl. stack	Forward implications	*D*-frontier
Test found: $(a, b, c, d, h, k) = (,,,,,);\ i1 =$				

Table 1

4. PODEM. Generate a test with the PODEM ATPG algorithm for the fault **g** (stuck-at-1) on the circuit shown in Figure 3. While you are performing the PODEM algorithm, follow the rules given below.

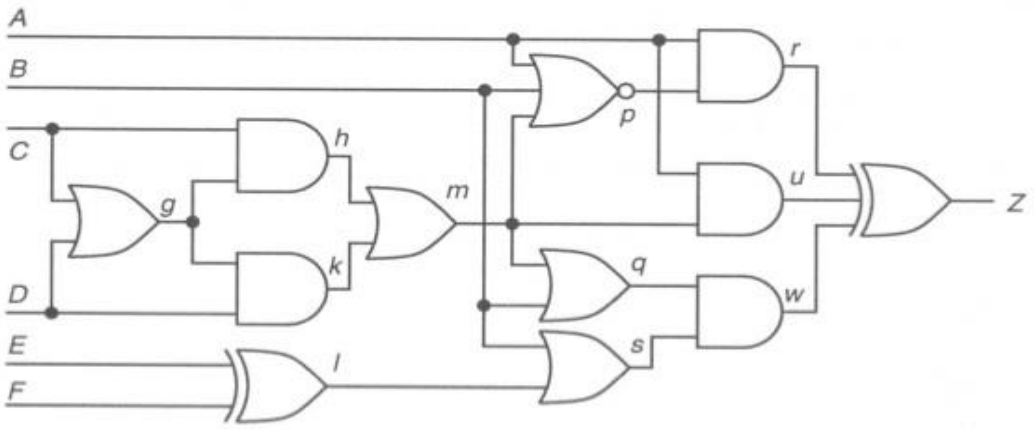

Figure 3

The Given Rules:

1) **Order**: First, try to excite the fault and then propagate.
2) **Back-trace**: Follow a path from the objective to a primary input while always following the alphabetical order (e.g. if a gate has input A and B, back-trace on that gate goes to line A first).
3) **PI assignment**: Always assign 0 first, then assign 1 in case of backtrack.
4) **Choice of D or $\overline{D}$**: Always try to propagate a D or $\overline{D}$ from the D-frontier that has the shortest path to the primary output. In the case of tie, follow the alphabetical order.

You can prepare a table like the one below while preparing your answer to this problem.

Step No.	Objec-tive	Action	Imp. stack	Implied signal values *ABCDEFghklmpqsruwZ*	*D* front.	*X* path
test is ; *number of backtracks:*						

Table 2