UtahStateUniversity

# Department of Electrical and Computer Engineering
# Utah State University

## ECE 5930/6930: VLSI Testing and Verification

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**Homework 01**

Solution Outline

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### Answer 1.

Use the following convention for this problem:

1. PQ: Chip is good.
2. P: Chip passes the test.
3. FQ: Chip is bad.
4. F: Chip fails the test.

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An 80% good device production means:

$$\text{Probability (PQ)} = 0.80 \text{ and Probability (FQ)} = 0.20$$

Similarly, from the given data, we can see that:

$$\text{Probability (P/PQ)} = 0.95 \text{ and Probability (P/FQ)} = 0.05$$

We have to calculate the probability of passing [Probability (P)] i.e. the yield.

$$\text{Probability (P)} = [\text{Probability (P/PQ)} \times \text{Probability (PQ)}] + [\text{Probability (P/FQ)} \times \text{Probability (FQ)}] =$$

$$= (0.95 \times 0.80) + (0.05 \times 0.20) = 0.77$$

Similarly, using the definitions given in the problem, Yield Loss:

$$(0.8 \times 0.05) / 0.77 = 0.051948$$

And Defect Level:

$$(0.2 \times 0.05) / 0.77 = 0.01298$$

Often expressed in parts per million which is 12980 ppm.

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## Answer 2.

Assuming that one vector is applied per clock cycle during the digital test, the rate of test application is 200 million vectors per second. Therefore,

$$\text{Digital Test Time} = (1000 \times 10 \text{ ^ } 6) / (200 \times 10 \text{ ^ } 6) = 5 \text{ seconds}$$

Adding the analog test time, we get

$$\text{Total Test Time} = 1.5 + 5.0 = 6.5 \text{ seconds}$$

The testing cost for a 500 MHz, 1,024 pins tester was obtained as 4.5 cents in Example 1.2 (see page 11 of the book.). Thus,

$$\text{Cost of Testing a Chip} = 6.5 \times 4.5 = 29.25 \text{ cents}$$

The cost of testing bad chips should also be recovered from the price of good chips. Since the yield of good chips is 70%, we obtain

$$\text{Test cost in the price of a chip} = 29.25 / 0.7 = 41.8 \text{ cents}$$

Hence, 41.8 cents should be included as the cost of testing while figuring out the price of chips.

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## Answer 3.

For the circuit of Figure 1, we have

$$\text{Number of fault sites} = \text{PIs} + \text{gates} + \text{fan-out branches} = 14$$

Therefore,

$$\text{Number of single faults} = 14 \times 2 = 28$$

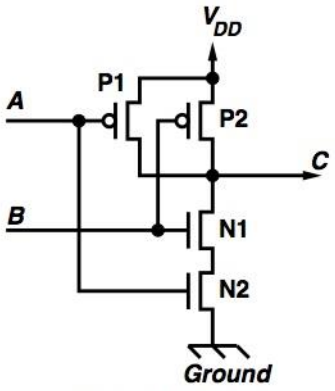
$$\text{Number of single and multiple faults} = 3^{\text{number of fault sites}} - 1 = 3^{14} - 1 = 4782968$$

The circuit has 4,782,968 single and multiple stuck-at faults.

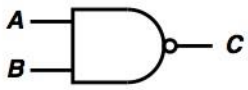
$$\text{Total number of transistors} = 26$$

Therefore the circuit has 26 stuck-open faults.

## Answer 4.




CMOS NAND gate.




Logic NAND gate.

**(a)** The following table gives tests for transistor **stuck-open (sop)** faults:

| Test No. | Fault | Test: Vector 1, Vector 2 |
|---|---|---|
| 1 | P1 sop | 11, 01 |
| 2 | P2 sop | 11, 10 |
| 3 | N1 sop | 01, 11 or 10, 11 or 00, 11 |
| 4 | N2 sop | 01, 11 or 10, 11 or 00, 11 |

Notice that the sop faults of N1 and N2 have exactly the same tests. These two faults are equivalent.

**(b)** The following sequence of four vectors contains one vector pair for each fault in the above table:

$$11, 01, 11, 10$$

Notice that this sequence also detects all single stuck-at faults in the logic model of the NAND gate.

Notice: **stuck-short (ssh)**

**(c)** A stuck-at fault in a signal affects two transistors in the two-input NAND gate. For example, the fault A (stuck-at-1) will mean that N1 remains permanently shorted (N1-ssh) and P1 remains permanently open (P1-sop). The following table gives all equivalences:

| Stuck-at fault | Equivalent transistor faults |
|---|---|
| $A$ s-a-1 | N2-ssh **and** P1-sop |
| $B$ s-a-1 | N1-ssh **and** P2-sop |
| $C$ s-a-1 | (P1 **or** P2 **or** both ssh ) **and** (N1 **or** N2 **or** both sop) |
| $A$ s-a-0 | N2-sop **and** P1-ssh |
| $B$ s-a-0 | N1-sop **and** P2-ssh |
| $C$ s-a-0 | N1-ssh **and** N2-ssh **and** P1-sop **and** P2-sop |

Notice that the three equivalent faults, A (stuck-at-0), B (stuck-at-0) and C (stuck-at-0), are actually caused by different faulty transistors. They are detected by the same test (11).

## Answer 5.

Show that the two faults **c** (stuck-at-0) and **f** (stuck-at-1) are equivalent in the circuit of Figure 2.

Faulty functions for the circuit for this problem corresponding to the two faults are:

$$\begin{aligned} m(c\ s-a-0) &= \bar{b}+ab = a+\bar{b} \\ n(c\ s-a-0) &= (\bar{b}+ab)\bar{j} = (a+\bar{b})\bar{j} \end{aligned}$$

$$\begin{aligned} m(f\ s-a-1) &= a+\overline{a+b} = a+\bar{a}\bar{b} = a+\bar{b} \\ n(f\ s-a-1) &= (a+\overline{a+b})\bar{j} = (a+\bar{a}\bar{b})\bar{j} = (a+\bar{b})\bar{j} \end{aligned}$$

The two faulty functions are indistinguishable and hence the two faults are equivalent.