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Creating Test Patterns for Combinational Logic circuits using Synopsys TetraMAX :

1. After a successful synthesis, the "*.tcl" script that you used in design vision, will have produced a synthesized version of your circuit under the "src" directory, verify this file exists before beginning this section. You should see a file called: "***.v" under the src directory. if you do not see this file, your synthesis is incomplete.

2. Start the synopses TetraMAX GUI by typing: tmax &

3. Once the GUI opens, notice that you are in the "BUILD" mode. TetraMAX has 3 modes:
BUILD, DRC, and TEST
You cannot go from BUILD to TEST, you must go in the BUILD -> DRC -> TEST order.

4. Load the Library

5. Load you synthesized circuit

6. BUILD,

7. DRC (Design Rule Check): It is checking to see if your design is in fact valid "Testable" code.

8. Generate the Test Patterns for the circuit:

a. Running "ATGP" : It stands for "automatic test pattern generation"
b. Inserting the "add all faults"
c. Checking the "stuck" at fault model
d. Basic scanning
e. Read the generated report

9. Click on the "Schematic View" icon at the top of the screen. Then, click on the "Show" icon that appears in the schematic view window, scroll down and select: "ALL"
Next, click on the "Setup" :
a. Set the Pin Data Type to: "PATTERN"
b. Set the Pattern No. to: "0", click OK
c. Click on the "Zoom Full" button and see the schematic
Note: You will see a schematic of your circuit with Pattern#0 (of all the patterns), showing you what input is at the input PINS and what "good-non-faulted" data should be at the output PINS. You can change the "Setup" to show the other patterns and their expected data

10. View the results of a possible stuck-at-fault:
a. Click on "Setup" button again

b. Set the Pin Data Type to: "Fault Sim Results" and then click OK
Note: You can also determine "stuck-at" fault and the number of patterns.

11. Write out the test patterns to a verily file
a. Click on the "Write Pat." button on the top of the TetraMAX window
b. For the Pattern File Name type: ./src/***_tb_patterns.v
c. For the File Format, select: Verilog-Single File
d. Press OK

12. Test the patterns out against your synthesized circuit
a. Close TetraMAX
b. In "src" folder, type:
sim-nc ***(Library Name).v ***(Test Bench Patterns).v ***(Synthesized Circuit).v
Note: Since your verily has no manufacturing defects, you will always get 0 errors. The idea is to use these patterns against a chip that you some day fabricate, and see if you still get 0 errors.

13. Viewing the patterns in SimVision
a. Open up an editor (like gedit) and edit the file: ***(Test Bench Patterns).v
b.Go to the very bottom of the code and right before the "end module" statement, add the following lines of verilog:

```
initial begin
        $shm_open ("***.db (The ATGP File)");
        $shm_probe ("AS");
end
```

c. This code makes it so the TetraMAX test bench will generate Simvision waveforms
d. Once you have saved the file, type the following:
sim-nc ***(Library Name).v ***(Test Bench Patterns).v ***(Synthesized Circuit).v
e. After the run, open up Simvision and view the waveforms in the "shm_atgp.db" directory
f. Send the waveforms from the "DUT" sub-module to the waveform viewer