Department of Electrical and Computer Engineering
Utah State University

ECE 5930/6930: VLSI Testing and Verification

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Homework 02

Assigned Date: Month/Day/Year

Due Date: Month/Day/Year

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1. Using TetraMAX tool:

1) Draw each of the attached circuits (circuit-1.v and circuit-2.v).

2) Using your circuit drawn for "circuit-1", simulate the following four vectors and specify the output of each vector.

PI	1	2	3	4	5
V1	1	0	0	0	0
V2	X	0	0	0	0
V3	0	1	0	X	X
V4	1	0	X	0	1

Note: Refer to "TetraMAX and Simulation" tutorial.

2. For this problem, you should use the circuit shown in Figure 1.

A) The Table 1 gives a fault list for the circuit, after equivalence fault collapsing. Fill in the blanks with equivalent fault sets for each listed fault.

B) Assume that you are applying exhaustive test set for the circuit. In the Table 2, mark all the faults

that are detected by each vector. Note that only the collapsed faults are listed in Table 2. For this problem you should use TetraMAX tool.

Note: Refer to “Analyzing Faulty Signals in Digital Circuits using TetraMAX” tutorial.

Important Hints (TetraMAX tool):

1) Insert only one test pattern (of the 16 test patterns) in the generated STIL file.

2) Use the following command to get the fault report of the test pattern:

```
>> report_faults -all
```

3) Eliminate the test pattern from STIL file and insert another test pattern to get the fault report of the new inserted test pattern.

4) Fill up the table using the produced fault reports.

Remember: You should have only one test pattern (e.g. pattern 0) in your STIL file, because if you insert more test patterns in the STIL file, the tool will choose the minimal set of those patterns.

Note: In the report that you will get, only those faults can be considered as detected (by the inserted test pattern) that belong to "DT" fault class.

DT - Detected fault class:

- DS = Detected by Simulation
- DI = Detected by Implication
- DR = Robustly Detected Delay Fault

C) From the cover table of (B),

1. Find minimum number of vectors that detect all detectable faults.

2. List a minimum test set.

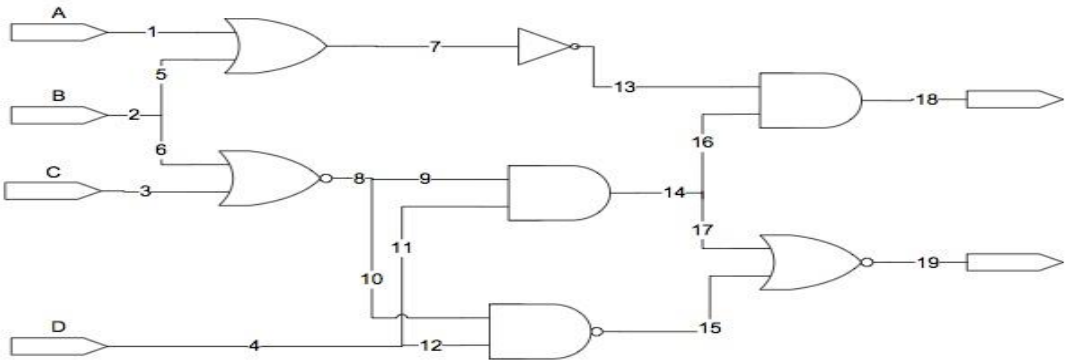

Figure 1

Fault	List all equivalent Faults
1/0	Ø
1/1	
2/0	
2/1	
5/0	
6/0	
6/1	
3/0	
4/0	
4/1	
7/0	13/1
8/1	
9/0	
9/1	
10/0	
10/1	
11/1	
12/1	
14/1	
15/0	
16/1	
17/0	
18/1	
19/1	

Table 1

1 2 3 4	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
1/0																
1/1																
2/0																
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11/1																
12/1																
14/1																
15/0																
16/1																
17/0																
18/1																
19/1																

Table 2

3. Equivalent and Dominance Fault Collapsing.

For the circuit of Figure 2,

A) What is the number of all potential fault sites?

B) Derive the equivalence collapsed set. What is the collapsed ratio?

C) Derive the dominance collapsed set. What is the collapsed ratio?

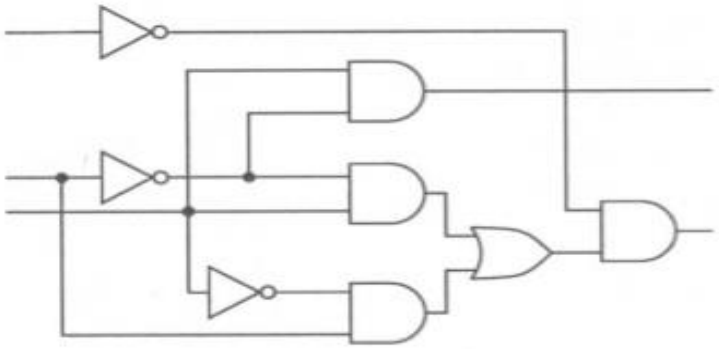

Figure 2

4. Dominance Fault Collapsing. For the circuit of Figure 3,

A) Enumerate the minimal set of single stuck-at faults that must be tested according to the Checkpoint theorem.

Note 1: Checkpoints = Primary inputs and fan-out branches of a combinational circuit consisting only of “Primitive Boolean” Gates are called checkpoints.

Note 2: Refer to Figure 4.9 in the textbook for more information (Equivalent of XOR Gate in “Primitive Boolean” Gates).

B) Show that the two faults **d** (stuck-at-0) and **g** (stuck-at-1) are equivalent.

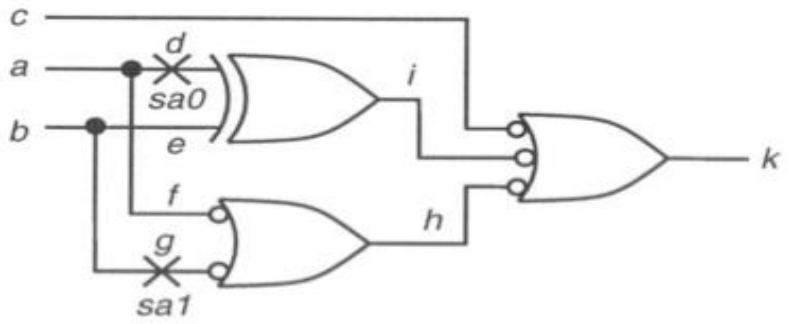

Figure 3

5. Fault Sampling. Determine the sample size for fault simulation to achieve $\pm$2% accuracy in the coverage estimate when the actual coverage is known to be above 70%.

Note: Read section 5.6.1 in the textbook.

6. For the circuit shown in the Figure 4 and Figure 5, perform:

A) Parallel pattern single fault simulation targeting the fault **h** (stuck-at-1). You are given 4 vectors to simulate and the vectors are encoded as 11 for **1**, 00 for **0** and 01 for **X**.

B) Parallel fault simulation for the vector **abc** = 110 and three faults, **d** (stuck-at-0), **h** (stuck-at-0) and **n** (stuck-at-1), to determine which faults will be detected at the primary output.

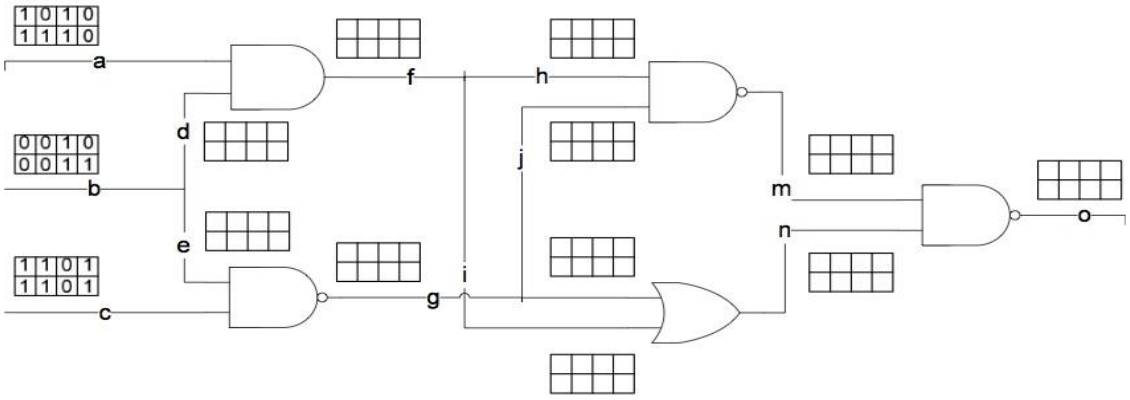

Figure 4

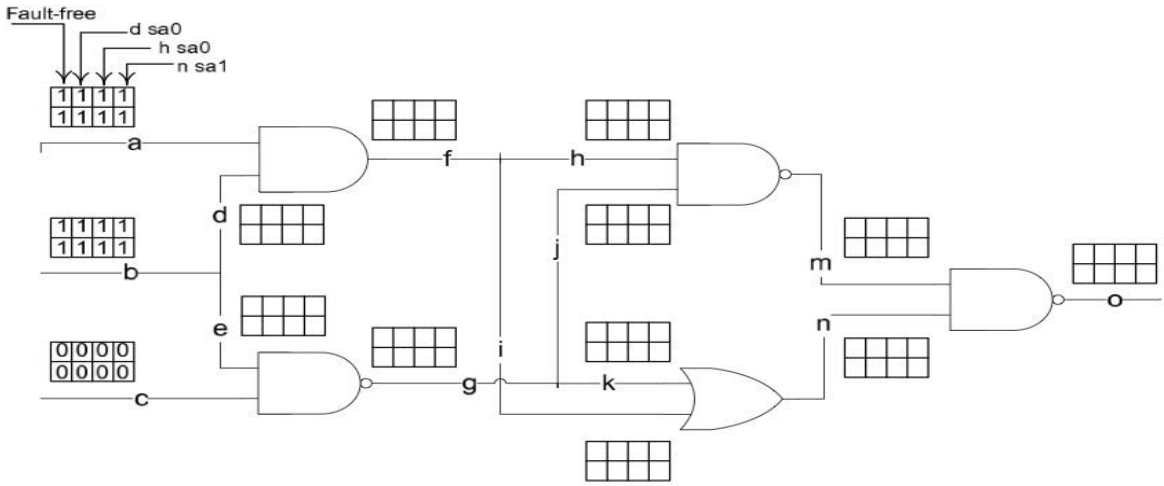

Figure 5

7. For the same circuit as Problem 6, perform deductive fault simulation to determine what faults will be detected at the primary output **'o'** for the test vector **abc** = 101.