Department of Electrical and Computer Engineering
Utah State University

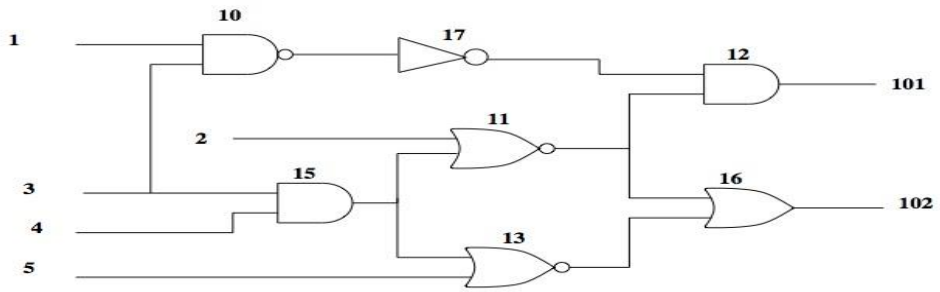
ECE 5930/6930: VLSI Testing and Verification
Created By: Shayan (Sean) Taheri

Homework 02
Solution Outline

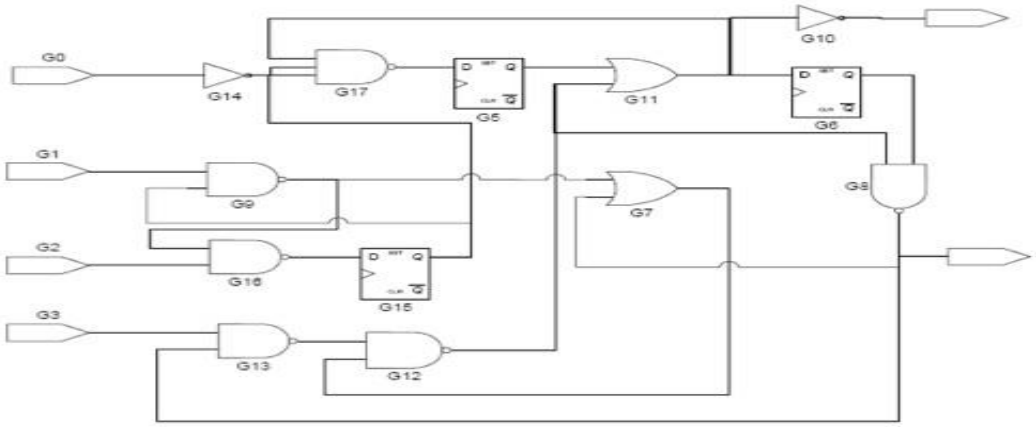
Answer 1.

See figures drawn for the two circuits:

PI	(1	2	3	4	5)	PO	(101	102)
V1	1	0	0	0	0		0	1
V2	X	0	0	0	0		0	1
V3	0	1	0	X	X		0	X
V4	1	0	X	0	1		X	1



Circuit 1



Circuit 2

Answer 2.

A) The completed table for equivalence faults is:

Fault	List all equivalent Faults
1/0	Ø
1/1	7/1 , 5/1, 13/0, 16/0, 18/0
2/0	Ø
2/1	Ø
5/0	Ø
6/0	Ø
6/1	3/1, 8/0
3/0	Ø
4/0	Ø
4/1	Ø
7/0	13/1
8/1	Ø
9/0	11/0, 14/0
9/1	Ø
10/0	12/0,15/1,17/1,19/0
10/1	Ø
11/1	Ø
12/1	Ø
14/1	Ø
15/0	Ø
16/1	Ø
17/0	Ø
18/1	Ø
19/1	Ø

Table 1

B) The completed table of part “B” is given below. Note that only the collapsed faults are listed in Table 2.

1 2 3 4	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
1/0										v						
1/1		v														
2/0						v										
2/1		v														
5/0																
6/0																
6/1		v	v													
3/0				v												
4/0		v														
4/1	v															
7/0										v						
8/1				v												
9/0		v								v						
9/1				v												
10/0																
10/1				v		v		v				v	v	v		v
11/1	v															
12/1	v															
14/1	v	v	v	v												
15/0	v		v	v	v	v	v	v	v		v	v	v	v	v	v
16/1	v		v	v												
17/0		v														
18/1	v		v	v	v	v	v	v	v	v	v	v	v	v	v	v
19/1	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v

Table 2

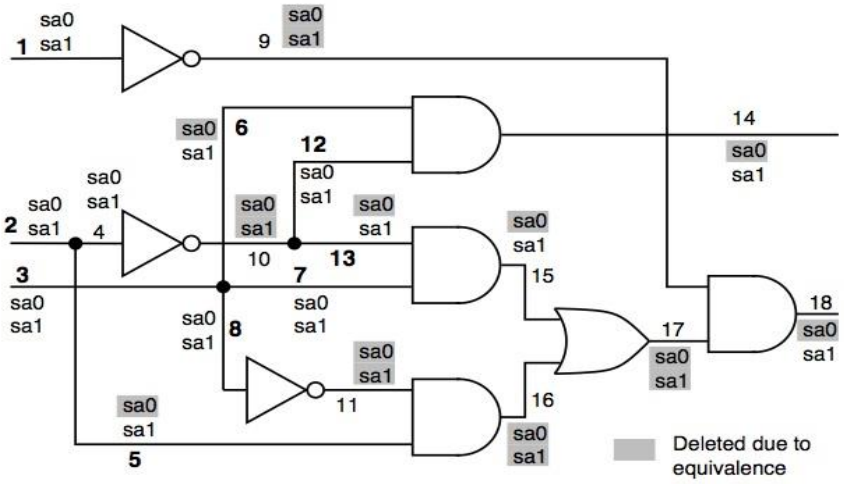
C) At least 5 vectors are required to detect all detectable faults. There are 5 essential vectors to detect all detectable faults:

0000, 0001, 0011, 0101 and 1001

There are however a few faults such as 5/0, 10/0 and 6/0 and their equivalent faults that are undetectable.

Answer 3.

A) The given circuit is shown below with fault sites marked with numbers. The number of potential fault sites is 18.



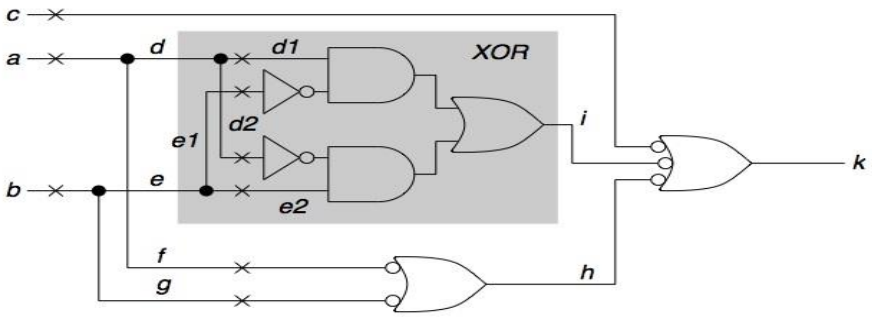
B) The figure shows deletion of equivalent faults using an output to input pass. Of the 36 faults, 20 remain, giving a collapse ratio 20/36 = 0.56.

C) Checkpoint lines are shown in boldface numbers. These are three PIs and seven fan-out branches. There are ten checkpoints and 20 checkpoint faults (There are some people treated a single input gate (inverter) as continuation of its input line. Thus, line 2 is assumed to fan-out to 5, 12 and 13. There are nine checkpoints and 18 checkpoint faults. For grading, I give full credit for both cases).

Furthermore, stuck-at-0 faults on lines 6 and 12 are equivalent and any one of them can be chosen. Similarly, stuck-at-0 faults on 7 and 13 are equivalent, and so are stuck-at-0 on 5 and stuck-at-0 on 11. Thus, the set of fault set is reduced to 17, giving a collapse ratio 17/36 = 0.472.

Answer 4.

A) To find checkpoints of the circuit, we must replace the exclusive-OR (XOR) function by a primitive Boolean gate implementation. AND, OR, NAND, NOR and NOT gates are called the primitive Boolean gates. Functions such as XOR are sometimes referred to as complex gates. In the following figure, we have assumed one such implementation. Our result is, therefore, based on this assumption. Other implementations of the XOR function are possible and can give a different set of checkpoints.



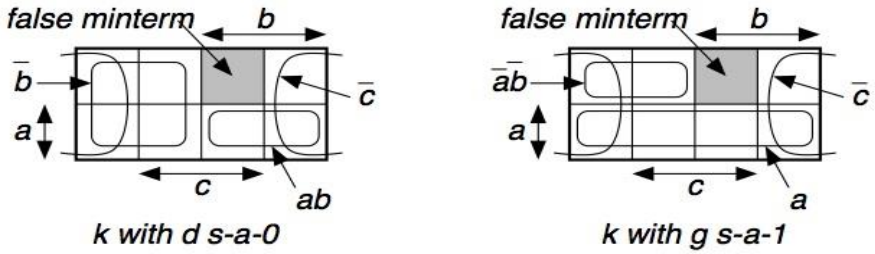
There are nine checkpoints in this circuit. These include three primary inputs, **a**, **b** and **c**, and six fan-out branches, **d1**, **d2**, **f**, **e1**, **e2** and **g**. The checkpoint fault set consists of eighteen faults (stuck-at-0 and stuck-at-1) faults on the nine lines.

Notice that lines **d** and **e** of the original circuit are not checkpoints. If we did not model the XOR block with Boolean gates, then those lines will appear to be checkpoints, whose number will be fourteen. However, detection of those faults will not guarantee detection of faults on the fan-outs that are internal to the XOR block. Considering the Boolean gate structure, a fault on **d** corresponds to a simultaneous (multiple) fault on **d1** and **d2** and, in general, the detection of a multiple fault is not equivalent to detection of the component faults.

B) We evaluate the output function k corresponding to the two faults:

$$\begin{aligned} k(d\ s-a-0) &= \bar{c}+\bar{b}+\overline{\bar{a}+\bar{b}} \\ &= \bar{c}+\bar{b}+ab \\ k(g\ s-a-1) &= \bar{c}+\overline{a\bar{b}+\bar{a}b}+a \\ &= \bar{c}+\bar{a}\bar{b}+a \end{aligned}$$

The two faulty functions are shown by Karnaugh maps below. In both cases, the functions have exactly one false Minterm, **abc**. Since the two faulty functions are identical the corresponding faults are equivalent.



Note: this type of fault equivalence is functional and is often difficult to find by typical fault analysis tools, which rely on structurally identifiable equivalences.

Answer 5.

Assuming that the fault sample size is much smaller than the total fault population, i.e., Ns ≪ Np, we use the result of Equation 5.9 (page 124 in the book), which can be written as,

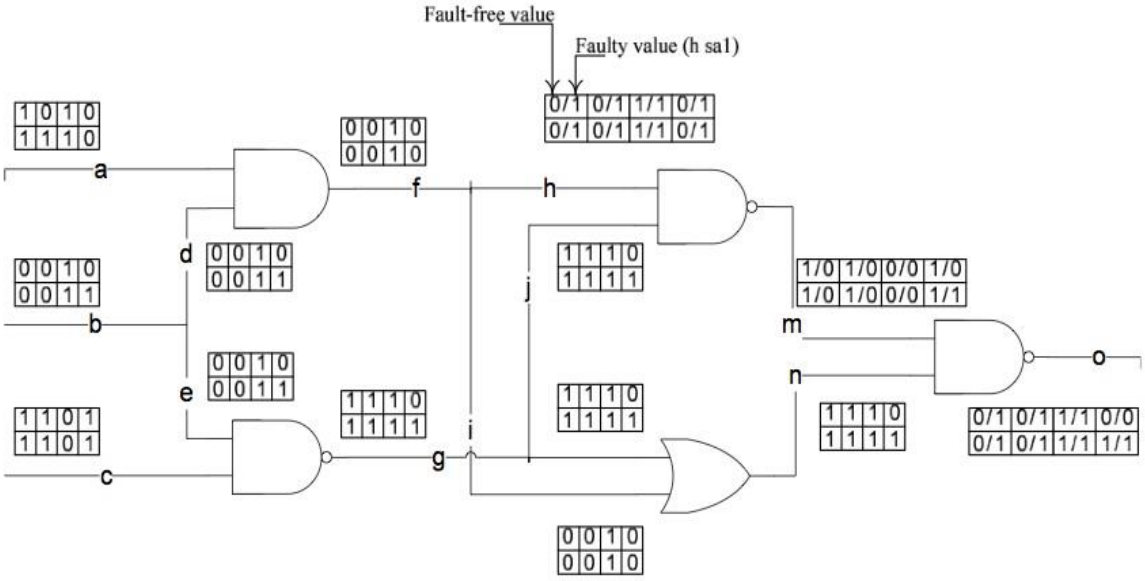
$$\text{Sample size, } N_s = \frac{4.5^2}{\Delta^2} 0.44x(1-x)$$

where ±Δ is the 3σ range of the coverage estimate and x is the sample coverage. Using the given data, Δ = 0.02 and x = 0.70, we obtain

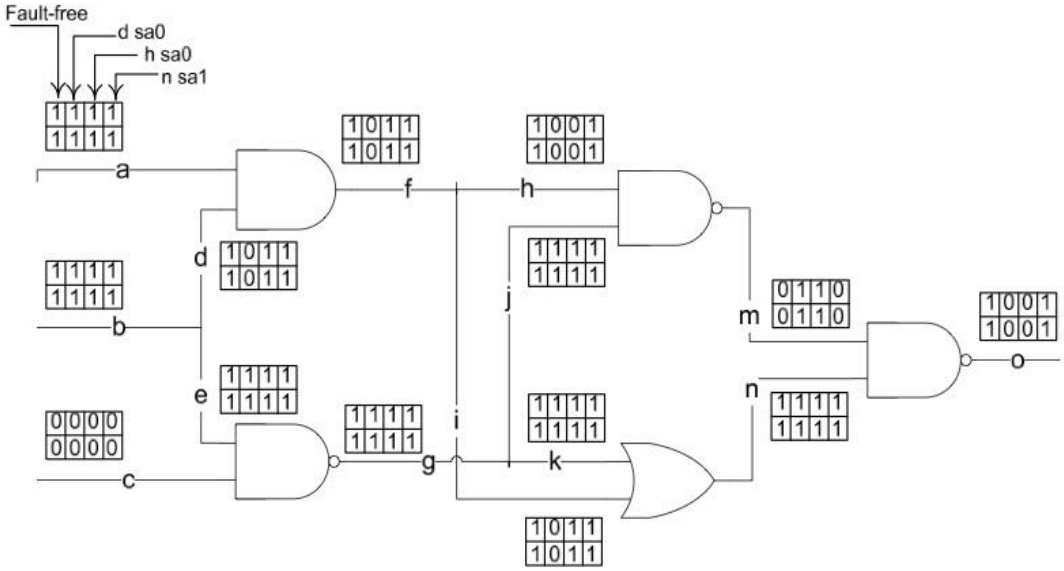
$$N_s = \frac{4.5^2 \times 0.44 \times 0.7 \times 0.3}{0.02^2} = 4,678 \text{ faults}$$

Answer 6.

A) From the figure, we can see that vectors 1 and 2 produce a different output from the fault free circuit at the output and hence the fault is detectable by these two vectors. However vector 3 fails to distinguish between the faulty and fault-free circuits at the PO and hence the fault is undetectable by vector 3. Vector 4 is a special case as it produces an X at the primary output and hence the fault is said to be potentially detectable by vector 4.



B) From the figure, we can see that **d** (stuck-at-0) and **h** (stuck-at-0) produce different outputs from the fault free circuit at the output and hence the two faults are detectable by the vector **abc** = <u>110</u>. However **n** (stuck-at-1) fails to distinguish between the faulty and fault-free circuits at the PO and hence the fault is undetectable under the vector.



Answer 7.

$L_a = \{a/0\}$
$L_b = \{b/1\}$
$L_c = \{c/0\}$
$L_d = \{b/1, d/1\}$
$L_e = \{b/1, e/1\}$
$L_f = L_d \cap \overline{L_a} \cup L_f = \{b/1, d/1, f/1\}$
$L_g = L_e \cap \overline{L_c} \cup L_g = \{b/1, e/1, g/0\}$

$L_h = L_f \cup L_h = \{b/1, d/1, f/1, h/1\}$
$L_i = L_f \cup L_i = \{b/1, d/1, f/1, i/1\}$
$L_j = L_g \cup L_j = \{b/1, e/1, g/0, j/0\}$
$L_k = L_g \cup L_k = \{b/1, e/1, g/0, k/0\}$
$L_m = L_h \cap \overline{L_j} \cup L_m = \{d/1, f/1, h/1, m/0\}$
$L_n = L_k \cap \overline{L_i} \cup L_n = \{e/1, g/0, k/0, n/0\}$
$L_o = L_m \cup L_n \cup L_o = \{d/1, e/1, f/1.g/0, h/1, k/0, m/0, n/0, o/1\}$

Thus the faults in the final list d/1, e/1, f/1, g/0, h/1, k/0, m/0, n/0, and o/1 can be detected with the given vector.