Department of Electrical and Computer Engineering
Utah State University

ECE 5930/6930: VLSI Testing and Verification

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Final Project

Assigned Date: 04/03/2014

Due Date: 04/24/2014

Introduction

The main goal of the project is generating economical test set and performing fault diagnosis procedure. Producing economical test set which considers life-cycle cost can have advantage in reducing less-functional test vectors, increasing fault/defect coverage, and diminution in time to revenue. Meanwhile, the most important utility of the test set is reduction that we can achieve in run-time of automatic test equipment.

In logic diagnosis, fault models (e.g. stuck-at fault, bridge fault, open fault, and etc.) are used to model the failure behavior caused by a physical defect. Using logic level fault model can simplify simulating the fault effect caused by the real defect. When a chip fails test, fault diagnosis can determine the most likely faulty locations and fault types. Meanwhile, fault diagnosis focuses on the defects that are present on the pins of a library cell or the interconnecting wires between library cells.

Generating Economical Test Set

In this part, you should develop an economical test set which has sufficient test and fault coverage and has somewhat minimum size for a given circuit by using TetraMAX tool. Each person will be provided its own circuit. All the circuits are developed in a way to have the same test generation complexity. As a hint, you can generate test vectors using ATPG tool or random test vectors and leverage various techniques such as combination, compaction, replacement, and etc. to create the economical test set. If you accomplish this part, you will achieve 40 points out of 100 points.

Performing Fault Diagnosis Procedure

You will be given three net-lists as the realizations of the circuit for which you generated test vectors. We can call each of these net-lists as “Hypothetical Fabricated Chip”. For identifying the operation (faulty or fault-free) of each HFC, you need to apply the economical test set to it. You will find some of them are faulty (i.e. it can be one or more). After determining the faulty HFC(s), you are required to pick one (if you find more than one faulty HFC) and perform fault diagnosis procedure to find the actual fault in that HFC. Regarding to the fact that the fault, which is in the faulty HFC, can be equivalent to some other faults and collapsed by them, your test set might not be able to excite the fault. In this situation, you need to find the desired test vector for exciting the fault and add it to your test set. Completion of this part will award you 35 points out of 100 points of the project.

Important Hint: After finding the possible faults in the faulty HFC, you can inject each of them in the circuit and comparing their results. Based on the comparison, you will be able to identify the actual fault. It should be said that this technique is just a suggestion and your allowed to figure out and implement other useful techniques as well.

Objects of the package to deliver:

The package that you deliver for the project must contain the following objects and requirements:

1) **Report**: The ingredients of the report are required to be according to the following. Meanwhile, providing the report awards you 25 points.

I. Result: Please include all the reports and results that you achieved during the process of completing each part (such as total number of test vectors in your test set, test report and fault coverage, total number of detected faults and undetected/undetectable faults, all simulation results for the given circuit and HFCs). Also, you should include the results that achieved during the process of fault diagnosis on the picked faulty HFC.

II. Discussion: This section needs to contain the initial strategy and techniques that you planned for doing each part and the final strategy and techniques that you followed for completing it. You should prove the effectiveness of your strategies and techniques to us. Also, the details of the process that you used for each part need to be covered (e.g. in generating economical test set, the steps that you used and the improvements, such as fault coverage or lower number of test vectors, that you achieved). Furthermore, you are required to create flowchart for your final strategy of each part. Finally, please explain the problem(s) that you faced in each part and your solution(s) for them as well as suggest and discuss other strategies that can be used for each part.

2) **Files**: You ought to deliver all the programs and scripts that you created and all the net-lists that you modified. Meanwhile, please provide an explanation for each of them.

3) **Format**: Please use $8\frac{1}{2} \times 11$ inch pages for the report with $1\frac{1}{2}$ line spacing and point size no smaller than 10. Figures and computer outputs, if included with the report, must also fit into the $8\frac{1}{2} \times 11$ inch page size and in the page limit specified.

Summary of the Deliverable:

1) Your information (Name, A-Number).

2) Your given circuit and HFCs.

3) Results:

- Total number of tests.
- Fault Coverage.
- List of undetected/undetectable faults.
- The test result for three circuits.
- The diagnosis result on faulty HFC.

4) In “Generating Economical Test Set” part:

- The initial planned strategy.
- The final strategy used.
- The details of the test generation process.
- Discussion and Comments.
- Flowchart.

5) In “Performing Fault Diagnosis Procedure” part:

- The initial planned strategy.
- The final strategy used.
- The details of the diagnosis process.
- Discussion and Comments.
- Flowchart.

And all other objects that has been mentioned in “Objects of the package to deliver” section.

Important:

Please contact the TA to get your package.

Good Luck