Analyzing Faulty Signals in Digital Circuits using TetraMAX

Posted: D/M/Y – Due: D/M/Y via Canvas
By: Sean Taheri

In this lab, your task is applying a set of test vectors that is generated by TetraMAX tool and then getting the information of the faults that can be detected by these test vectors.

Before starting the project you need to be familiarized with some related commands for this lab.

According to the User Guide of TetraMAX, there are two commands for analyzing the faults of a circuit:

1) **`report_faults  istance_name|pin_pathname  -stuck <0|1|01>|-slow<r|f|rf>`**

`istance_name`: Reports all faults associated with the selected instance name.

`pin_pathname`: Reports faults associated with the selected pin pathname.

`-stuck <0|1|01>`: Reports only the stuck-at-1 or stuck-at-0 faults, or both stuck-at-faults associated with the specified `pin_pathname`. The default is 01 (both).

`-slow <r|f|rf>`: Reports slow-to-rise, slow-to-fall, or both transition delay faults for the specified `pin_pathname`.

2) **`report_faults -pattern_id n      // n = 0, 1, 2, …`**

It reports the faults that can be detected by the selected test pattern, but no patterns preceding it. To see results of this command, you need to first issue a `run_fault_sim -detected_pattern_storage` command.

Starting the Lab

You can start from the following commands in a directory that you want to do your lab:

1. `tmax &`

Please follow the following steps in Command-Line Text Field:

2. `read_netlist /opt/software/cadence/library/tcbn45nm/verilog/HVT/tcbn45gsbwphvt.v -library`
3. `read_netlist /*** (your directory)/circuit-1.v`
4. `run_build_model circuit1`
5. `run_drc`
6. `remove_faults -all`
7. `add_faults -all`
8. `run_atpg`
9. `run_simulation`
10. Click on the "`Schematic View`" icon at the top of the screen. Then, click on the "`Show`" icon that appears in the schematic view window, scroll down and select: "`ALL`"

11. `write_patterns name.stil -format stil`
12. `reset_state`
13. `set_patterns –delete`
14. `set_patterns -external name.stil`
15. `run_simulation`
16. `run_fault_sim -detected_pattern_storage`
17. `report_faults -pattern_id 1`
18. `report_faults N3 -stuck 1`

Notice 1: Command number “17” reports the faults detected by the selected pattern (= pattern 1). In this circuit, we have 8 generated patterns (0-7) and we can analyze each of them by this command.

Notice 2: Command number “18” reports the faults associated with the selected pin pathname (pin = N3). The inputs in this circuit are from N1 to N5 and the associated faults of any of them can be achieved by this command.

Notice 3: You can go to your directory and change each of the patterns in `name.stil` file to every patterns that you want to view the effect of new patterns on specified faulty signals.

What to turn in for this lab:

Please submit the following via canvas:

The fault report for all patterns and all input pins.