Department of Electrical and Computer Engineering
Utah State University

ECE 5930/6930: VLSI Testing and Verification

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Homework 01

Assigned Date: Month/Day/Year

Due Date: Month/Day/Year

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1. A certain fabrication process has a true yield of 80%, i.e. it produces 80% good devices. The testing mechanism for the finished ICs has an accuracy of 95%. Find the yield, yield loss, and the defect-level for this test process.

Note: This problem is similar to Problem 1-1 of the textbook and does not use the yield model of chapter 3.

Use the following definitions:

Yield: Ratio of devices tested “Good”, relative to the total number of devices tested in percentage.

Yield Loss: Ratio of “Good” devices tested “Bad”, relative to the total number of devices tested “Good” in percentage.

Defect Level: Ratio of “Bad” devices tested “Good”, relative to the total number of devices tested “Good” in percentage.

2. Test Cost. The analog part of a mixed-signal chip takes 1.5 seconds to test. The chip has 1,024 pins. There are 1,000 million vectors that must be applied to test the digital logic and the embedded memory block. The rated clock speed is 200 MHz. Assuming that the wafer yield is %70 and a 500 MHz ATE is used, calculate the test component that should be added in the price of a good chip.

Note: Use Example 1.2 in the textbook for ATE purchase price, depreciation rate, maintenance, and operating cost.

3. For the logic circuit in Figure 1, compute the following parameters:

A) The total number of single stuck-at faults.

B) The total number of all possible multiple stuck-at fault combinations.

C) The total number of stuck-open faults.

Note: You can assume that 3-input AND gate is realized using 8 transistors, a two-input OR gate is realized using 6 transistors, and an inverter is realized using 2 transistors.

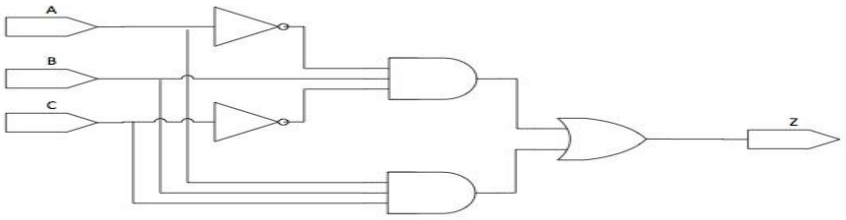

Figure 1

4. CMOS Faults. For a two-input CMOS NAND circuit:

A) Find a two-pattern test for each single-transistor stuck-open fault.

B) Rearrange the right vectors in a compact set and show that this set can be constructed from the single stuck-at fault tests for the NAND gate.

C) For each stuck-at fault of the NAND gate, find an equivalent transistor (stuck-open, stuck-short, or a combination) fault.

5. Show that the two faults **c** (stuck-at-0) and **f** (stuck-at-1) are equivalent in the circuit of Figure 2.

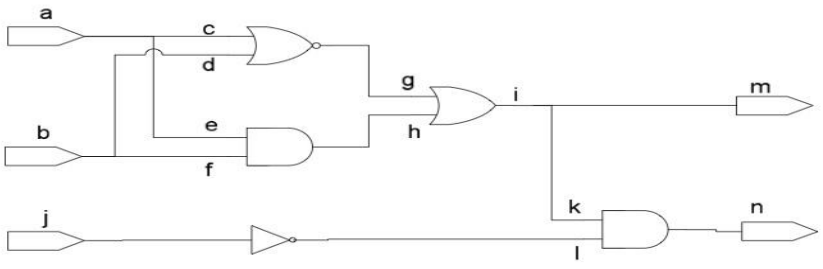

Figure 2