Table. Parameters required in the configuration for power analysis by each power model

There are currently 5 component types supported in SST for power analysis (core, clock, memory controller, IO, NoC/router). Each component may be broken into several sub-components for power analysis. For example, the component, core, has several sub-components, such as il1, dl1, logic, alu, fpu, etc.

Each sub-component requires a set of parameters set up in the configuration file for power analysis. The set of parameters also varies between different power models. The table below lists the parameters required for power analysis of each component/sub-component. It shows,

Parameter Description (unit of the parameter or options)

configuration parameter name

For example, one of the parameters that level 1 instruction cache requires for power analysis by Sim-Panalyzer is capacitance. To set this up in the configuration file, one should include

<cache_il1_sC>*value*</cache_il1_sC>

where *value* is the value of il1's capacitance whose unit is the pF.

		Sim-Panalyzer	**McPAT**
Component Type	**Sub-component Type (ptype)**		
core	**level 1 instruction cache (CACHE-IL1)**	Capacitance (pF) *cache_il1_sC*	Capacity (Bytes) *cache_il1_sC*
		Supply voltage (v) *supply_voltage*	Line size *cache_il1_line_size*
		Cache frequency (Hz) *cache_freq*	Associativity *cache_il1_associativity*
		Number of read ports *cache_il1_number_read_ports*	Throughput *cache_il1_throughput*

		Sim-Panalyzer	**McPAT**
		Number of write ports *cache_il1_number_write_ports*	Latency *cache_il1_latency*
		Number of read/write ports *cache_il1_number_readwrite_ports*	Miss buffer size *cache_il1_miss_buffer_size*
		Number of sets *cache_il1_number_sets*	Fill buffer size *cache_il1_fill_buffer_size*
		Line size *cache_il1_line_size*	Prefetch buffer size *cache_il1_prefetch_buffer_size*
		Number of bitlines *cache_il1_number_bitlines*	Number of banks *cache_il1_number_banks*
		Number of wordlines *cache_il1_number_wordlines*	Physical address width *core_physical_address_width*
		Associativity *cache_il1_associativity*	Core temperature (Fahrenheit) *core_temperature*
			Technology node *core_tech_node*
			Clock rate *core_clock_rate*
	level 1 data cache (CACHE-DL1)	Capacitance (pF) *cache_dl1_sC*	Capacity (B) *cache_dl1_sC*
		Supply voltage (v) *supply_voltage*	Line size *cache_dl1_line_size*
		Cache frequency (Hz) *cache_freq*	Associativity *cache_dl1_associativity*
		Number of read ports *cache_dl1_number_read_ports*	Throughput *cache_dl1_throughput*
		Number of write ports *cache_dl1_number_write_ports*	Latency *cache_dl1_latency*

		Sim-Panalyzer	**McPAT**
		Number of read/write ports *cache_dl1_number_readwrite_ports*	Miss buffer size *cache_dl1_miss_buffer_size*
		Number of sets *cache_dl1_number_sets*	Fill buffer size *cache_dl1_fill_buffer_size*
		Line size *cache_dl1_line_size*	Prefetch buffer size *cache_dl1_prefetch_buffer_size*
		Number of bitlines *cache_dl1_number_bitlines*	Number of banks *cache_dl1_number_banks*
		Number of wordlines *cache_dl1_number_wordlines*	Physical address width *core_physical_address_width*
		Associativity *cache_dl1_associativity*	Core emperature *core_temperature*
			Technology node *core_tech_node*
			Clock rate *core_clock_rate*
	level 2 instruction cache (CACHE-IL2)	Capacitance (pF) *cache_il2_sC*	N/A
		Supply voltage (v) *supply_voltage*	
		Cache frequency (Hz) *cache_freq*	
		Number of read ports *cache_il2_number_read_ports*	
		Number of write ports *cache_il2_number_write_ports*	
		Number of read/write ports *cache_il2_number_readwrite_ports*	

		Sim-Panalyzer	**McPAT**
		Number of sets *cache_il2_number_sets*	
		Line size *cache_il2_line_size*	
		Number of bitlines *cache_il2_number_bitlines*	
		Number of wordlines *cache_il2_number_wordlines*	
		Associativity *cache_il2_associativity*	
	level 2 data cache (CACHE-DL2)	Capacitance (pF) *cache_dl2_sC*	N/A
		Supply voltage (v) *supply_voltage*	
		Cache frequency (Hz) *cache_freq*	
		Number of read ports *cache_dl2_number_read_ports*	
		Number of write ports *cache_dl2_number_write_ports*	
		Number of read/write ports *cache_dl2_number_readwrite_ports*	
		Number of sets *cache_dl2_number_sets*	
		Line size *cache_dl2_line_size*	
		Number of bitlines *cache_dl2_number_bitlines*	

		Sim-Panalyzer	**McPAT**
		Number of wordlines *cache_dl2_number_wordlines*	
		Associativity *cache_dl2_associativity*	
	level 2 cache (CACHE-L2)	N/A	Capacity (B) *cache_l2_sC*
			Line size *cache_l2_line_size*
			Associativity *cache_l2_associativity*
			Throughput *cache_l2_throughput*
			Latency *cache_l2_latency*
			Miss buffer size *cache_l2_miss_buffer_size*
			Fill buffer size *cache_l2_fill_buffer_size*
			Prefetch buffer size *cache_l2_prefetch_buffer_size*
			Number of banks *cache_l2_number_banks*
			Physical address width *core_physical_address_width*
			Core temperature *core_temperature*
			Technology node *core_tech_node*

		Sim-Panalyzer	**McPAT**
			Core clock rate *core_clock_rate*
			L2 clock rate *cache_l2_clock_rate*
			Directory capacity (B) *cache_l2dir_sC*
			Directory line size *cache_l2dir_line_size*
			Directory associativity *cache_l2dir_associativity*
			Directory throughput *cache_l2dir_throughput*
			Directory latency *cache_l2dir_latency*
	instruction TLB (CACHE-ITLB)	Capacitance (pF) *cache_itlb_sC*	Capacity (B) *cache_itlb_sC*
		Supply voltage (v) *supply_voltage*	Line size *cache_itlb_line_size*
		Cache frequency (Hz) *cache_freq*	Associativity *cache_itlb_associativity*
		Number of read ports *cache_itlb_number_read_ports*	Throughput *cache_itlb_throughput*
		Number of write ports *cache_itlb_number_write_ports*	Latency *cache_itlb_latency*
		Number of read/write ports *cache_itlb_number_readwrite_ports*	Miss buffer size *cache_itlb_miss_buffer_size*
		Number of sets *cache_itlb_number_sets*	Fill buffer size *cache_itlb_fill_buffer_size*

		Sim-Panalyzer	**McPAT**
		Line size *cache_itlb_line_size*	Prefetch buffer size *cache_itlb_prefetch_buffer_size*
		Number of bitlines *cache_itlb_number_bitlines*	Number of banks *cache_itlb_number_banks*
		Number of wordlines *cache_itlb_number_wordlines*	Physical address width *core_physical_address_width*
		Associativity *cache_itlb_associativity*	Core temperature *core_temperature*
			Technology node *core_tech_node*
			Core clock rate *core_clock_rate*
	data TLB (CACHE-DTLB)	Capacitance (pF) *cache_dtlb_sC*	Capacity (B) *cache_dtlb_sC*
		Supply voltage (v) *supply_voltage*	Line size *cache_dtlb_line_size*
		Cache frequency (Hz) *cache_freq*	Associativity *cache_dtlb_associativity*
		Number of read ports *cache_dtlb_number_read_ports*	Throughput *cache_dtlb_throughput*
		Number of write ports *cache_dtlb_number_write_ports*	Latency *cache_dtlb_latency*
		Number of read/write ports *cache_dtlb_number_readwrite_ports*	Miss buffer size *cache_dtlb_miss_buffer_size*
		Number of sets *cache_dtlb_number_sets*	Fill buffer size *cache_dtlb_fill_buffer_size*
		Line size *cache_dtlb_line_size*	Prefetch buffer size *cache_dtlb_prefetch_buffer_size*

		Sim-Panalyzer	**McPAT**
		Number of bitlines *cache_dtlb_number_bitlines*	Number of banks *cache_dtlb_number_banks*
		Number of wordlines *cache_dtlb_number_wordlines*	Physical address width *core_physical_address_width*
		Associativity *cache_dtlb_associativity*	Core temperature *core_temperature*
			Technology node *core_tech_node*
			Core clock rate *core_clock_rate*
	branch predictor (BPRED)	Capacitance(pF) *bpred_sC*	Global predictor bits *bpred_global_predictor_bits*
		Supply voltage (v) *supply_voltage*	Number of global predictor entries *bpred_global_predictor_entries*
		Branch predictor frequency (Hz) *bpred_freq*	Prediction width *bpred_prediction_width*
		Number of rows *bpred_number_rows*	Local predictor size *bpred_local_predictor_size*
		Number of columns *bpred_number_cols*	Number of local predictor entries *bpred_local_predictor_entries*
		Number of read ports *bpred_number_read_ports*	Chooser predictor bits *bpred_chooser_predictor_bits*
		Number of write ports *bpred_number_write_ports*	Number of chooser predictor entries *bpred_chooser_predictor_entries*
		Number of read/write ports *bpred_number_readwrite_ports*	Architecture floating point register file size *archi_Regs_FRF_size*
			Number hardware threads *core_number_hardware_threads*

		Sim-Panalyzer	**McPAT**
			Virtual address width *core_virtual_address_width*
			RAS size *core_RAS_size*
			Core temperature *core_temperature*
			Technology node *core_tech_node*
			Core clock rate *core_clock_rate*
	Register file (RF)	Capacitance(pF) *rf_sC*	Machine bits *machine_bits*
		Supply voltage (v) *supply_voltage*	Architecture integer register file size *archi_Regs_IRF_size*
		Register file frequency (Hz) *rf_freq*	Architecture floating point register file size *archi_Regs_FRF_size*
		Number of rows *rf_number_rows*	Physical integer register file size *core_phy_Regs_IRF_size*
		Number of columns *rf_number_cols*	Physical floating point register file size *core_phy_Regs_FRF_size*
		Number of read ports *rf_number_read_ports*	Issue width *core_issue_width*
		Number of write ports *rf_number_write_ports*	Register windows size *core_register_windows_size*
		Number of read/write ports *rf_number_readwrite_ports*	Number of hardware threads *core_number_hardware_threads*

		Sim-Panalyzer	**McPAT**
			Core temperature *core_temperature*
			Tech node *core_tech_node*
			Opcode width *core_opcode_width*
			Virtual address width *core_virtual_address_width*
			Core clock rate *core_clock_rate*
	Logic (LOGIC)	Supply voltage (v) *supply_voltage*	Instruction window size *core_instruction_window_size*
		Logic frequency (Hz) *logic_freq*	Issue width *core_issue_width*
		Logic style (STATIC or DYNAMIC) *logic_style*	Number of hardware threads *core_number_hardware_threads*
		Number of gates *logic_num_gates*	Decode width *core_decode_width*
		Number of functions *logic_num_functions*	Architecture integer register file size *archi_Regs_IRF_size*
		Number of fan in *logic_num_fan_in*	Architecture floating point register file size *archi_Regs_FRF_size*
		Number of fan out *logic_num_fan_out*	Core temperature *core_temperature*
			Technology node *core_tech_node*

		Sim-Panalyzer	**McPAT**
			Core clock rate *core_clock_rate*
	ALU (ALU)	Capacitance (pF) *alu_eC*	Capacity (B) *alu_sC*
		Supply voltage (v) *supply_voltage*	
		ALU frequency (Hz) *alu_freq*	
	FPU (FPU)	Capacitance (pF) *fpu_eC*	Capacity (B) *fpu_sC*
		Supply voltage (v) *supply_voltage*	
		ALU frequency (Hz) *fpu_freq*	
	multiplier (MULT)	Capacitance (pF) *mult_eC*	N/A
		Supply voltage (v) *supply_voltage*	
		ALU frequency (Hz) *mult_freq*	
	instruction buffer (IB)	N/A	Number of read/write ports *ib_number_readwrite_ports*
			Issue width *core_issue_width*
			Number of hardware threads *core_number_hardware_threads*
			Instruction buffer size *core_instruction_buffer_size*

		Sim-Panalyzer	**McPAT**
			Instruction length *core_instruction_length*
			Core temperature *core_temperature*
			Technology node *core_tech_node*
			Virtual address width *core_virtual_address_width*
			Virtual memory page size *core_virtual_memory_page_size*
			Core clock rate *core_clock_rate*
	issue queue (ISSUE_Q)	N/A	Number of hardware threads *core_number_hardware_threads*
			Instruction length *core_instruction_length*
			Instruction window size *core_instruction_window_size*
			Issue width *core_issue_width*
			Core temperature *core_temperature*
			Technology node *core_tech_node*
			Core clock rate *core_clock_rate*
			Architecture integer register file size *archi_Regs_IRF_size*

		Sim-Panalyzer	**McPAT**
			Architecture floating point register file size *archi_Regs_FRF_size*
			physical integer register file size *core_phy_Regs_IRF_size*
			Physical integer register file size *core_phy_Regs_FRF_size*
			Machine bits *machine_bits*
	instruction decoder (INST_DECODER)	N/A	Opcode width *core_opcode_width*
			Core temperature *core_temperature*
			Technology node *core_tech_node*
			Core clock rate *core_clock_rate*
	bypass (BYPASS)		Number of hardware threads *core_number_hardware_threads*
			Number of ALU in the core *ALU_per_core*
			Machine bits *machine_bits*
			Number of FPU in the core *FPU_per_core*
			Opcode width *core_opcode_width*
			Virtual address width *core_virtual_address_width*

		Sim-Panalyzer	McPAT
			Machine bits *machine_bits*
			Store buffer size *core_store_buffer_size*
			Number of memory ports *core_memory_ports*
			Core temperature *core_temperature*
			Technology node *core_tech_node*
			Core clock rate *core_clock_rate*
			Physical floating point register file size *core_phy_Regs_FRF_size*
	EXEU (EXEU)	N/A	Capacitance (pF) *exeu_sC*
	pipeline (PIPELINE)	N/A	Number of hardware threads *core_number_hardware_threads*
			Fetch width *core_fetch_width*
			Decode width *core_decode_width*
			Issue width *core_issue_width*
			Commit width *core_commit_width*
			Instruction length *core_instruction_length*

		Sim-Panalyzer	**McPAT**
			Virtual address width *core_virtual_address_width*
			Opcode width *core_opcode_width*
			Integer pipeline depth *core_int_pipeline_depth*
			Machine bits *machine_bits*
			Architecture integer register file size *archi_Regs_IRF_size*
			Core temperature *core_temperature*
			Technology node *core_tech_node*
	LSQ (LSQ)	N/A	Opcode width *core_opcode_width*
			Virtual address width *core_virtual_address_width*
			Number of hardware threads *core_number_hardware_threads*
			Machine bits *machine_bits*
			Store buffer size *core_store_buffer_size*
			Load buffer size *core_load_buffer_size*
			Number of memory ports *core_memory_ports*

		Sim-Panalyzer	**McPAT**
			Core temperature *core_temperature*
			Technology node *core_tech_node*
			Core clock rate *core_clock_rate*
	register alias table (RAT)	N/A	Architecture integer register file size *archi_Regs_IRF_size*
			Physical integer register file size *core_phy_Regs_IRF_size*
			Architecture floating point register file size *archi_Regs_FRF_size*
			Physical floating point register file size *core_phy_Regs_FRF_size*
			Reorder buffer size *core_ROB_size*
			Number of hardware threads *core_number_hardware_threads*
			Decode width *core_decode_width*
			Issue width *core_issue_width*
			Commit width *core_commit_width*
			Core temperature *core_temperature*

		Sim-Panalyzer	**McPAT**
			Technology node *core_tech_node*
			Core clock rate *core_clock_rate*
	reorder buffer (ROB)	N/A	Physical floating point register file size *core_phy_Regs_FRF_size*
			Physical integer register file size *core_phy_Regs_IRF_size*
			Architecture integer register file size *archi_Regs_IRF_size*
			Architecture floating point register file size *archi_Regs_FRF_size*
			Virtual address width *core_virtual_address_width*
			Number of hardware threads *core_number_hardware_threads*
			Machine bits *machine_bits*
			Reorder buffer size *core_ROB_size*
			Issue width *core_issue_width*
			Core temperature *core_temperature*
			Technology node *core_tech_node*

		Sim-Panalyzer	**McPAT**
			Core clock rate *core_clock_rate*
	branch target buffer (BTB)	N/A	Capacity (B) *btb_sC*
			BTB associativity *btb_associativity*
			BTB throughput *btb_throughput*
			BTB latency *btb_latency*
			BTB number of banks *btb_number_banks*
			BTB line size *btb_line_size*
			Core temperature *core_temperature*
			Technology node *core_tech_node*
			Core clock rate *core_clock_rate*
			Branch predictor prediction width *bpred_prediction_width*
			Virtual address width *core_virtual_address_width*
			Number of hardware threads *core_number_hardware_threads*
memory controller	**memory controller (MEM_CTRL)**	N/A	Memory controller(MC) clock rate *mc_clock_rate*

		Sim-Panalyzer	**McPAT**
			MC LLC line length *mc_llc_line_length*
			MC databus width *mc_databus_width*
			MC addressbus width *mc_addressbus_width*
			MC register window size per channel *mc_req_window_size_per_channel*
			memory channels per MC *mc_memory_channels_per_mc*
			MC IO buffer size per channel *mc_IO_buffer_size_per_channel*
			MC peak transfer rate *mc_peak_transfer_rate*
			MC number of ranks *mc_number_ranks*
			Physical address width *core_physical_address_width*
			Opcode width *core_opcode_width*
			Core temperature *core_temperature*
			Technology node *core_tech_node*
			Core clock rate *core_clock_rate*
NoC	**NoC (ROUTER)**	N/A	NoC clock rate *router_clock_rate*

		Sim-Panalyzer	**McPAT**
			NoC topology (2DMESH or RING or CROSSBAR) *router_topology*
			NoC: number of horizontal nodes (ignored if CROSSBAR) *router_horizontal_nodes*
			NoC: number of vertical nodes (ignored if CROSSBAR) *router_vertical_nodes*
			If NoC has global link (ignored if CROSSBAR) *router_has_global_link*
			NoC: link throughput (ignored if CROSSBAR) *router_link_throughput*
			NoC: link latency (ignored if CROSSBAR) *router_link_latency*
			Router: number of flit bits *router_flit_bits*
			Router: input buffer entries per virtual channel *router_input_buffer_entries_per_vc*
			Router: virtual channel per port *router_virtual_channel_per_port*
			Router: number of input ports *router_input_ports*
			Router: number of output ports *router_output_ports*

		Sim-Panalyzer	**McPAT**
			Number of NoCs in the core *core_number_of_NoCs*
			Core temperature *core_temperature*
			Technology node *core_tech_node*
			Core clock rate *core_clock_rate*
clock	**clock (CLOCK)**	Supply voltage (v) *supply_voltage*	Core temperature *core_temperature*
		Clock frequency (Hz) *clock_freq*	Technology node *core_tech_node*
		Clock style (NORM_H or BALANCED_H) *clock_style*	Core clock rate *core_clock_rate*
		Clock skew *clock_skew*	
		Optimal clock buffer number *opt_clock_buffer_num*	
IO	**IO (IO)**	Capacitance (pF) *io_sC*	N/A
		Supply voltage *supply_voltage*	
		IO frequency *io_freq*	
		IO style (IN or OUT or BI) *io_style*	
		Optimal Io buffer number *opt_io_buffer_num*	

		Sim-Panalyzer	**McPAT**
		IO microstrip length *io_ustrip_len*	
		IO bus width *io_bus_width*	
		IO transaction size *io_transaction_size*	
		IO access time *io_access_time*	
		IO cycle time *io_cycle_time*	