Sudarshan Sharma

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Education

- **Indian Institute of Technology (IIT), Kharagpur India** **Current CGPA:8.66/10.00**
  B.Tech + M.Tech in Electronics and Electrical Communication Engineering **2015-2020**
  with specialization in Microelectronics and VLSI Design
  Minor in (B.Tech) Computer Science and Engineering
- **Delhi Public School, B.S City, Jharkhand, India** **95.60%**
  Grade XII, All India Senior Secondary Central Examination (CBSE) **2015**
- **Delhi Public School, Bhagalpur, Bihar,India** **10.00/10.00**
  Grade X, Secondary School Certificate (CBSE) **2013**

Publications

- **Sudarshan Sharma**, Dhruv Thapar, Nikhil Bhelave, and Mrigank Sharad "Adaptive Multi-bit SRAM Topology Based Analog PUF", in IEEE iSES 2019, Rourkela, India. *Submitted*
- Gopabandhu Hota, **Sudarshan Sharma**, Aditya Rathore, Shailesh Joshi, and Het Shah "An Integrated Visual Signalling, Localisation & Health Monitoring System for Soldier Assistance", in IEEE ICECCT 2019, Coimbatore, India. *Accepted*
- "KGPKubs Team Description Paper 2018: RoboCup Small Sized League" - *RoboCup Symposium, Montreal Canada 2018.*
- "KGPKubs Team Description Paper 2017: RoboCup Small Sized League" - *RoboCup Symposium, Nagoya Japan 2017.*

Internship

- **Acceleration of Neural Network Simulation with Binary Values for Logic Synthesis** **University of Tokyo**
  VDEC Intern, FUJITA Lab *May 2018-July 2018*
  Advisor: *Prof. Masahiro Fujita, Director, VLSI Design and Education Center, University of Tokyo*
  - Worked on the development of a **CAD tool** for solving partial logic synthesis problem using discrete valued **DNN** architecture.
  - Modelled an approach based on And Inverted Graphs (**AIG's**) structure instead of existing Satisfiability (**SAT**) based solution.
  - Implemented existing discrete DNN training algorithm on **tensorflow** to train boolean functions from benchmarks and worked on Quantified Boolean Formula (**QBF**) based DNN architecture verification.
- **Car Electronics and Control Engineering** **Pix Moving, China**
  Winter Intern, Guiyang *Dec 2018*
  Advisor: *Sen Zeng, Mechanical Design & Automation Engineer*
  - Developed the **CAN system** comprising of the braking, steering and accelerator unit using 32 bit ARM Cortex M-3 microcontrollers.
  - Hacked the **BAIC EV car ultrasonic system** for parking assistance using the existing CAN Bus through statistical modelling.
  - Worked on **Autoware** and assisted the team in debugging the pix autonomous Robo-vehicle motor driver units.

Research Experience/Projects

- **Side Channel Attacks and Fault Analysis of Crypto Hardware** **IIT Kharagpur**
  Bachelor Thesis, SEAL Lab *July 2018-Present*
  Advisor: *Prof. Debdeep Mukhopadhyay, Dept. of Computer Science and Engineering*
  - Working on Side Channel Attack on lightweight **block cipher** through correlation power analysis.
  - The project involves **Register Transfer Level (RTL) design** of block cipher in Verilog, **Statistical modelling** of attacks based results and development of heuristic for best implementation. Currently working on Publication.
- **Analog Physically Unclonable Functions** **IIT Kharagpur**
  Team Member *June 2017-Present*
  Advisor: *Prof. Mrigank Sharad, Dept. of Electronics and Electrical Communication Engineering*
  - Working on **robust,low power and area efficient** SRAM topology based multibit analog physically unclonable functions (PUFs).
  - Developed analog modules such as **Single Slope** variable bit ADC scheme and offset cancellation based operational amplifiers.
  - The project involves circuit design,analysis and layout design on Virtuoso Cadence using Calibre DRC.Presently the chip is in layout phase and is expected to be submitted for fabrication using **scl180nm CMOS technology**.

- **Kharagpur Robosoccer Students' Group (KRSSG)** **IIT Kharagpur**
  ***Head**,Electronics and Embedded Team* *Aug 2015-Present*
  Advisor: *Prof. Jayanta Mukhopadhyay, Dept. of Computer Science and Engineering*
  - The group involves the development of a team of **autonomous soccer playing robot** for RoboCup Small Sized League.
  - Conceptualized and fabricated printed circuits boards based on AVR, ARM microcontrollers and FPGA architecture.
  - Designed and implemented a **proprietary BLDC motor controller** for the robots. Devised Verilog modules for close loop PID tuned Trapezoidal control of the BLDC motorand successfully optimised the communication system for least data loss.

- **Rehabilitation Robotics** **IIT Kharagpur**
  Algorithm Designer and Hardware Developer *Aug 2016-Present*
  Advisor: *Prof. Dilip Kumar Pratihar, Dept. of Mechanical Engineering*
  - The group aims to develop an **exoskeleton for the lower extremity** of the human body consisting of actuators and feedback sensors, to impart a locomotive ability to the physically disabled people
  - Implemented a wireless network of RF modules, each node consisting of an Inertial Measurement Unit (IMU) to record gait cycle data in the real time which send the data to Raspberry Pi for further processing
  - Designed a **plantar system** for measuring ground reaction forces and pressure at crucial points in the foot sole during the gait cycle using strain gauge load cells and force sensitive resistors

Training Experience

- **VLSI Summer School** **IIT Kharagpur**
  Student *May 2017-Jun 2017*
  Advisor: *Prof. Mrigank Sharad, Dept. of Electronics and Electrical Communication Engineering*
  - Participated in 8 weeks long VLSI Summer course organized by Electronics and Electrical Communication Engineering Department,IIT Kharagpur.Worked on various design problems in analog and digital domains.
  - Designed a low noise amplifier for **bio-medical frontend** involving capacitive and active common-mode feedback using Cadence Virtuoso and LTSpice along with noise and stability analysis,the circuits were simulated with scl180nm technology.
  - Learned about various analog to digital convertors, offset cancellation schemes, current generation circuit and devised RTL modules for Hamming Distance Calculation on Xilinx ISE.

Projects

- **Design of Verilog Modules on Xilinx ISE**
  VLSI Engineering Lab, Term Project & Extended Pet Project *April 2018-Present*
  - Implemented 16 bit radix two and radix four **booth's multiplier**, compared the performance of designs based on various adders including carry chain, carry look ahead and carry select adders.
  - Working on the architecture of pipelined **CORDIC** (Co-ordinate Rotation Digital Computer) processor.

- **Technologies for Soldier Support**
  Inter-IIT Tech Meet 2018 *Dec 2017-Jan 2018*
  - Built **gesture, localization, video transmission, and health monitoring** modules to upgrade the soldier gears.
  - Interfaced Flex sensors, IMU and trained CNN for the gesture identification module, Implemented an ad-hoc wireless localization framework using **Decawave** based radio modules and **LLS** algorithm, used Amitec SDRs to successfully achieve two way video transmission, health parameter monitoring modules included EEG, temperature and SpO2 probe.

- **Smart Steer**
  Technology General Championship 2015-16 *Jan 2016-Mar 2016*
  - Built a manual cum **autonomous wheel chair** controlled via mobile app to traverse a path while avoiding obstacles.
  - Structured the communication, localization and steering control, designed the main circuit of the robot, integrated the bluetooth module with the mobile app.The team won the **GOLD** medal in the competition.

- **Linked Car**
  Pet Project *Aug 2017-Present*
  - LinkedCar is a **V2X** platform which upgrades the cars of yesterday with the concepts of **Connected Autonomous Shared and Services and Electric (C.A.S.E.)** to harness the power of masses to enhance premium car experience.
  - Special Mention Prize at **Hack.Bangalore 2018** a Digital Life @Daimler initiative.
  - Selected for **India Innovation Challenge Design Contest 2017** organised by Texas Instruments and NSRCEL, IIM Bangalore.

- **Person Following Turret**
  IEEE Certified Winter Workshop|Texas Instruments *Dec 2015*
  - Learned basics about **embedded electronics** and implemented it on various micro controllers- ATMEGA 16, Arduino.
  - Built a robot using three sonars and a servo motor capable of following the object using the triangulation technique.

- **Comparison of Impedance Matching Networks**
  Term Project, Network Theory Lab Jul-2016-Aug 2016
  - Performed the **reliability analysis** of Impedance Matching Networks using **Monte Carlo simulation** in MATLAB ,studied two possible L-type IMNs and compared their performance on the basis of bandwidth.
- **ECG Signal Acquisition**
  Term Project, Analog Electronics *Feb-2017-Mar 2017*
  - The project included designing of different modules for ECG signal signal acquisition, modules include low noise frontend amplifier, V to I converter using differential amplifier and **single slope ADC** to get the ECG signal analog voltage levels in digital domain.
- **ICCAD CAD Contest 2018**
  ICCAD 2018 *May-2018-Present*
  - Worked on Problem A: Smart EC: Program-Building for Name Mapping by **Cadence Design Systems, Inc** with team members from IITB and UTokyo. Secured Special Mention Award.

Technical Skills

- **Programming Languages:**C, Python, Verilog, C++, , C#, LaTeX.
- **Microcontroller and Microprocessor:**FPGA, AVR(Atmega), ARM Cortex Mx (STM), ARM Cortex A7 (RaspPi).
- **Software/Scientific tool:**LTSpice, PSpice, Cadence, Xilinx ISE, Coocox CoIDE, AVR Studio, Eagle, Proteus, MATLAB.

Relevant Courses

Analog Electronics	Algorithms	Programming and Data Structures
Digital Electronics	Semiconductor Devices	Signals and System
VLSI Engineering	Digital Communication	Micro-controllers & Embedded Sys.
Computer Architecture and OS	Architectural Design of ICs	VLSI System Design
Analog VLSI Circuits	VLSI for Telecommunication	Semiconductor Device Modelling
Probability and Stochastic Processes	Electromagnetic Engineering	RF and Microwave Engineering

Position of Responsibility

Designation	Organization	Activities	Duration
Mentor	Student Welfare Group	◦ Guiding a group of second year students of IIT Kharagpur to excel academic and extra academic life under Student Mentorship Program	July 2017 - Present
Project Head & Mentor	IEEE Workshop	◦ Mentored a **group of 43** robotics enthusiasts to build an Obstacle removing autonomous robot. ◦ Accomplished the Problem Statement in given time frame	Dec 2016
Student Coordinator	Code-O-Soccer	◦ Chaired Code-O-Soccer (event.krssg.in), national coding event for the first time managed the in house prelims and workshop for the students of IIT Kharagpur.	Feb 2015 - Present

Extra-Curricular Achievements/Involvements

- Selected as an undergraduate representative for the university for Small Sized League **RoboCup Nagoya Japan 2017**.
- Represented IIT Kharagpur's Gold winning Contingent at Inter IIT Tech Meet, IIT Madras 2018.
- **First place** at the Xilinx Innovation Challenge during Kshitij. 2018.
- Secured 4th position in the **Finals** of event Anadigx (Analog and Digital Circuit Design Competition) during Kshitij 2017.
- Won the **Best Freshers Award** in a semi-autonomous event Warehouse during Kshitij 2016,IIT KGP.
- Secured **First Position** in the Robosapiens Hackathon held after the overnight Workshop during NSSC 2015,IIT KGP.
- Secured **CGPA 10.00/10.00** during Grade X,All India Senior Secondary Central Examination(CBSE), 2013.
- Completed two years as **National Cadet Corps'(NCC)** Cadet, under Ministry of Defence,Government of India.
- Selected as **Captain** for Hardware Modelling Team, MS Hall for Technology General Championship 2018-19, IIT Kharagpur.