Closed Loop BLDC Motor Controller using FPGA

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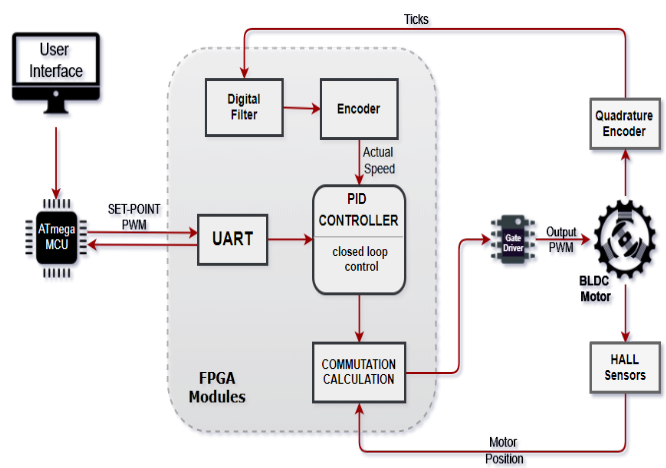
Introduction

In specific applications such as Electric Vehicles (EVs), electric motor has an essential effect on the overall performance of the system. In such applications, efficient and reliable control and operation of the overall systems are mainly dependent on the selected motor type and its control drive. Correct selection of electric motor drive is highly dependent on application requirements. High efficiency, high speed ranges and high power/torque to size ratio are main advantages of BLDC motors compared to other electric motor types. BLDC motors need less maintenance due to the elimination of the mechanical commutators and brushes. BLDC motors have faster dynamic response due to their low inertia (permanent magnet) rotor compared to induction motors. With these advantages, utility of BLDC motor is widespread. Available market motor drivers for BLDC motor demand higher prices and also they are limited to particular current range. Therefore developing a low cost and efficient BLDC motor control drive by comprising new techniques, tools and circuits is in high demand.

There are two types of permanent magnet synchronous motors based on their back Electromotive Force (EMF) waveforms. Permanent magnet synchronous motors with sinusoidal wave back-EMF that are well known as Permanent Magnet Synchronous AC Motors (PMSMs) and the other type with trapezoidal-wave back-EMF that are called Permanent Magnet Brushless DC (BLDC) Motors. BLDC motors produce larger torque compared to PMSMs. Electronic commutation of the BLDC motor is based on position of permanent magnet rotor. Rotor position is either detected through inbuilt sensors or through sensorless algorithms by back-EMF zero crossing detection (ZCD). Position detection sensors provide signals based on rotor position. Hall Effect sensors are generally used for low resolution application and optical encoders are generally used for high resolution applications. Back-EMF sensing, back-EMF integration, free-wheeling diode conduction of unexcited phase, flux linkage based, third-harmonic analysis of back-EMF are various BLDC motor sensorless control techniques. Reduction of motor maintenance, extra wiring, temperature sensitivity, cost and complexity of motor construction are main advantages of

sensorless control algorithms. However control algorithms complexity, starting and low speed commutation difficulties are main drawbacks of sensorless BLDC motor drives. Hence for simplicity purpose, the proposed closed loop control is designed on BLDC motor with three hall sensors.

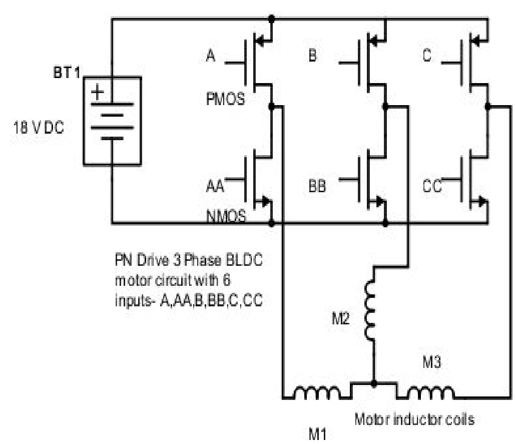
Block Diagram



Modules:

- Commutation
- Pulse Width Modulation (PWM)
- UART
- Encoder
- PID controller

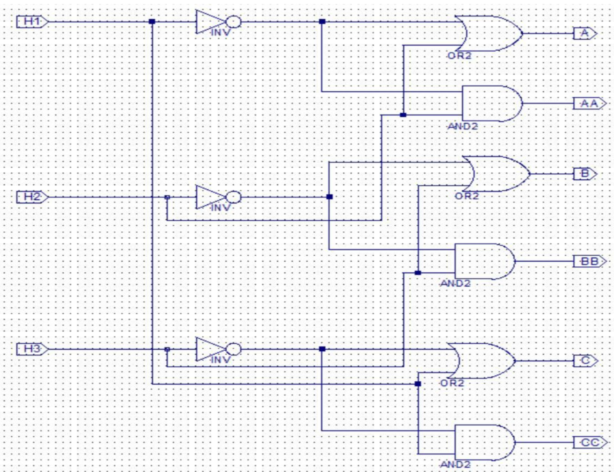
Commutation:



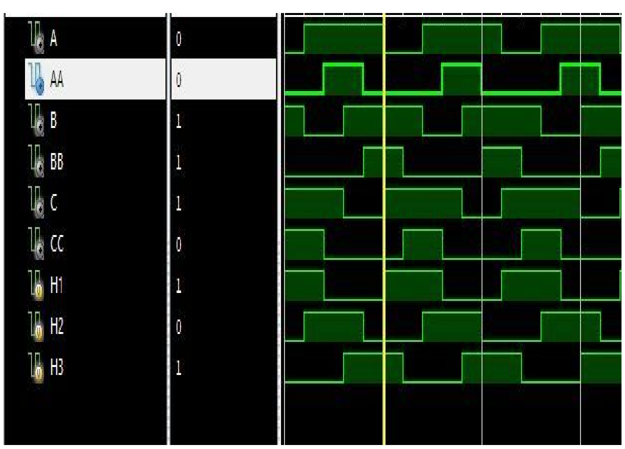
It takes in the output of Hall sensors to identify the position of coils of motor. Then the output commutations are calculated according to the position of motor. With the help of K-MAP logic for each power mosfet gate input is derived.

H1	H2	H3	PHASE A	PHASE B	PHASE C
1	1	0	OFF	+	-
0	1	0	-	+	OFF
0	1	1	-	OFF	+
0	0	1	OFF	-	+
1	0	1	+	-	OFF
1	0	0	+	OFF	-

Schematic design for commutation module:
Inputs: H1,H2,H3
Outputs: A,AA,B,BB,C,CC



Simulation results:



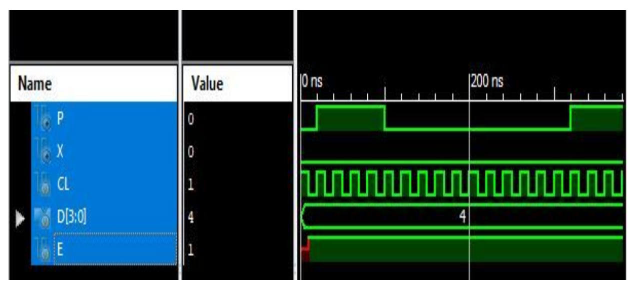
PWM Module

PWM (Pulse width modulation) for varying the speed of BLDC motor is implemented using verilog. We have designed 8 bit PWM module for varying the speed. 1 Direction bit for clockwise and anticlockwise rotation of motor and 7 Speed bits for varying the speed from 0 to 127

Simulation results

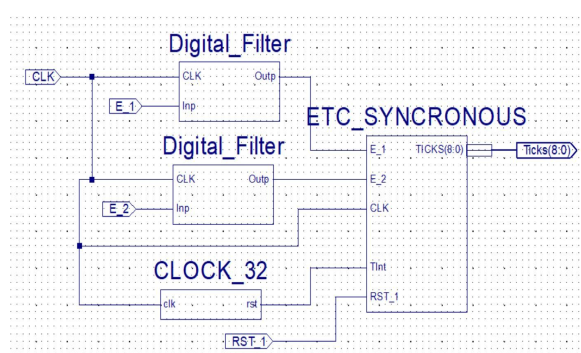
(Note: for presentation purpose we have simulated 4 bit PWM module)

Inputs: CL(clock), E(enable bit), X(control bit), D(PWM input value, here 4)
Output: P(PWM output)

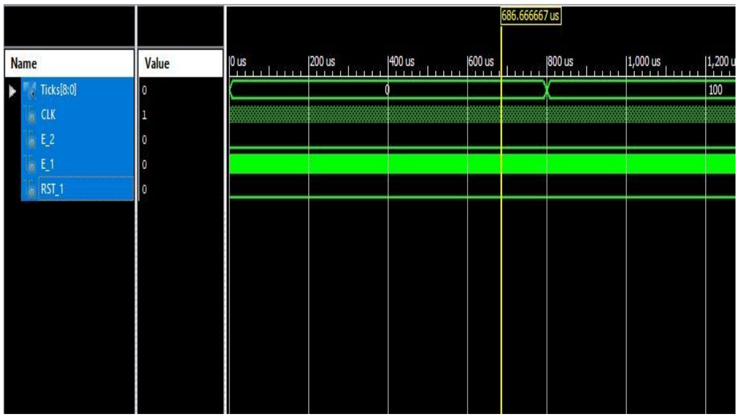


Encoder Module:

This consists of digital filter, 0.8ms clock pulse generating and encoder ticks counting modules. The input is passed through digital filter and then fed to the ticks counting unit which outputs the total ticks in 0.8 millisecs. Two inputs E_1 and E_2 give the idea of speed as well as direction of rotation of motor.



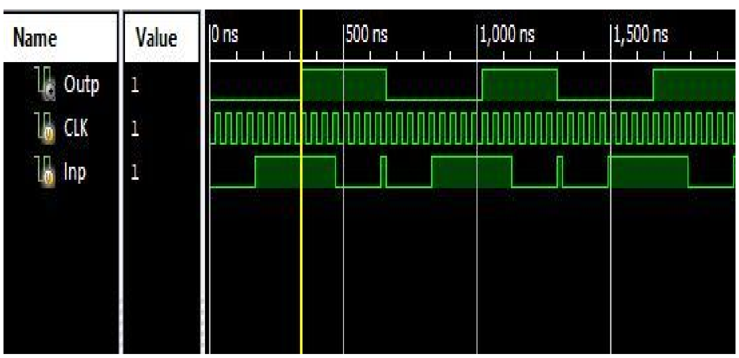
Simulation Encoder: E_1 input, 0.8 ms Sampling time, Clock Freq= 50 MHz, Encoder output= 100 ticks



Digital Filter:

Digital filter is used to avoid counting of unnecessary spikes from encoder and gives filtered output as shown in the simulation. It works on the principle of **Moving Average Filter** and consecutively 4 bits are first sampled and their 'AND' is passed as an output. So, any unwanted spikes are filtered out.

Digital Filter Simulation (Clearing the spikes)

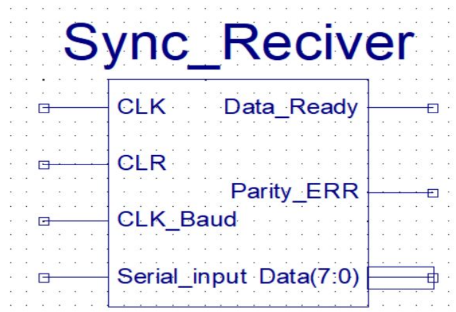


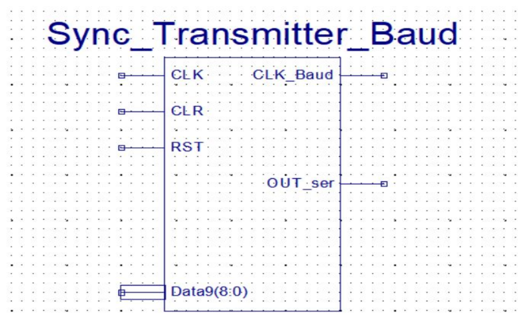
User Interface:

The desired RPM is feeded from PC to Arduino Board using Realterm software which then transmits the RPM to Xilinx Mimas Board through UART(Universal Asynchronous Receiver Transmitter) based communication. Similarly it receives the current velocity of motor to track whether the motor is rotating at desired velocity. Hence it helps in plotting the PID plot as well which further benefits in deciding the control loop architecture.

UART interface with the FPGA:

The FPGA is continuously sampling the Seria_Input line.The sampling is done by the clock at 100 MHz which is much faster than the data rate, in this case 38400 bits per second, used in the UART module.So, all the processing is done on positive edges of the clock and thus is the only event driving line in the module thus maintaining uniformity of code. Once it sees the line transition from high to low, state of the receiver is changed and the incoming bits are fed to a SIPO(Serial In Parallel Out) register. A counter keeps tracks of the number of bits sampled by sensing the CLK_Baud which is synchronous clock between the transmitter and receiver. After the byte word is received the state again changes and the passed as byte word to PWM module which controls the speed of the BLDC motor. The figure below shows how the UART receiver is used inside the FPGA.

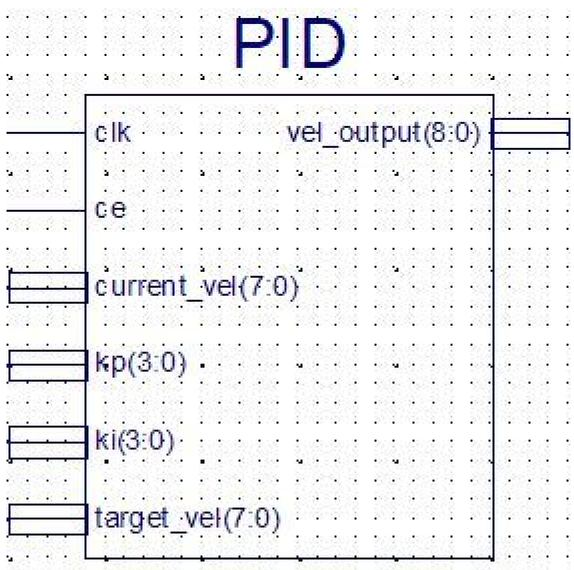




UART will be in transmission mode when CLR is enabled as the module uses CTS(Clear to Send) mechanism. The encoder provides the 8 bit value, defined as its speed, to the transmitter module and these transmission data bytes are saved into an internal TX buffer before being processed for Sync_Transmitter module. Transmitter module converts the data received from the encoder into a full serialized tx packet by adding a start bit of '0', odd parity bit and stop bit of '1'. Transmitter module changes its state from IDLE to transmission mode and a PISO(Parallel In Serial Out) is used to transmit the complete 11-bits character, bit-by-bit. A counter keeps a track of the bits transmitted. A baud generator is present inside the transmitter module which synchronises the receiver and transmitter at the prescribed baud-rate.

PID Module: PID module is developed using verilog. Tuning PID control parameters is very difficult, poor robustness, therefore, it's difficult to achieve the optimal state under field conditions in the actual production. PWM control method is a better method of controlling, to the complex and unclear model systems, it can give simple and effective control. Proportional-integral (PI) control with hysteresis or pulse width modulation (PWM) switching is the most widely used speed control technique for BLDC motors with trapezoidal back EMF. It can be easily implemented on analog or digital components because it is well understood, simple, and in practice for a fairly long period of time. And hence it is implemented in this design.

Schematic:



The Ziegler-Nichols method used was done based on obtaining the open loop transfer function and thereafter obtaining the necessary parameter values needed for the various evaluation of the P, PI and PID parameters.

Applications

- Being FPGA based architecture, these driver can be used for driving multiple motors parallely in Quadcopters, Humanoids, etc.

Results and discussion

- Due to the flexibilities of FPGA, the proposed modules can be configured for different control drive of electric machines.
- No load current for maximum RPM is recorded to be 0.15 A at 18V DC supply.
- Number of ticks obtain through encoder at maximum RPM is very close to the calculated value (127).

Cost

The estimated cost of for the developed architecture is around 10% of those motor drivers available in the market for BLDC motor.

Link to the Video:
BLDC motor working