Islamic University of Technology

Department : EEE

Course : EEE- 4308 (HW+SW)

Subject : Project Report of Digital Logic Design Phase (A, B, C, D & E)

Section : A

Group Members:

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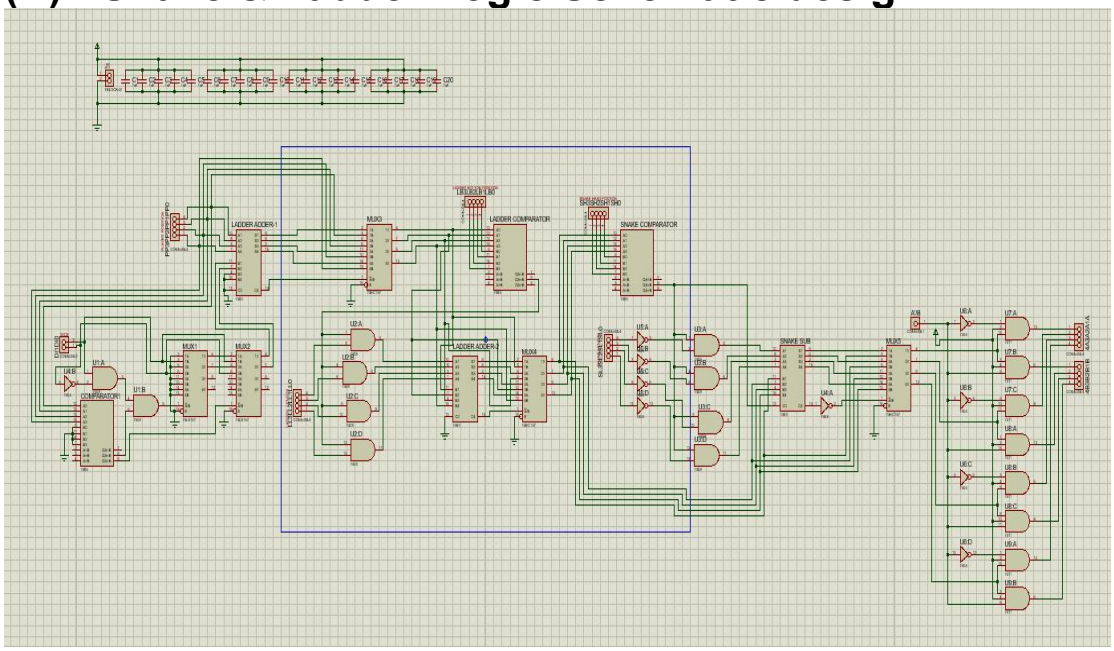
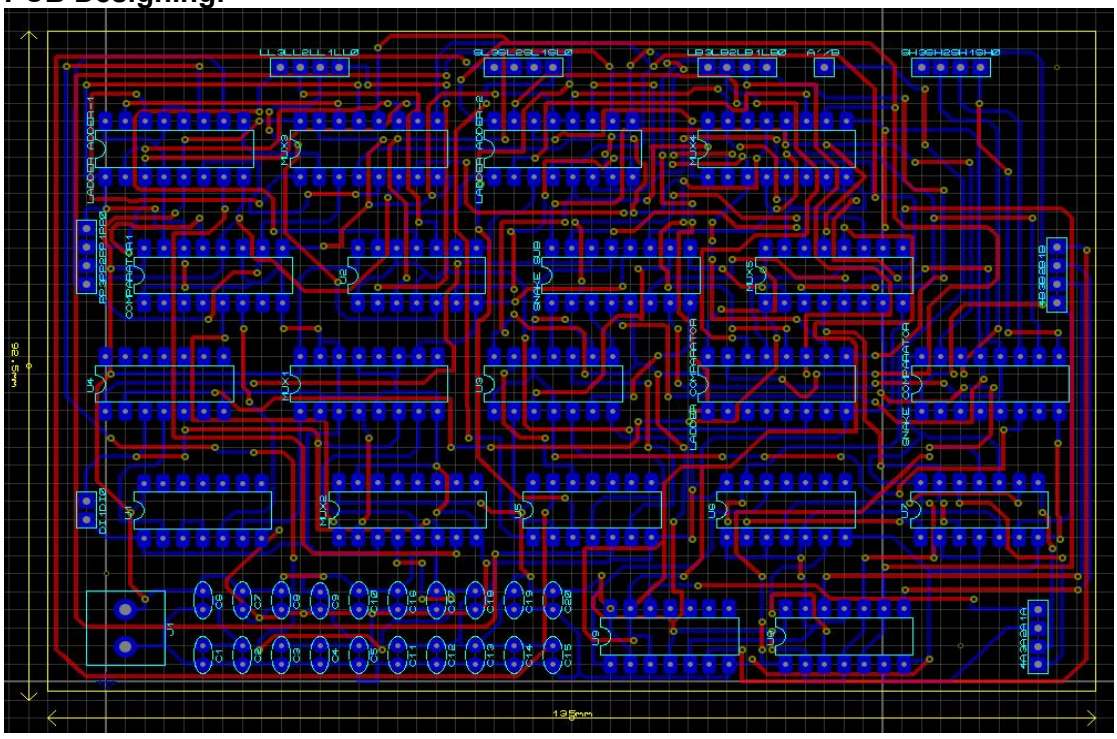
- **220021123- Fahim Rezwan Shifat**
- **220021127- Ahnaf Sakif**
- **220021130- Mahib Abtahi**
- **220021151- Abdullah Jubayer**
- **220021157- Hasib Ahmed Anik**

(A) Snake & Ladder Logic Schematic design:



PCB Designing:



Explanation:

In the PCB technology portion, Design Rule Manager part:

A)Design Rule:

- **Pad - Pad** Clearance: 20 th
- **Pad - Trace** Clearance: 30 th
- **Trace - Trace** Clearance: 30 th
- **Graphics** Clearance: 15 th
- **Edge/Slot** Clearance: 15 th

B)Net Classes:

Both **POWER** & **SIGNAL**. Here are the configurations **:** • **Routing Styles:**

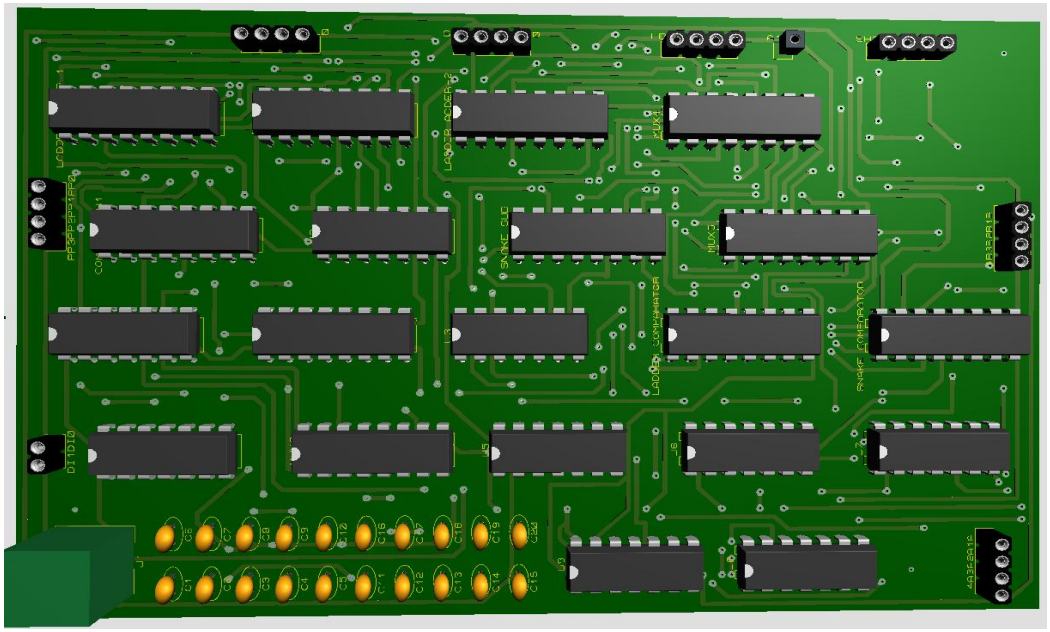
- **Trace** Style: T50
- **Via** Style: V80

• **Via Type: Thru-Hole**

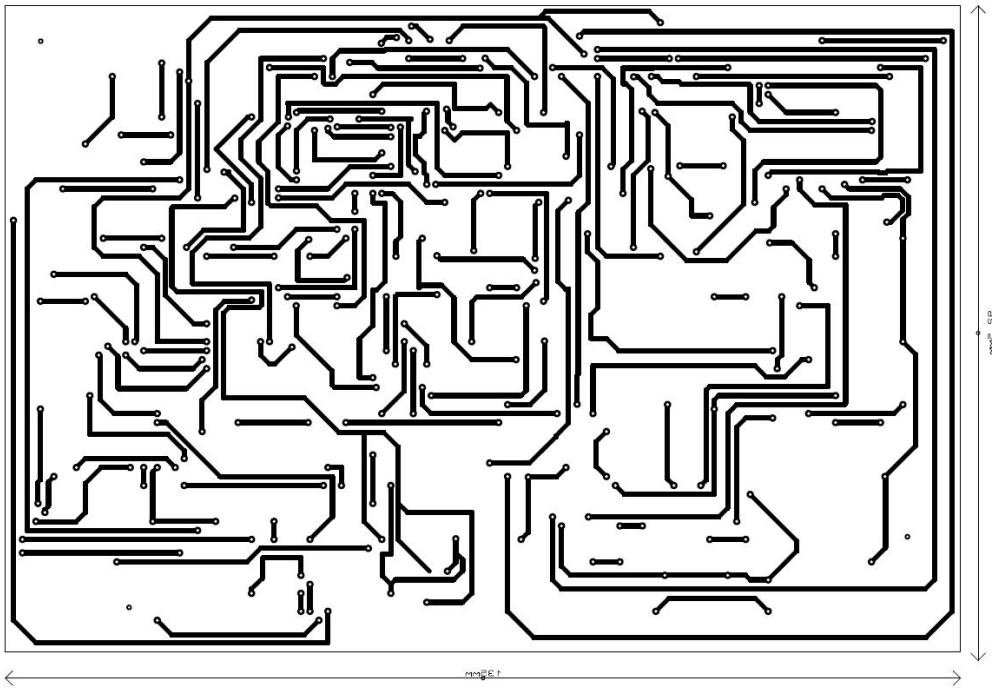
• **Ratsnest Display:**

- **Color:** Green

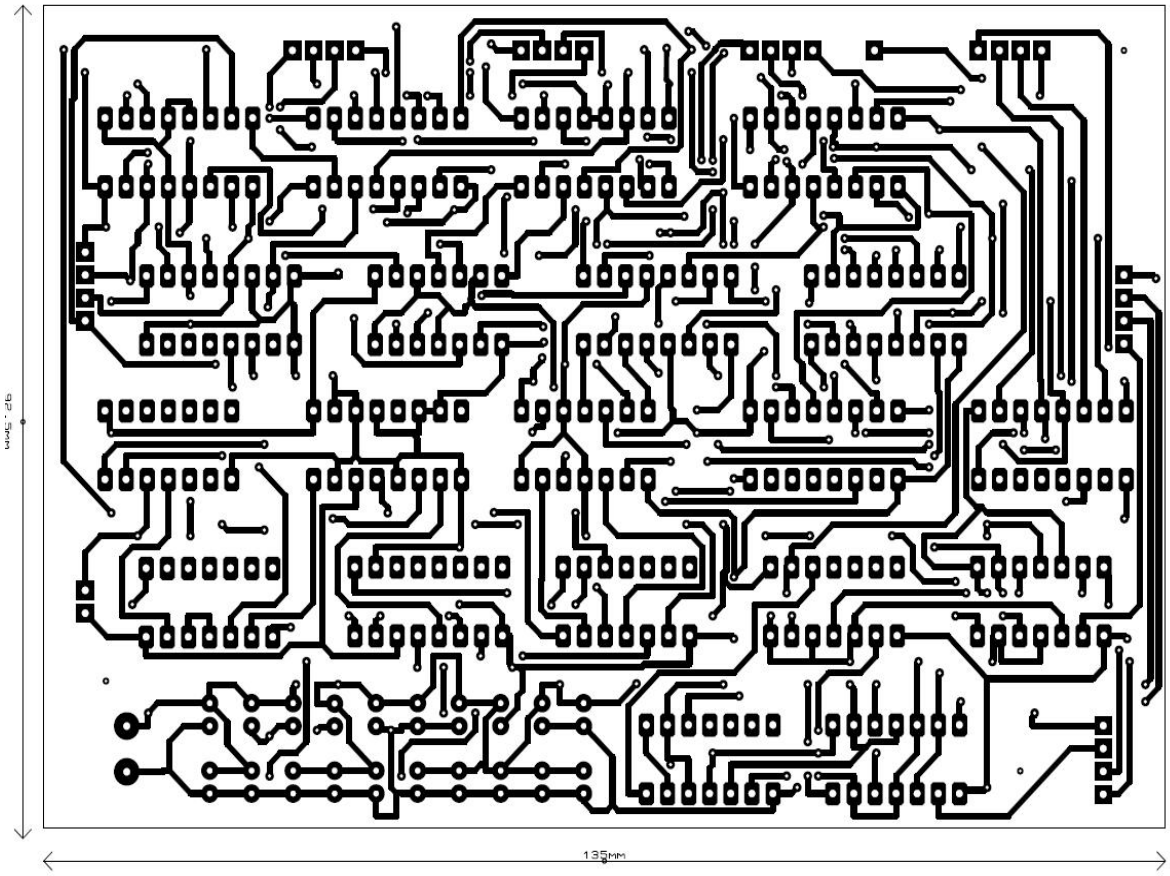
3D Visualizer:



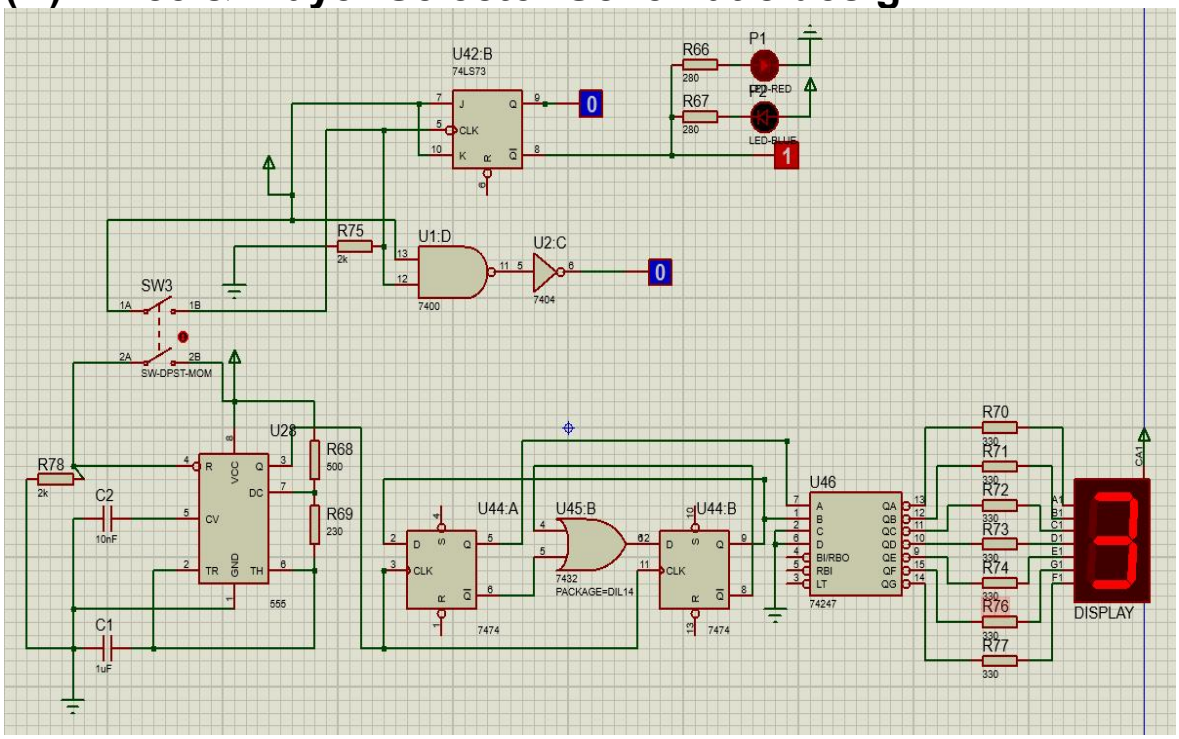
Top Layer Ouput :Mirror



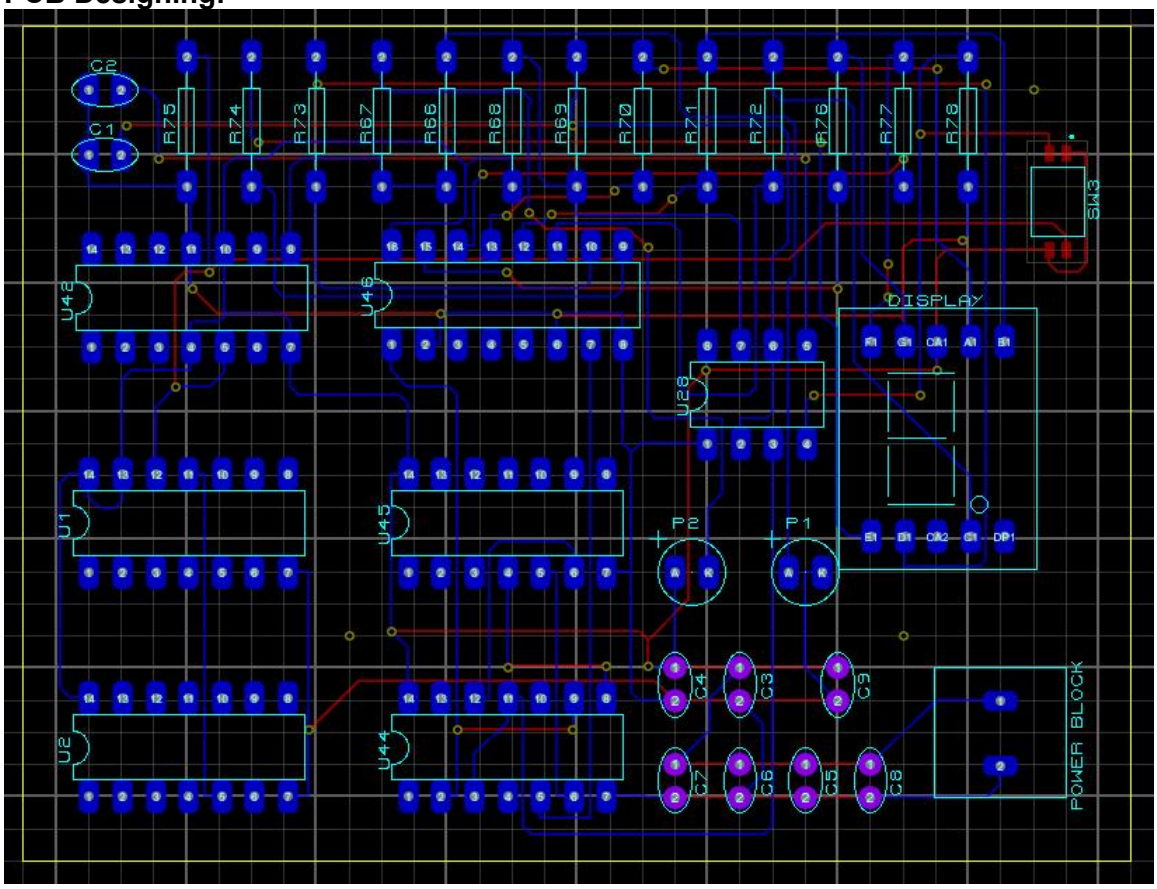
Bottom Layer Output :Normal



(B) Dice & Player Selector Schematic design:



PCB Designing:



Explanation:

In the PCB technology portion, Design Rule Manager part:

A)Design Rule:

- **Pad - Pad** Clearance: 10 th
- **Pad - Trace** Clearance: 10 th
- **Trace - Trace** Clearance: 10 th
- **Graphics** Clearance: 15 th
- **Edge/Slot** Clearance: 15 th

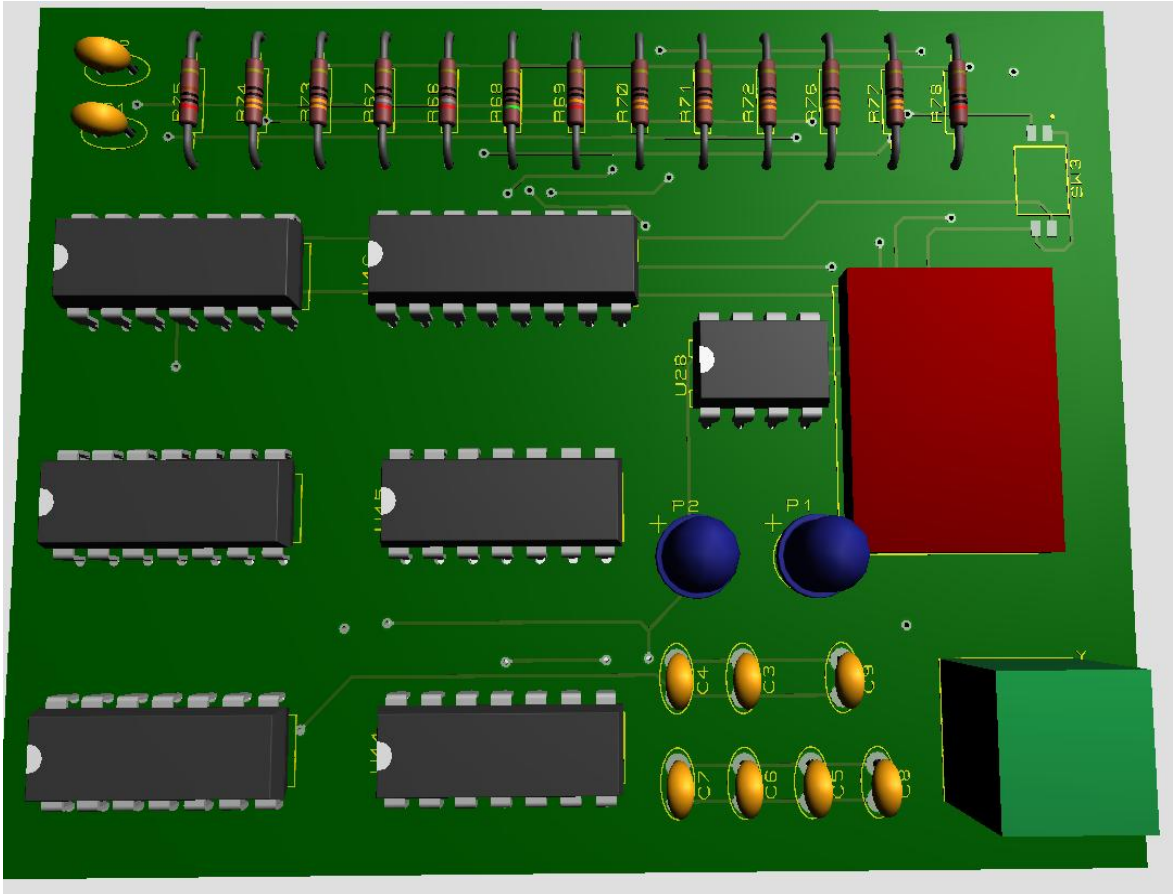
B)Net Classes:

Both **POWER** & **SIGNAL**. Here are the configurations **:** • **Routing Styles:**

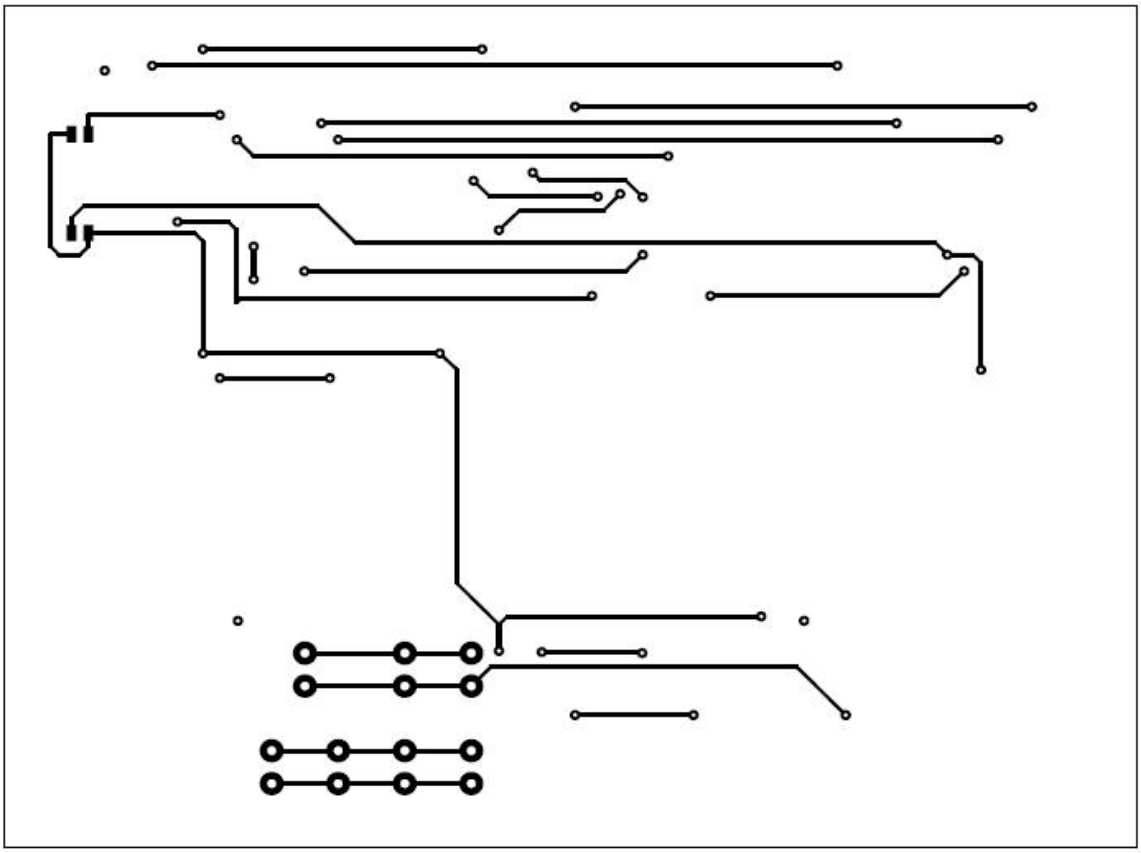
- **Trace** Style: DEFAULT
- **Via** Style: DEFAULT

- **Via Type: Thru-Hole**
- **Ratsnest Display:**
  - **Color:** Green

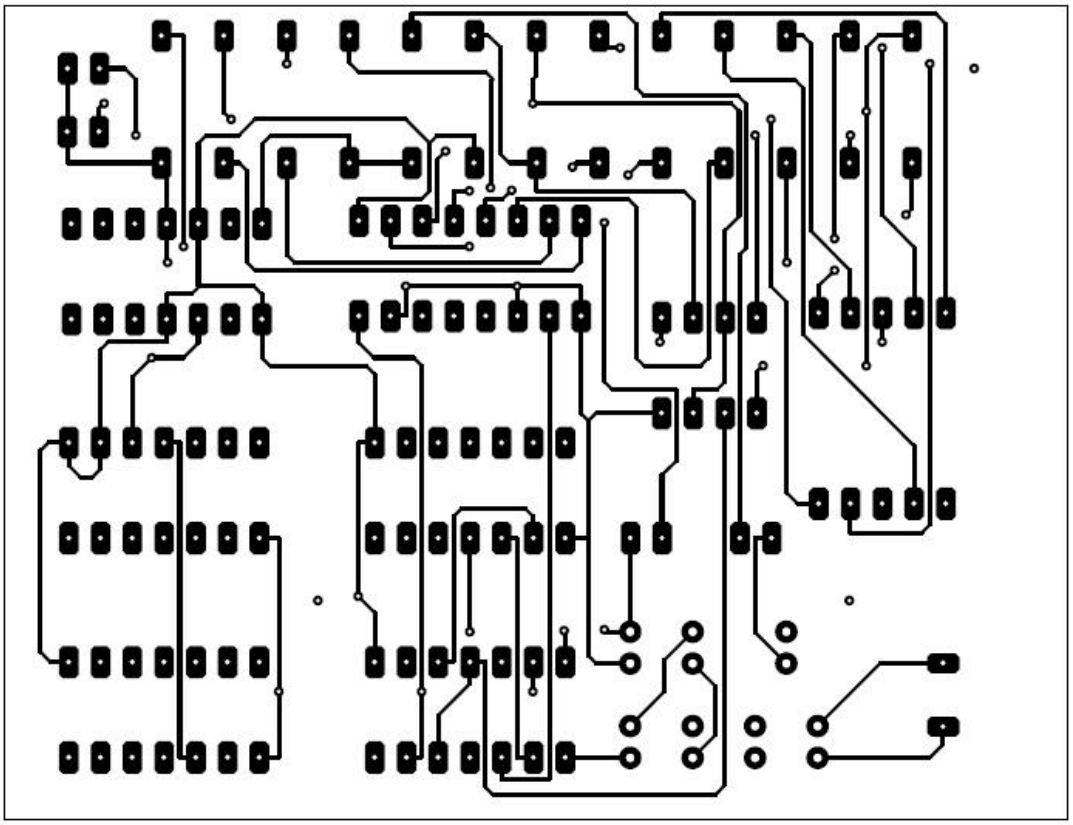
3D Visualizer:



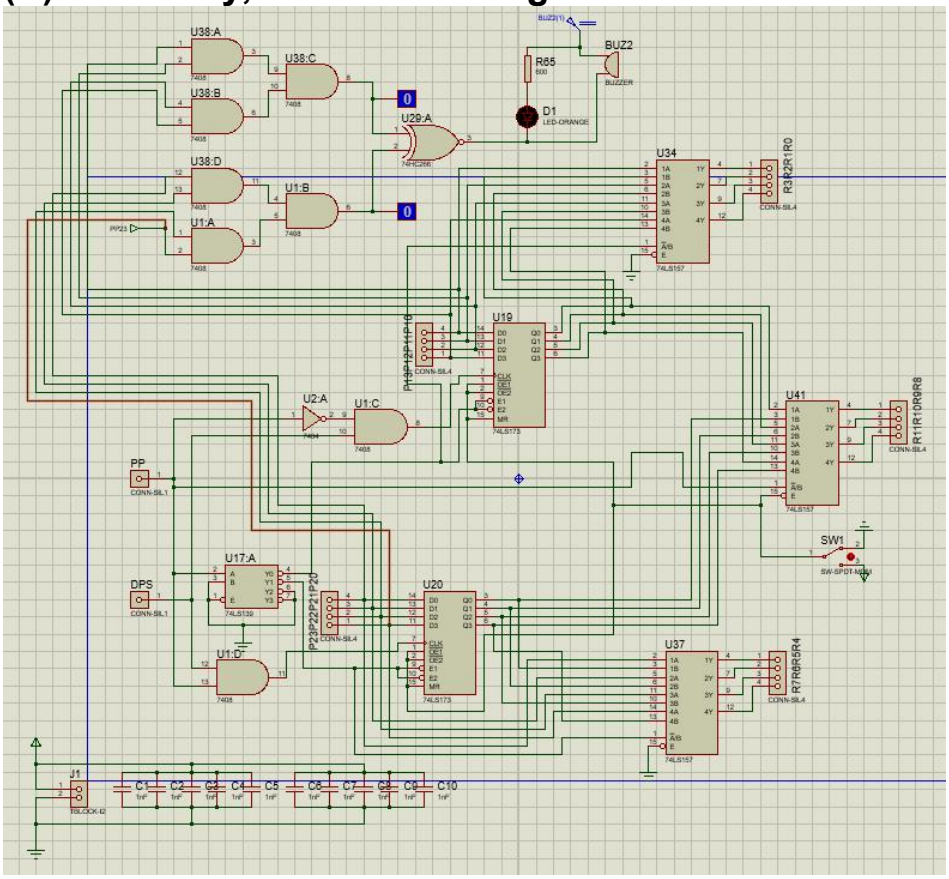
Top Layer Ouput :Mirror



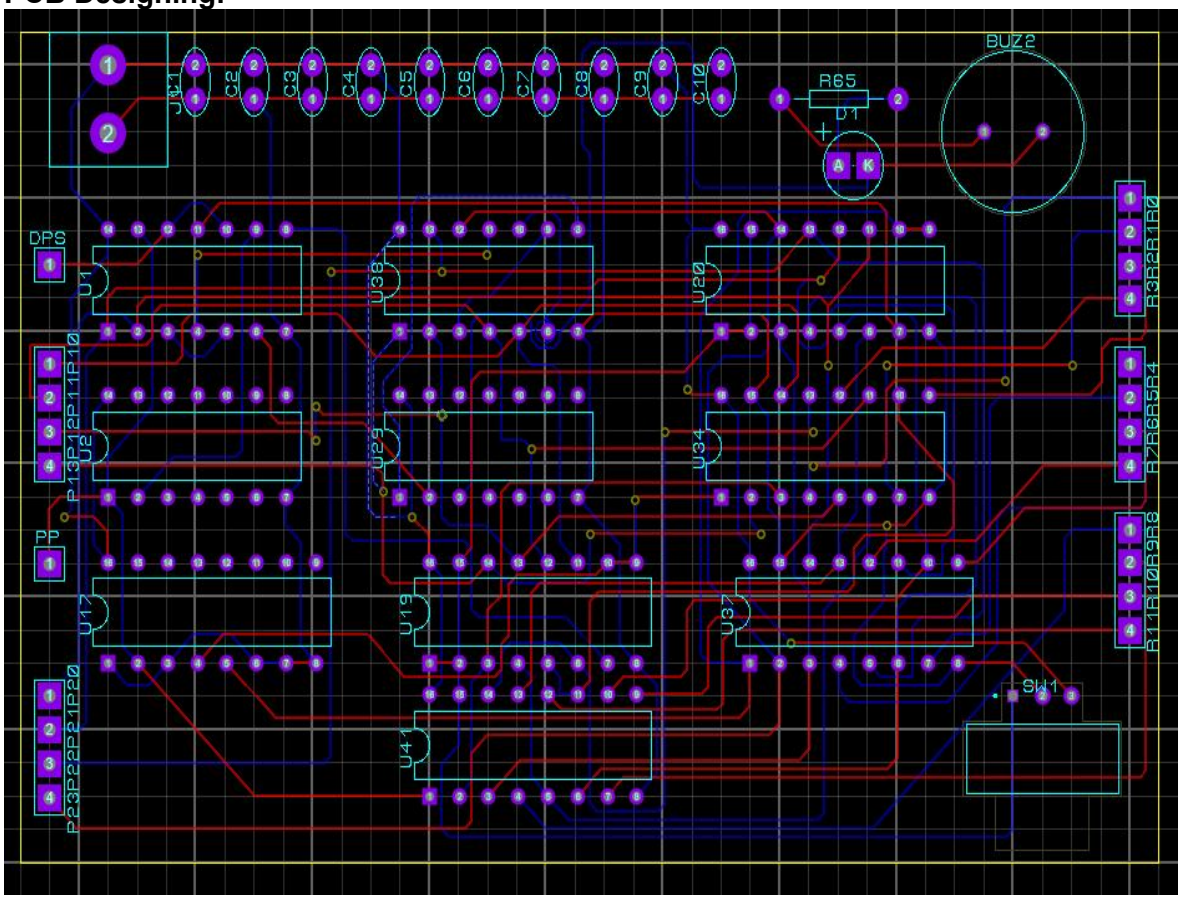
Bottom Layer Ouput :Normal



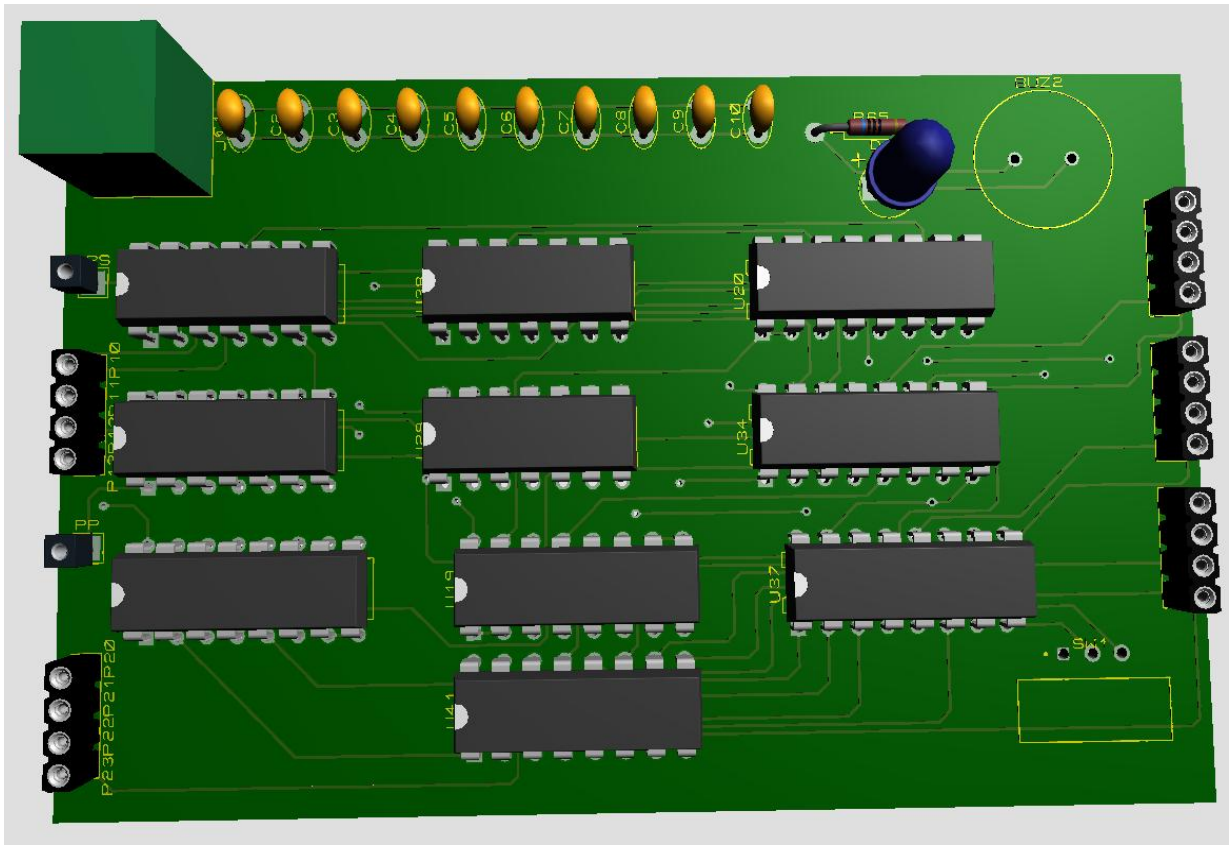
(C) Memory,Reset & Winning modul Schematic design:



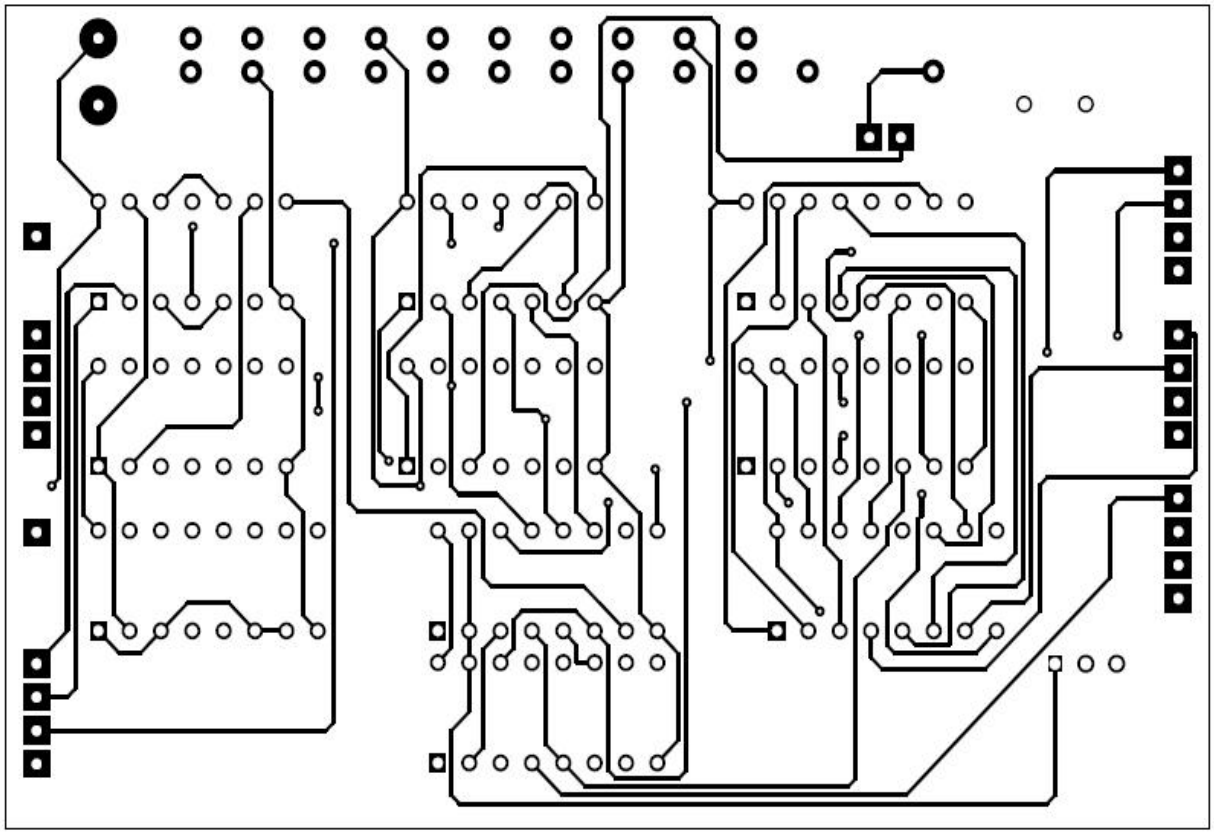
PCB Designing:



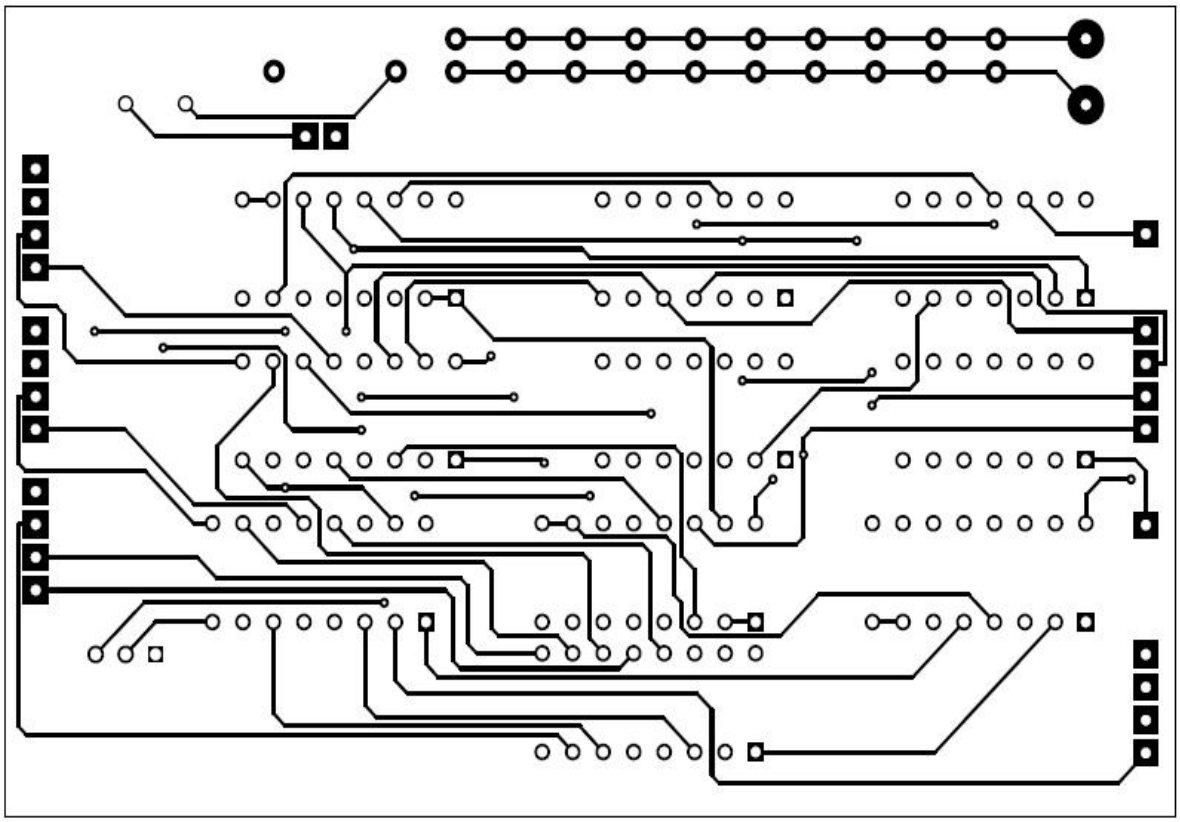
3D Visualizer:



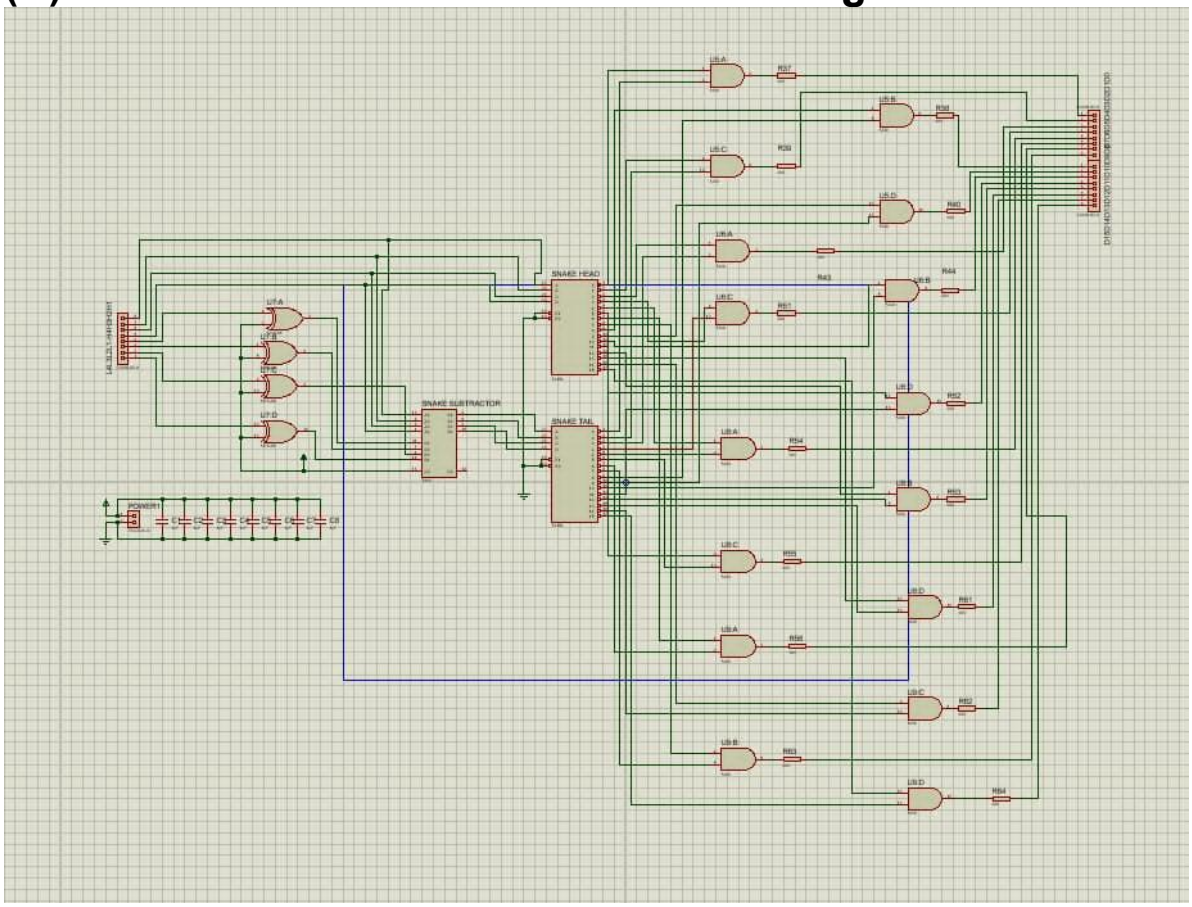
Bottom Layer Ouput :Normal



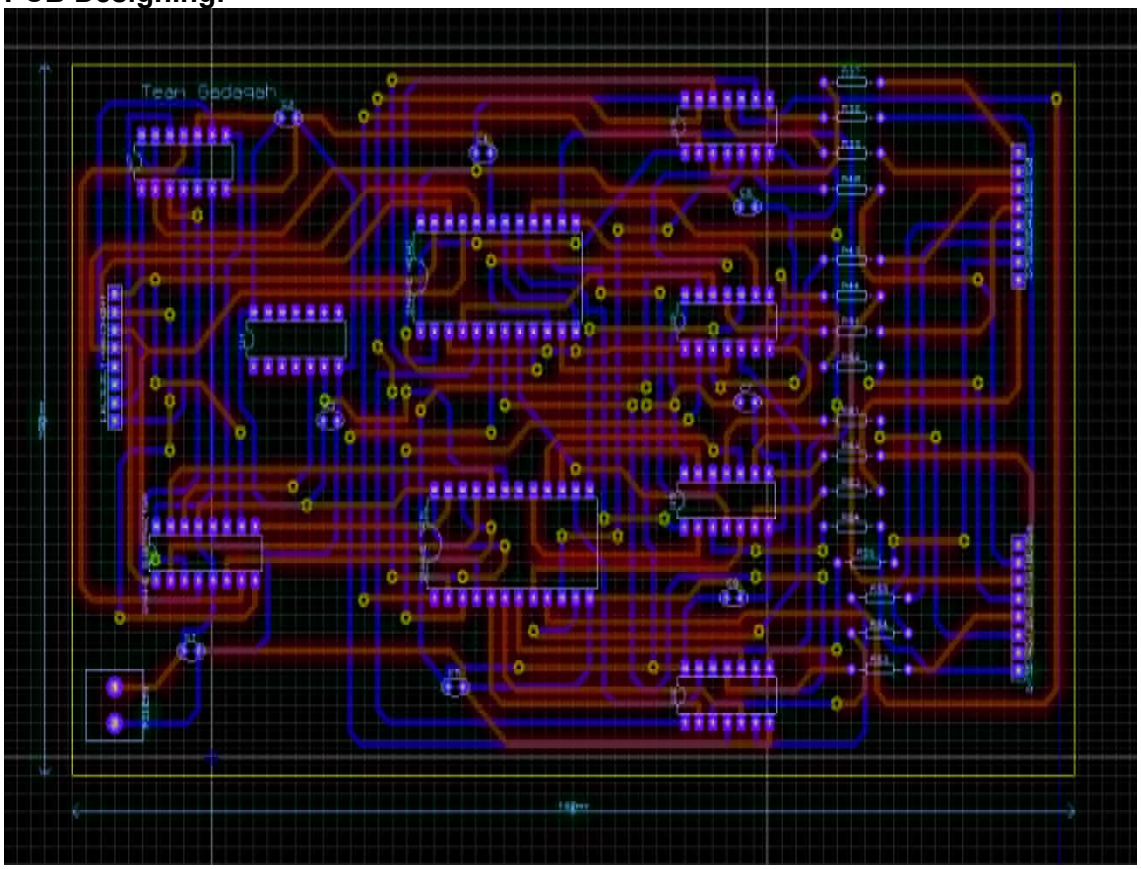
Top Layer Ouput :Mirror



(D)Snake Position ModuleSchematic design:



PCB Designing:



Explanation:

In the PCB technology portion, Design Rule Manager part:

A)Design Rule:

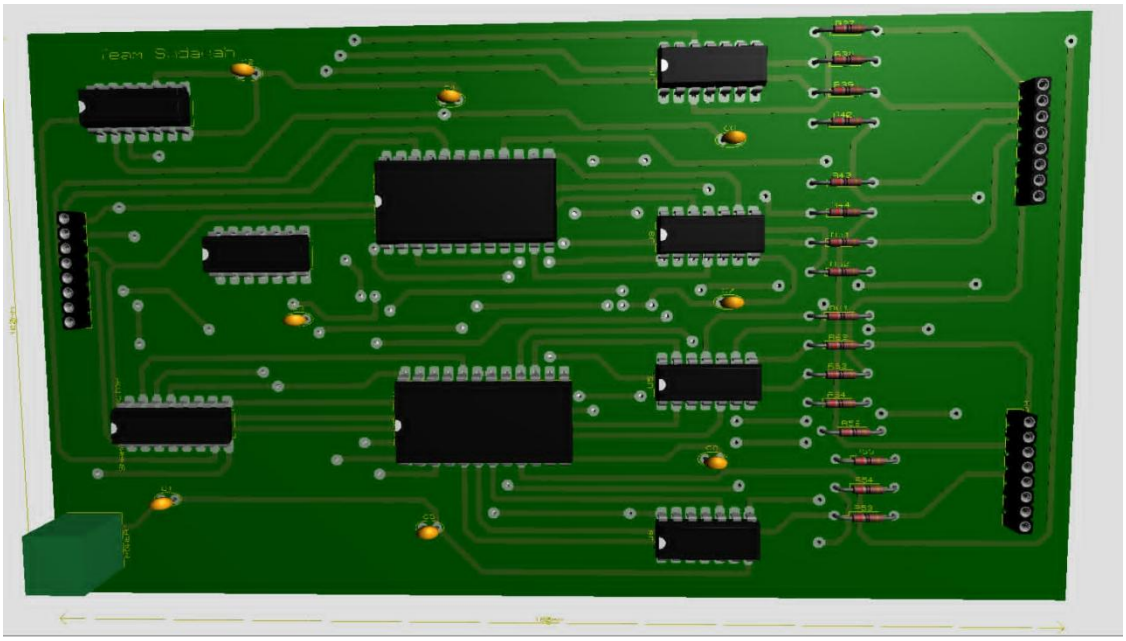
- **Pad - Pad** Clearance: 20 th
- **Pad - Trace** Clearance: 30 th
- **Trace - Trace** Clearance: 30 th
- **Graphics** Clearance: 15 th
- **Edge/Slot** Clearance: 15 th

B)Net Classes:

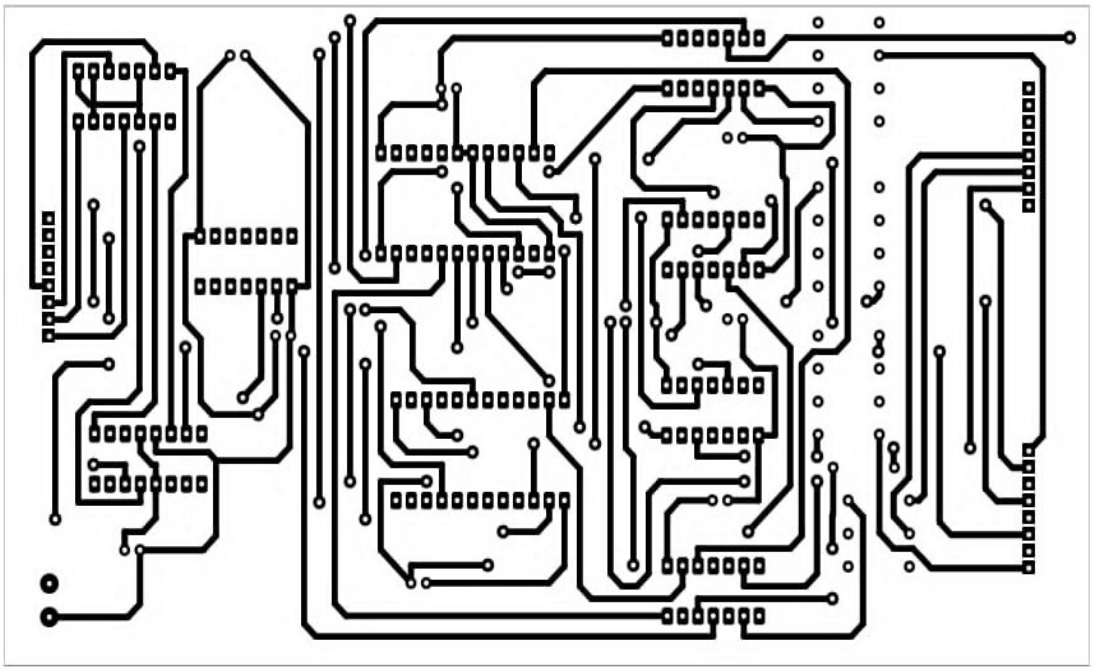
Both **POWER** & **SIGNAL**. Here are the configurations **:**

- **Routing Styles:**
  - **Trace** Style: T40
  - **Via** Style: V80
- **Via Type: Thru-Hole**
- **Ratsnest Display:**
  - **Color:** Green

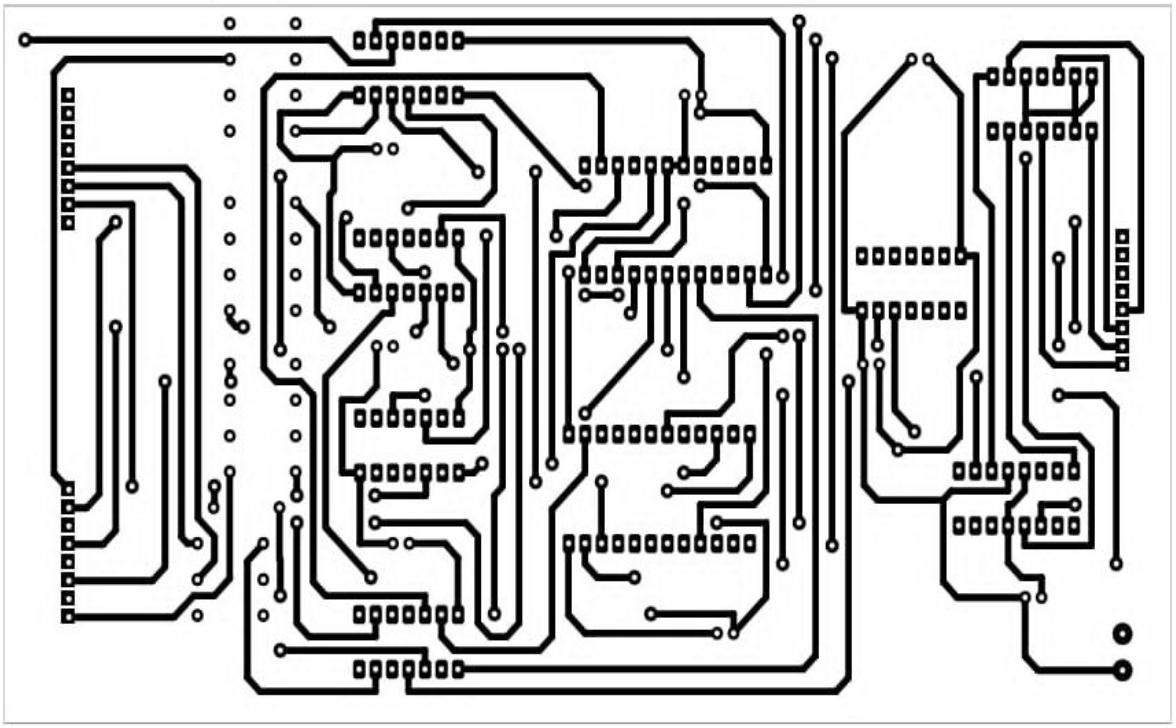
3D Visualizer:



Bottom Layer Ouput :Normal



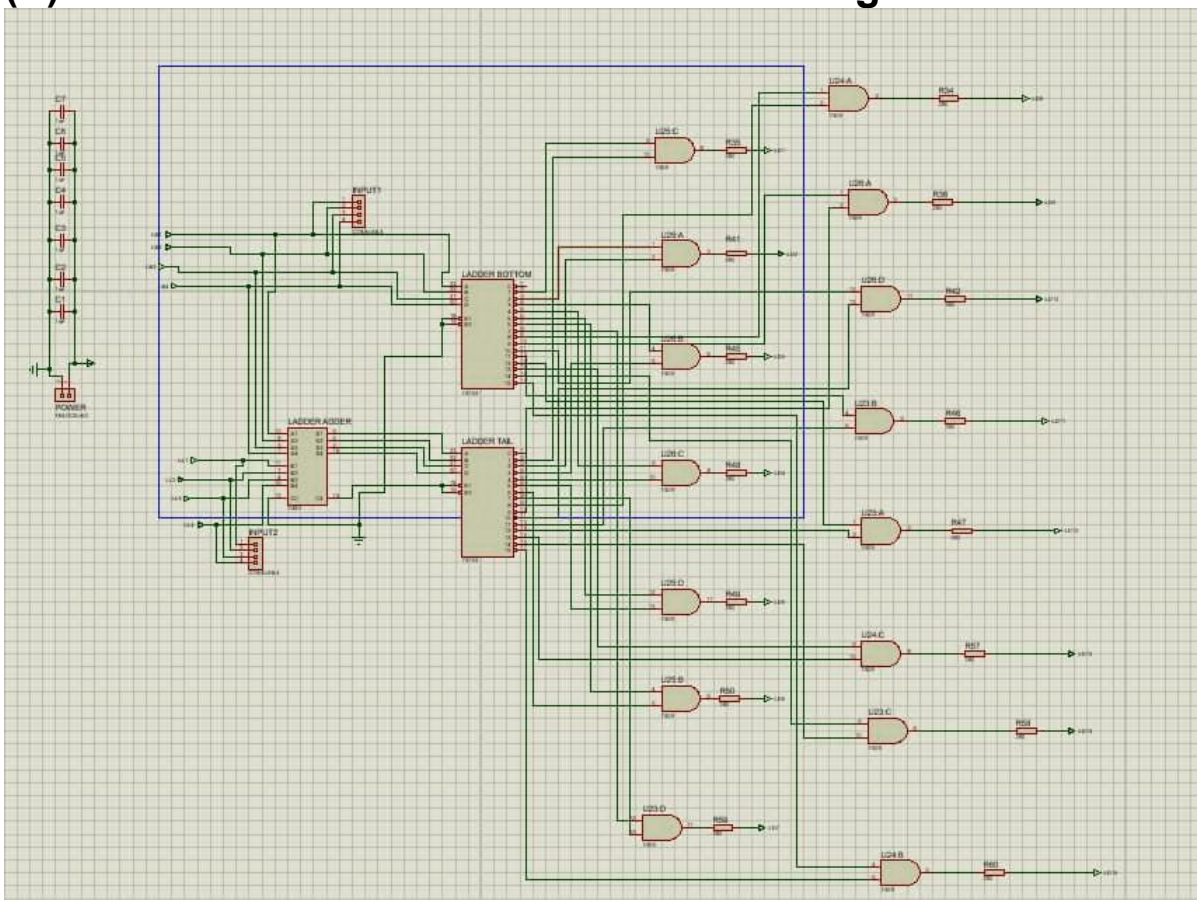
Top Layer Ouput :Mirror



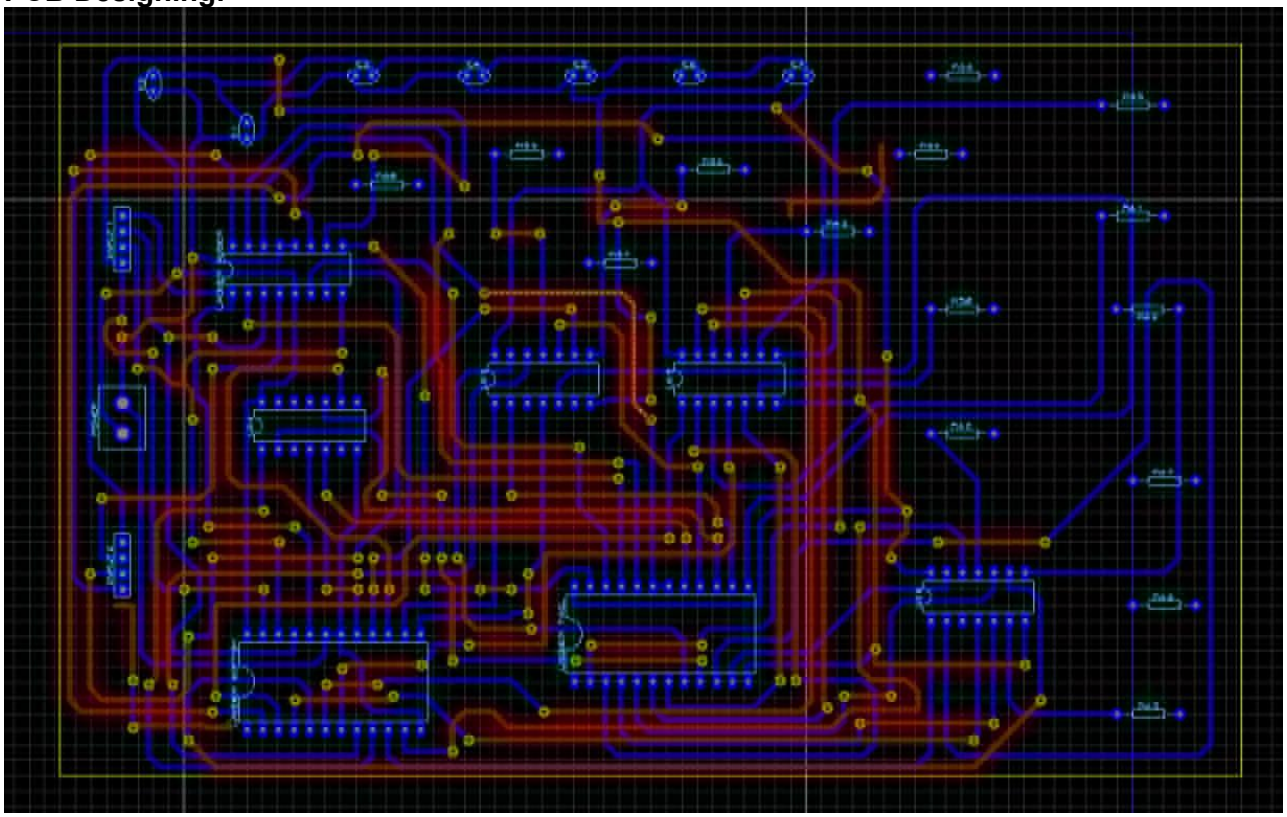
Discussion:

In this module, we have used 3 conn-sil4 and connected them with their corresponding IC's for our PCB design. A tblock has been taken for powering up the ICs. Eight(8) capacitors has been used as we have implemented the module using 8 ICs in the schematic. The capacitors are connected in parallel to the tblock to prevent the current overflowing. Once every component is in the PCB, we employ a gate-swap optimizer. We set the design rule manager then. DIL Pad, Square through hole pad, and round through hole pad have been used as they are larger. Some parameters were changed to avoid DRC error like we have used pad to pad 20th, pad to trace 30th, trace to trace 30th. Under the net classes Trace style T40, Via style V80 were implemented in power and signal . At first we found some DRC error while replacing the small pads by bottom copper in Pad. On the advice of one of our teachers we then implemented this using all copper and no DRC errors were found then. After this we took the help of auto router and connections were done automatically without any DRC and CRC errors. We have measured the board edge 180mm X 100mm.

(E)Ladder Position ModuleSchematic design:



PCB Designing:



Explanation:

In the PCB technology portion, Design Rule Manager part:

A)Design Rule:

- **Pad - Pad** Clearance: 10 th
- **Pad - Trace** Clearance: 10 th
- **Trace - Trace** Clearance: 10 th
- **Graphics** Clearance: 15 th
- **Edge/Slot** Clearance: 15 th

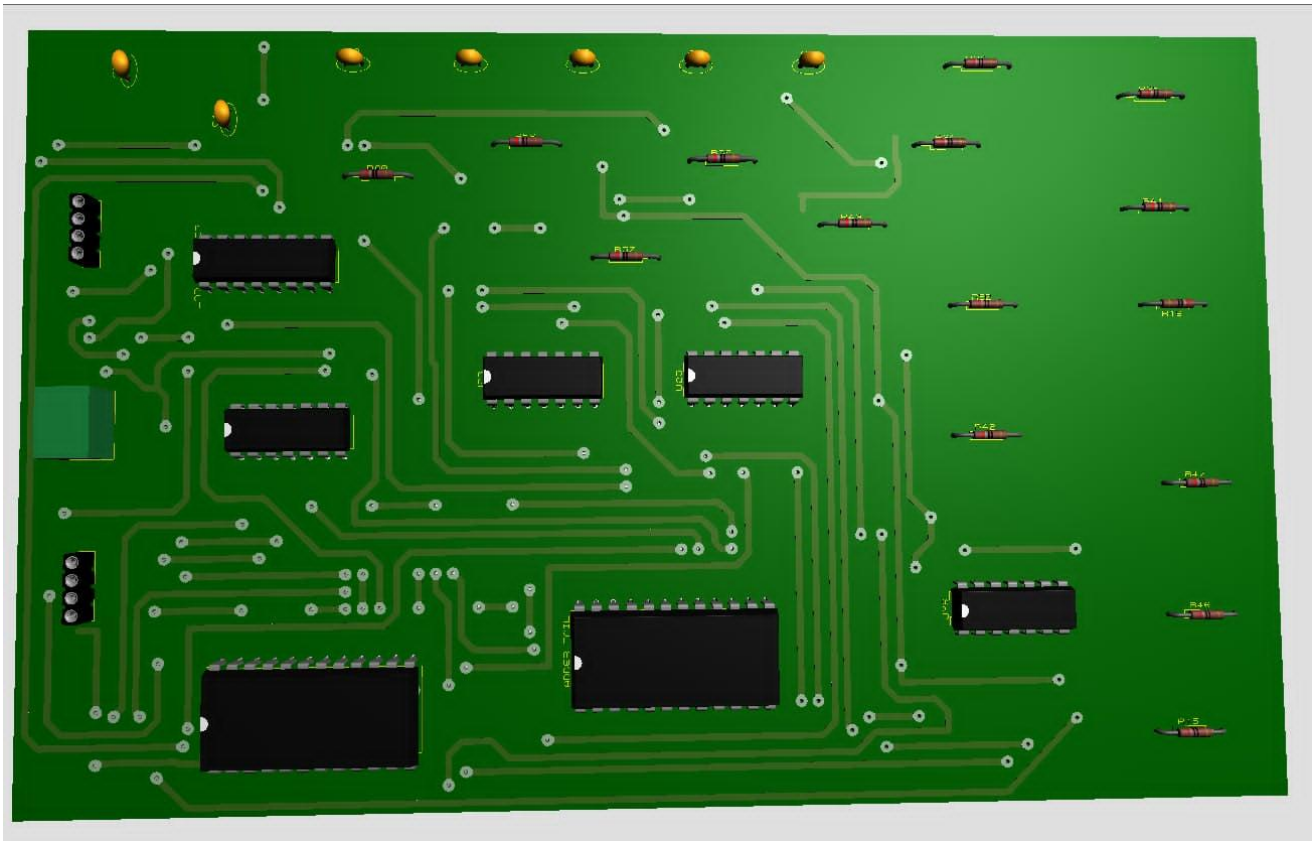
B)Net Classes:

Both **POWER** & **SIGNAL**. Here are the configurations **:** • **Routing Styles:**

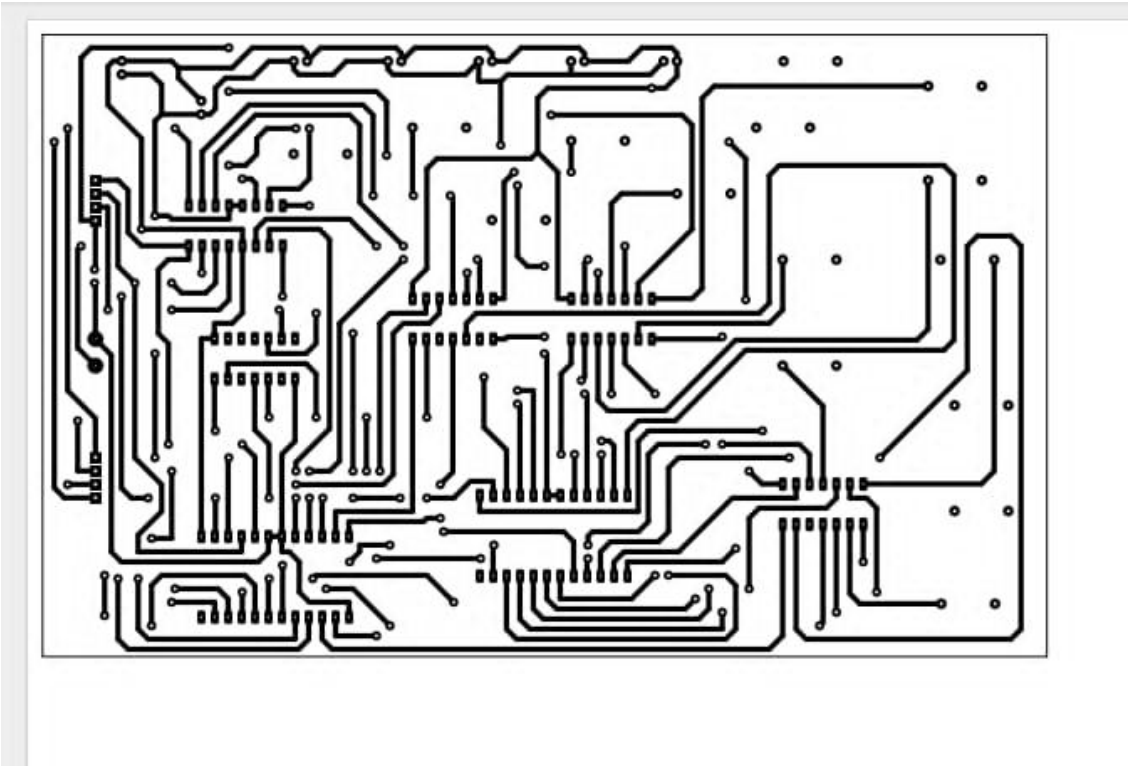
- **Trace** Style: DEFAULT
- **Via** Style: DEFAULT

- **Via Type: Thru-Hole**
- **Ratsnest Display:**
  - **Color:** Green

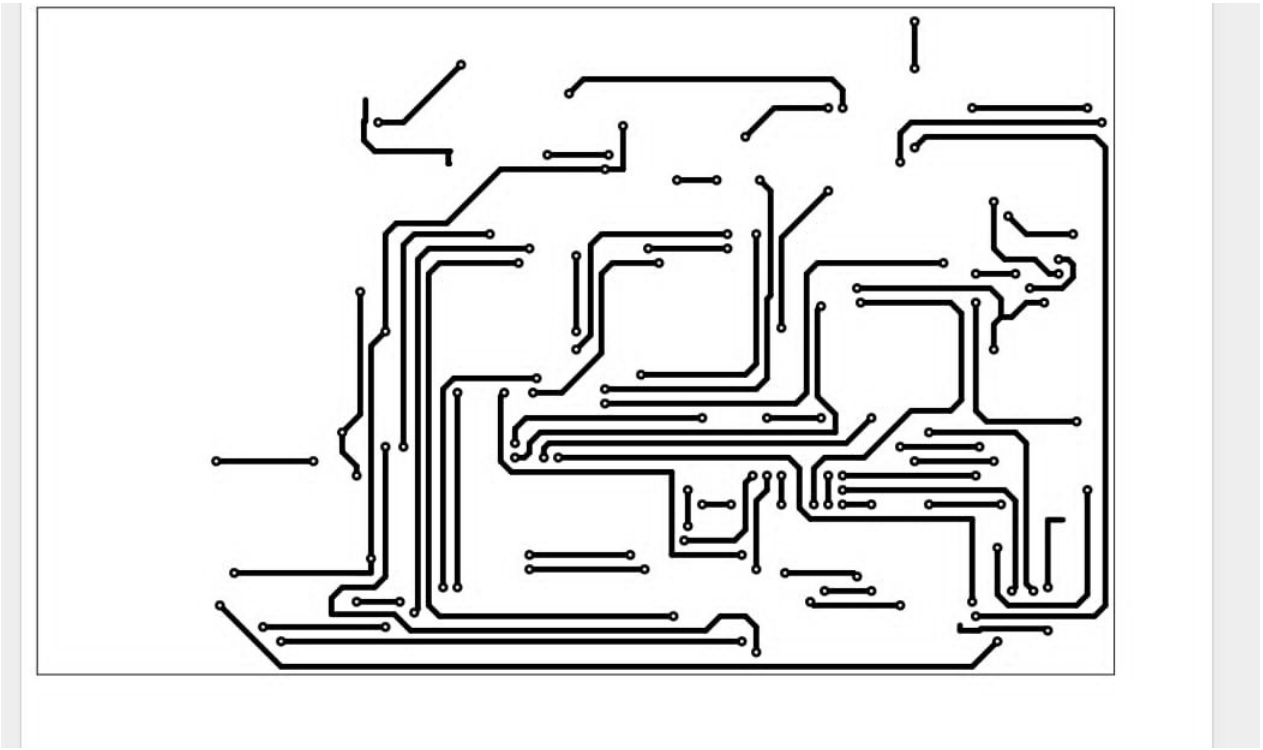
3D Visualizer:



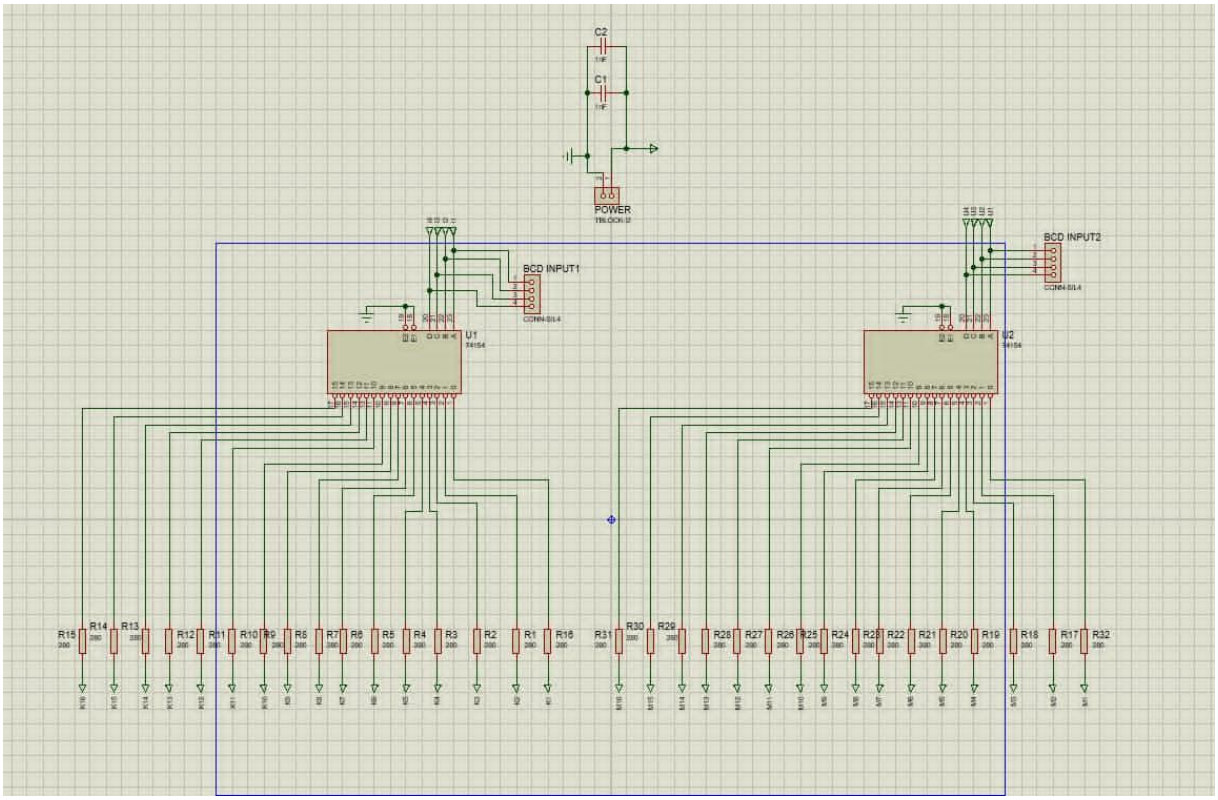
Bottom Layer Ouput :Normal



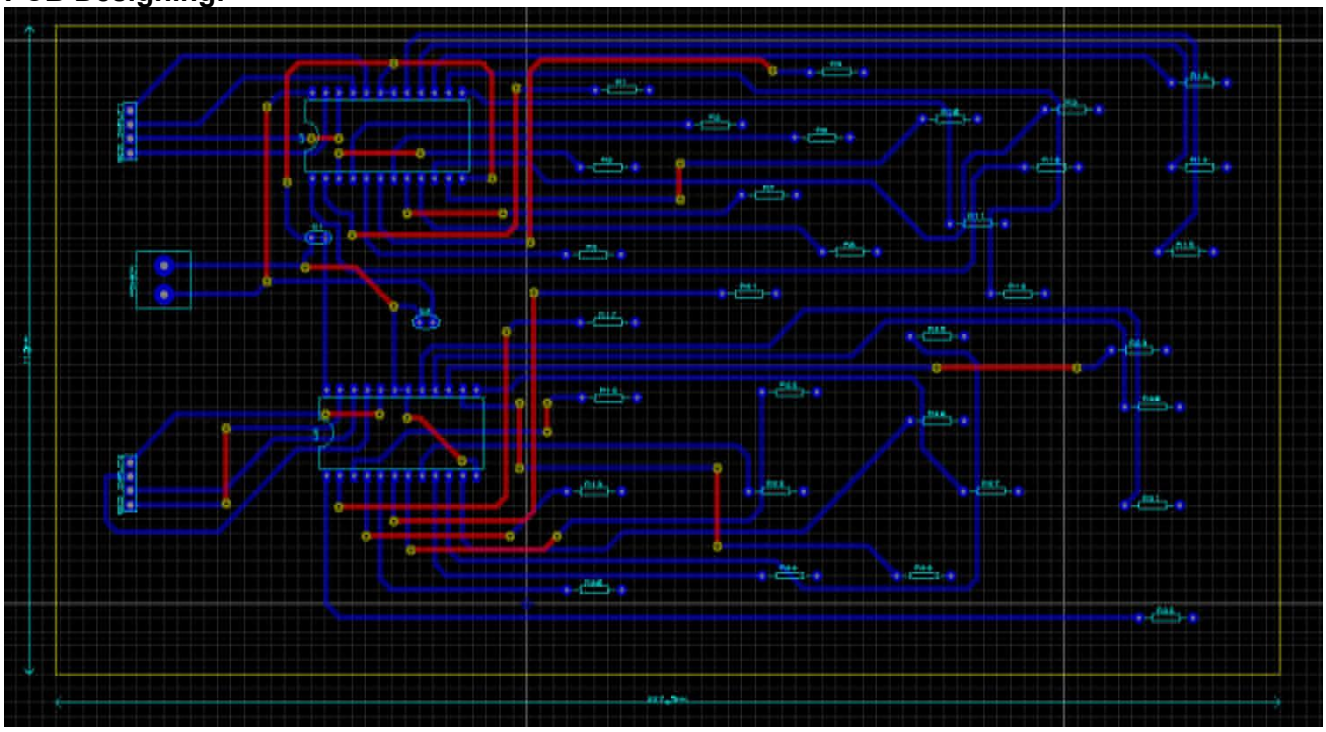
Top Layer Ouput :Mirror



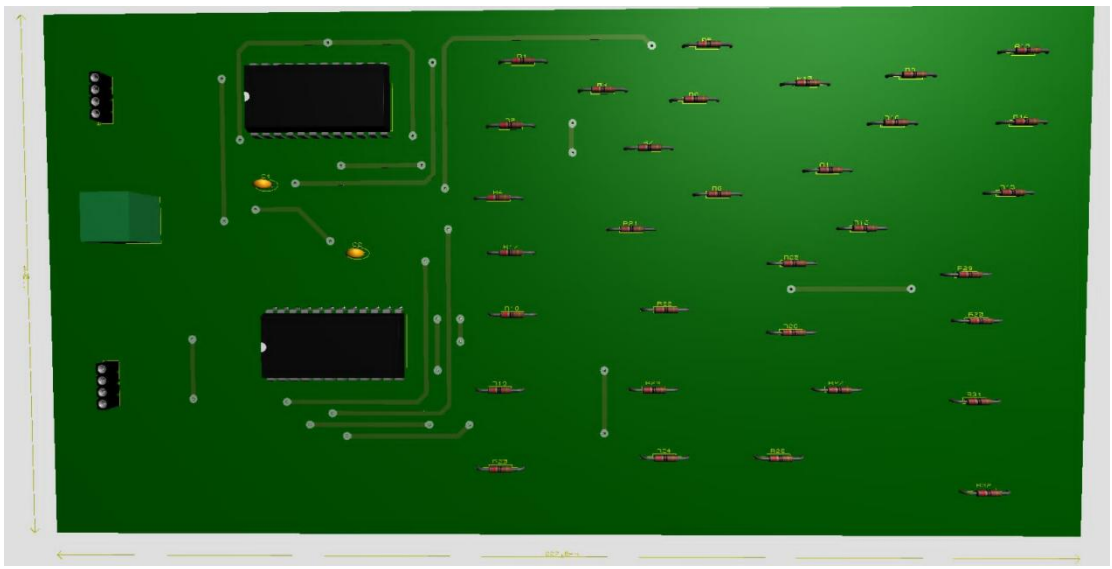
(F)Player Position Module Schematic design:



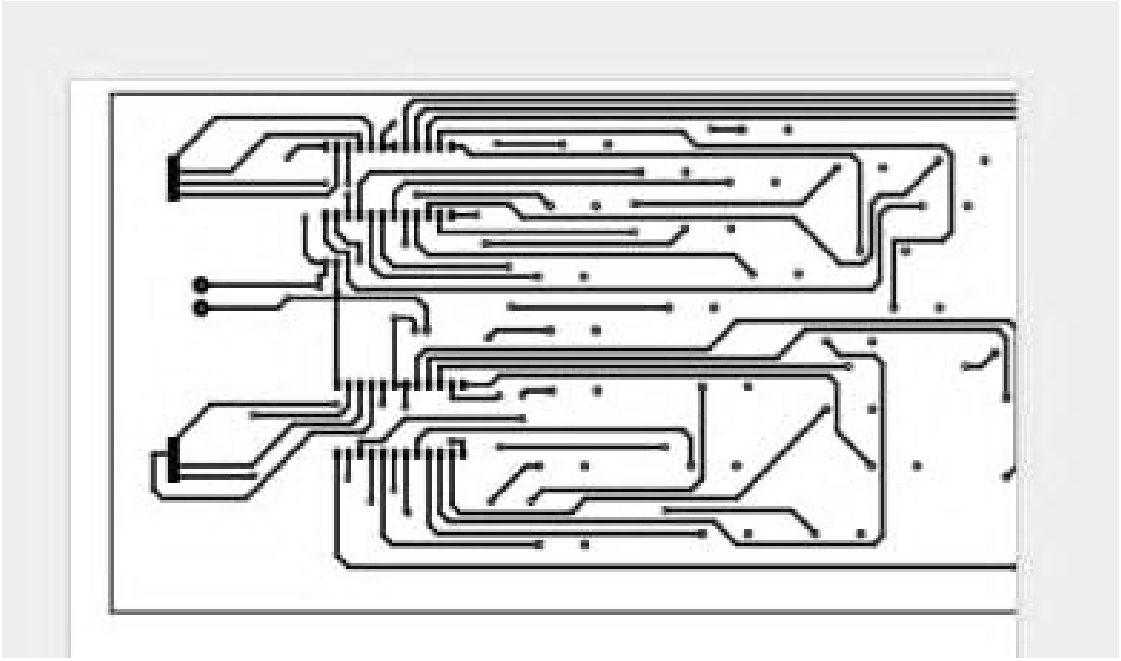
PCB Designing:



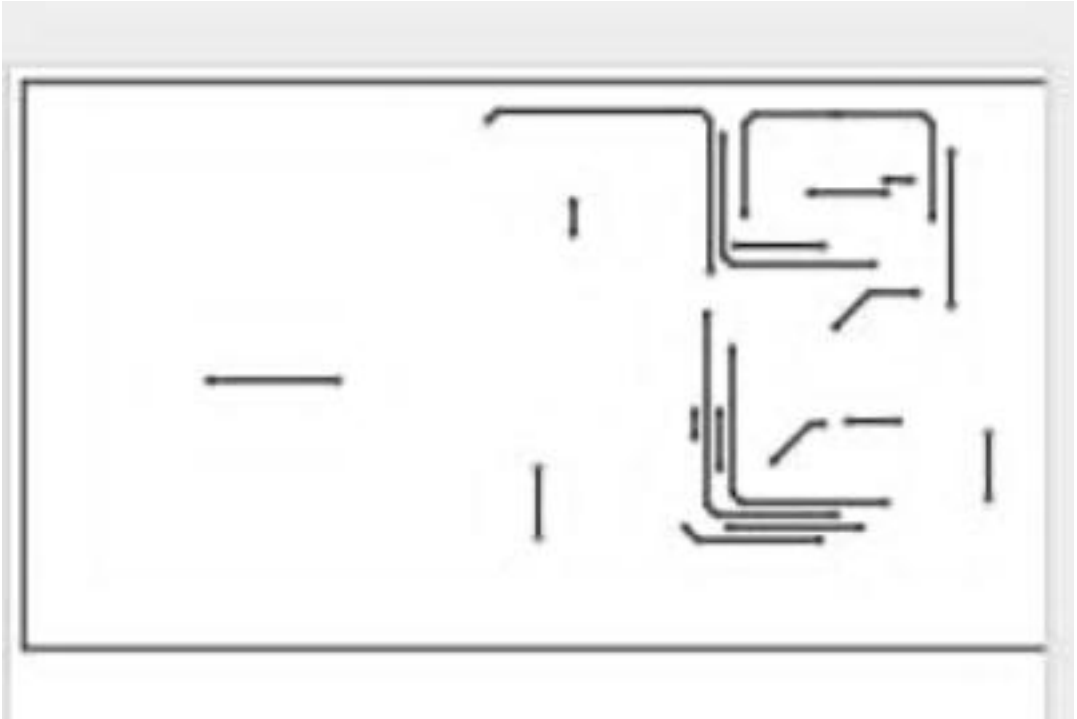
3D Visualizer:



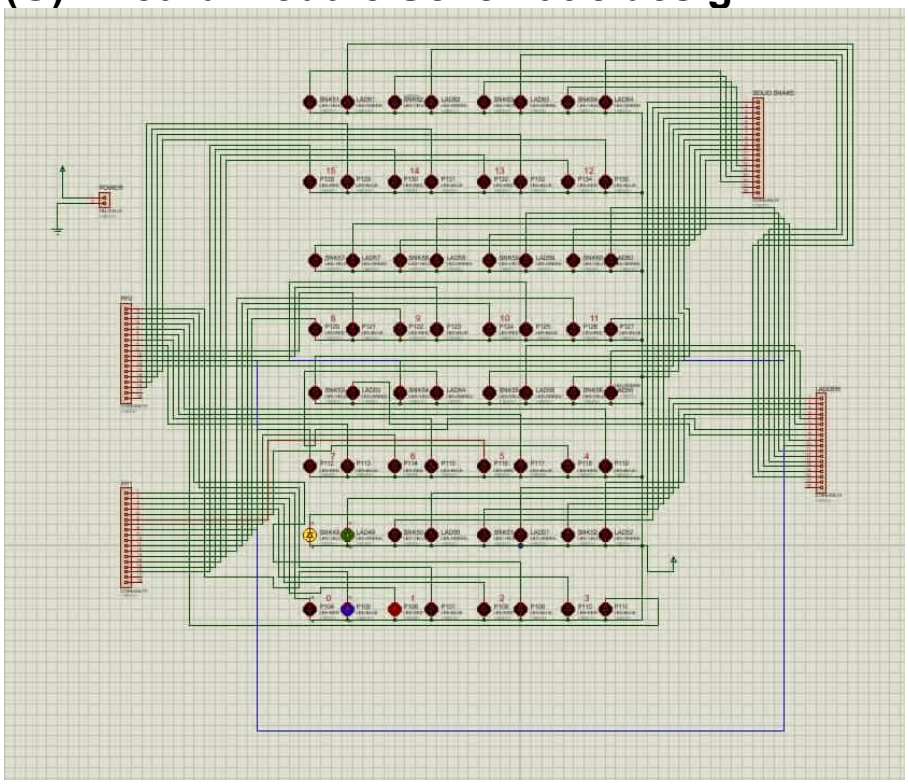
Bottom Layer Ouput :Normal



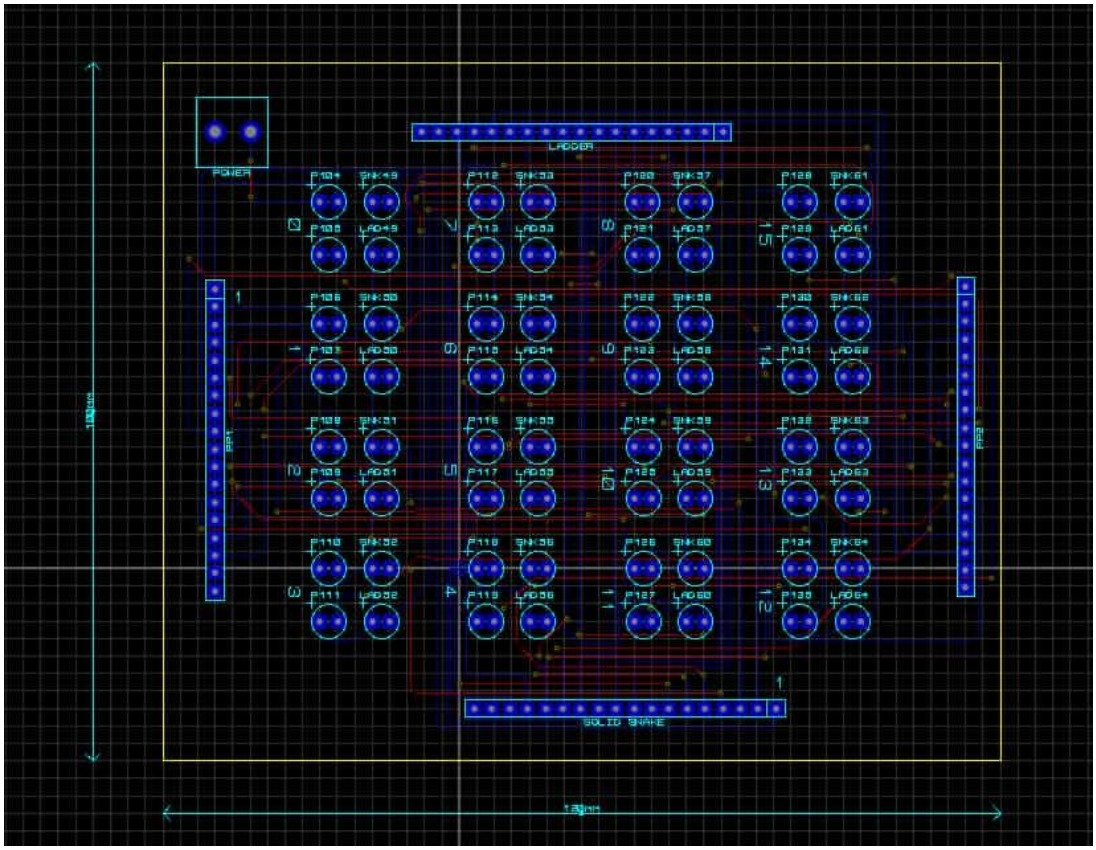
Top Layer Ouput :Mirror



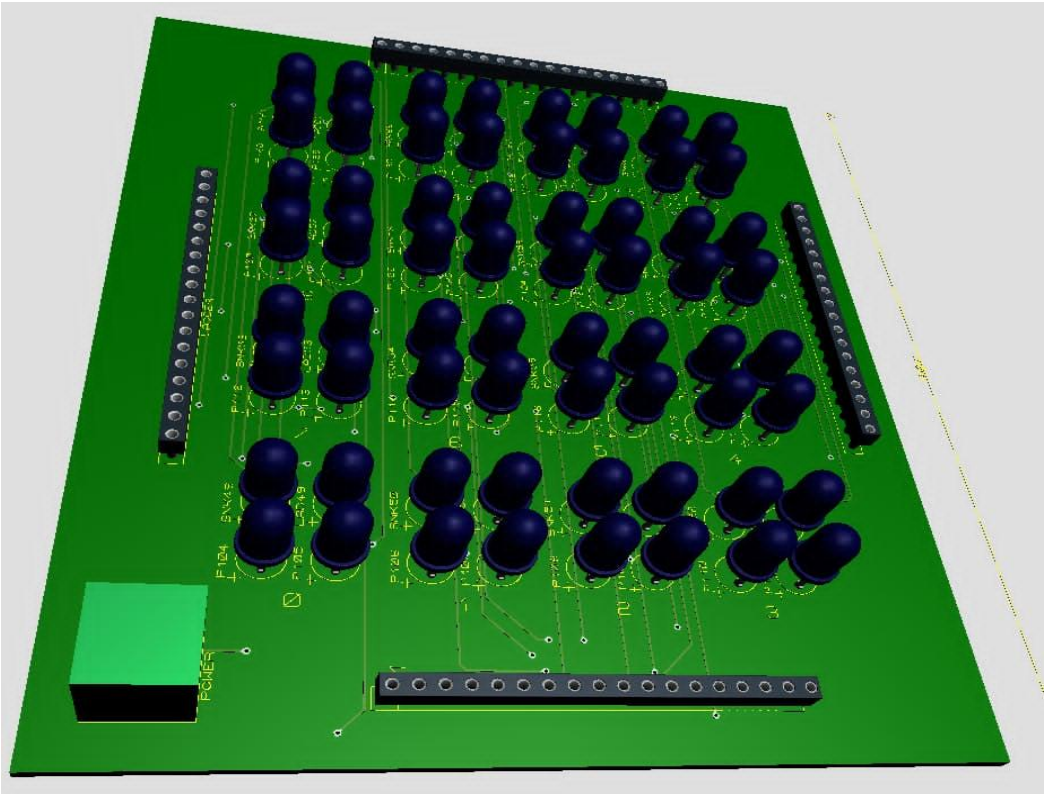
(G) Board Module Schematic design:



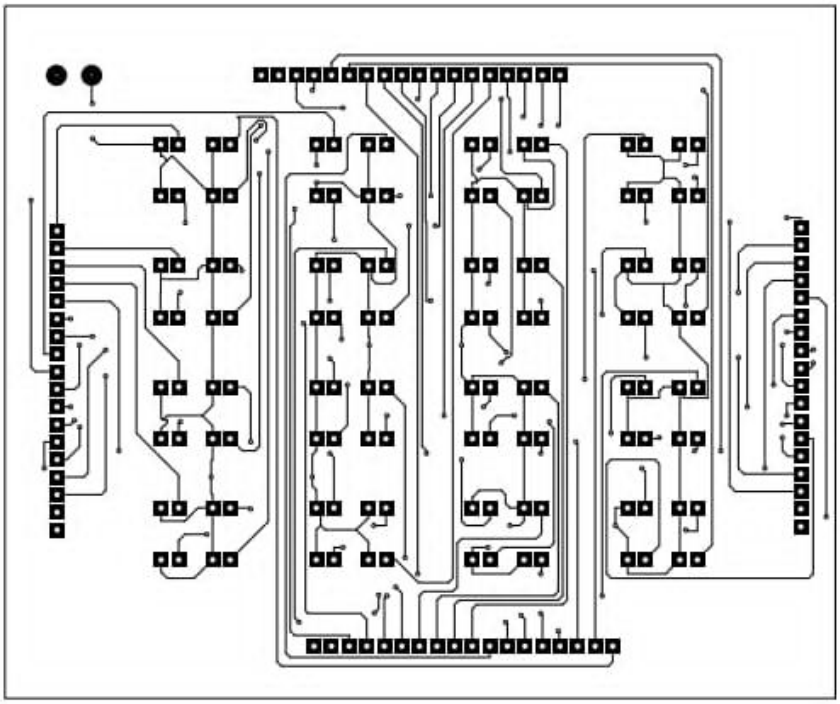
PCB Designing:



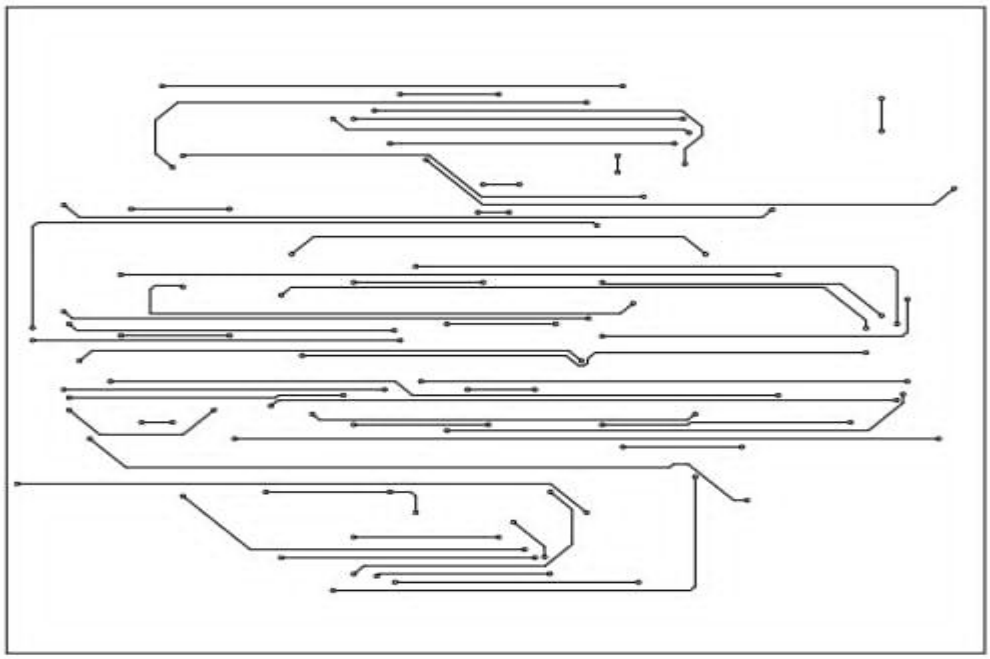
3D Visualizer:



Bottom Layer Ouput :Normal



Top Layer Ouput :Mirror



Discussion:

For designing the PCB of the board LED module, first, a board edge was selected with dimensions width x height = 120 mm x 100 mm. Then all of the components were placed on that board. The pads were replaced with only bottom copper pads to avoid any soldering issues. After aligning the LEDs and other components, design rule parameters were set. For power and signal net class, via type was selected as through hole, and all other settings were left at default. Then, the auto-router was applied. Finally, all the levels (level 0 to 15) were labeled in the PCB's top silk.

Group member contribution:

1. PDF written by Shazzad Ahmed Chowdhury, Mahib Abtahi, Ahnaf Sakif and Hasib Ahmed Anik
2. Snake & Ladder Logic PCB by Shazzad Ahmed Chowdhury
3. Dice Module PCB by Ahnaf Sakif
4. Snake Position PCB by Mahib Abtahi
5. Ladder Position PCB by Fahim Rezwan Shifat
6. Board Module PCB by Abdullah Jubayer
7. Player position Decoder PCB by Faiad Faisal Sarthok and Fahim Rezwan Shifat
8. Memory,Reset and Winning module PCB implemented by Shazzad Ahmed Chowdhury, Ahnaf Sakif and Faiad Faisal Sarthok