

Write-Rationing Garbage Collection for Hybrid Memories

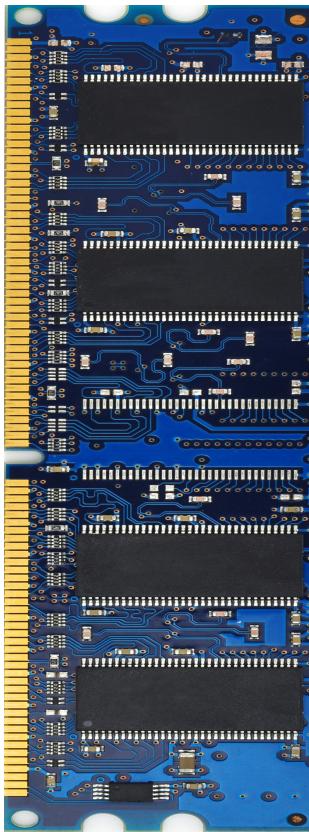
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DRAM is facing challenges

Scalability
Cost
Energy
Reliability



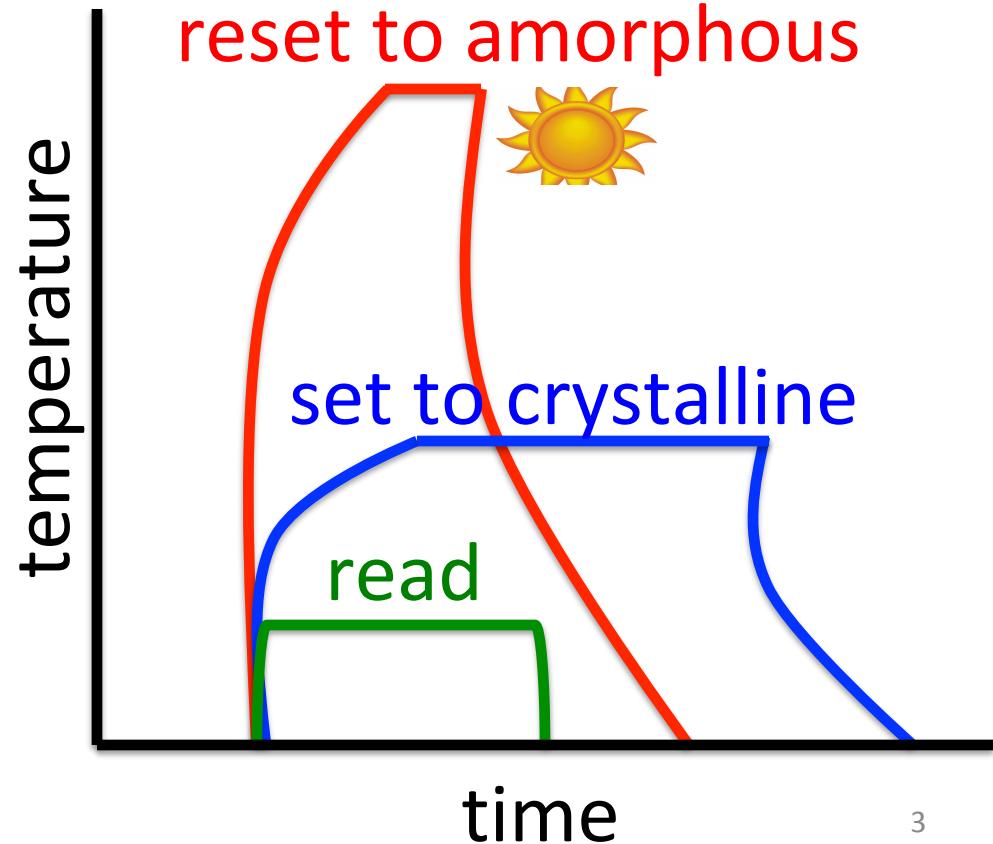
Phase change memory

Persistent

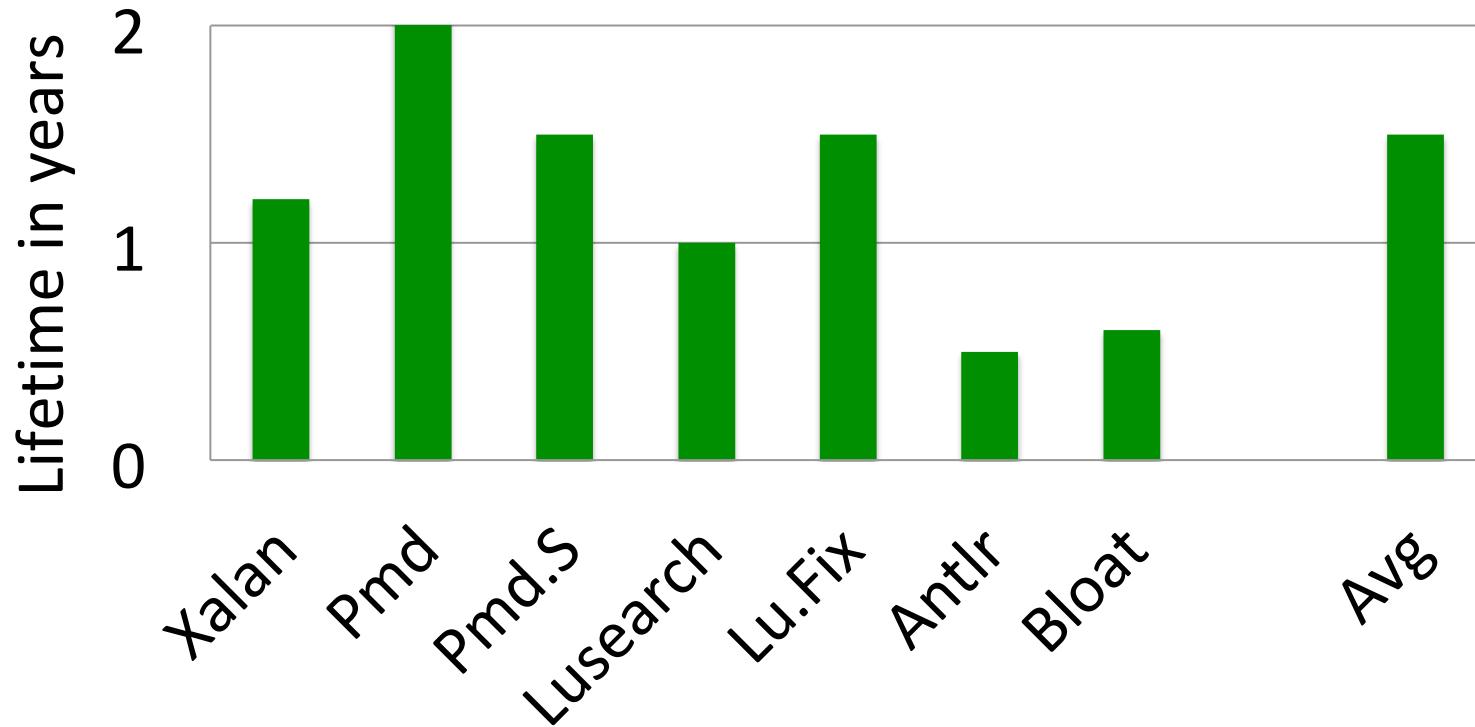
Byte addressable

High latency

Low endurance



PCM only is not practical



32 GB PCM with hardware wear-levelling

Hybrid DRAM-PCM memory

Speed
Endurance

Energy
Capacity

DRAM

Challenges

PCM

Bridging the DRAM-PCM latency gap

Mitigating PCM wear-out

Prior art in mitigating PCM wear-out

Hardware wear-leveling

Spread writes out across PCM

32 GB PCM lasts only two years!

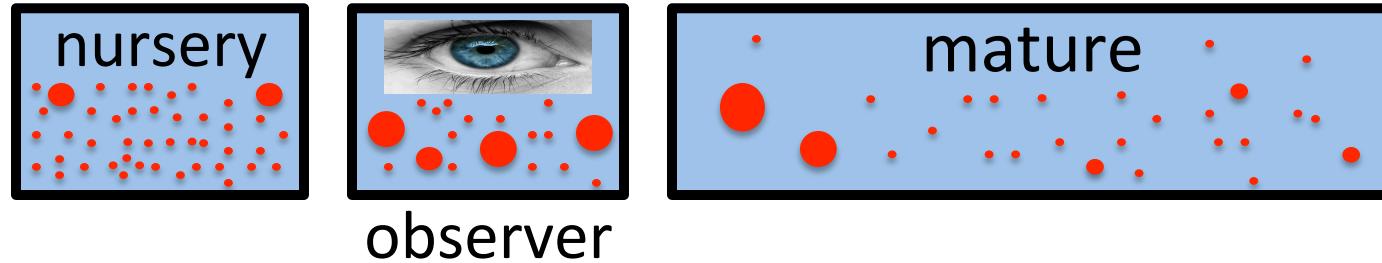
OS write partitioning

Keep highly written pages in DRAM

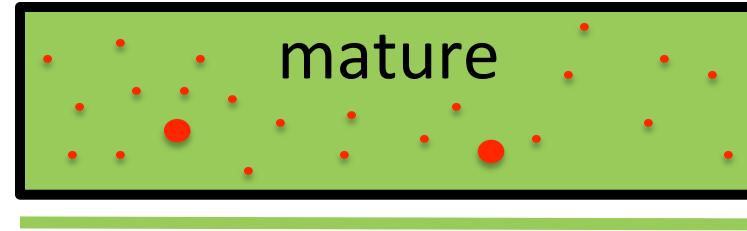
Coarse granularity

Costly page migrations

Garbage collection for hybrid memory



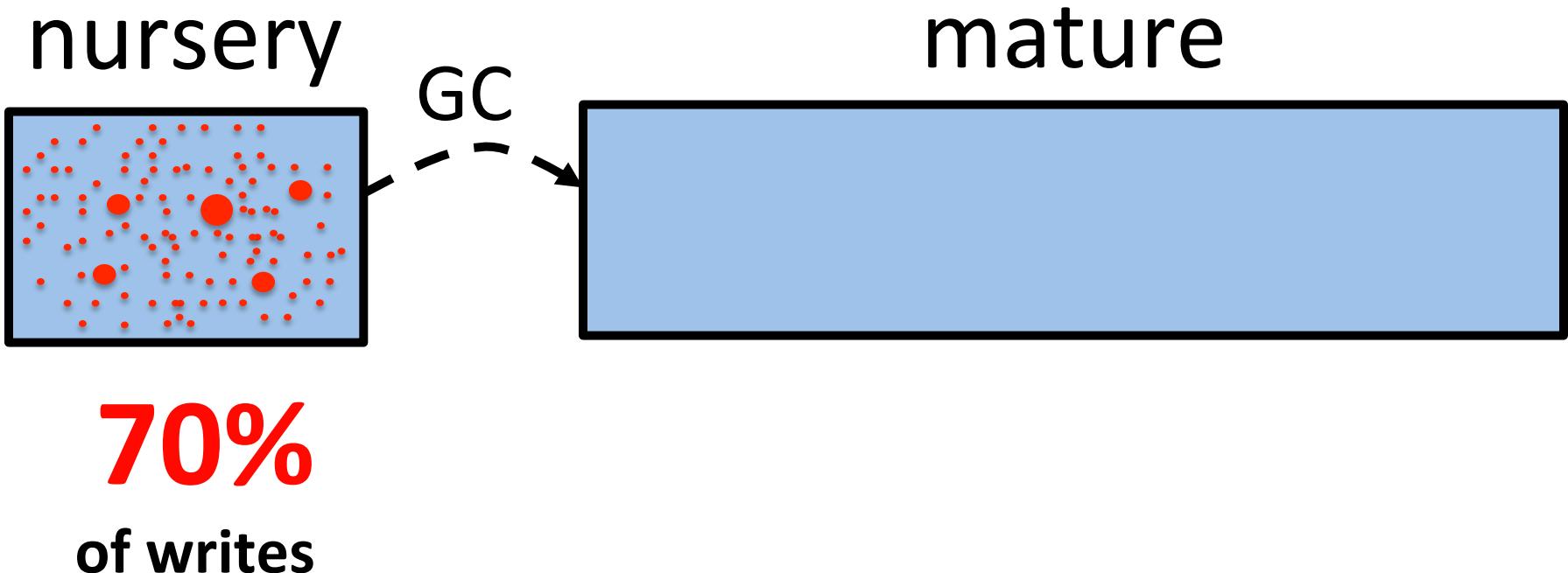
DRAM



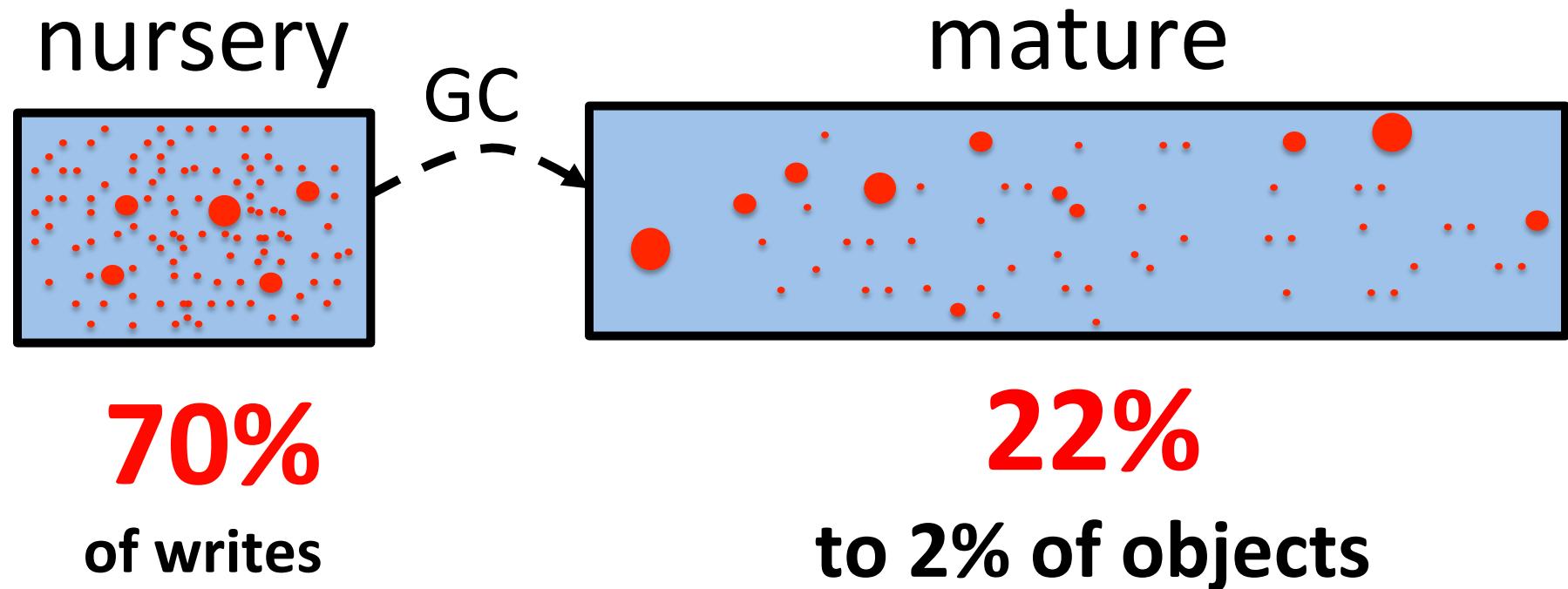
PCM

This work uses GC to keep highly written objects in DRAM

Distribution of **writes** in GC heaps

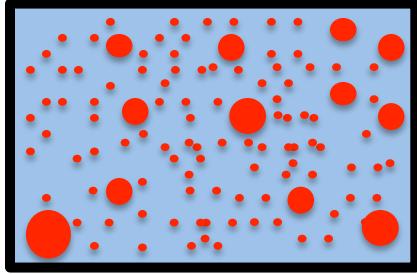


Distribution of writes in GC heaps

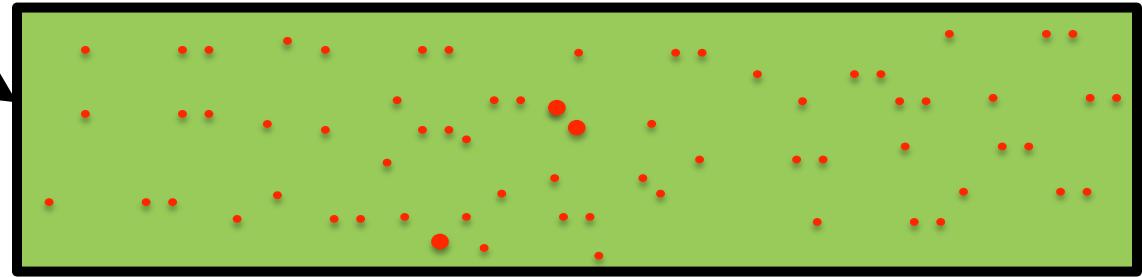


Contribution

Write-Rationing Garbage Collectors mature



GC



DRAM



PCM



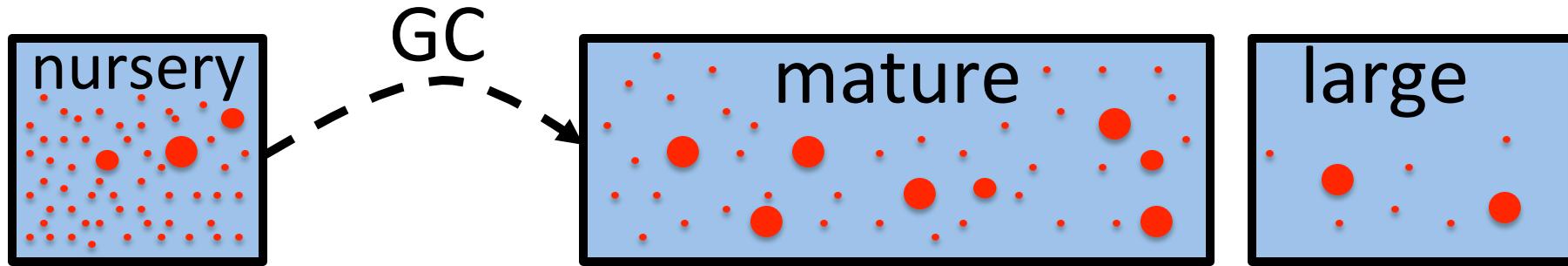
Two write-rationing garbage collectors

Kingsguard-
Nursery

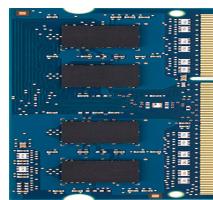
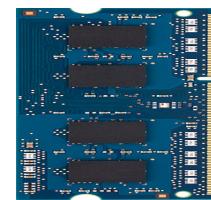
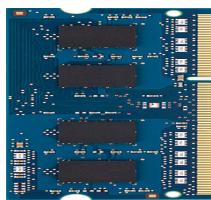
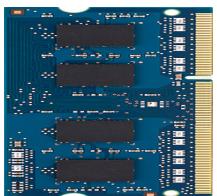
Kingsguard-
Writers



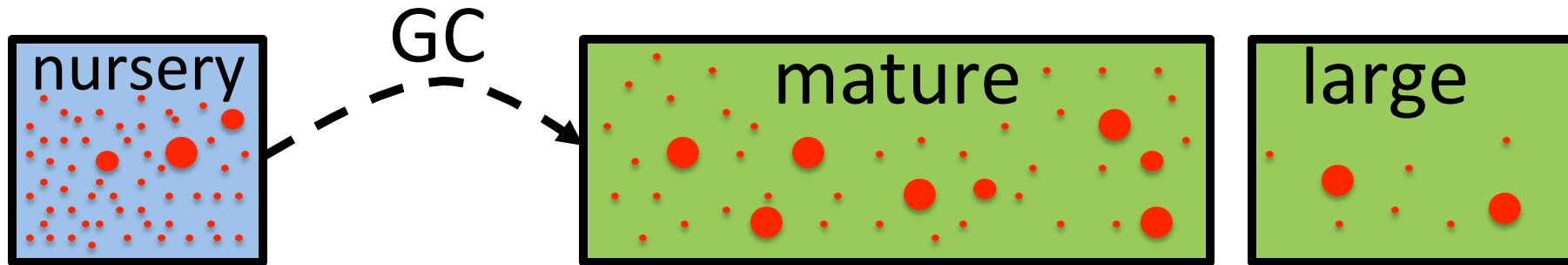
Heap organization in DRAM



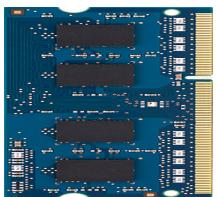
DRAM



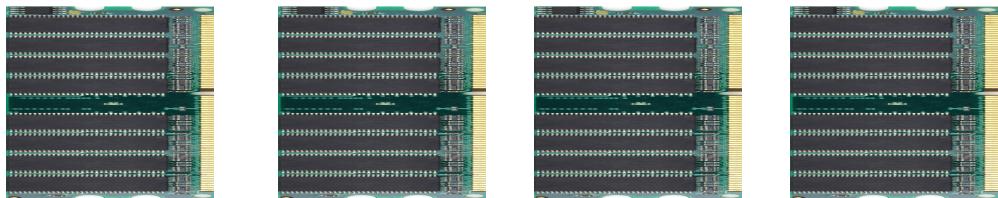
KG-N Kingsguard-Nursery



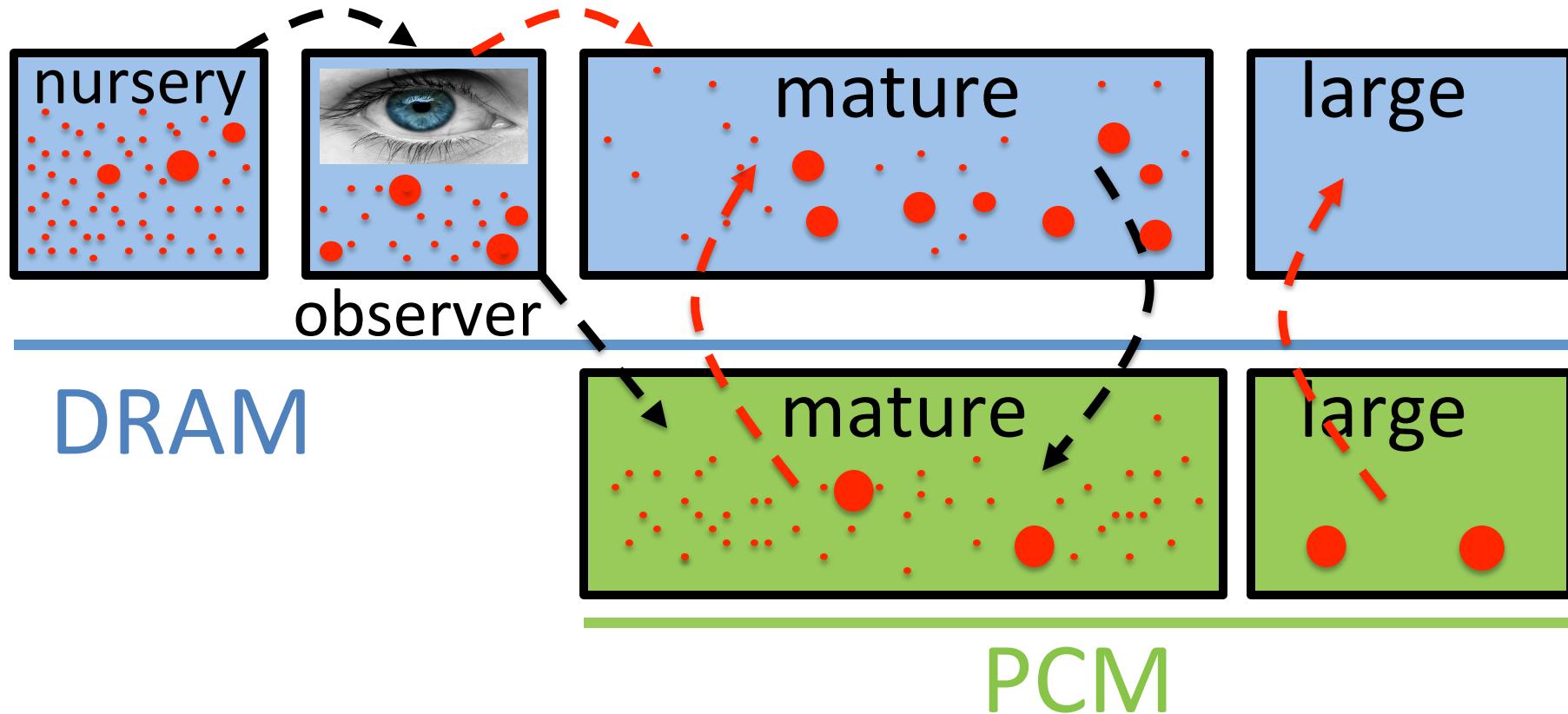
DRAM



PCM



KG-W Kingsguard-Writers



Monitoring writes



Header

References

Primitives

On a write to an object

 Write barrier sets a bit in header

Write barrier configurations

 Monitor references

 Monitor references and primitives

Two additional optimizations

Large object optimization

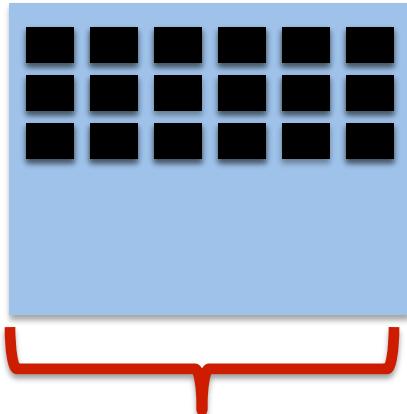
Selectively allocate large objects in DRAM

Metadata optimization

Place mark bits of PCM objects in DRAM

Large object optimization

nursery



large



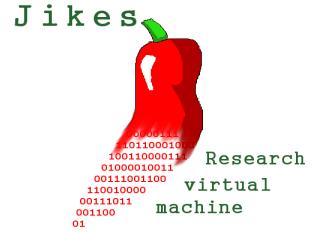
$\frac{1}{2}$ of remaining
nursery

Monitor PCM write rate
to tu [REDACTED]

Results

- (1) Measurements on real hardware
- (2) Simulation

Jikes research virtual machine



Java applications



Real hardware methodology

Use write barriers to count object writes

Applications: 12 DaCapo, 3 **GraphChi**, and Pjbb

Configurations

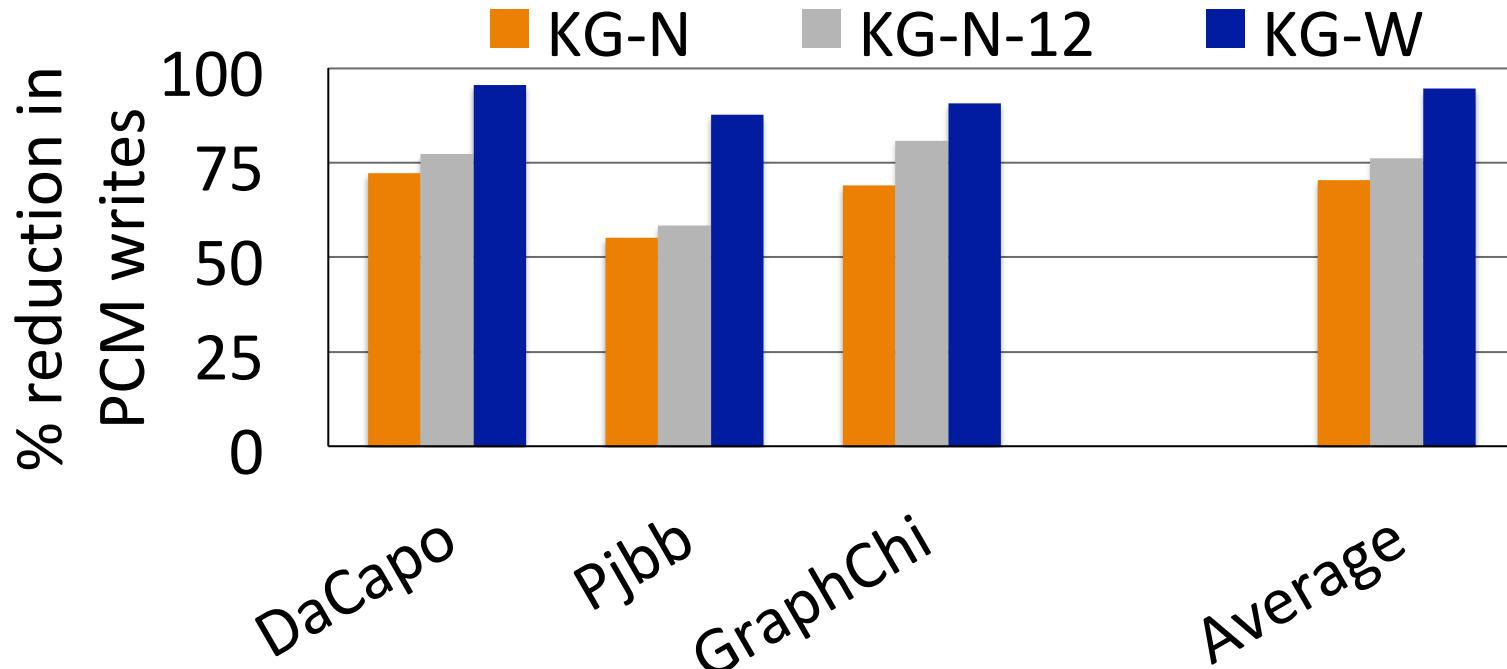
KG-N : 4 MB nursery

KG-W: 4 MB nursery, 8 MB observer

KG-N : 12 MB nursery

Reduction in PCM writes

Baseline: PCM-Only



KG-W reduces 95% of writes to PCM

Simulation methodology

7 DaCapo applications

Measure lifetime, energy, and
execution time in simulator



Memory systems

Homogeneous

32 GB DRAM

32 GB PCM

PCM parameters

4X read latency

4X write energy

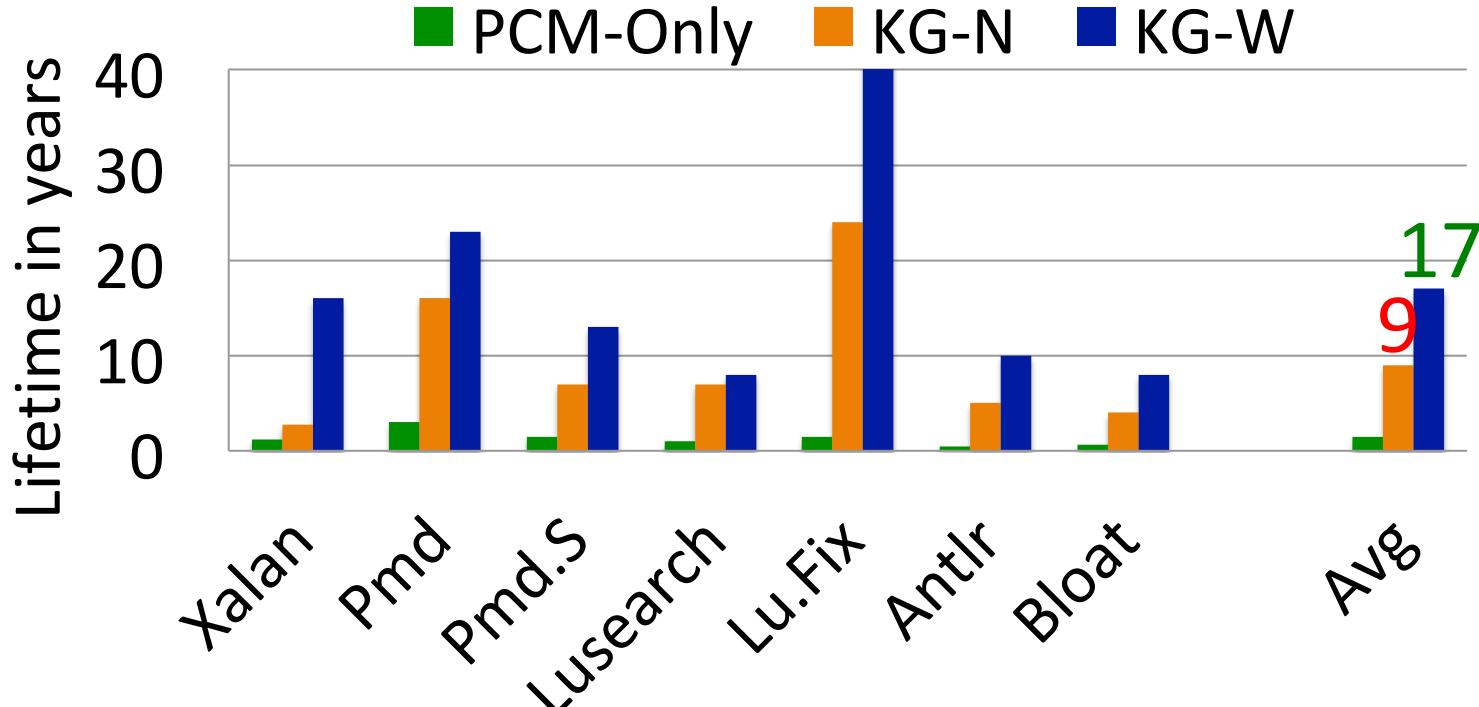
10 M writes/cell

Hybrid

1 GB DRAM

32 GB PCM

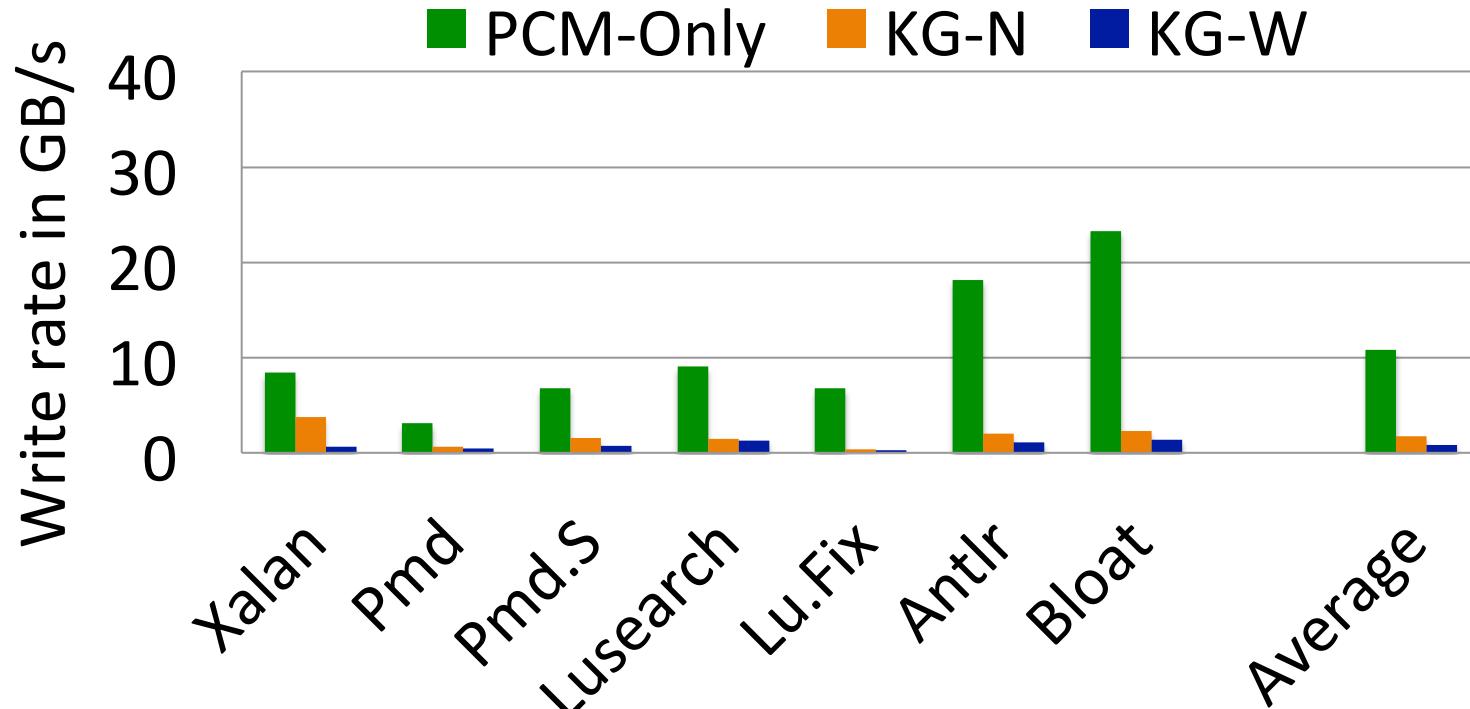
PCM lifetimes



PCM alone is not practical

PCM lasts more than 10 years with KG-W

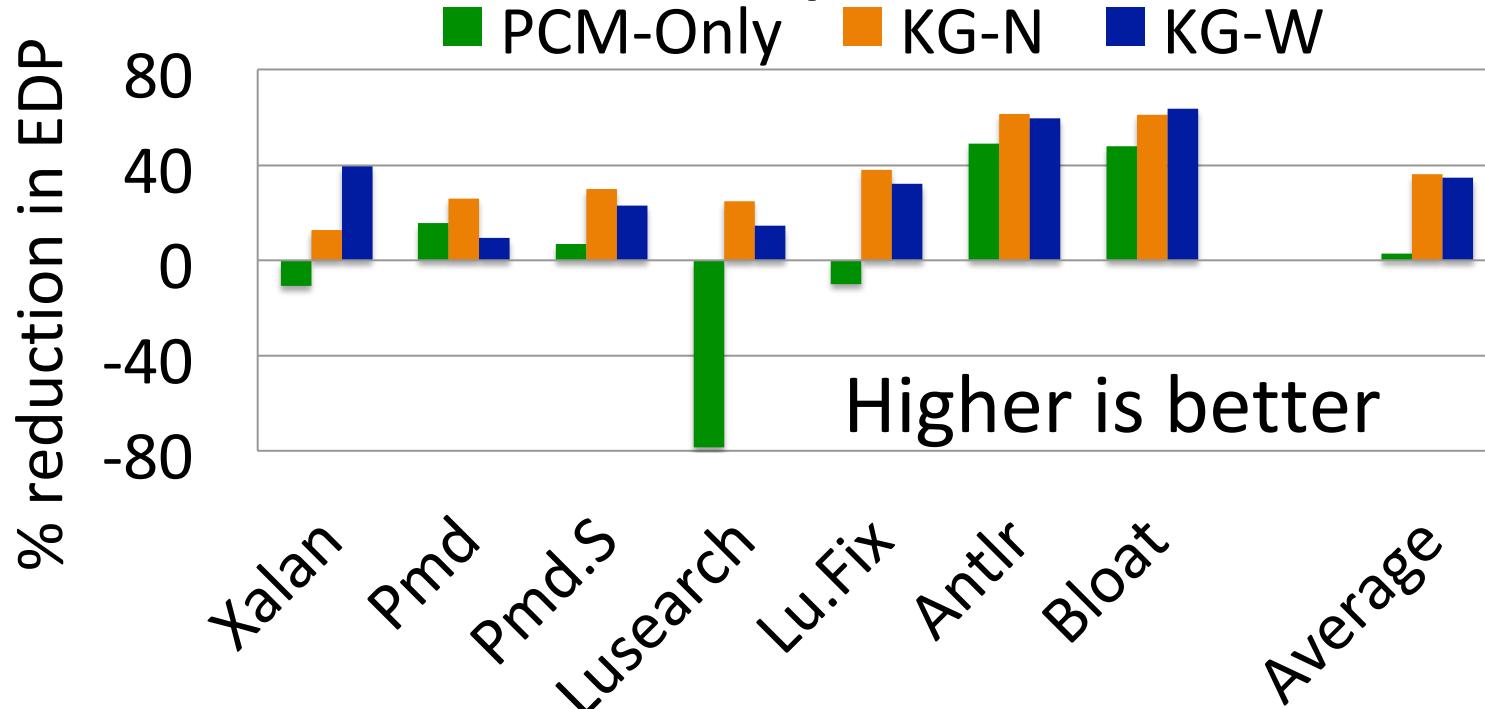
PCM write rates



KG-N reduces write rate by 6X over PCM-Only

KG-W reduces write rate by 2X over KG-N

EDP reduction compared to DRAM



EDP : Energy Delay Product

KG-W has 35% better EDP than DRAM-Only

In the paper

- Execution time results

- Breakdown of KG-W overheads

- Object demographics

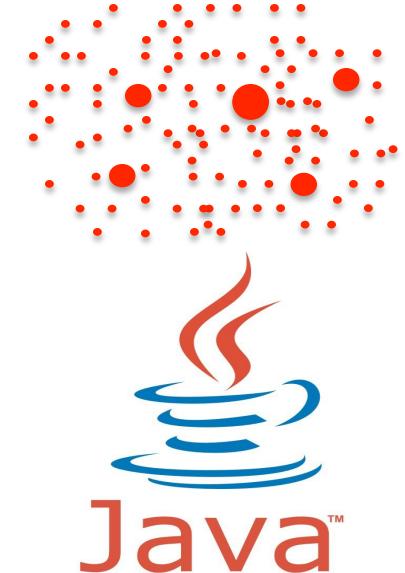
- Comparison with OS approach

Write rationing garbage collection

Monitor fine grained write behavior
of objects

Exploit managed runtimes to organize
objects in hybrid memory

Kingsguard collectors improve
PCM lifetime



Metadata optimization

GC **writes** mark bits of PCM objects

KG-W keeps mark bits of PCM objects in DRAM

markObject() indirection

