

# Logic Optimization

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Virendra Singh

Professor

Computer Architecture and Dependable Systems Lab

Department of Electrical Engineering

Indian Institute of Technology Bombay

<http://www.ee.iitb.ac.in/~viren/>

E-mail: [viren@ee.iitb.ac.in](mailto:viren@ee.iitb.ac.in)

*EE-224: Digital Systems*

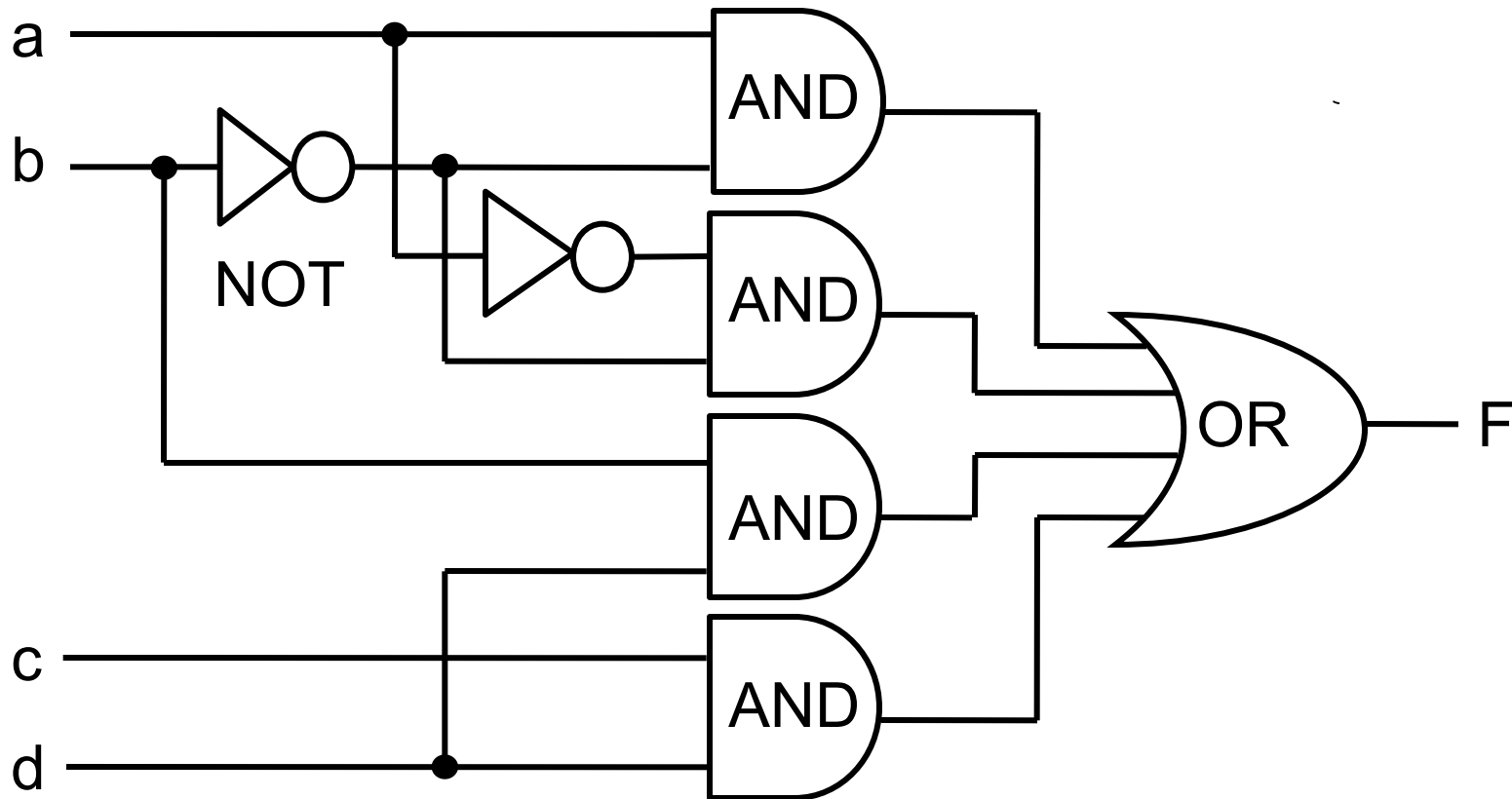
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*Lecture 16-A: 29 September 2020* **CADSL**

# Understanding Logic Minimization

- Logic function:  $F \equiv a\bar{b} + \bar{a}\bar{b} + bd + cd$



# Algebraic Logic Minimization

- Reducing products:

$$\begin{aligned} F &\equiv a\bar{b} + \bar{a}\bar{b} + bd + cd \\ &\equiv \bar{b}(a + \bar{a}) + bd + cd \\ &= \bar{b}1 + bd + cd \\ &= \bar{b}(c + \bar{c}) + bd + cd \\ &= bd + \bar{b}c + cd + \bar{b}\bar{c} \\ &= bd + \bar{b}c + \bar{b}\bar{c} \\ &= bd + \bar{b}(c + \bar{c}) \\ &= bd + \bar{b} \end{aligned}$$

Distributivity

Complementation

Identity

Complementation

Distributivity

Consensus theorem

Distributivity

Complement, identity

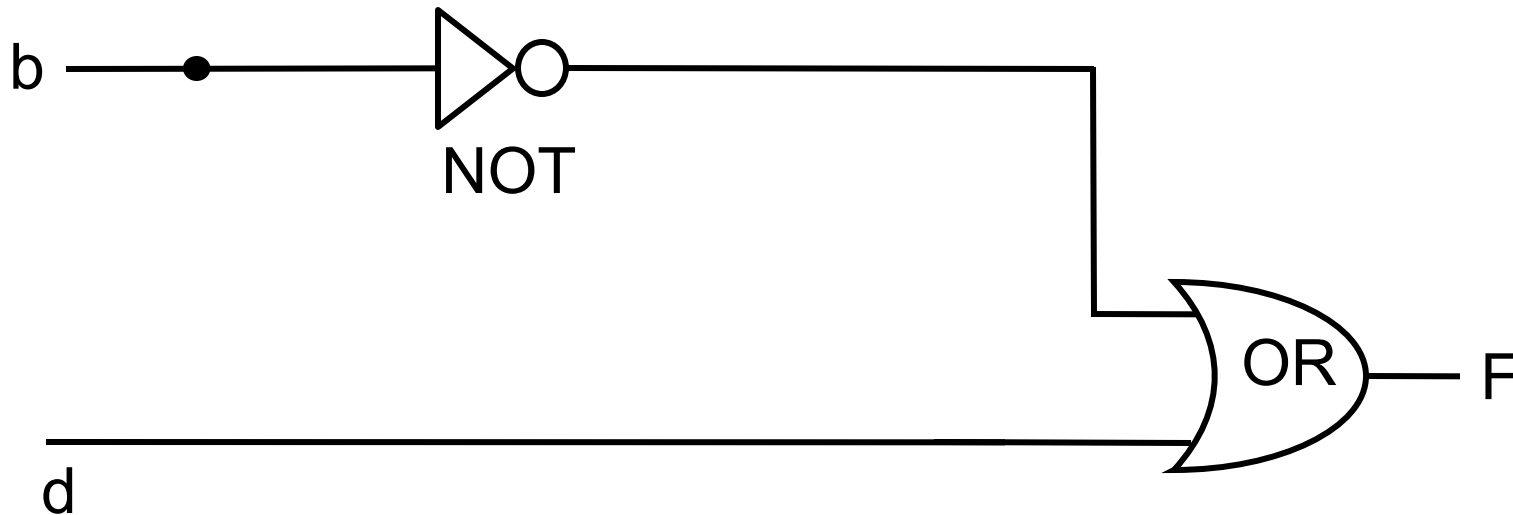
Absorption

$$F = \bar{b} + d$$



# Minimized Circuit

- Minimized expression:  $F = \bar{b} + d$



*Cost , performance*

# Standard Sum-of-Products (SOP)

- A Simplification Example:
- $F(A, B, C) \equiv \Sigma m(1, 4, 5, 6, 7)$
- Writing the minterm expression:

$$F = A'B'C + AB'C' + AB'C + ABC' + ABC$$

1      4      5      6      7

- Simplifying:

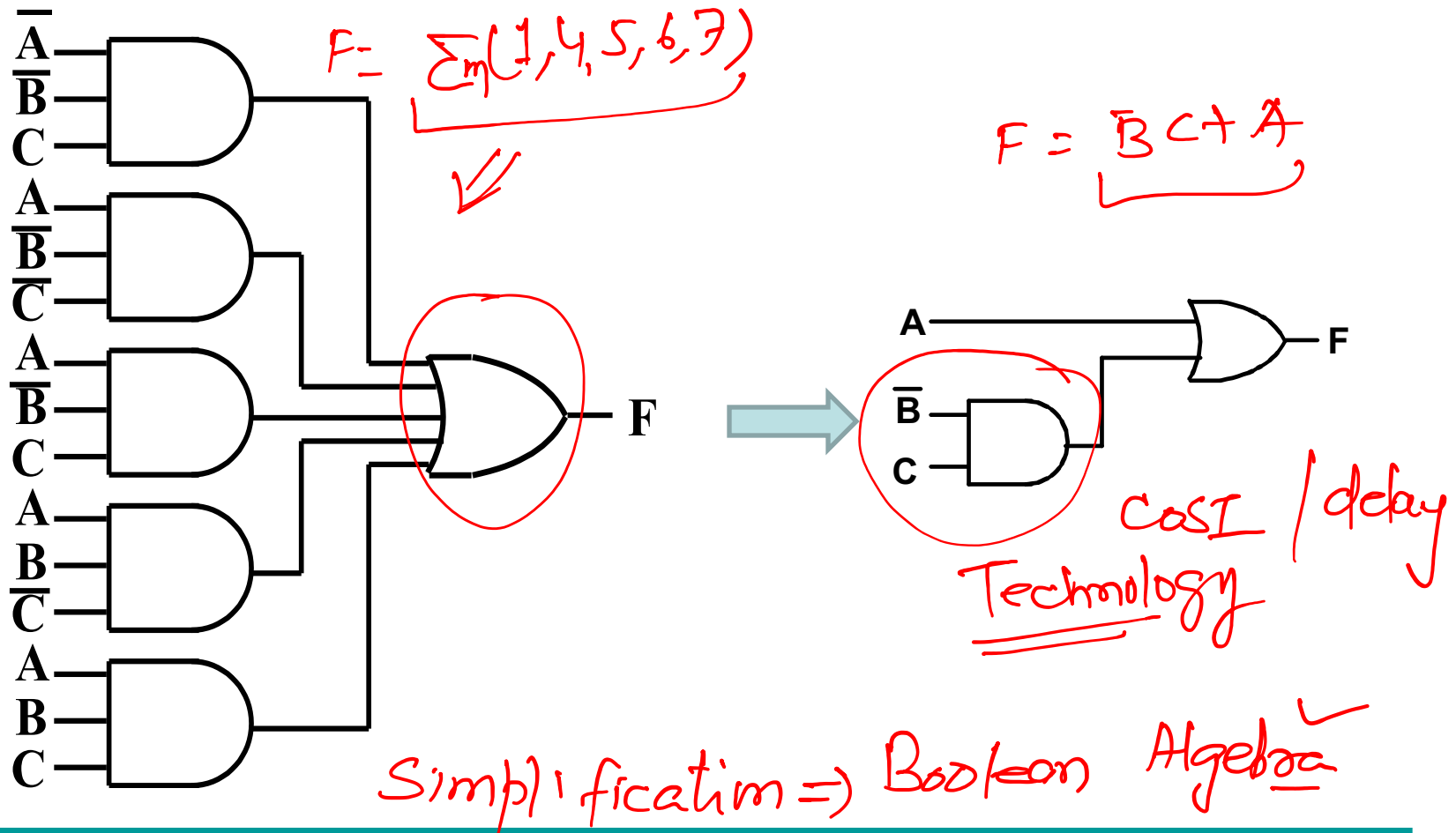
$$\begin{aligned} F &= A' B' C + A (B' C' + B C' + B' C + B C) \\ &= A' B' C + A (B' + B) (C' + C) \\ &= A' B' C + A \cdot 1 \cdot 1 \\ &= A' B' C + A \\ &= B' C + A \end{aligned}$$

- Simplified F contains 3 literals compared to 15 in minterm F



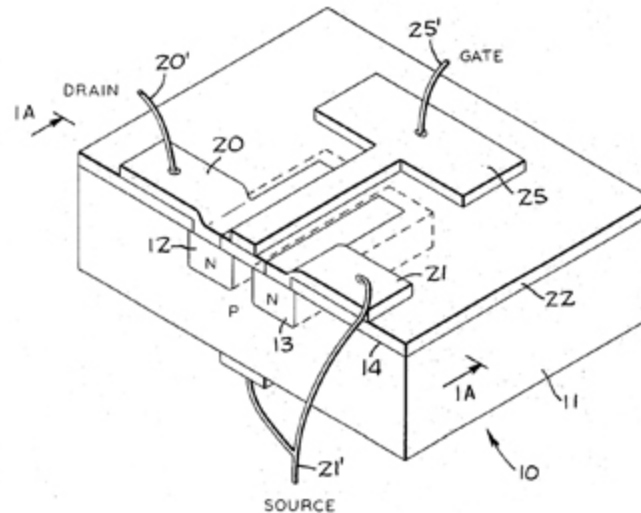
# AND/OR Two-level Implementation of SOP Expression

- The two implementations for F are shown below – it is quite apparent which is simpler!



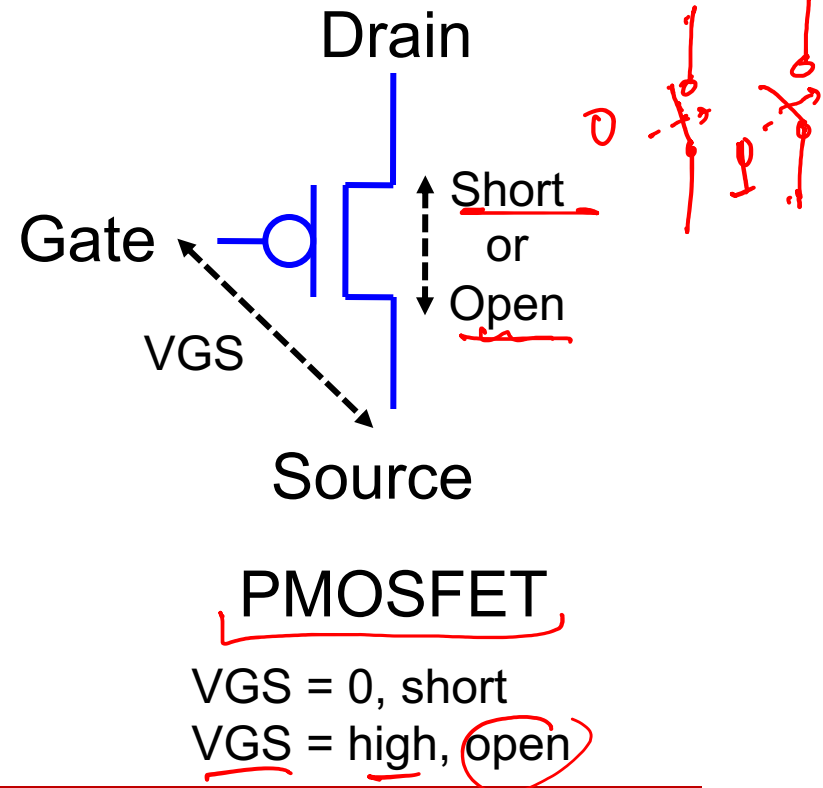
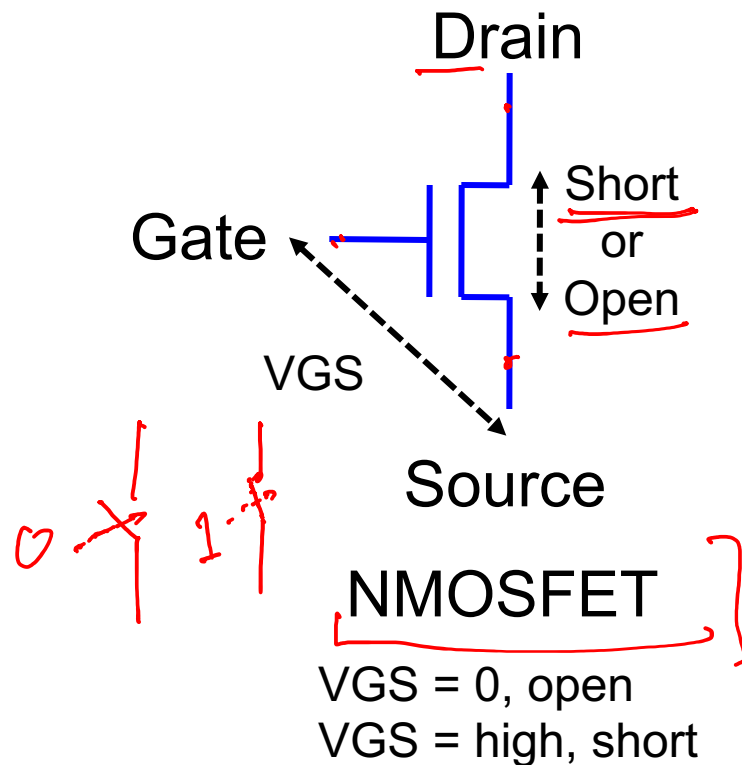
TTL

**Fig. 1**



Wanlass, F. M. "Low Stand-By Power Complementary Field Effect Circuitry."  
*U. S. Patent 3,356,858* (Filed June 18, 1963. Issued December 5, 1967).

# MOSFET (Metal Oxide Semiconductor Field Effect Transistor)



Reference:

R. C. Jaeger and T. N. Blalock, *Microelectronic Circuit Design, Third Edition*, McGraw Hill.



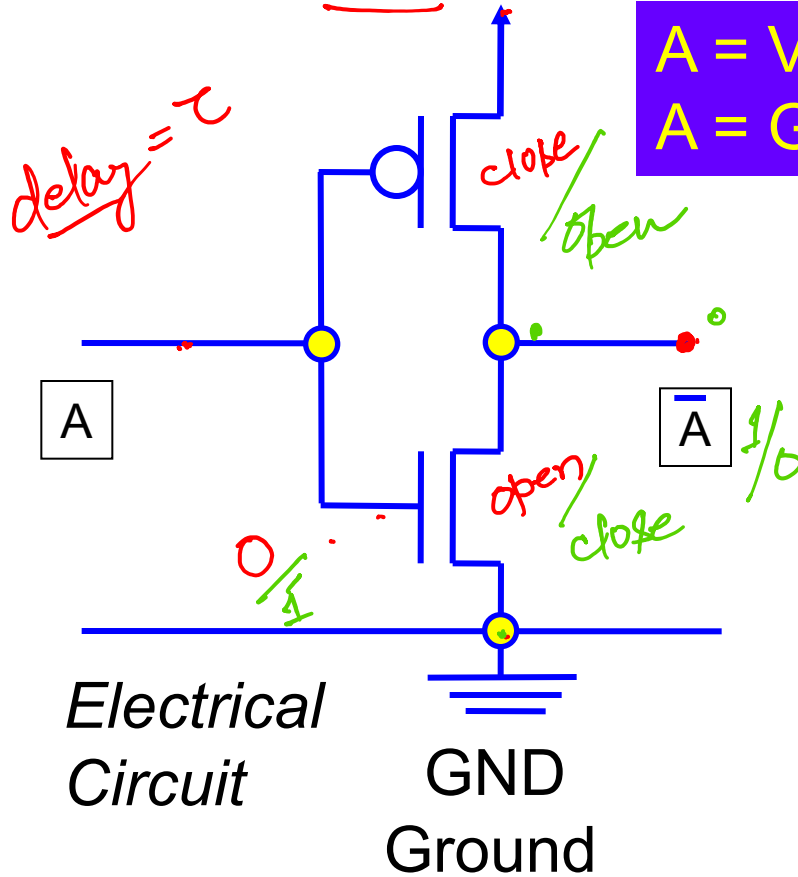


# CMOS NOT Gate (Modern Design)

Power supply

VDD = 1 volt; voltage depends on technology.

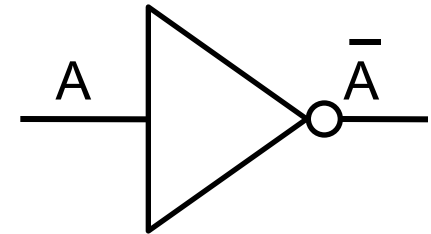
A = VDD = 1 volt is state "1"  
A = GND = 0 volt is state "0"



Truth Table

A	$\bar{A}$
0 ✓	1 ✓
1 ✓	0 ✓

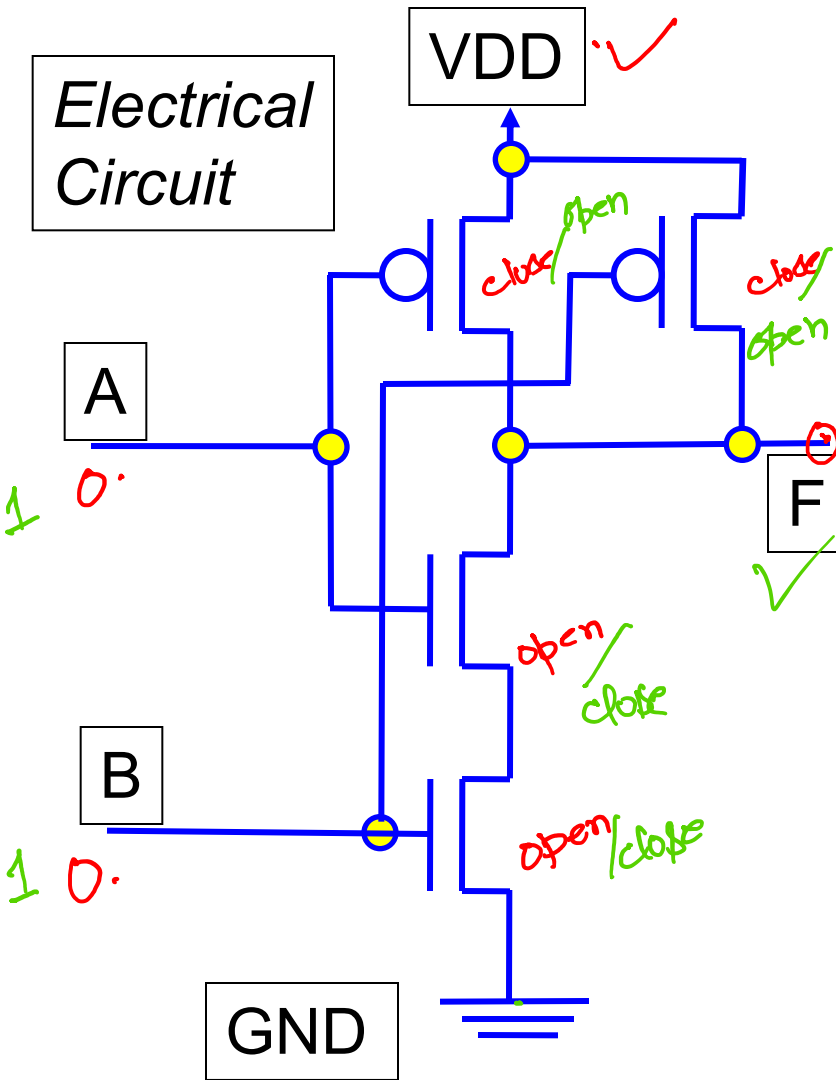
Boolean Function



Symbol

# CMOS Logic Gate: NAND

Electrical Circuit

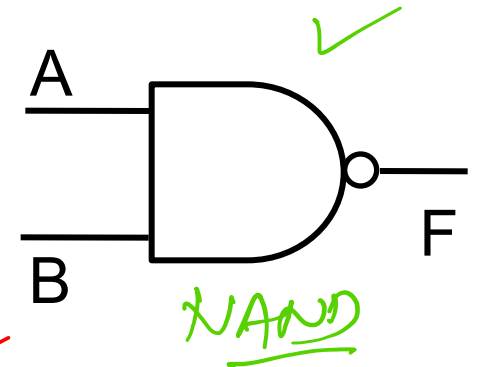


Boolean Function

Truth Table

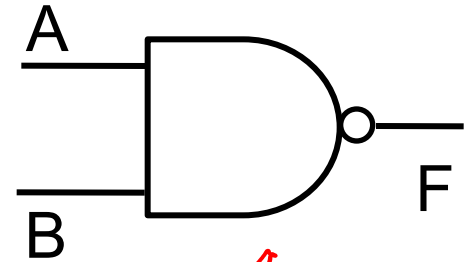
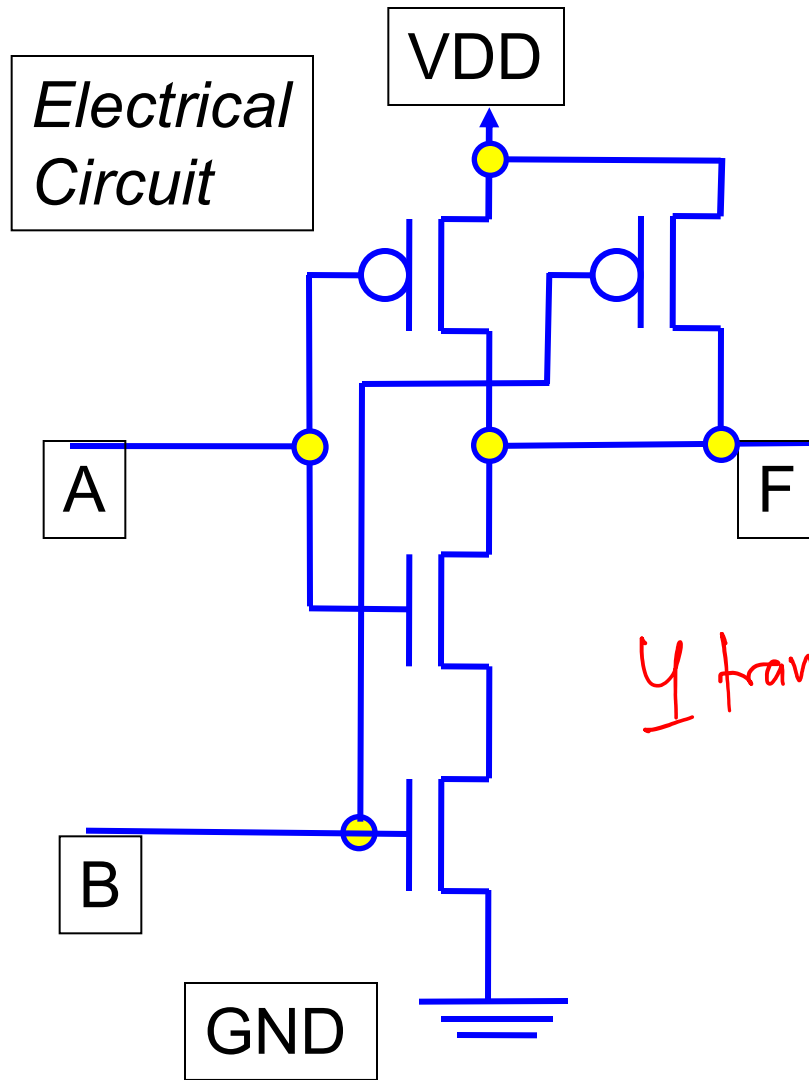
A	B	F
<u>0</u>	<u>0</u>	<u>1</u>
<u>0</u>	1	1
1	<u>0</u>	1
<u>1</u>	<u>1</u>	<u>0</u>

Symbol

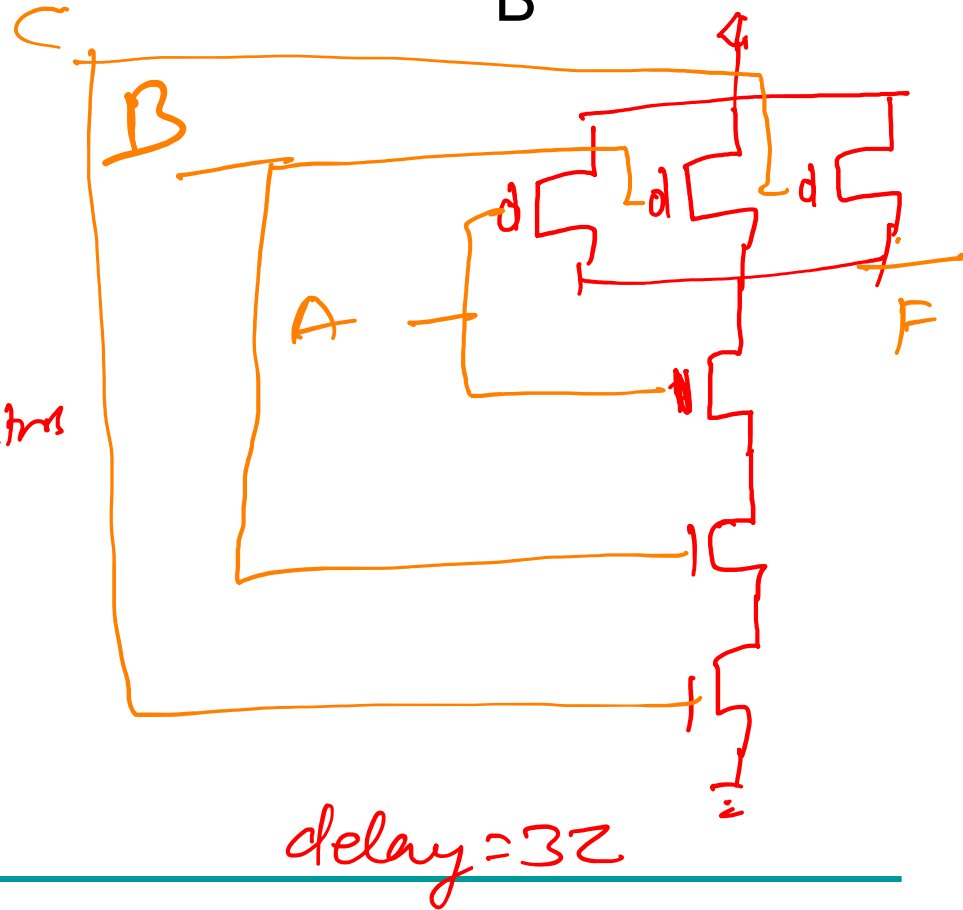


delay =  $2\tau$ .

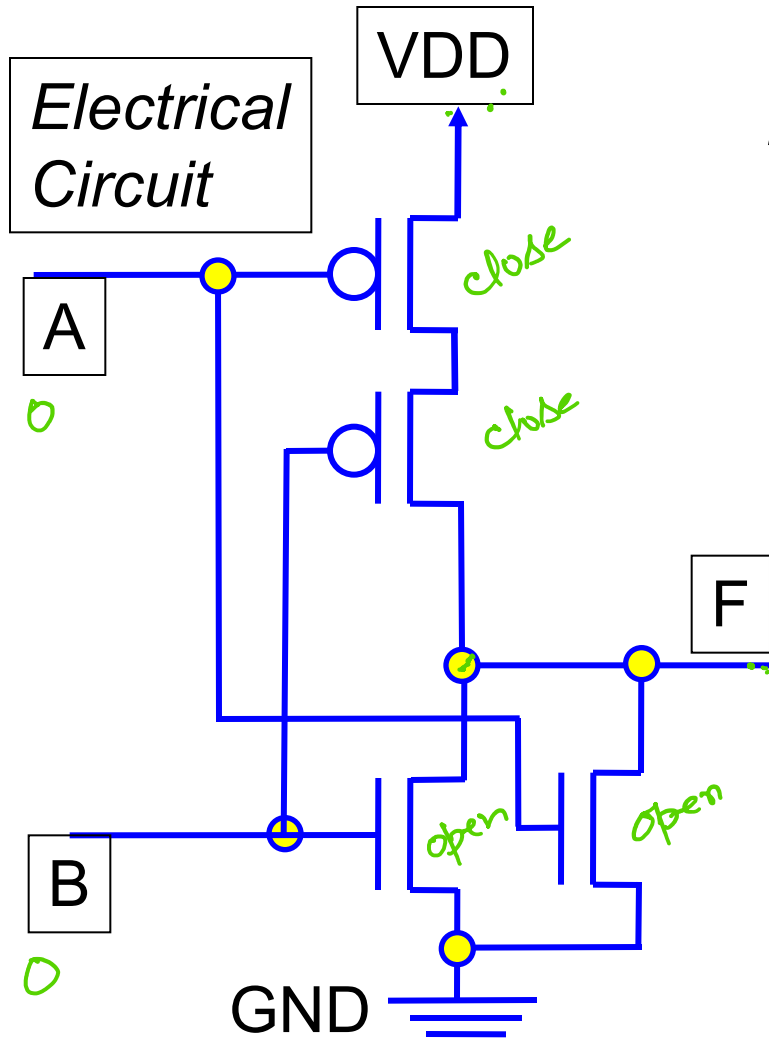
# CMOS Logic Gate: NAND



4 transistors



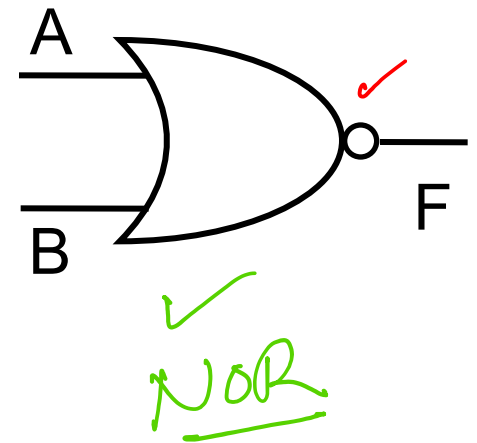
# CMOS Logic Gate: NOR



*Boolean Function*

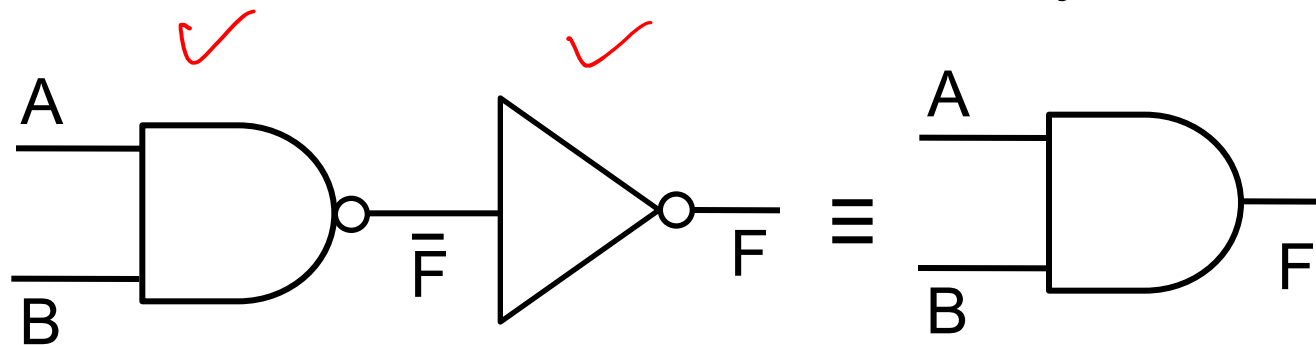
Truth Table		
A	B	F
<u>0</u>	<u>0</u>	<u>1</u>
0	<u>1</u>	0 ✓
<u>1</u>	0	0 ✓
1	1	0

*Symbol*



# CMOS Logic Gate: AND

*Boolean Function*

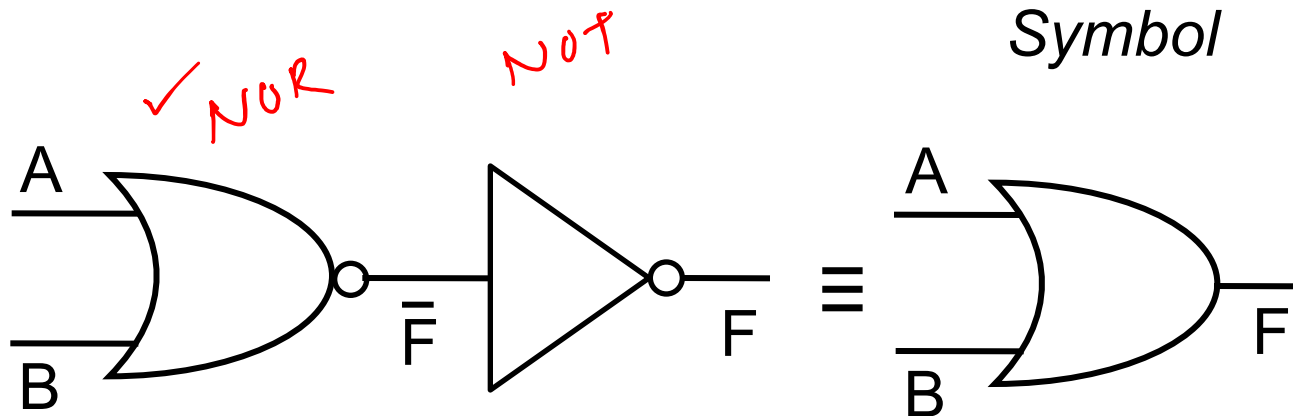


**Truth Table**

A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

# CMOS Logic Gate: OR

*Boolean Function*



*Symbol*

**Truth Table**

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

NOR-NOR  
NAND-NAND

# CMOS Gates

*COST*

Logic function	Number of transistors		<i>DELAY</i>
	1 or 2 inputs	N inputs	
NOT	2	-	$\tau$ 1
AND	6 ✓ $\cdot / 2\tau$	2N + 2 ✓ $2\tau$ 2 <i>2N</i>	
OR	6 ✓ $/ 2\tau$	2N + 2 ✓ $2\tau$ 2 <i>2N</i>	
<u>NAND</u>	4 $/ 2\tau$	2N $2\tau$ 2 <i>2N</i>	
NOR	4	2N $2\tau$ 2 <i>2N</i>	



# Logic Minimization

## Performance

$$\text{Inverter} = 1$$

$$\text{AND} = 2N$$

$$\text{OR} = 2N$$

$$\text{NAND} = 2N$$

$$\text{NOR} = 2N$$

$$\text{delay} \propto \underline{N}$$

Total delay]





# Thank You

