Semiconductor Devices

Junction Field-Effect Transistors: Part 2

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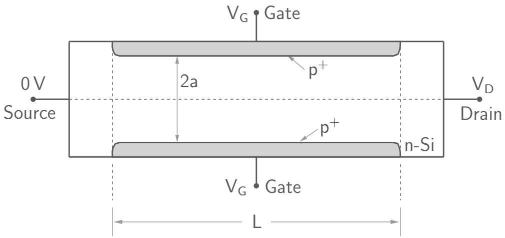
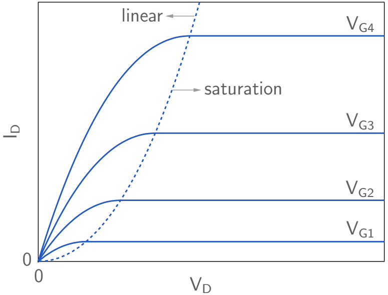
JFET I-V relationship





In the linear region, i.e., $V_D < V_D^{\text{sat}}$,

$$I_D = G_0 \left\{ V_D - \frac{2}{3}\,(V_{\text{bi}} - V_P) \left[\left(\frac{V_D + V_{\text{bi}} - V_G}{V_{\text{bi}} - V_P} \right)^{3/2} - \left(\frac{V_{\text{bi}} - V_G}{V_{\text{bi}} - V_P} \right)^{3/2} \right] \right\}, \quad G_0 = \frac{(2aZ)}{L} \times (q\mu_n N_d).$$

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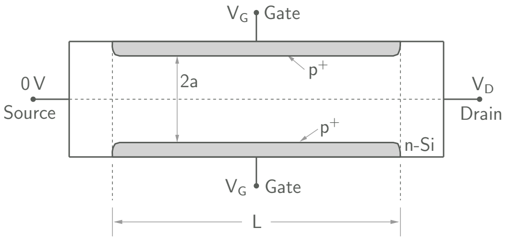

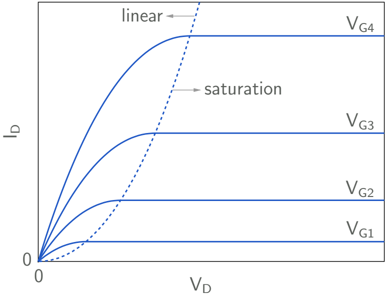

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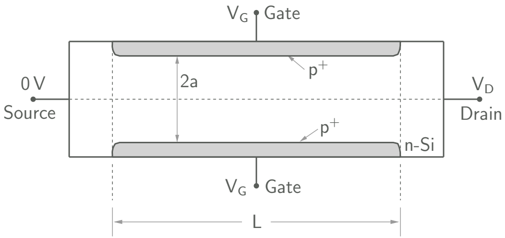

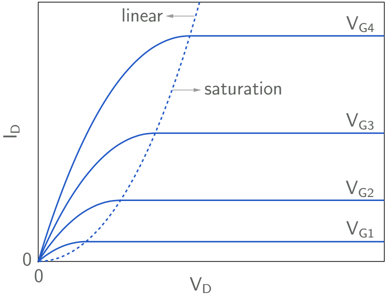

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Substituting in the I_D equation, we get

$$I_D^{\text{sat}}(V_G) = G_0 \left\{ (V_G - V_P) - \frac{2}{3}(V_{\text{bi}} - V_P)\left[1 - \left(\frac{V_{\text{bi}} - V_G}{V_{\text{bi}} - V_P}\right)^{3/2}\right]\right\}.$$

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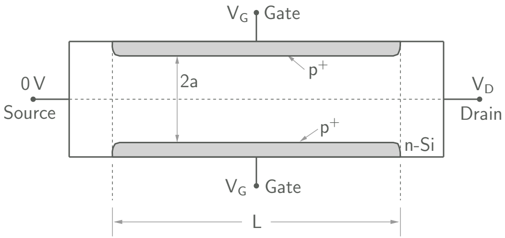

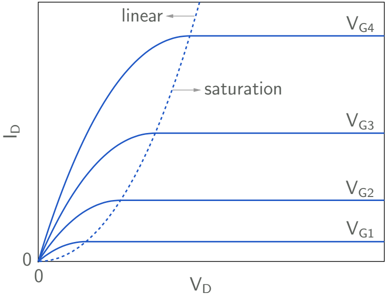

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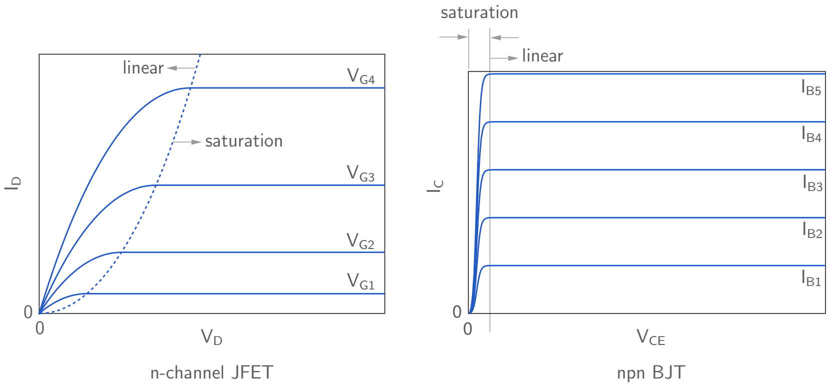
Note that I_D^{sat} depends on V_G. For an n-channel JFET, $I_D^{\text{sat}} \downarrow$ as $V_G \downarrow$

Comparison of JFET and BJT I-V relationships



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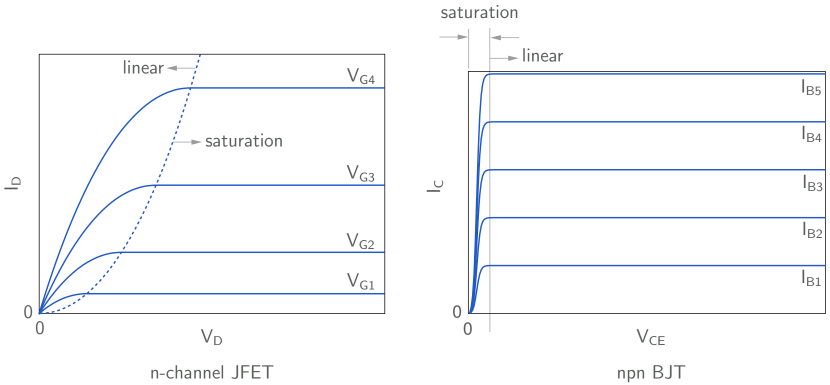

∗ Note the different nomenclature for linear and saturation regions.

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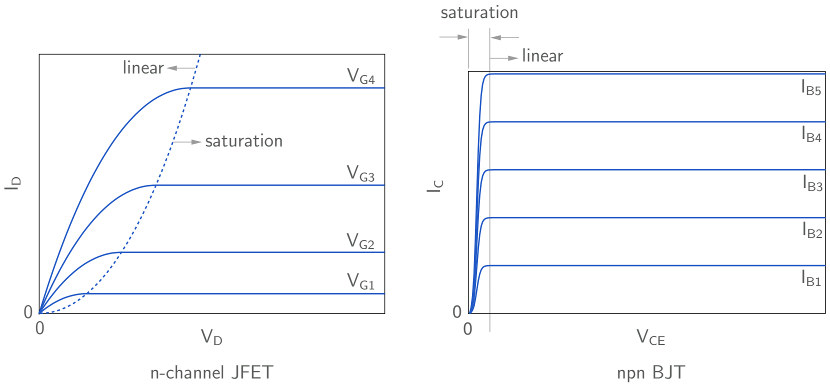

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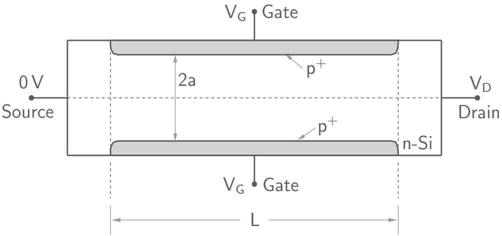
* In a BJT, $V_{CE}^{\text{sat}} \approx 0.2\,\text{V}$ irrespective of I_B.
  In a JFET, V_D^{sat} $(= V_G - V_P)$ depends on V_G.

Example



For an n-channel Si JFET with $N_d = 1 \times 10^{17}\,\text{cm}^{-3}$, $\mu_n = 300\,\text{cm}^2/\text{V-s}$, $a = 0.2\,\mu\text{m}$, $L = 5\,\mu\text{m}$, $Z = 10\,\mu\text{m}$, $V_{\text{bi}} = 0.9\,\text{V}$ for the p^+n gate-to-channel junction,

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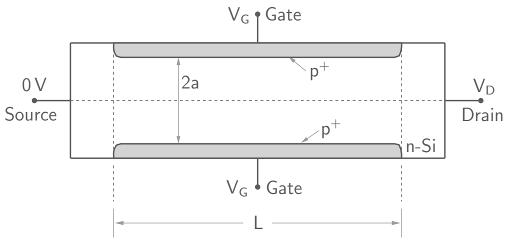

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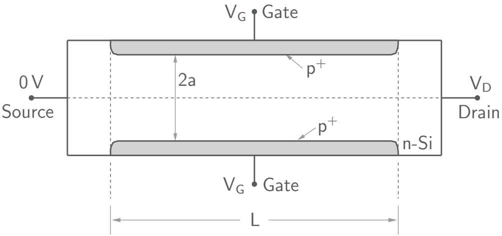

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(b) Plot I_D versus V_G for $-2.5\,\text{V} < V_G < 0\,\text{V}$ and with (i) $V_D = 0.1\,\text{V}$ and (ii) $V_D = 5\,\text{V}$.

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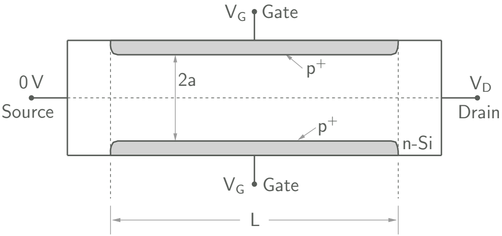

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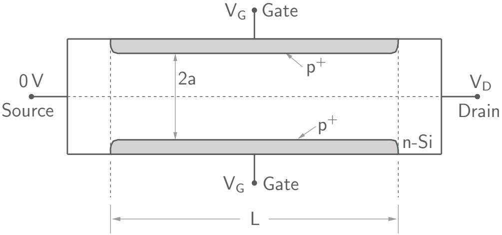
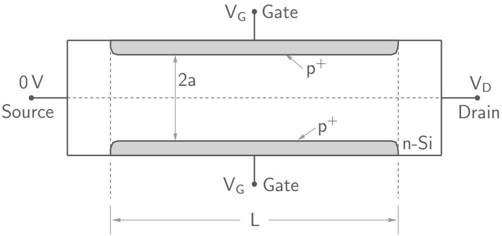
(c) Plot I_D versus V_D for $0\,\text{V} < V_D < 5\,\text{V}$ and $V_G = -1.5, -1, -0.5, 0\,\text{V}$. Mark the boundary between the linear and saturation regions.

Example



(a) $V_P = V_{\text{bi}} - \dfrac{qN_d}{2\epsilon}\, a^2 = -2.2\,\text{V}.$

Example



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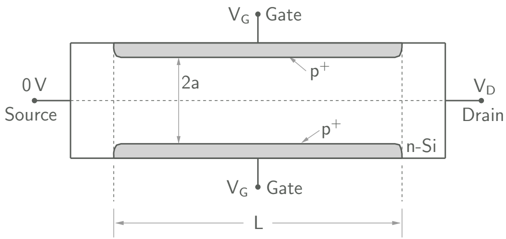

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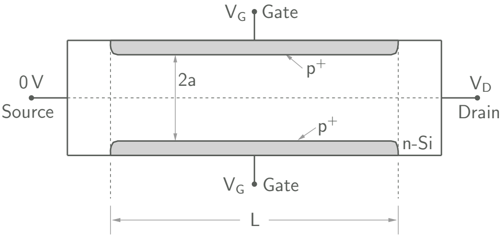

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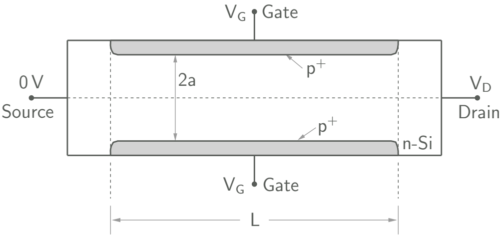

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Units: $\dfrac{\text{cm} \times \text{cm}}{\text{cm}} \times \text{Coul} \times \dfrac{\text{cm}^2}{\text{V-sec}} \times \dfrac{1}{\text{cm}^3} = \dfrac{\text{A}}{\text{V}} = \mho.$

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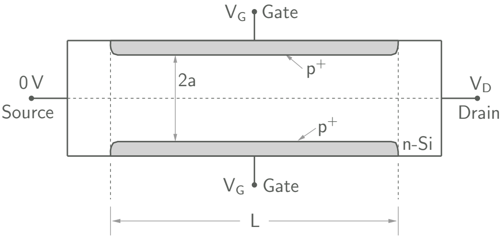
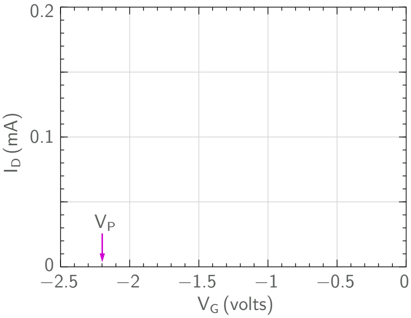
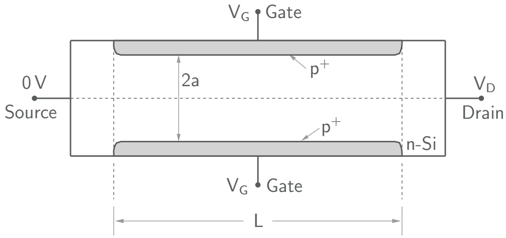


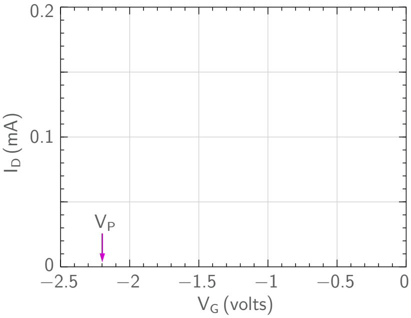
V_G Gate
p^+
2a
0 V
Source
V_D
Drain
p^+
n-Si
V_G Gate
L



0.2
0.1
0
I_D (mA)
V_P
−2.5
−2
−1.5
−1
−0.5
0
V_G (volts)

Example





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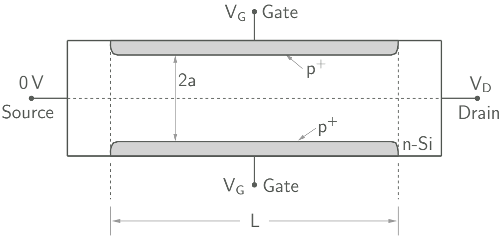

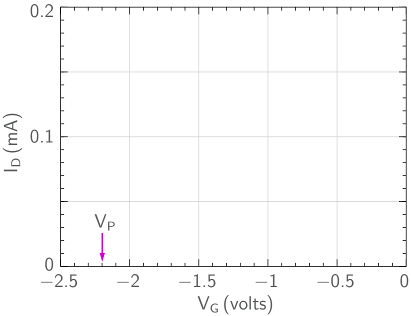

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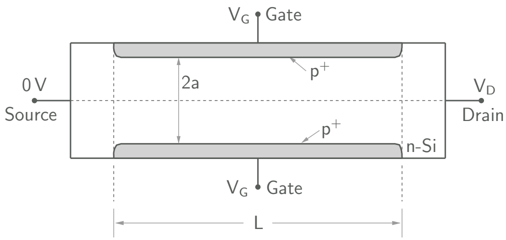

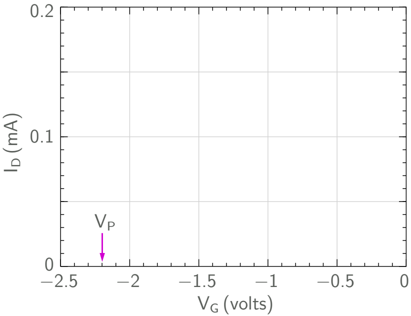

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(Note: such a large V_G is not realistic.)

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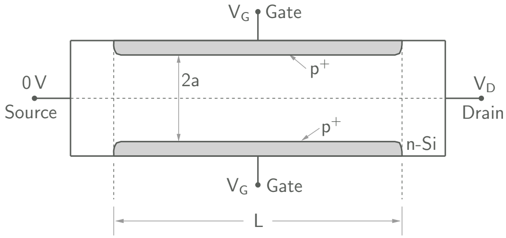

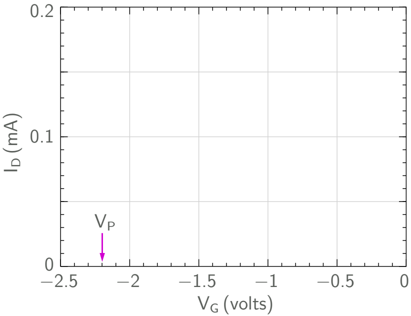

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The I_D-V_G plot can now be obtained using the appropriate I_D expression.

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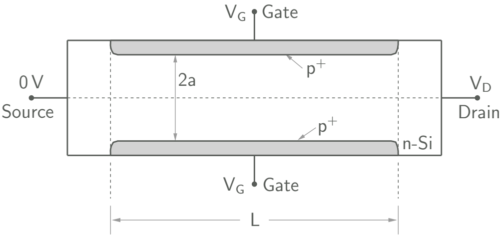

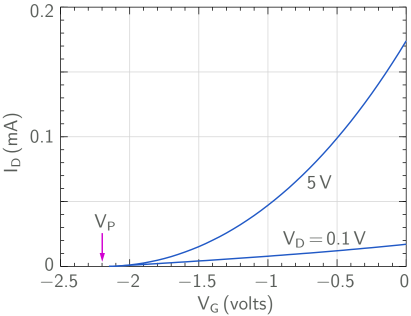

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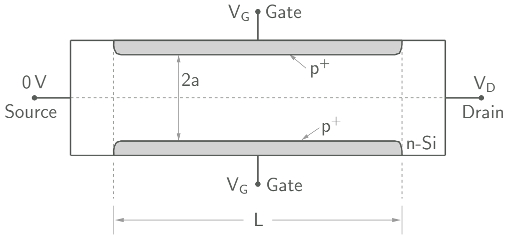

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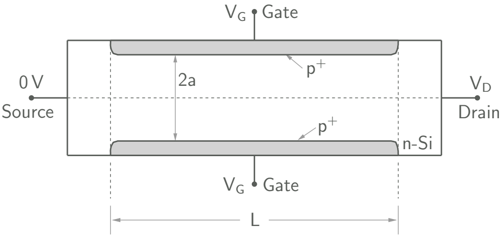

$$
\begin{aligned}
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&= G_0\left\{\left(V_G - V_P\right) - \frac{2}{3}\left(V_{\text{bi}} - V_P\right)\left[1 - \left(\frac{V_{\text{bi}} - V_G}{V_{\text{bi}} - V_P}\right)^{3/2}\right]\right\}, && V_D > V_D^{\text{sat}}
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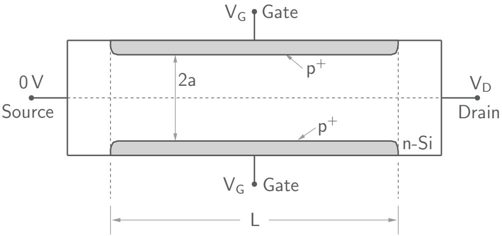

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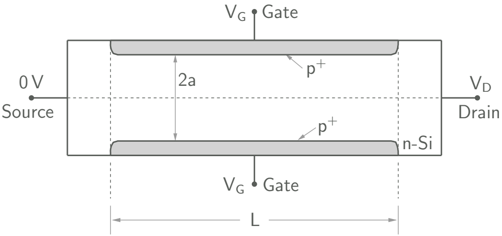
Example



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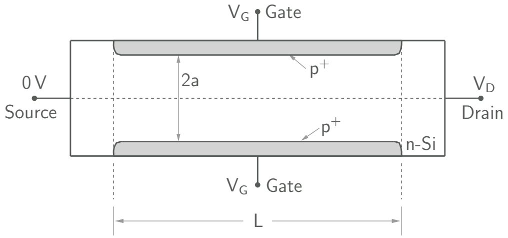

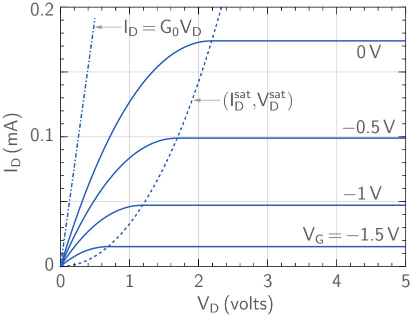

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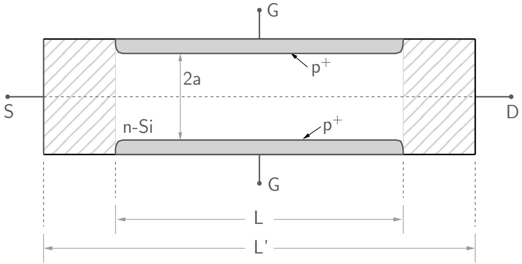
JFET source/drain resistances



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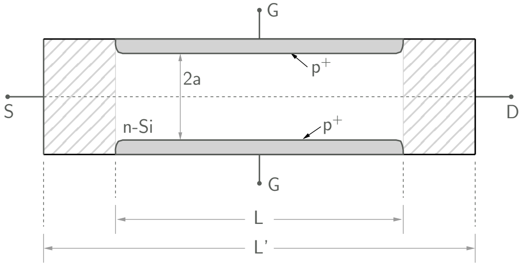

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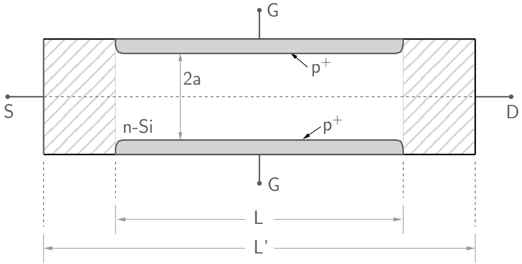

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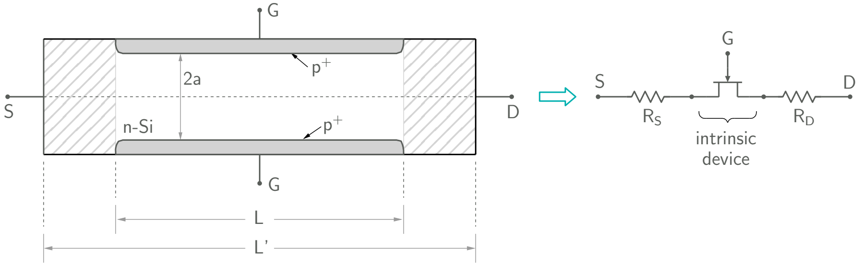

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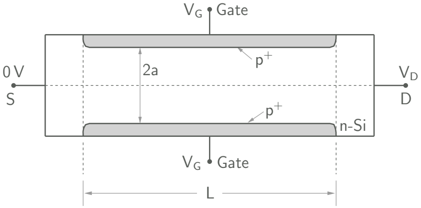
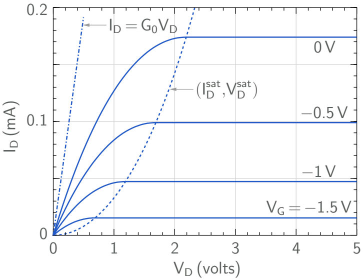
Simplified JFET model for circuit analysis





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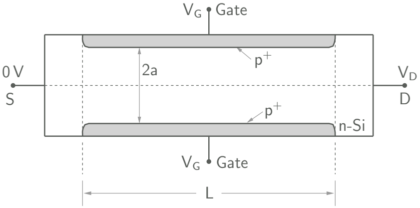

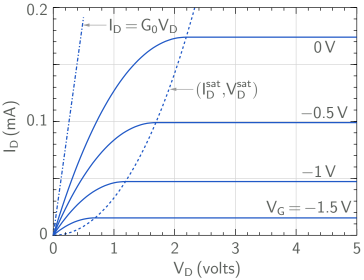

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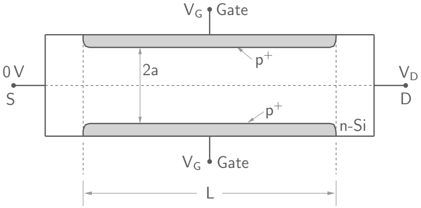

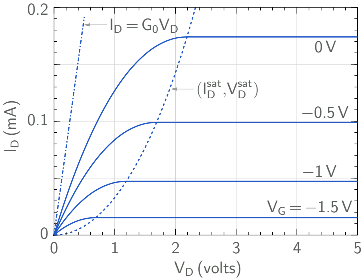

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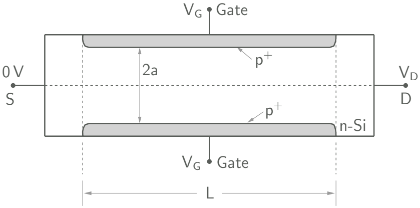

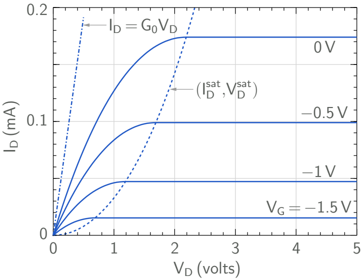

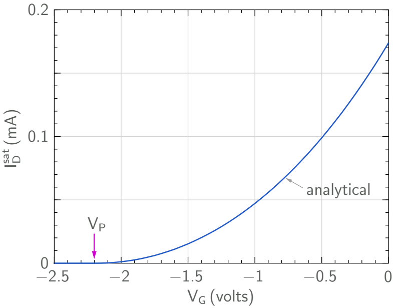

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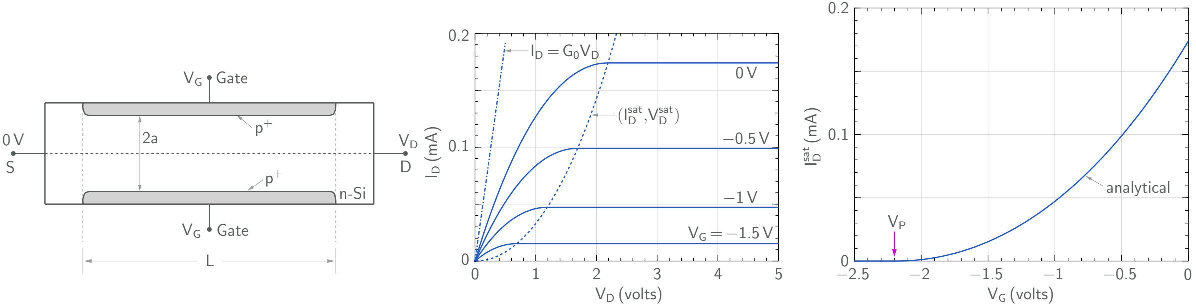

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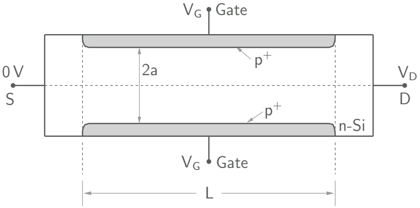

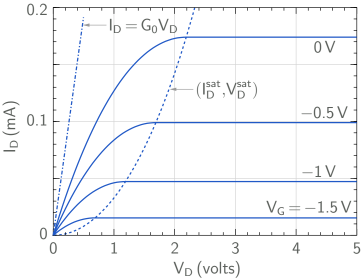

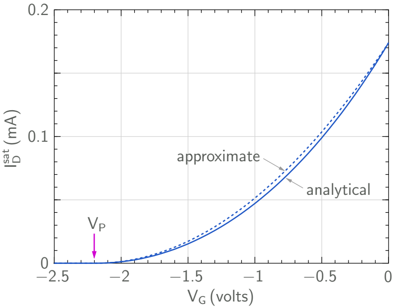

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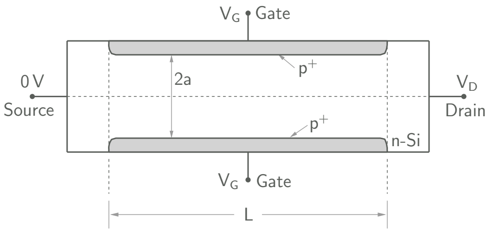
JFET small-signal model



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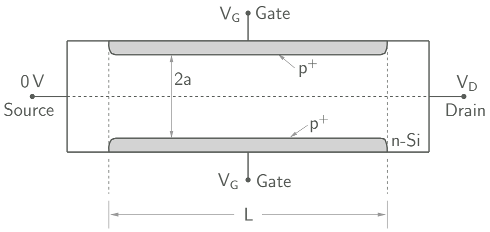

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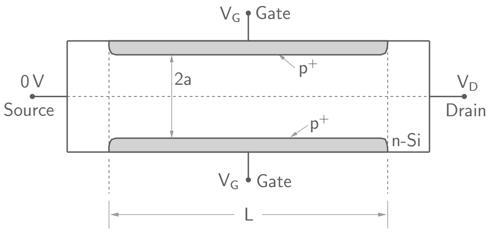

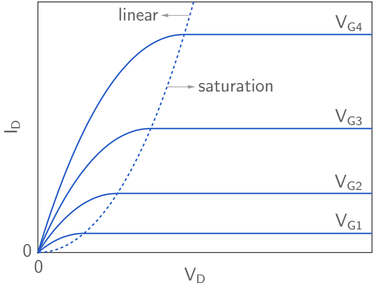

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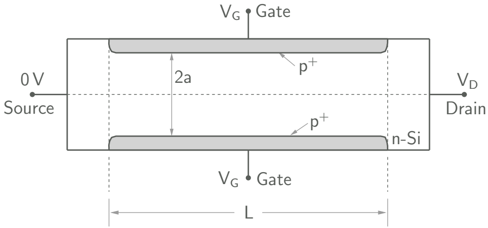

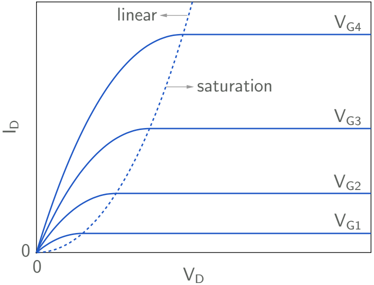

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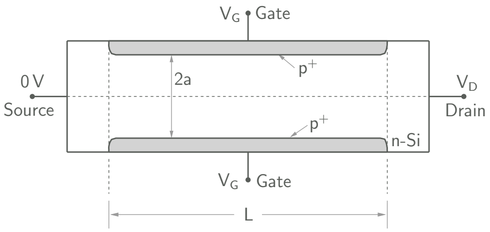

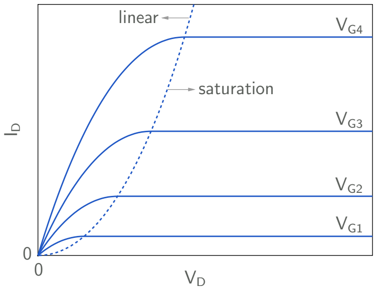

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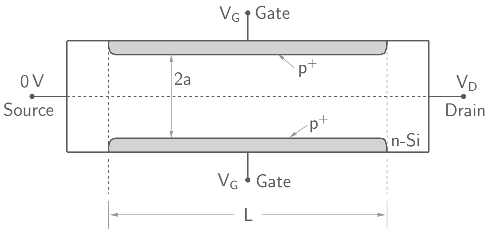

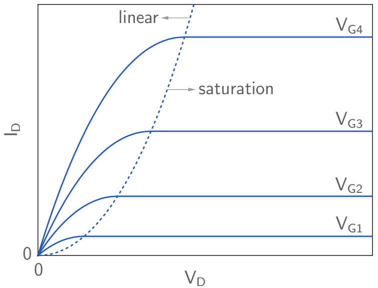

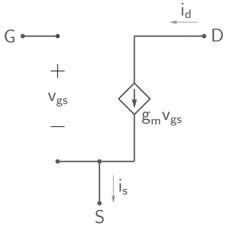

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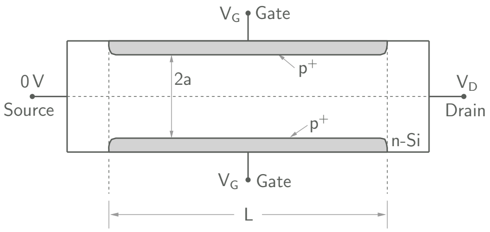

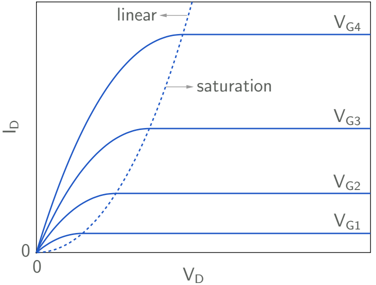

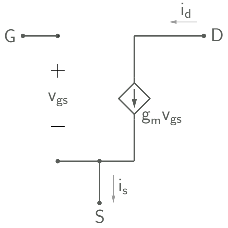

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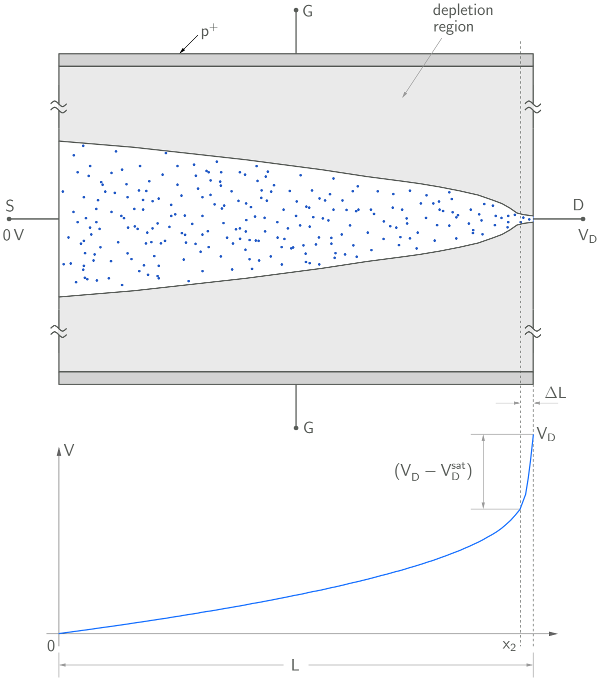
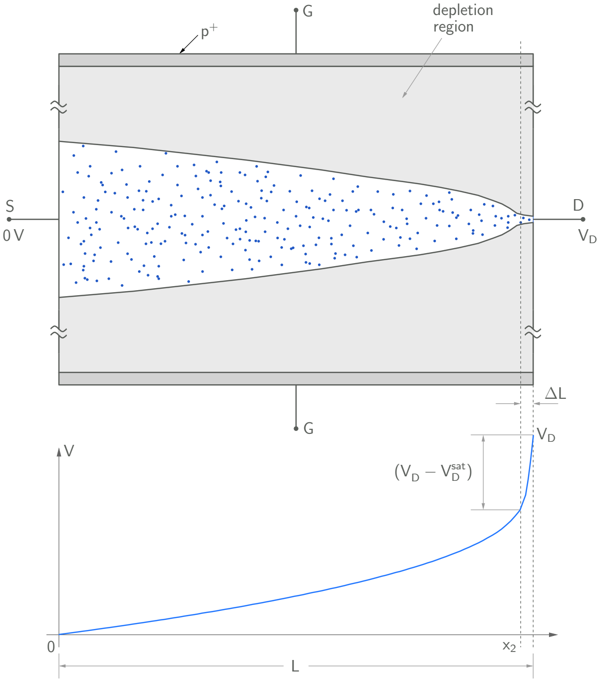
(Note that there is a reverse biased *pn* junction between G and S and betweeen G and D. $\rightarrow i_g = 0$.)



Channel length modulation:



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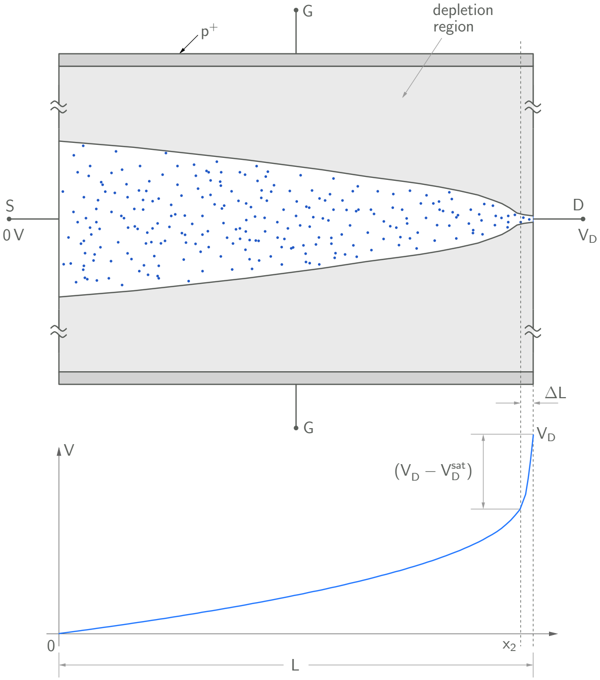

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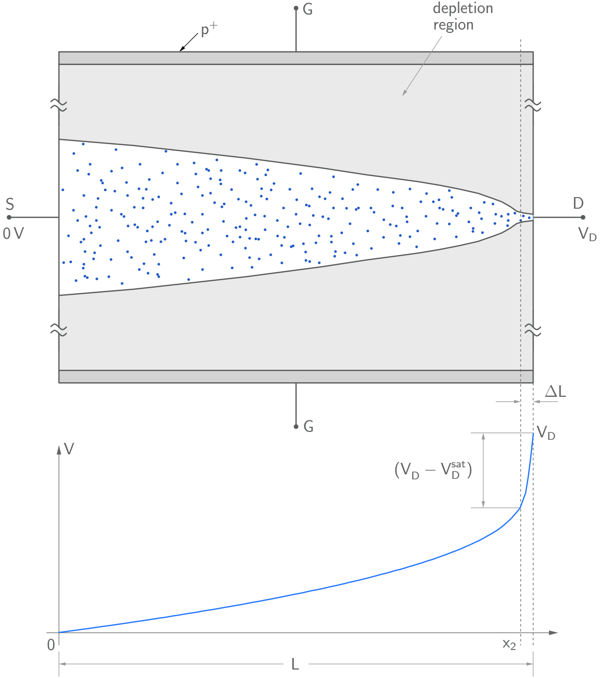

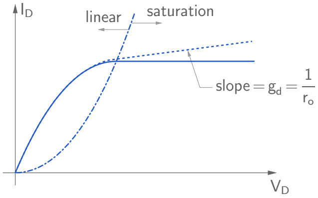

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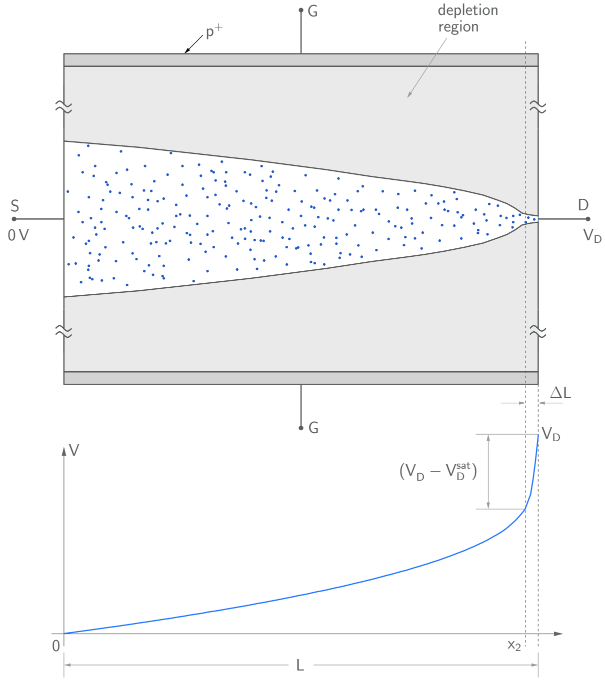

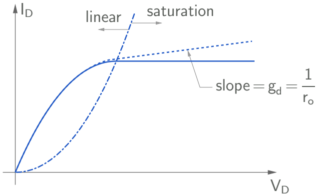

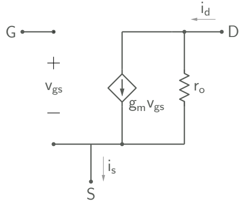

Small-signal model

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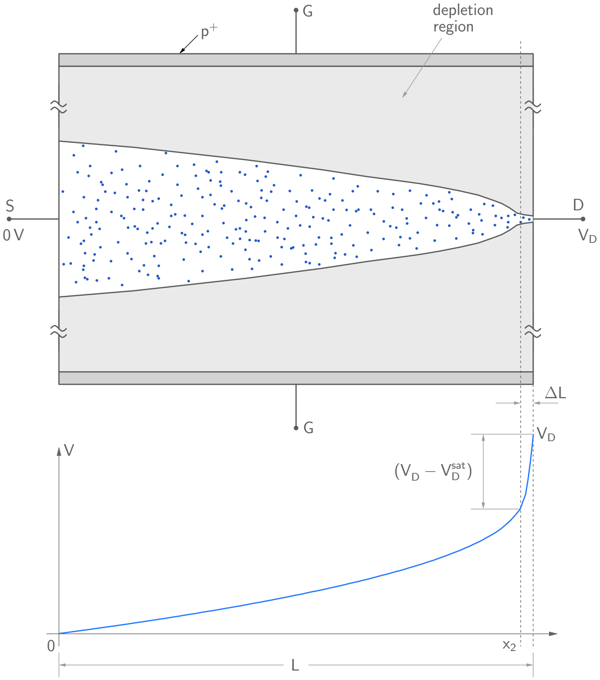

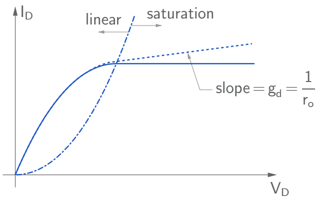

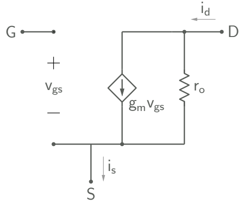

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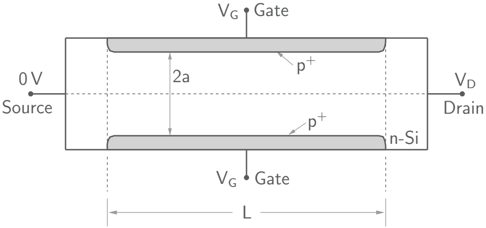
* This "channel length modulation" is significant in short-channel devices ($L \sim 1\,\mu$m).

JFET: small-signal model



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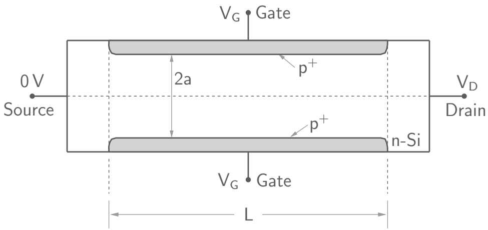

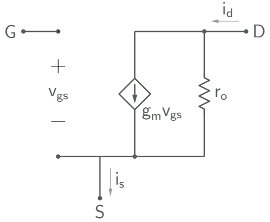

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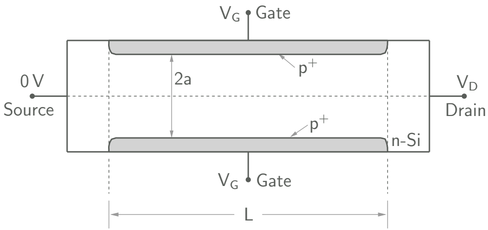

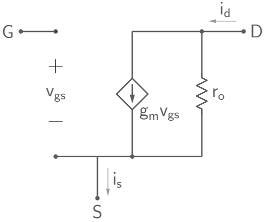

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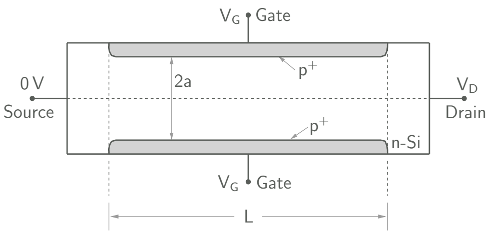

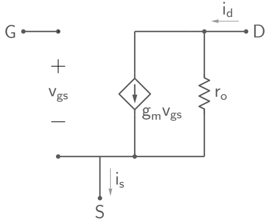

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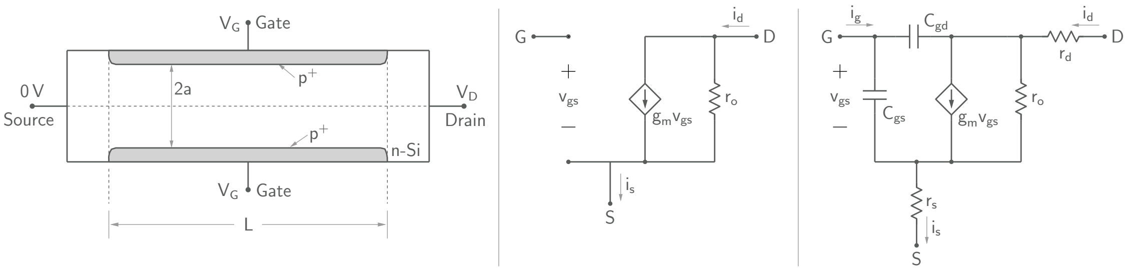

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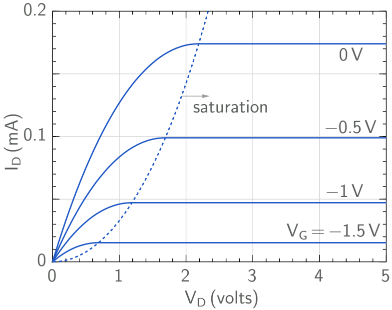
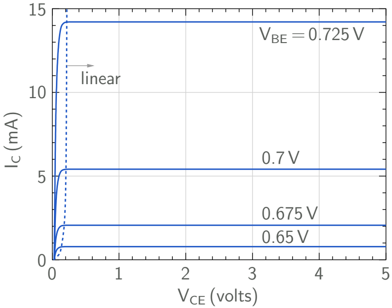
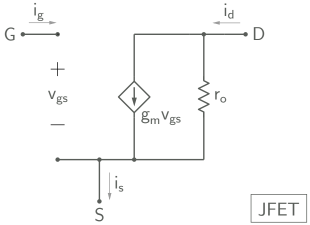
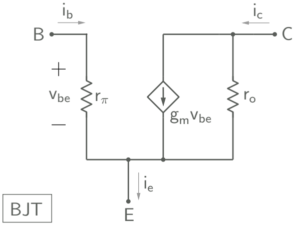
JFET amplifiers









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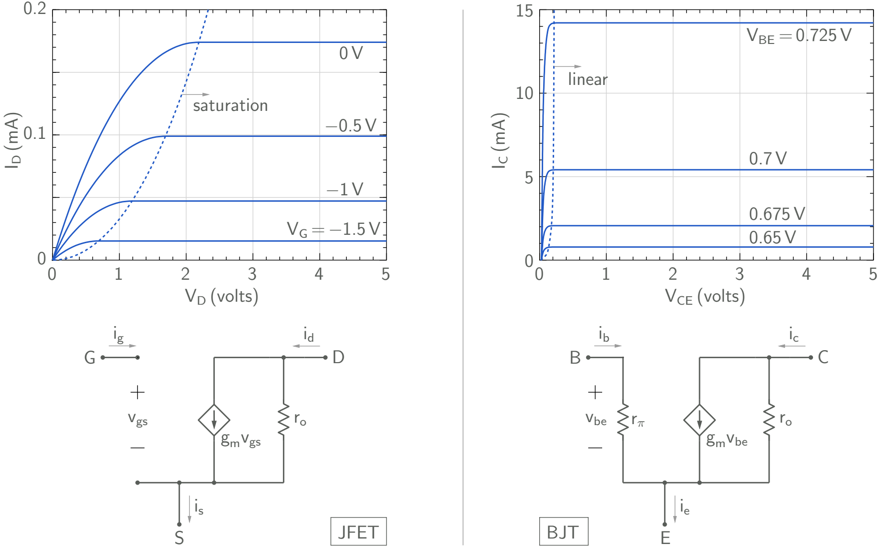

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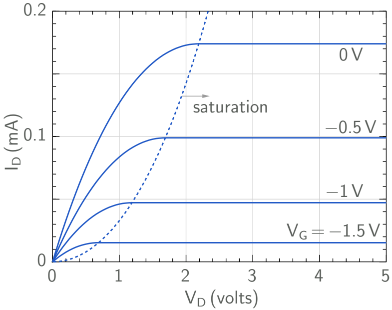
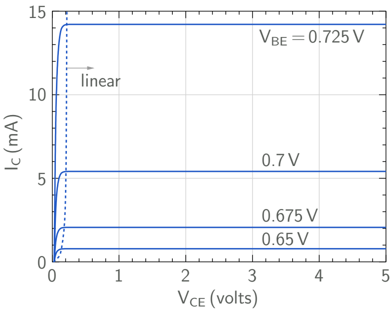
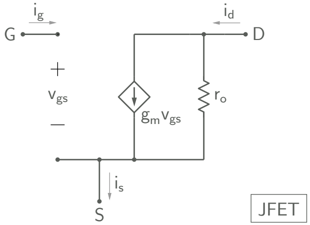
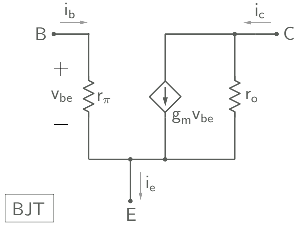
JFET amplifiers









* Qualitatively, the I_D-V_{DS} relationship of a JFET is similar to the I_C-V_{CE} relationship of a BJT.
* A JFET can be used for amplification, e.g., we can have a “common-source” amplifier which is similar to the “common-emitter” amplifier.

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* For amplification, a JFET needs to be biased in the saturation region, and the design goal is to bias it at a certain Q-point, (I_D, V_{DS}).

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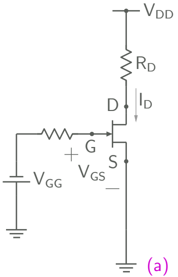

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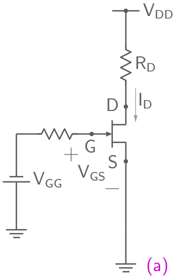

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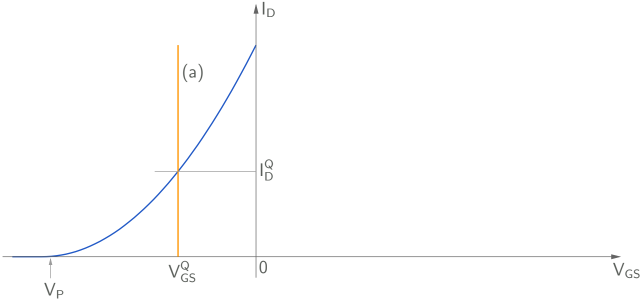

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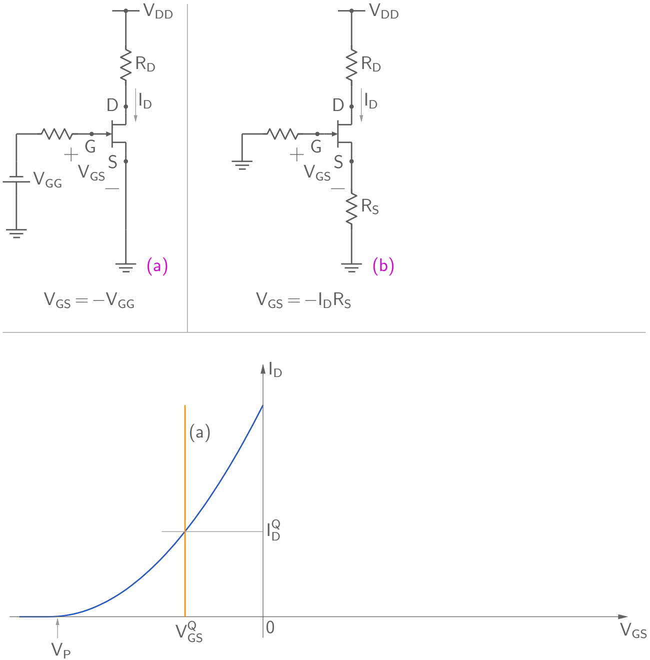

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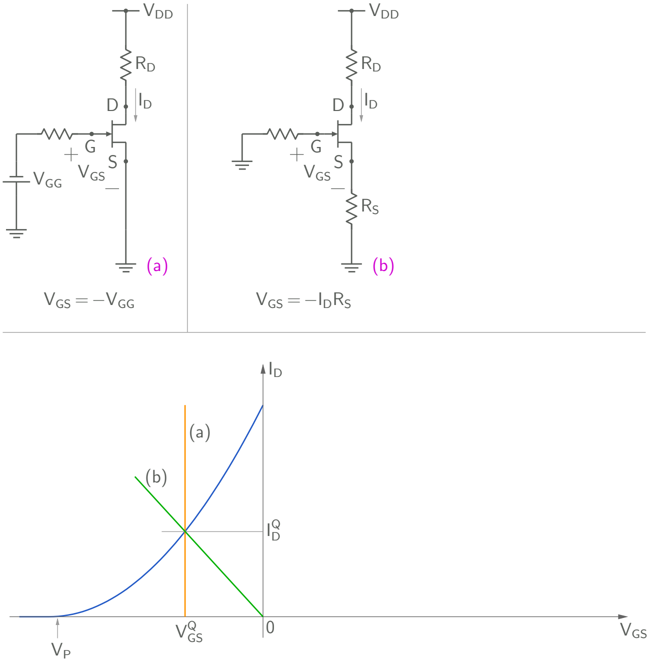

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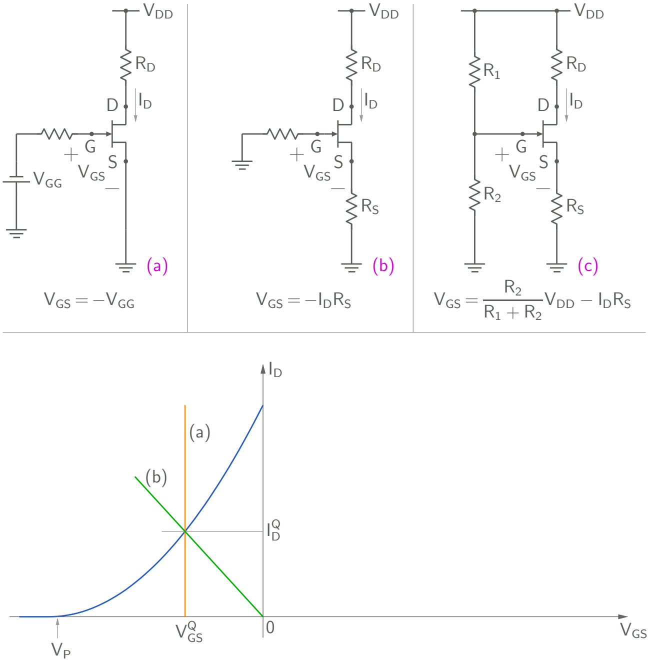

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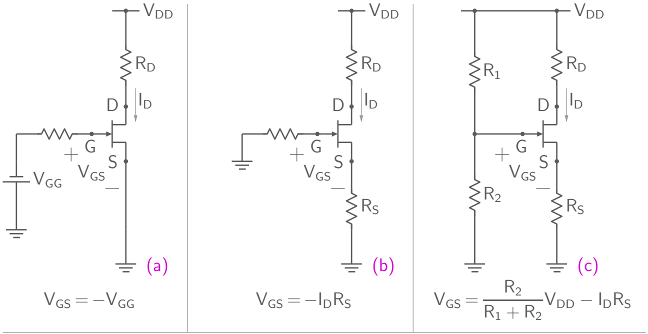

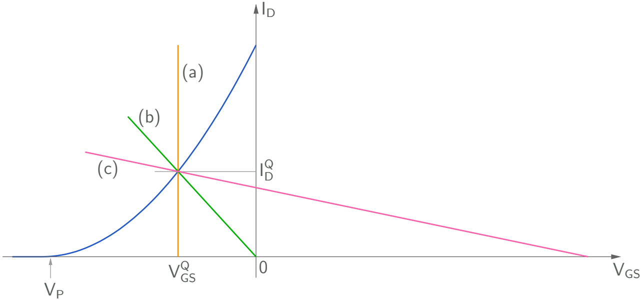

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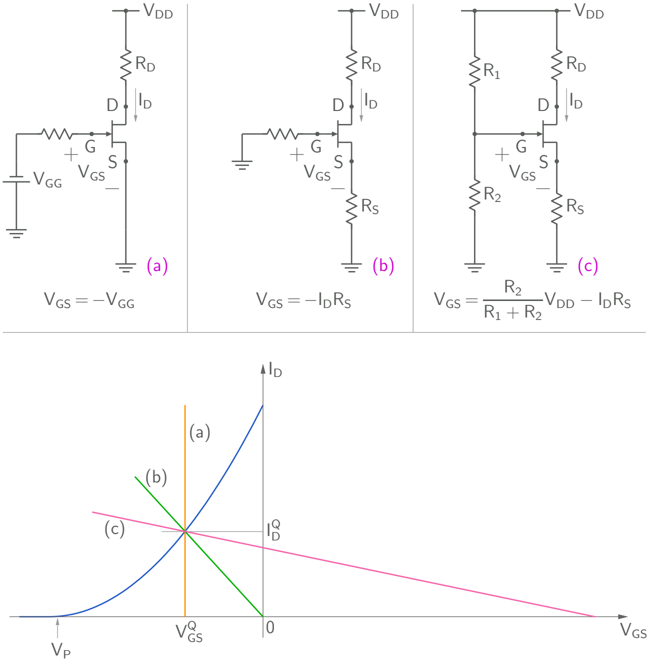

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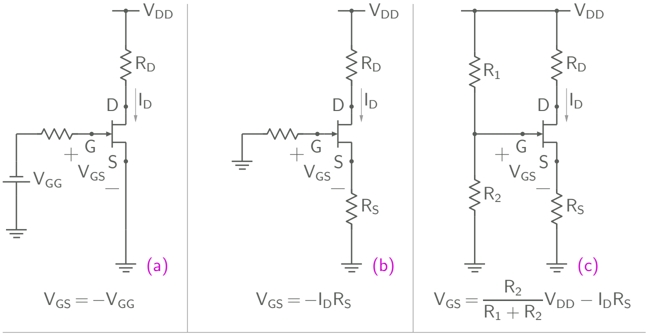

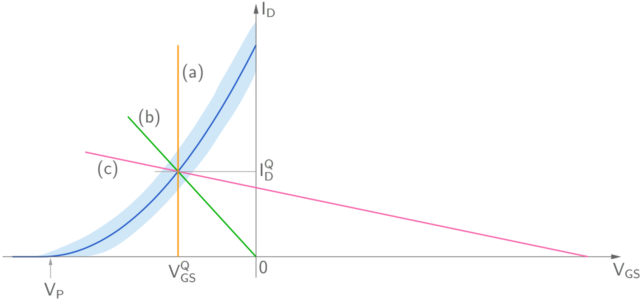

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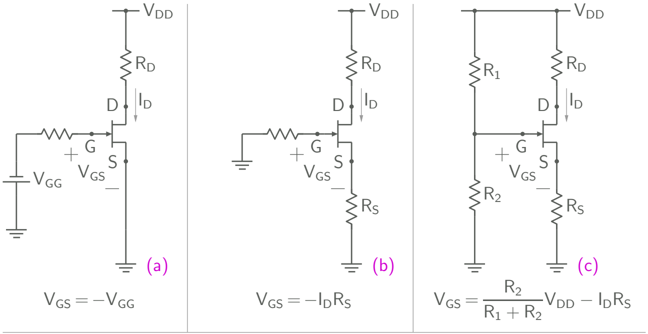
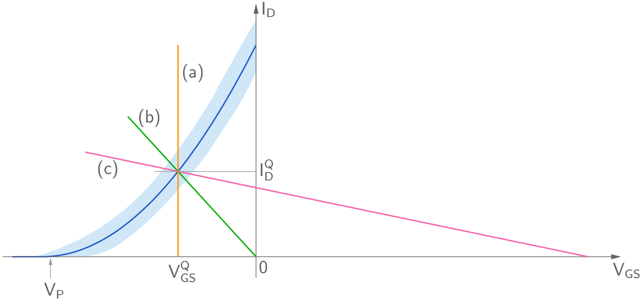
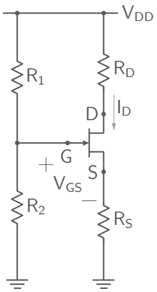
* The voltage divider scheme (c) is superior since it is least sensitive, i.e., the deviation in I_D is small compared to the other schemes.





Example

The JFET parameters are $I_{DSS} = 1\,\text{mA}$, $V_P = -2\,\text{V}$. For $V_{DD} = 12\,\text{V}$ and $R_D = 15\,\text{k}\Omega$, find suitable values of R_1, R_2, R_S to get a bias point of $I_D^Q = 0.4\,\text{mA}$ and $V_{DS}^Q = 4\,\text{V}$.



$$V_{GS} = \frac{R_2}{R_1 + R_2} V_{DD} - I_D R_S$$

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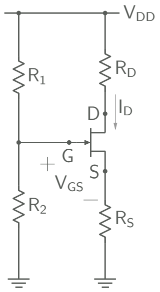

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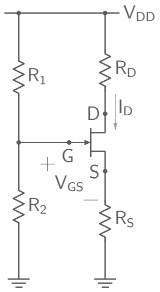

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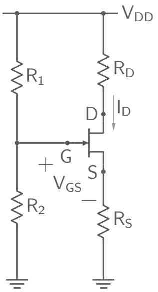

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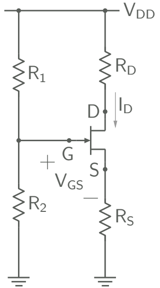

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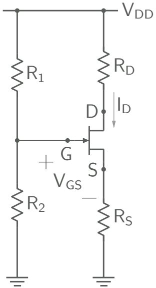

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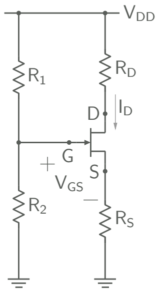

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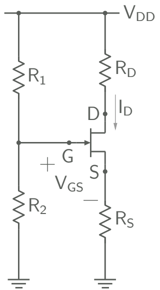
For V_{GS} to be $-0.735\,\text{V}$, we need $V_G = V_S + V_{GS} = 2\,\text{V} + (-0.735\,\text{V}) = 1.265\,\text{V}$.

The JFET parameters are $I_{DSS} = 1\,\text{mA}$, $V_P = -2\,\text{V}$. For $V_{DD} = 12\,\text{V}$ and $R_D = 15\,\text{k}\Omega$, find suitable values of R_1, R_2, R_S to get a bias point of $I_D^Q = 0.4\,\text{mA}$ and $V_{DS}^Q = 4\,\text{V}$.



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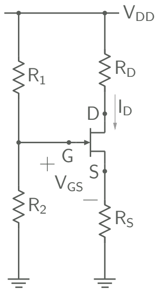
Since $V_G = \dfrac{R_2}{R_1 + R_2} V_{DD}$, we now need to choose suitable values of R_1 and R_2 to get the above V_G. $R_1 = 200\,\text{k}\Omega$ and $R_1 = 23.5\,\text{k}\Omega$ is one such choice.

The JFET parameters are $I_{DSS} = 1\,\text{mA}$, $V_P = -2\,\text{V}$. For $V_{DD} = 12\,\text{V}$ and $R_D = 15\,\text{k}\Omega$, find suitable values of R_1, R_2, R_S to get a bias point of $I_D^Q = 0.4\,\text{mA}$ and $V_{DS}^Q = 4\,\text{V}$.



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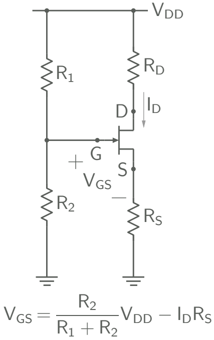
For V_{GS} to be $-0.735\,\text{V}$, we need $V_G = V_S + V_{GS} = 2\,\text{V} + (-0.735\,\text{V}) = 1.265\,\text{V}$.

Since $V_G = \dfrac{R_2}{R_1 + R_2} V_{DD}$, we now need to choose suitable values of R_1 and R_2 to get the above V_G. $R_1 = 200\,\text{k}\Omega$ and $R_1 = 23.5\,\text{k}\Omega$ is one such choice.

Finally, we check whether the transistor is indeed biased in saturation.

The JFET parameters are $I_{DSS} = 1\,\text{mA}$, $V_P = -2\,\text{V}$. For $V_{DD} = 12\,\text{V}$ and $R_D = 15\,\text{k}\Omega$, find suitable values of R_1, R_2, R_S to get a bias point of $I_D^Q = 0.4\,\text{mA}$ and $V_{DS}^Q = 4\,\text{V}$.



Solution: The drain current in the saturation region is given by

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Example

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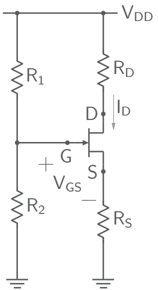

$$V_{GS} = \frac{R_2}{R_1 + R_2} V_{DD} - I_D R_S$$

Solution: The drain current in the saturation region is given by

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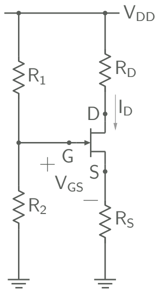

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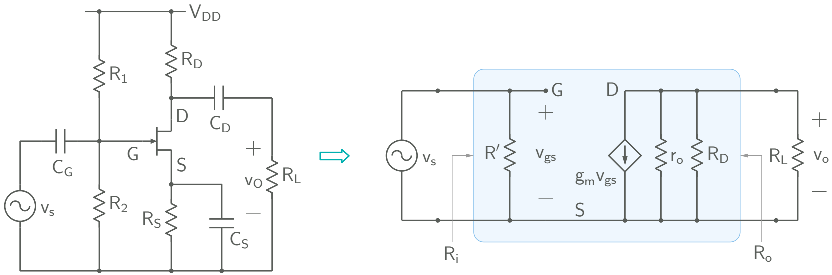
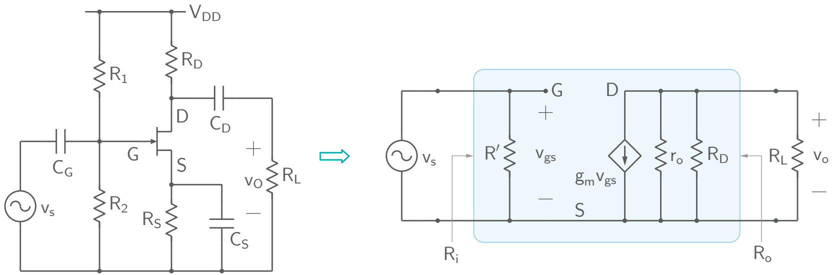
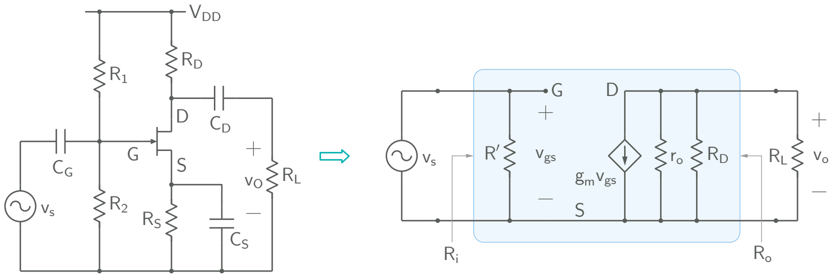
Common-source amplifier



Common-source amplifier



* $A_V \equiv \dfrac{v_o}{v_s} = -g_m(R'_D \parallel R_L)$, where $R'_D = R_D \parallel r_o \approx R_D$ if r_o is large.



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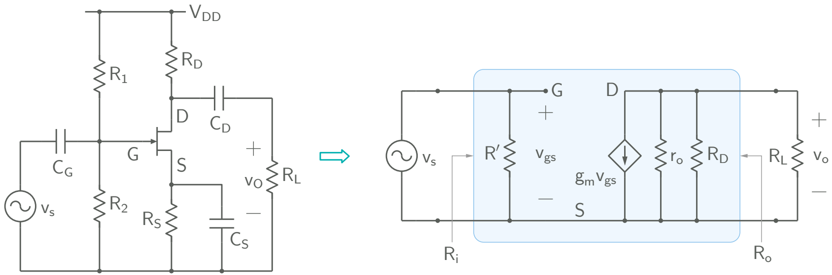

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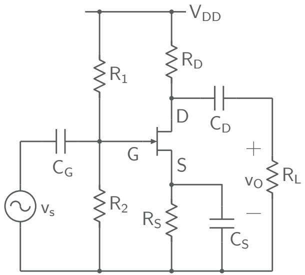
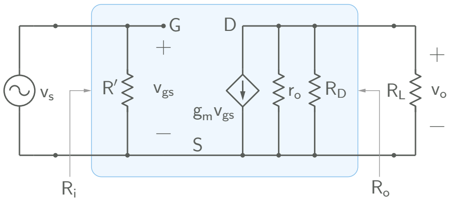
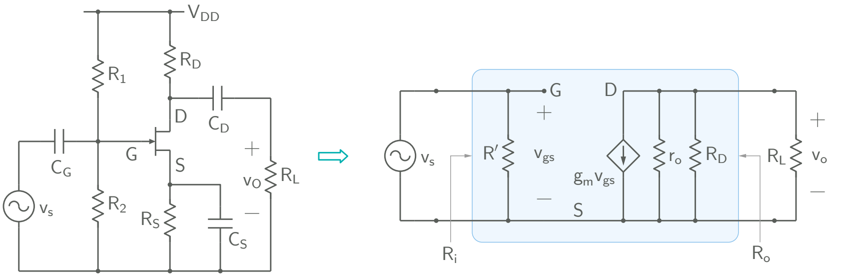
∗ $R_i = R' = R_1 \parallel R_2$, $R_o = R'_D$.

Common-source amplifier: Example





For the common-source amplifier of the last example, find (a) gain with $R_L \to \infty$ and (b) input resistance R_i.



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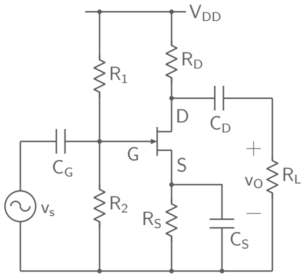

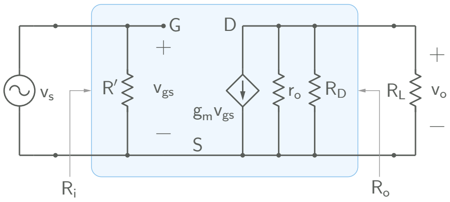

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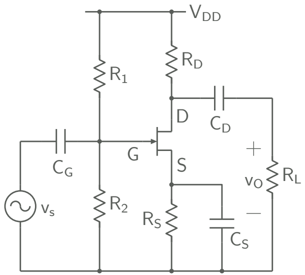

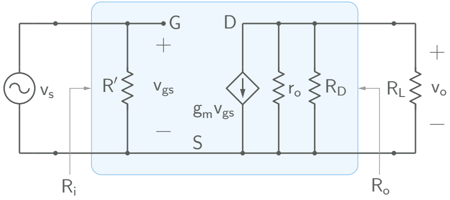

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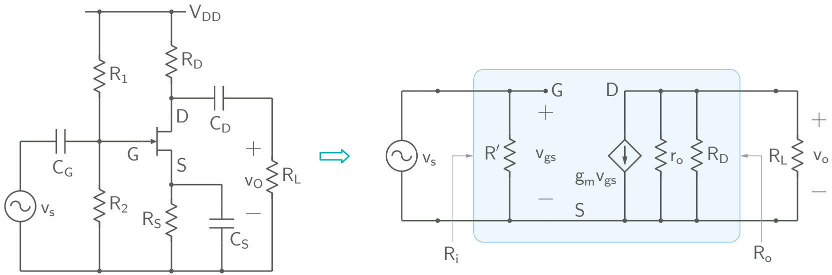

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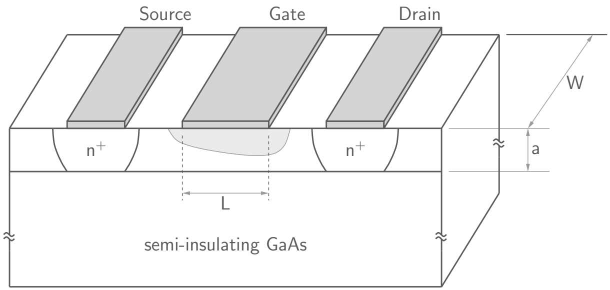
n-channel Metal-Semiconductor Field-Effect Transistor (MESFET)



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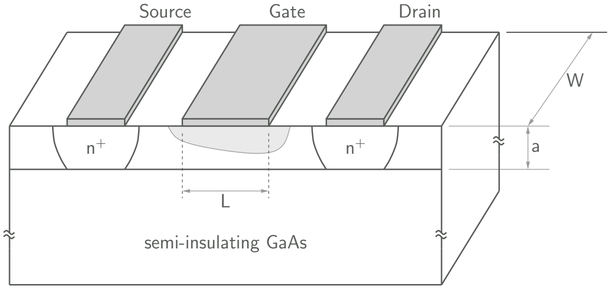

∗ In a MESFET, the channel conductance is modulated by a rectifying metal-semiconductor junction.

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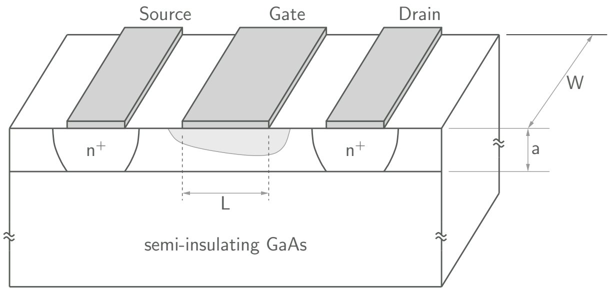

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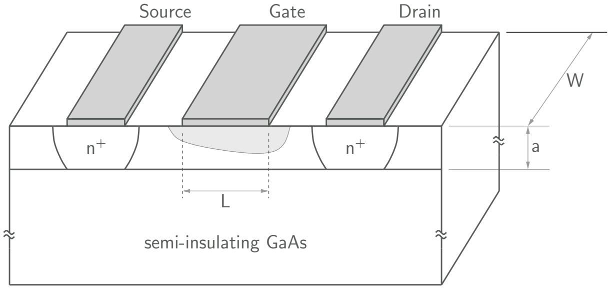

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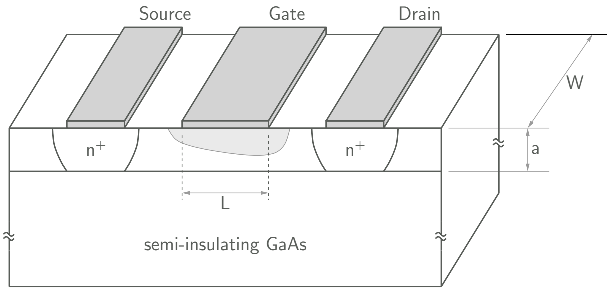

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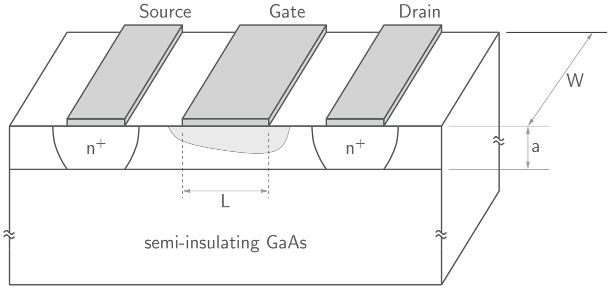

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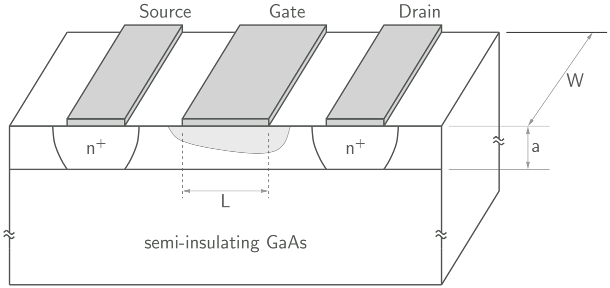

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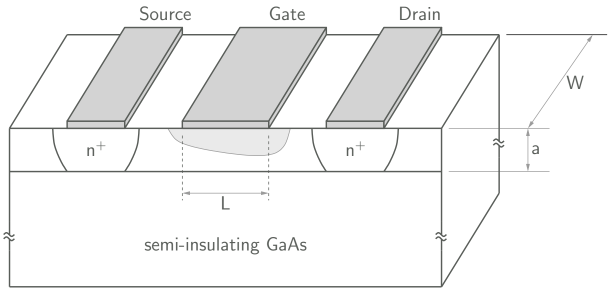

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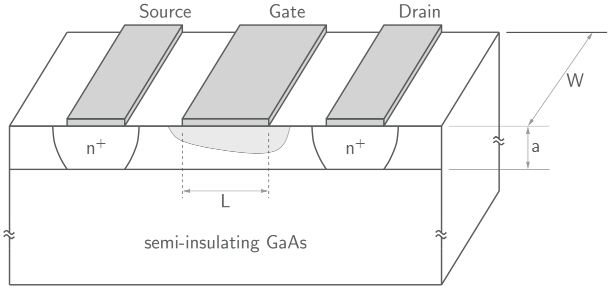

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* GaAs MESFETs are commonly used in high-frequency (a few GHz) applications.