Some implications of the Shockley diode equation

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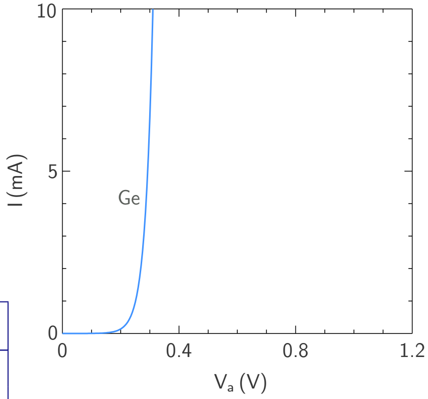

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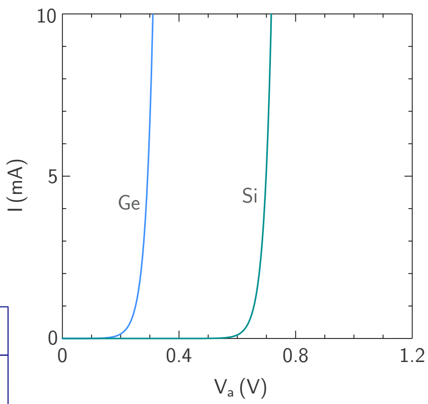

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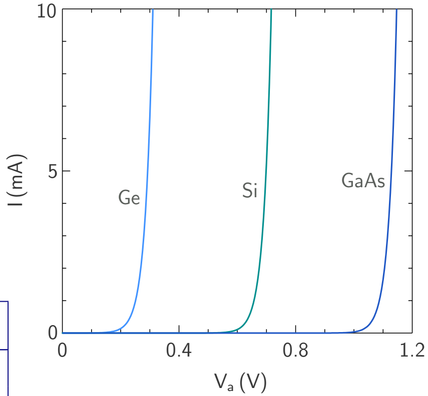

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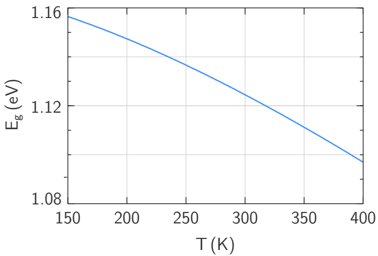

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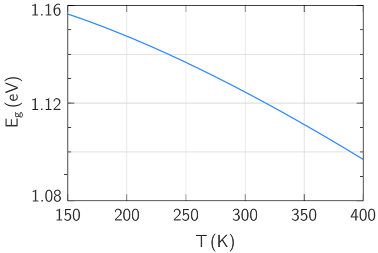

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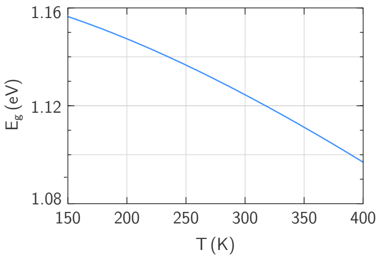

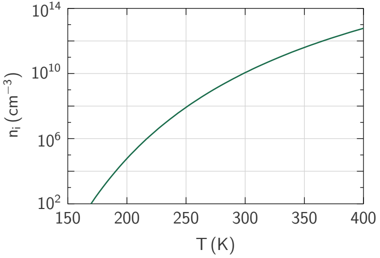

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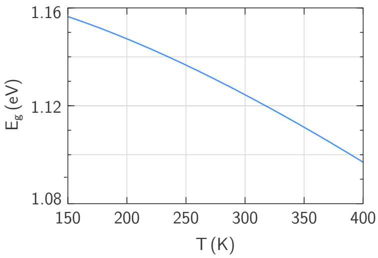

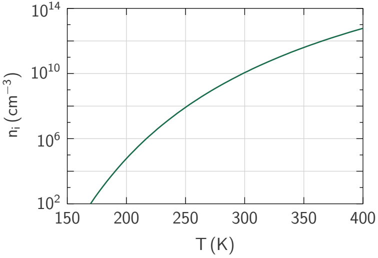

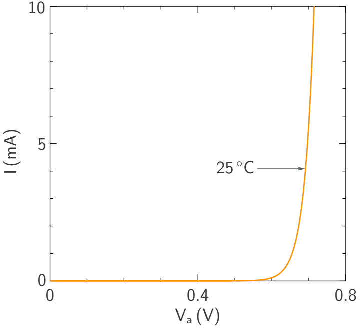

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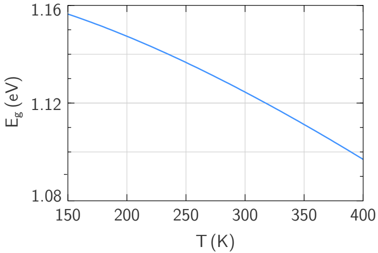

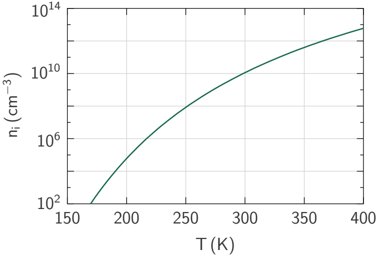

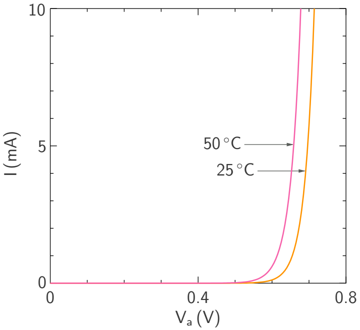

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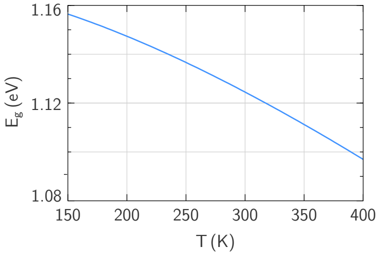

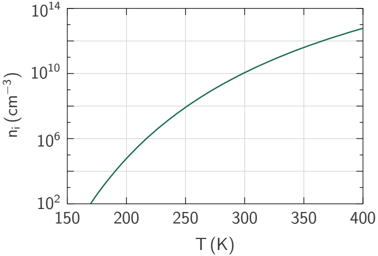

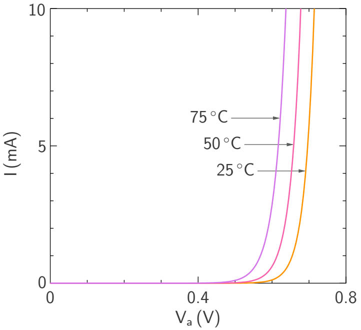

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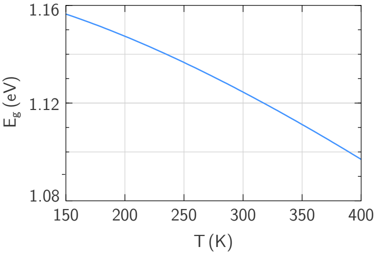
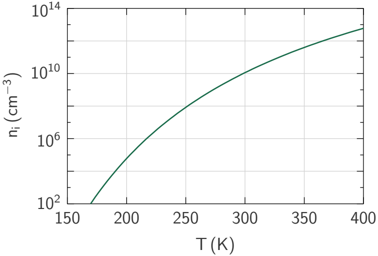
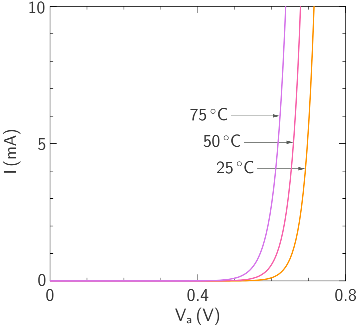
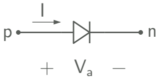
For silicon, the I-V curve shifts by about $-2\,\text{mV}/^\circ\text{C}$ as the temperature is increased.

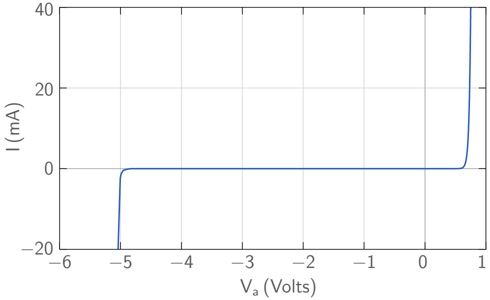


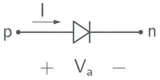


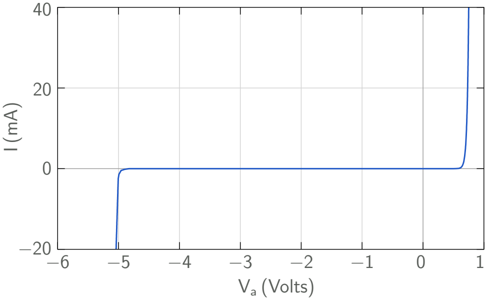


Reverse breakdown

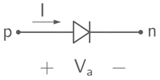


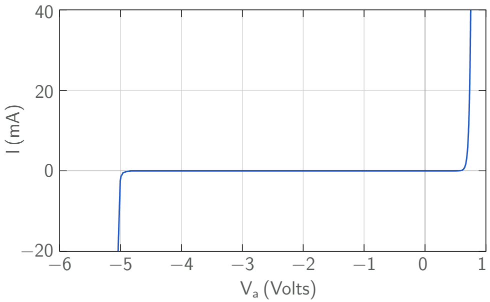






* A real diode cannot withstand indefinitely large reverse voltages and "breaks down" at some point as V_R is increased.





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* Reverse breakdown can be due to
  - impact ionisation (avalanche breakdown)
  - tunneling (Zener breakdown)

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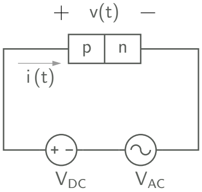
* Two situations are of interest:
    * Small-signal behaviour (AC): With $V_a(t) = V_{DC} + V_m \sin \omega t$, how does the current vary with time when V_m is "small?"
    * Large-signal behaviour: The variation in the applied voltage is not small. In particular, we are interested in the turn-off and turn-on transients.

Small-signal behaviour



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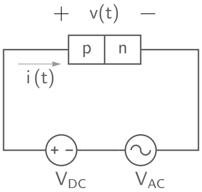

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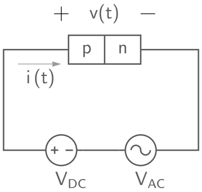

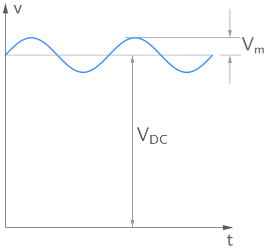

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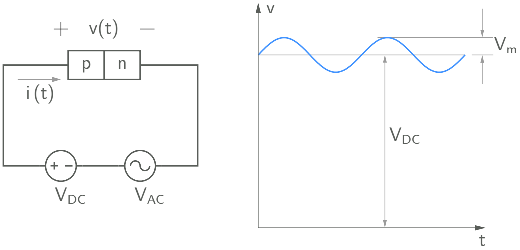

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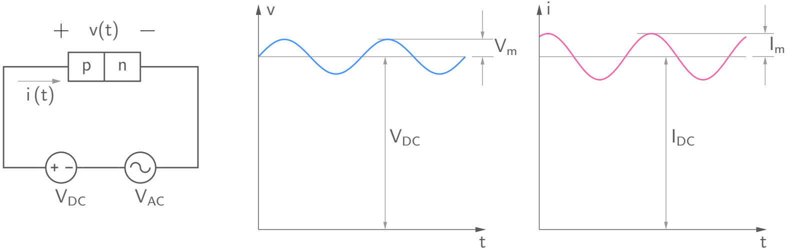

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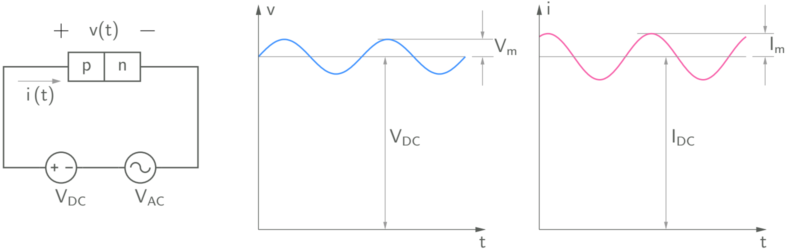

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* In small-signal analysis, we are interested in the relationship between the sinusoidal parts of the current and voltage, in particular, the ratio of the current and voltage phasors, $I_m \angle \phi / V_m \angle 0$.

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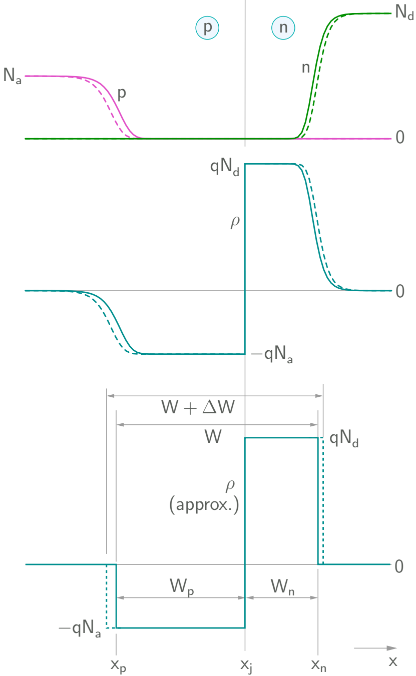

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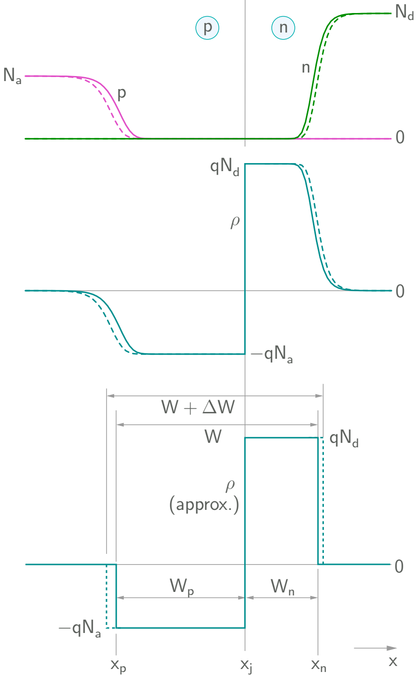
* This change is made possible by removal of majority carriers.



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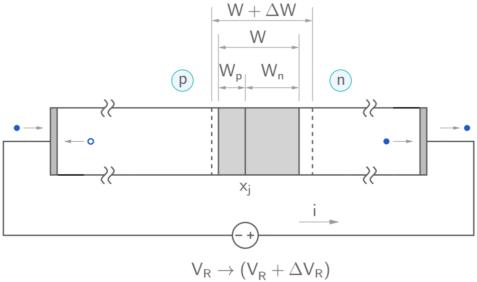

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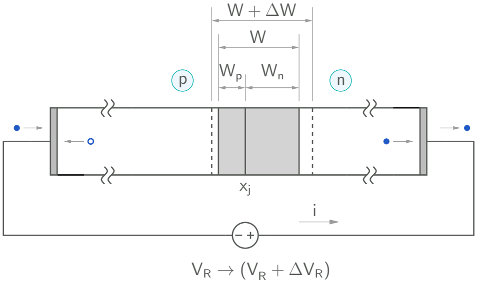

* Movement of majority carriers is relatively fast, and the time scale involved is $\sim \tau = \dfrac{\epsilon_s}{q \mu_n n}$ for electrons.

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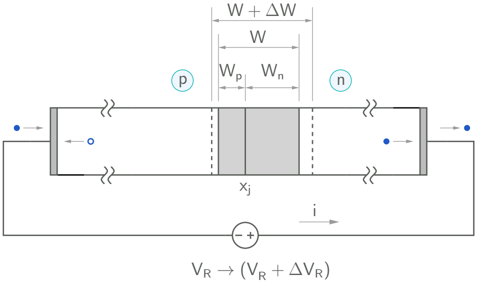

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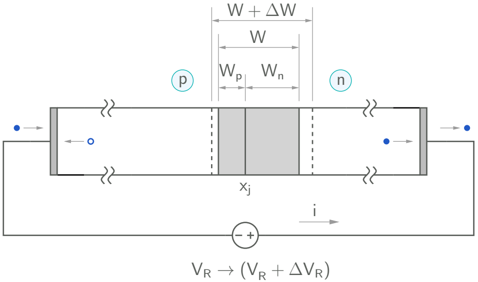

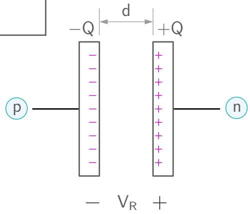

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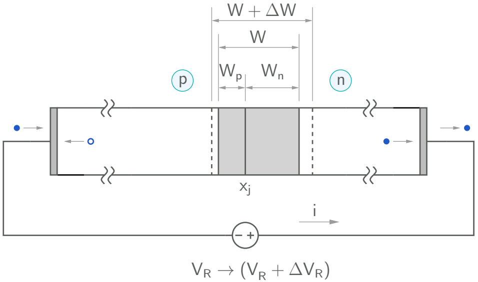

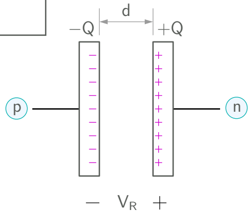

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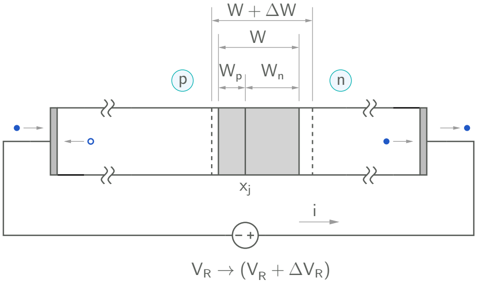

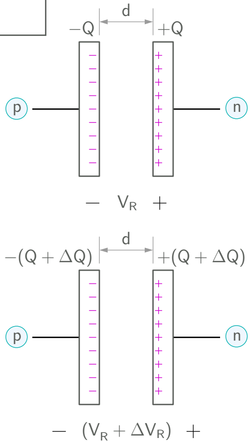

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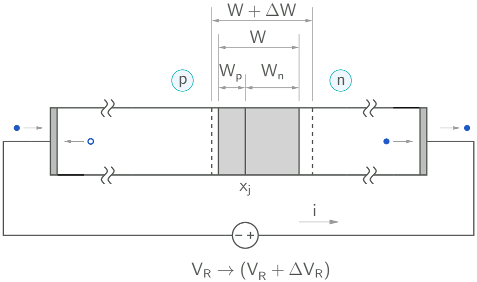

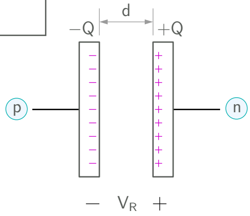

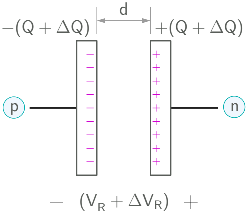

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  Note: For simplicity, we have not shown V_{bi} in the figure; the drop across the junction is actually $V_{\text{bi}} + V_R$, as seen before.

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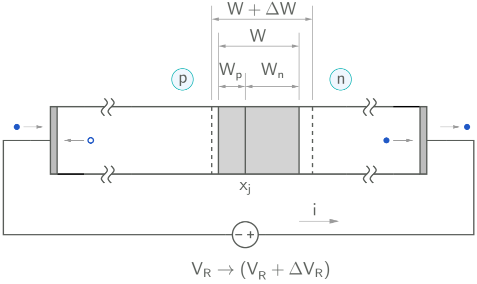

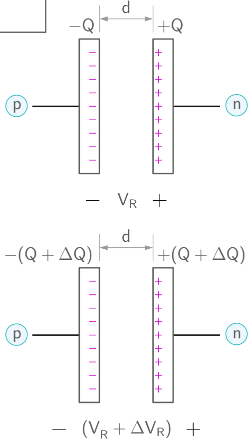

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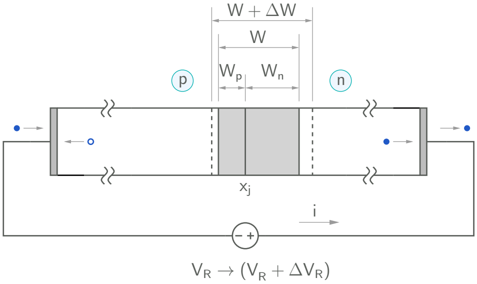

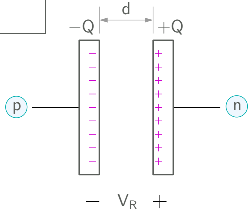

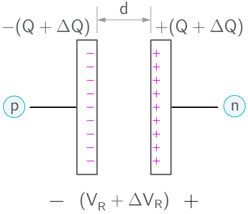

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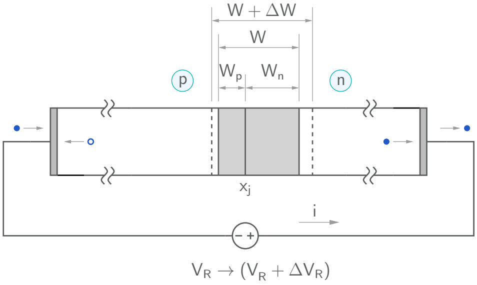

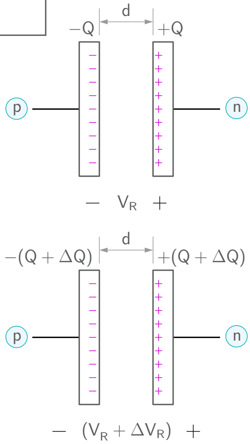

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* For a reverse-biased *pn* junction, $C = \dfrac{\Delta Q}{\Delta V_R}$.

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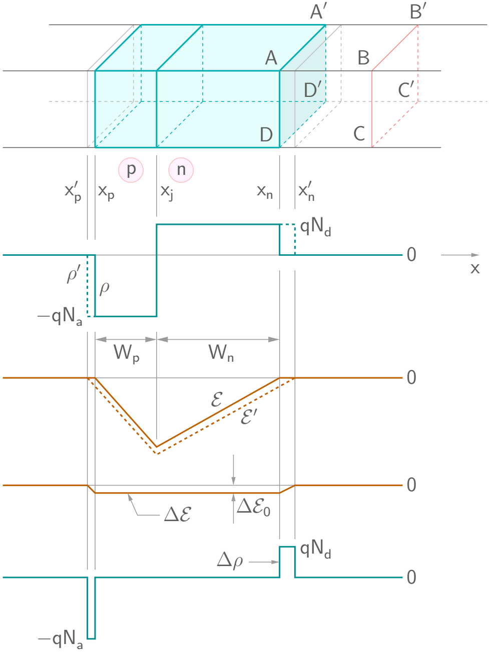
$$V_{\text{bi}} + V_R = -\int_{x_p}^{x_n} \mathcal{E}(x)dx$$



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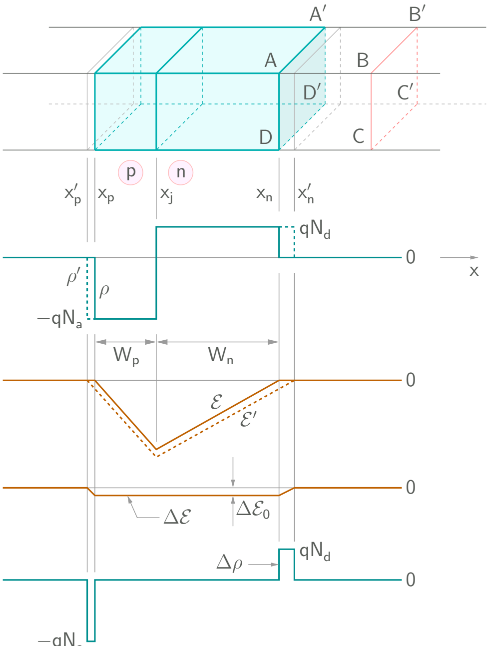

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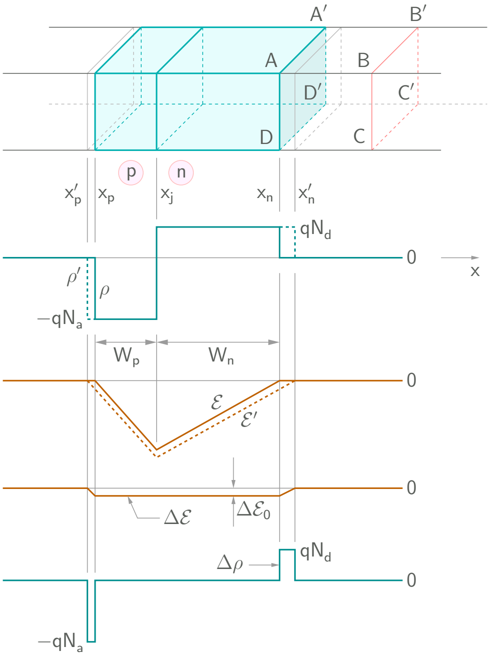

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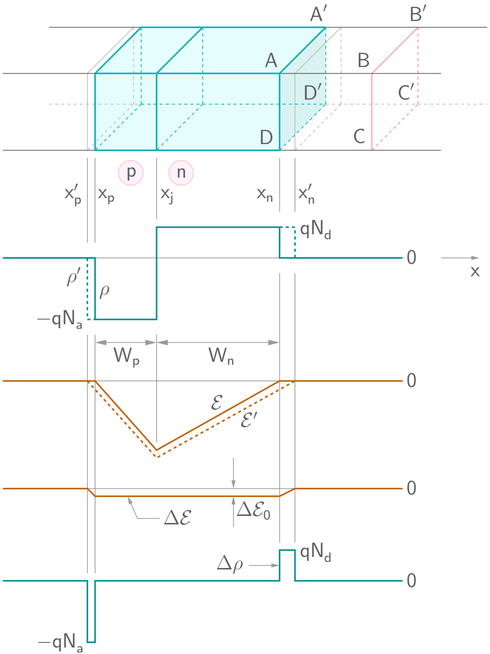

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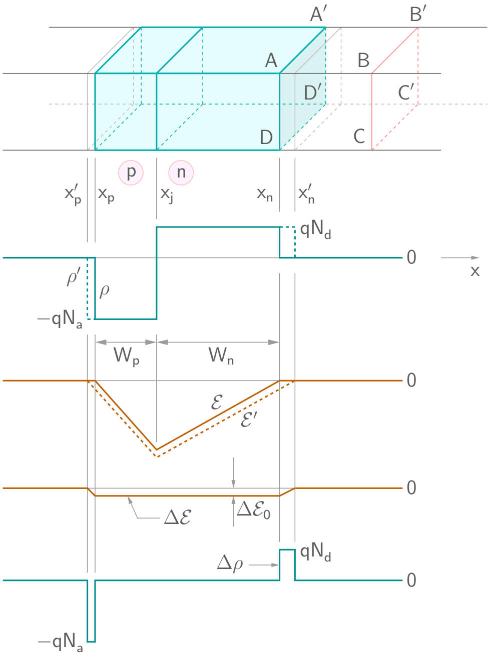

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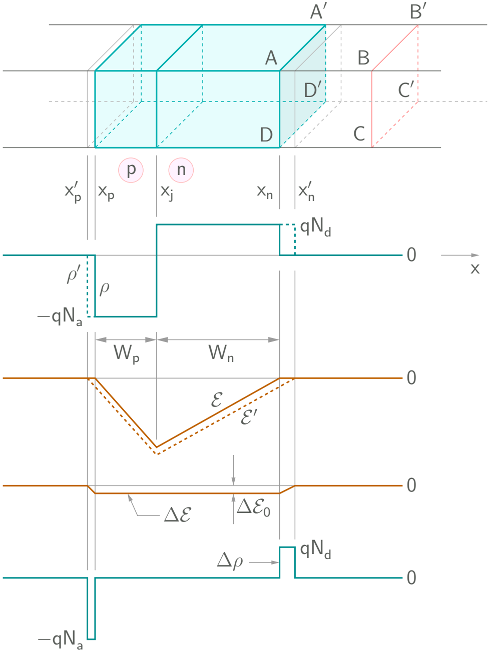
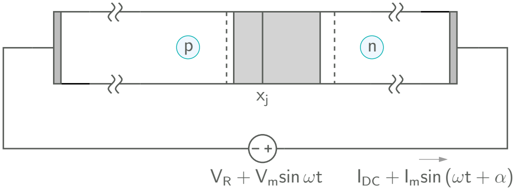
C_J is called the "junction capacitance" or "depletion layer capacitance."



Example



For an abrupt, uniformly doped silicon *pn* junction, with $N_a = 10^{17}\,\text{cm}^{-3}$ and $N_d = 2 \times 10^{16}\,\text{cm}^{-3}$, and area $= 0.01\,\text{cm}^2$, calculate the capacitance (i.e., the differential capacitance) for an applied reverse bias of $V_R = 2\,\text{V}$ $(T = 300\,\text{K})$.

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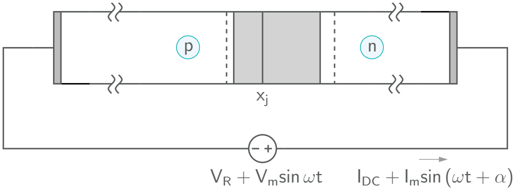

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Solution: The built-in voltage is

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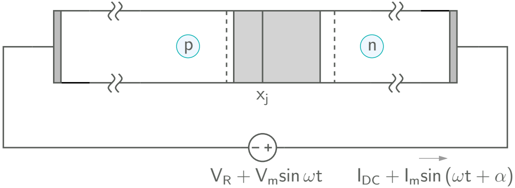

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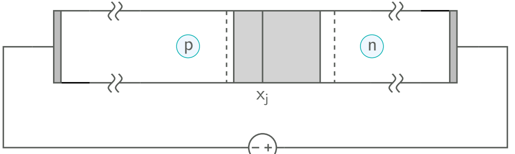

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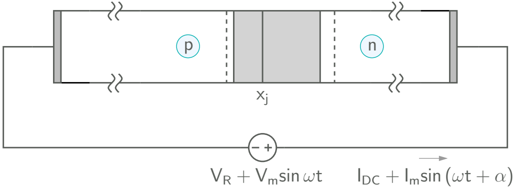
$$\text{Capacitance } C_J = \frac{A\,\epsilon_s}{W} = \frac{0.01\,\text{cm}^2 \times 11.7 \times 8.85 \times 10^{-14}\,\text{F/cm}}{0.464 \times 10^{-4}\,\text{cm}}$$

Example



For an abrupt, uniformly doped silicon *pn* junction, with $N_a = 10^{17}\,\text{cm}^{-3}$ and $N_d = 2 \times 10^{16}\,\text{cm}^{-3}$, and area $= 0.01\,\text{cm}^2$, calculate the capacitance (i.e., the differential capacitance) for an applied reverse bias of $V_R = 2\,\text{V}$ ($T = 300\,\text{K}$).

Solution: The built-in voltage is

$$V_{\text{bi}} = \frac{kT}{q} \log\left(\frac{N_a N_d}{n_i^2}\right) = 0.77\,\text{V}\,.$$

The depletion width for $V_R = 2\,\text{V}$ is $W = \sqrt{\frac{2\epsilon}{q} \frac{N_a + N_d}{N_a N_d} (V_{\text{bi}} + V_R)} = 0.464\,\mu\text{m}$.

$$\text{Capacitance } C_J = \frac{A\,\epsilon_s}{W} = \frac{0.01\,\text{cm}^2 \times 11.7 \times 8.85 \times 10^{-14}\,\text{F/cm}}{0.464 \times 10^{-4}\,\text{cm}}$$

$$= 2.23 \times 10^{-10}\ \text{F}$$

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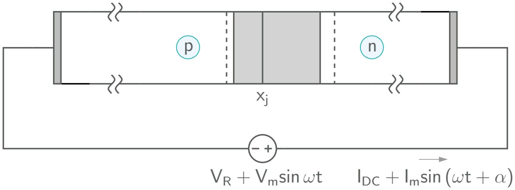

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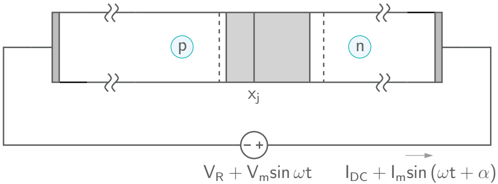

For a silicon n^+p junction, $N_a = 10^{16}\,\mathrm{cm}^{-3}$, and area $= 0.01\,\mathrm{cm}^2$. Plot C_J versus V_a for $-5\,\mathrm{V} < V_a < -0.1\,\mathrm{V}$. Also, plot $1/C_J^2$ versus V_a. What information can one obtain from the second plot? Take $V_{bi} \approx 0.9\,\mathrm{V}$. ($T = 300\,\mathrm{K}$)

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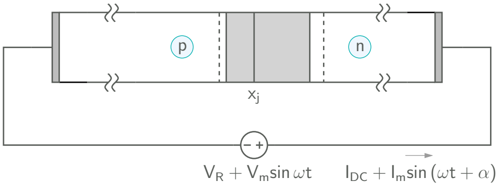

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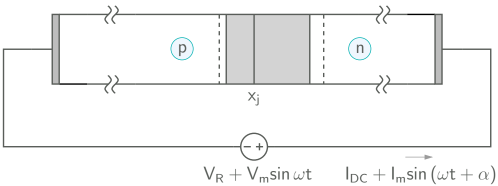

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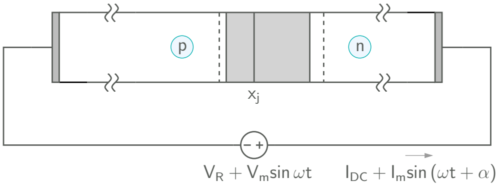

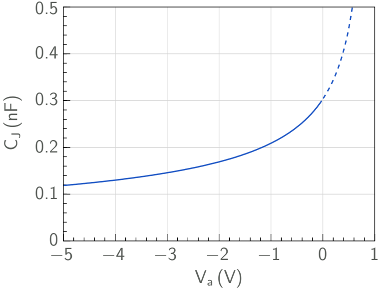

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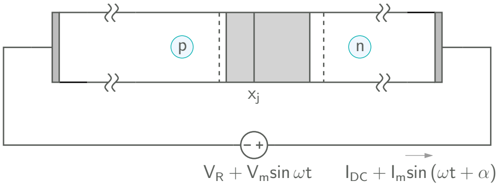

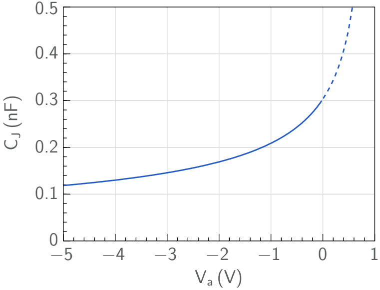

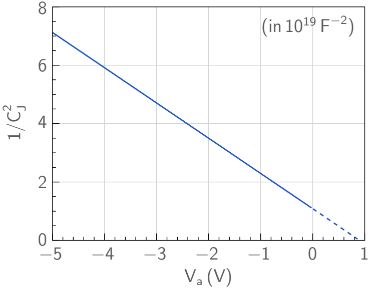

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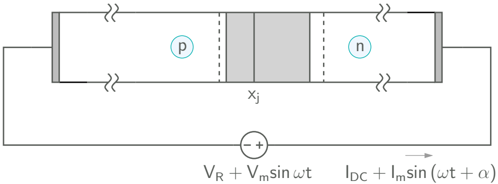

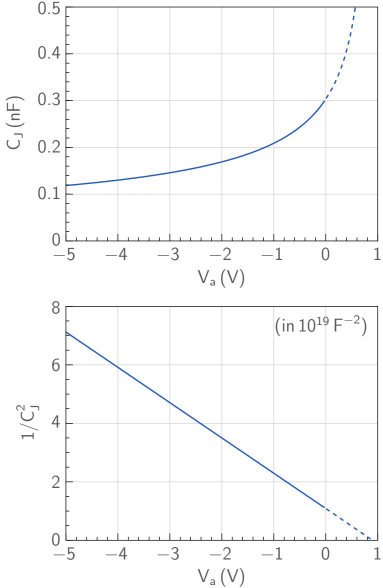

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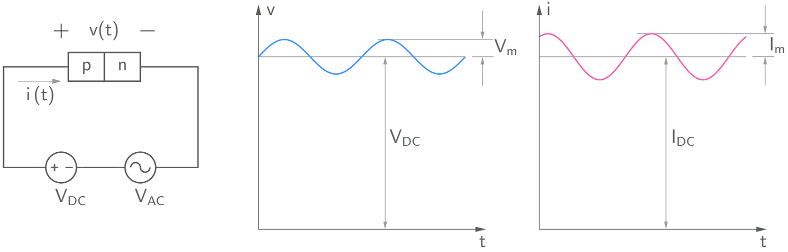
$\rightarrow 1/C_J^2$ versus V_a: Slope gives N_a; x-intercept gives V_{bi}.

What is meant by "small-signal" condition?



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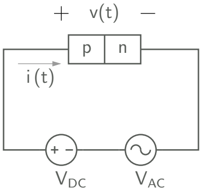

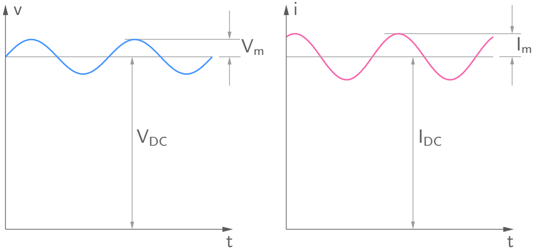

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For a reverse-biased *pn* junction, $C_J = \dfrac{dQ}{dV_a} = \dfrac{A\epsilon_s}{W(V_a)} = \dfrac{K}{\sqrt{V_{\mathrm{bi}} - V_a}}$, with $K = A\epsilon_s \sqrt{\dfrac{qN_aN_d}{2\epsilon_s(N_a + N_d)}}$.

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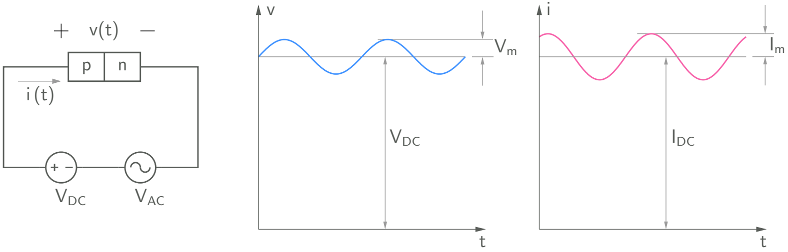

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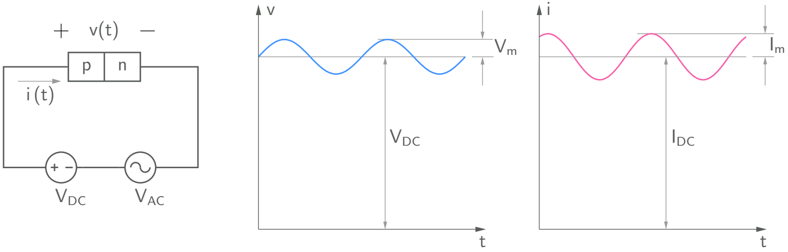

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$\rightarrow$ $i(t)$ is sinusoidal if C_J can be treated as a constant.

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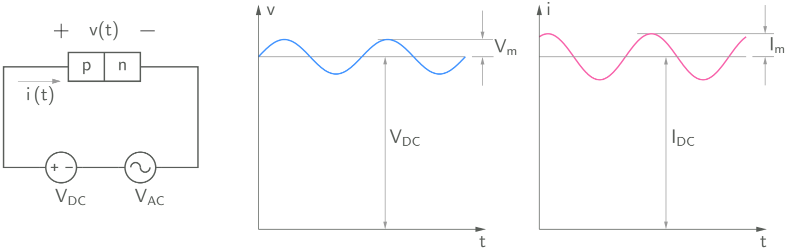

$$v_a(t) = -(V_R + V_m \sin \omega t) \rightarrow -(V_R + V_m) < v_a < -(V_R - V_m).$$

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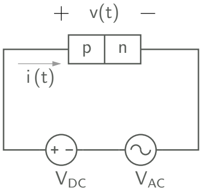

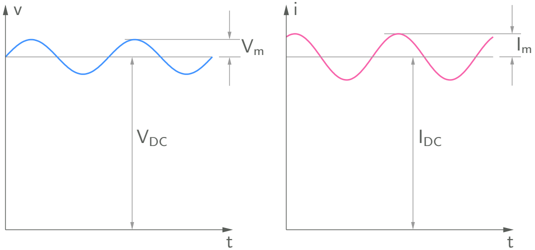

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Consider one of these two extreme values,

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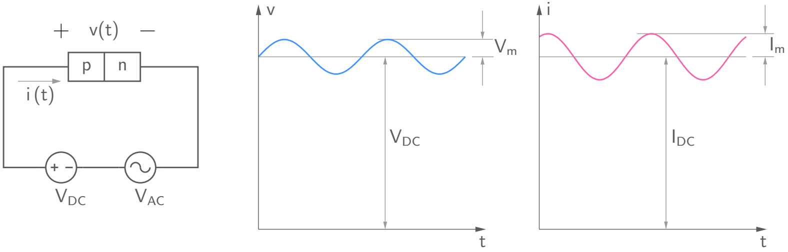

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If $\dfrac{V_m}{2\,(V_{\text{bi}} + V_R)} \ll 1$, C_J can be treated as a constant.

M. B. Patil, IIT Bombay

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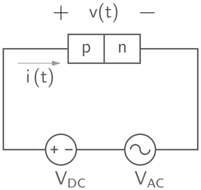

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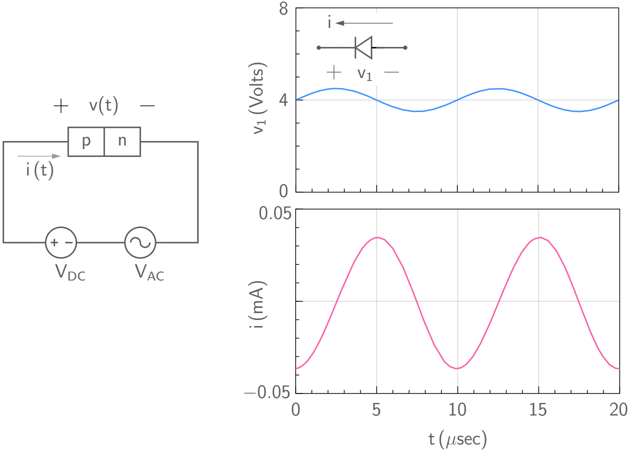

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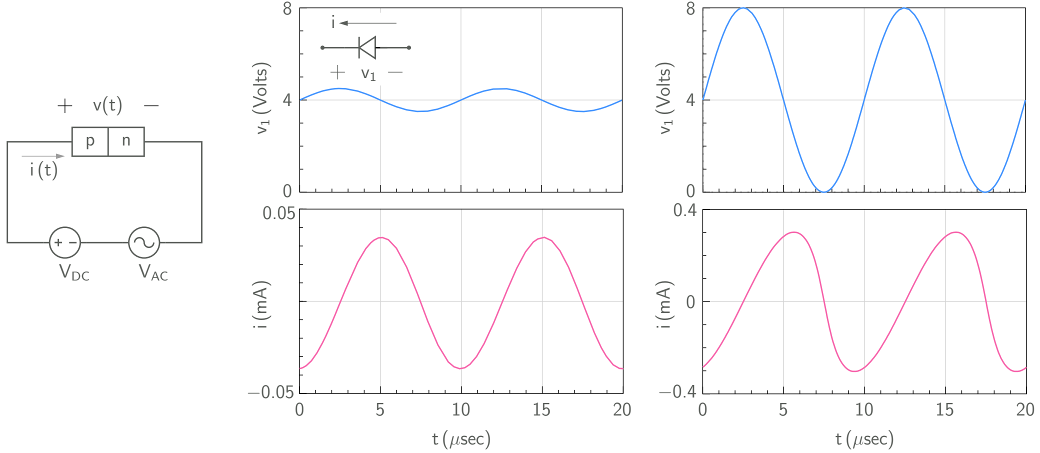

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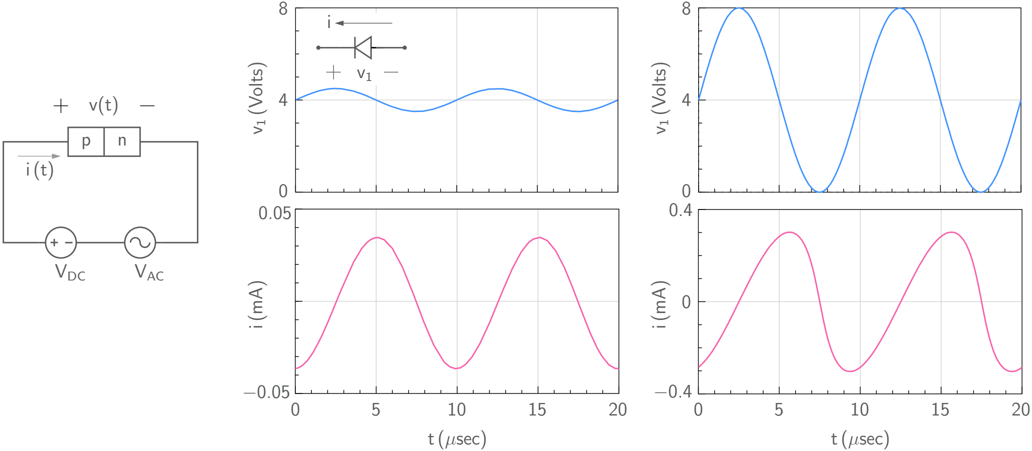
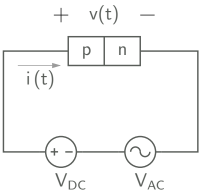
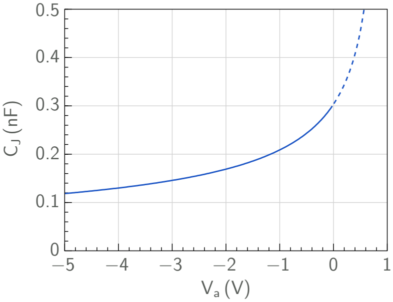
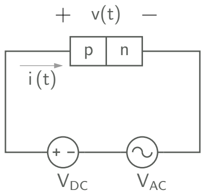


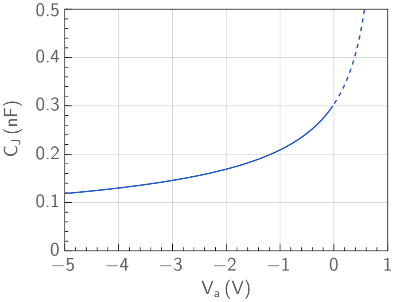
* Small-signal condition: $\dfrac{V_m}{2\,(V_{\mathrm{bi}} + V_R)} \ll 1.$
* If the small-signal condition is not satisfied, $i(t)$ shows distortion.

Small-signal behaviour: reverse bias









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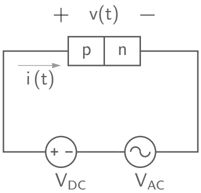

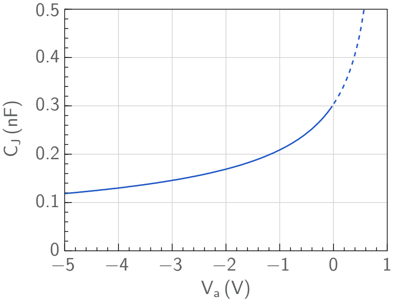

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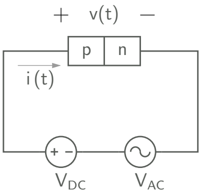

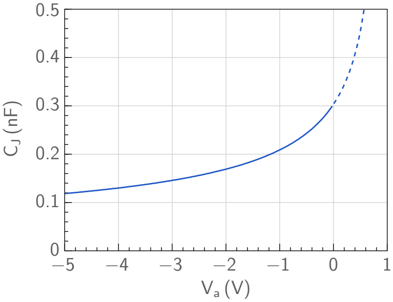

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* Specially designed diodes called "varactors" (variable reactors) are used in applications such as voltage-variable tuning, mixing, detection, etc.
* In these devices, the doping density profiles are designed so as to get a large capacitance change for a small change in reverse bias.