Semiconductor Devices

MOS Transistors: Part 3

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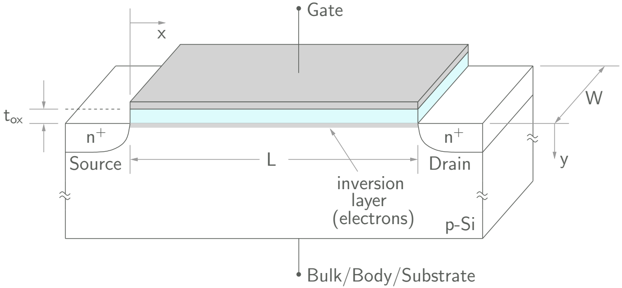
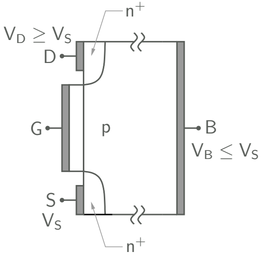
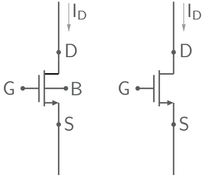
NMOS transistor





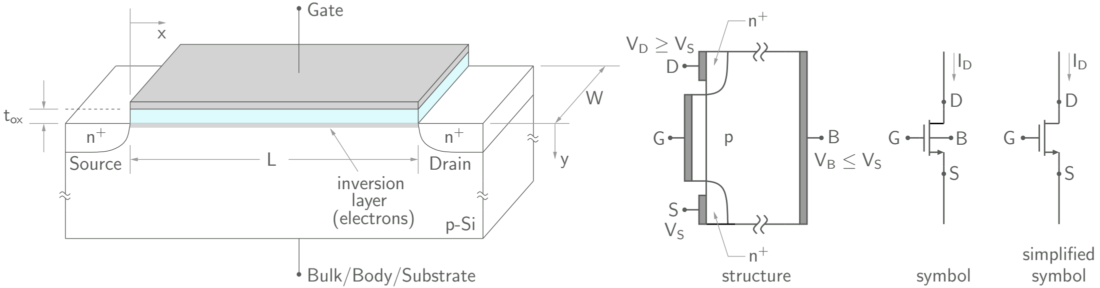
structure



symbol

simplified symbol

NMOS transistor



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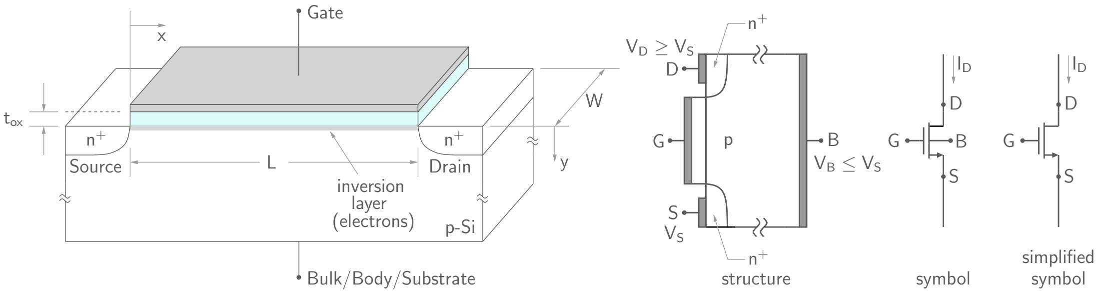
NMOS transistor



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* The bulk terminal must be suitably biased for the transistor to work properly, with the S-B and D-B junction under reverse bias.

  Generally, the bulk terminal for an NMOS transistor is connected to the lowest potential in the circuit (typically, 0 V).

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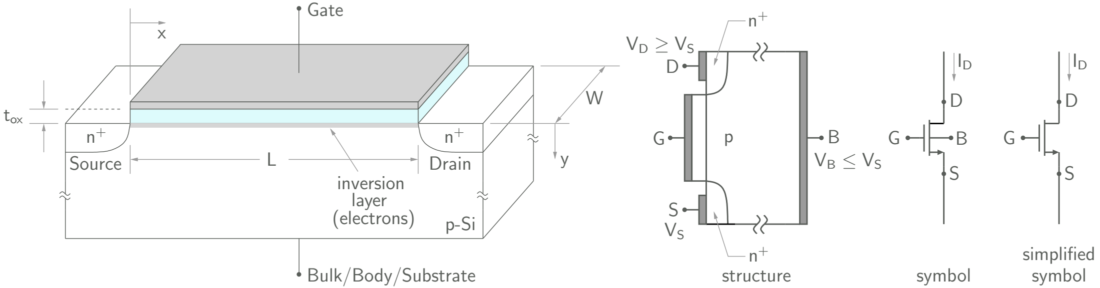

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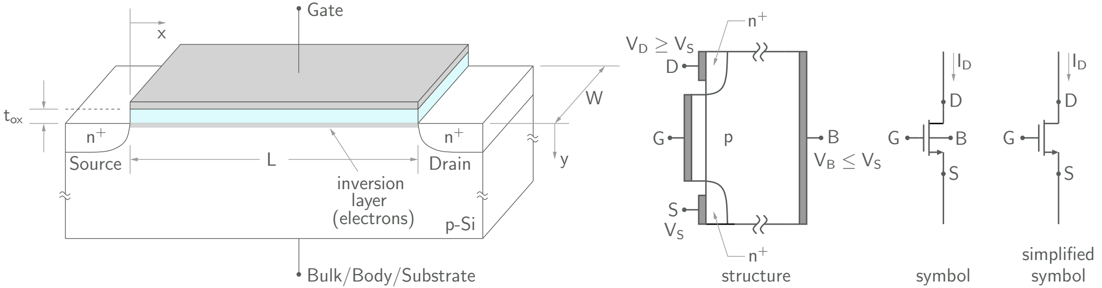
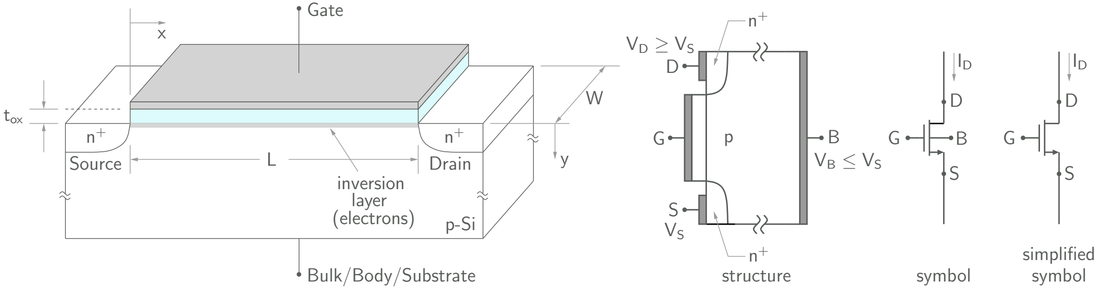
- The bulk terminal must be suitably biased for the transistor to work properly, with the S-B and D-B junction under reverse bias.

  Generally, the bulk terminal for an NMOS transistor is connected to the lowest potential in the circuit (typically, 0 V).
- The source and drain terminals are often interchangeable.

NMOS transistor

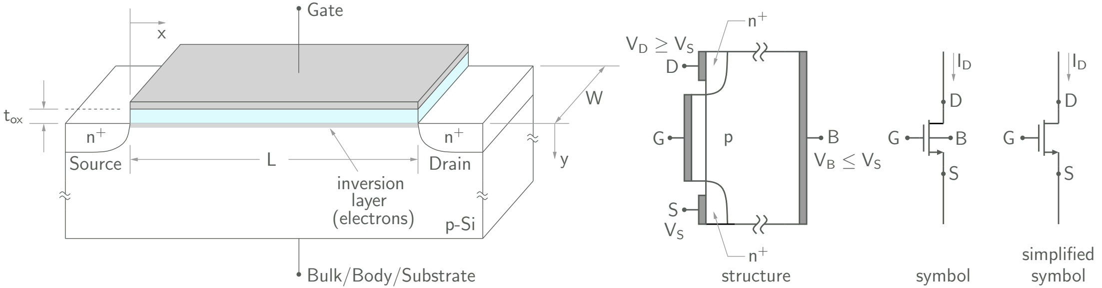


NMOS transistor

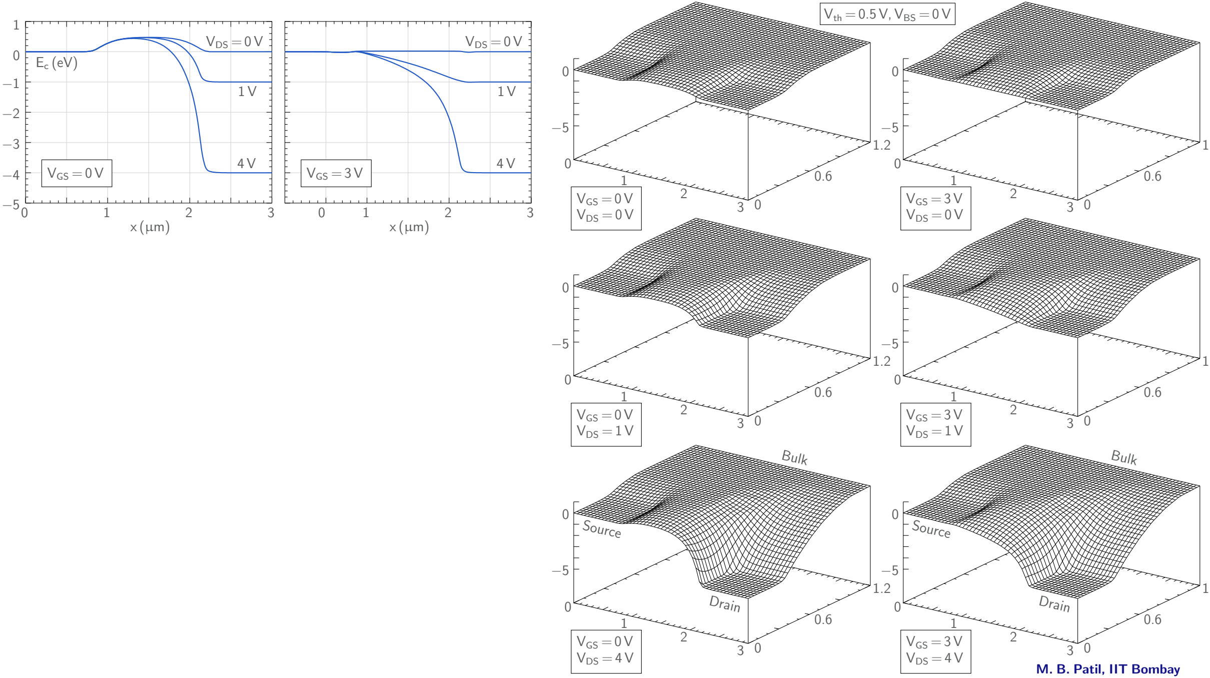


* When $V_G - V_S < V_{\text{th}}$, the device is under accumulation (i.e., p-type near the surface) or depletion, and no significant current is possible. This is the non-conducting or "off" state.

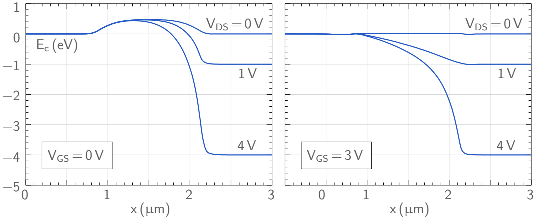
NMOS transistor

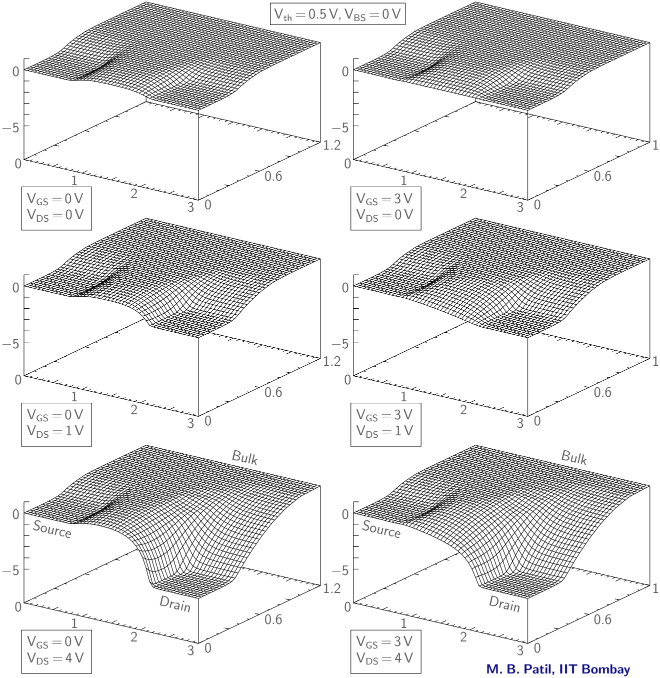


* When $V_G - V_S < V_{\text{th}}$, the device is under accumulation (i.e., *p*-type near the surface) or depletion, and no significant current is possible. This is the non-conducting or "off" state.
* When $V_G - V_S \geq V_{\text{th}}$, an inversion layer (*n*-type) forms at the surface and "connects" the source and drain regions. A substantial current flow is now possible — electrons flow from source to drain, and I_D flows in the opposite direction, i.e., in the direction shown by the source arrow in the symbol. This is the conducting or "on" state.

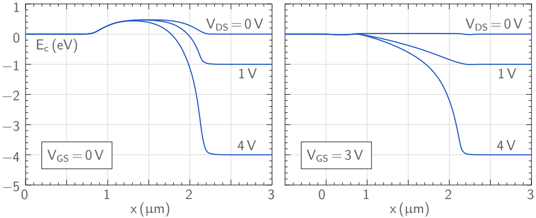


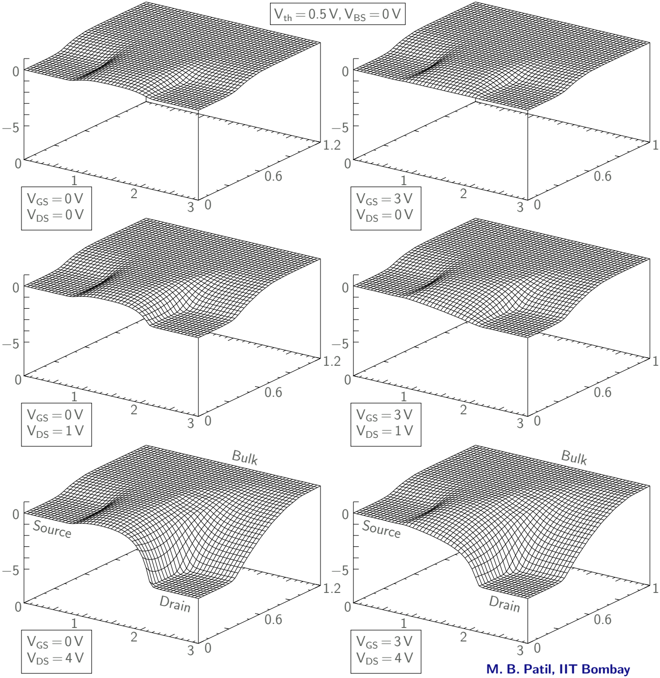
M. B. Patil, IIT Bombay





* As we would expect from heavily doped regions, there is no perceptible variation in E_c (and therefore in ψ, since $E_c \sim -q\psi$) in the source and drain regions under all bias conditions. These regions are basically charge neutral and equipotential because of their high conductivity.





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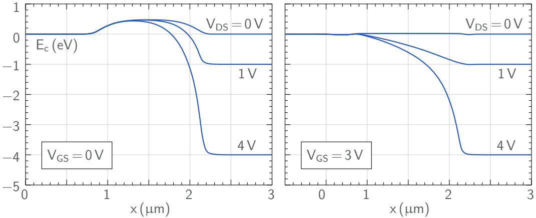

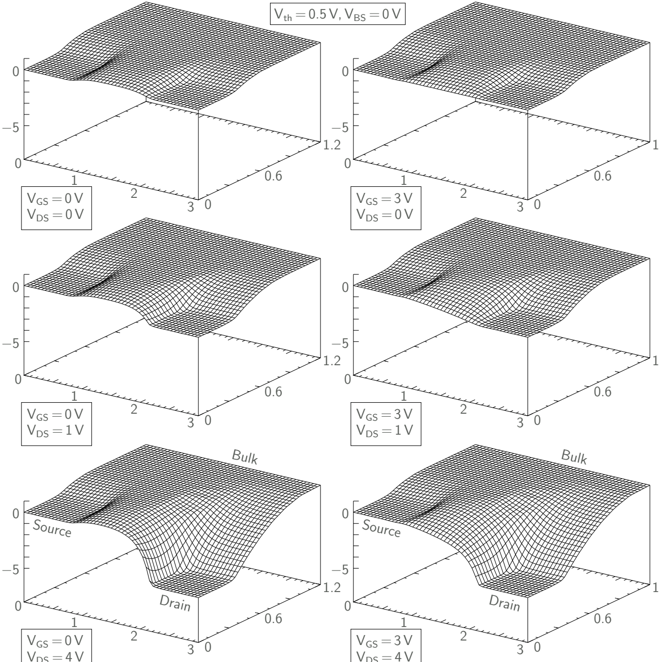

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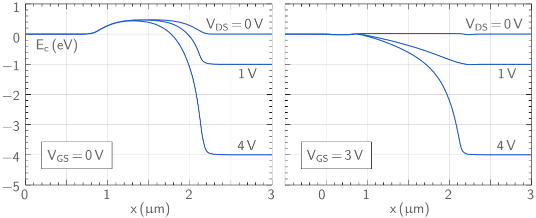

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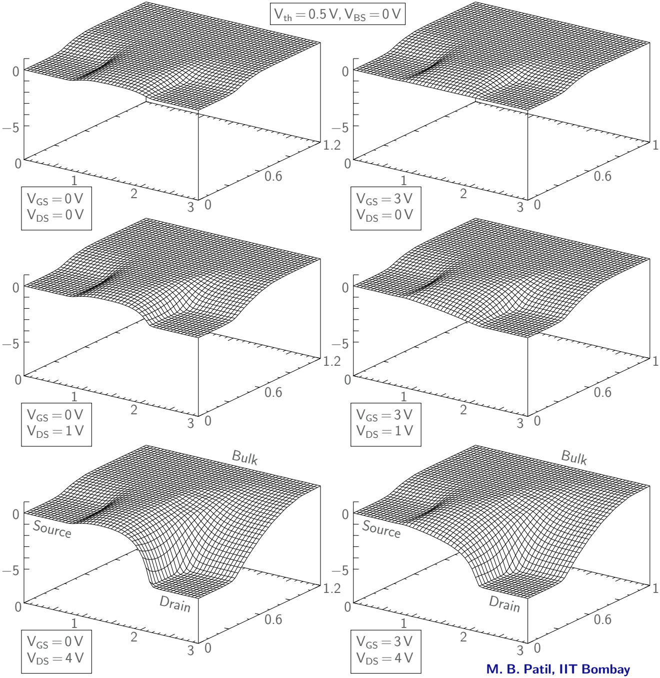
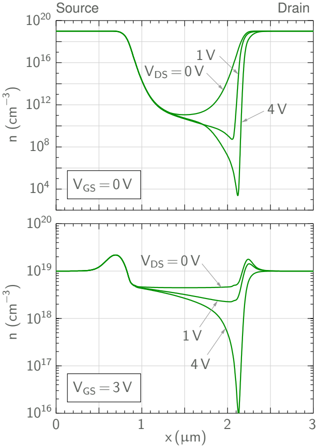
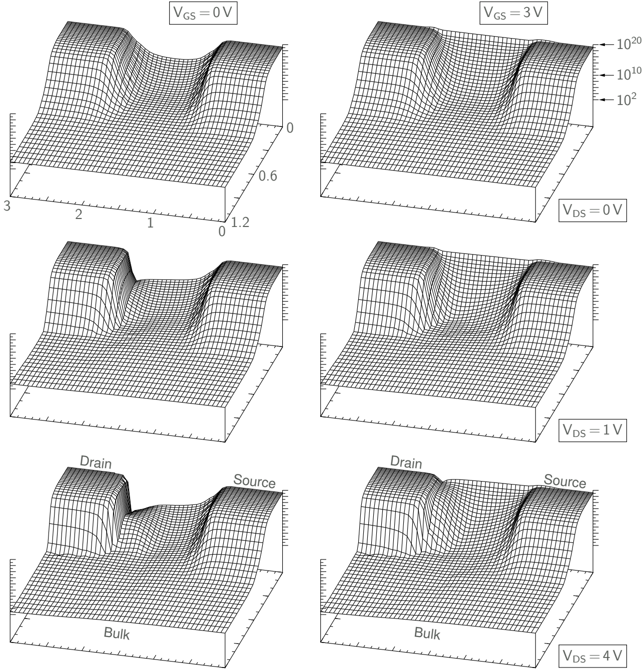
* The depletion region edge is roughly where the gradient of E_c becomes zero in the bulk. We can see that, as V_{DS} increases, the depletion region near the drain extends more into the bulk.

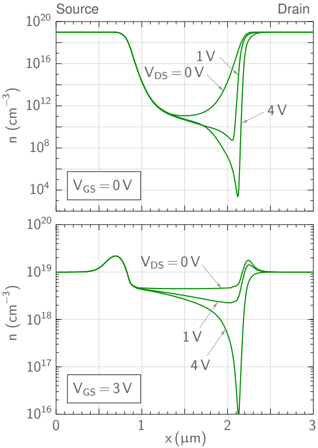


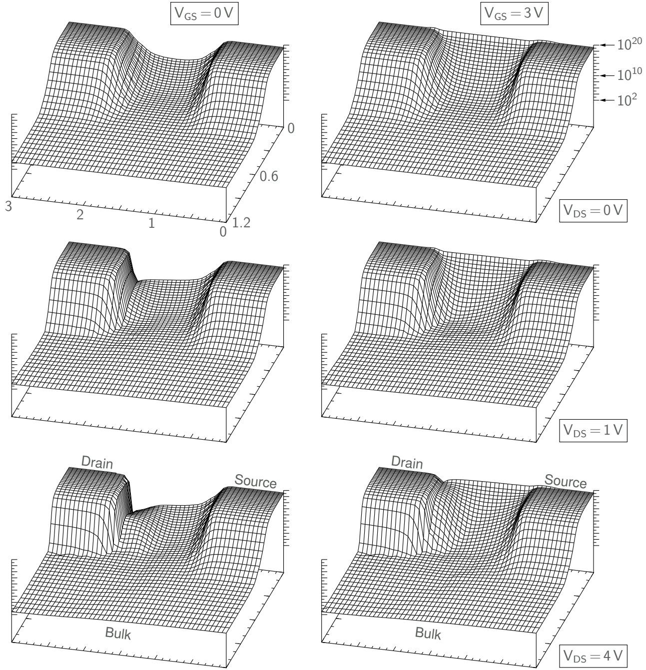


Source
Drain
10^{20}
10^{16}
10^{12}
10^{8}
10^{4}
n (cm^{-3})
1 V
$V_{DS} = 0$ V
4 V
$V_{GS} = 0$ V
10^{20}
10^{19}
10^{18}
10^{17}
10^{16}
$V_{DS} = 0$ V
1 V
4 V
$V_{GS} = 3$ V
0
1
2
3
x (μm)

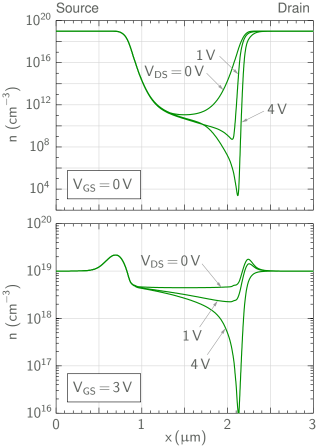


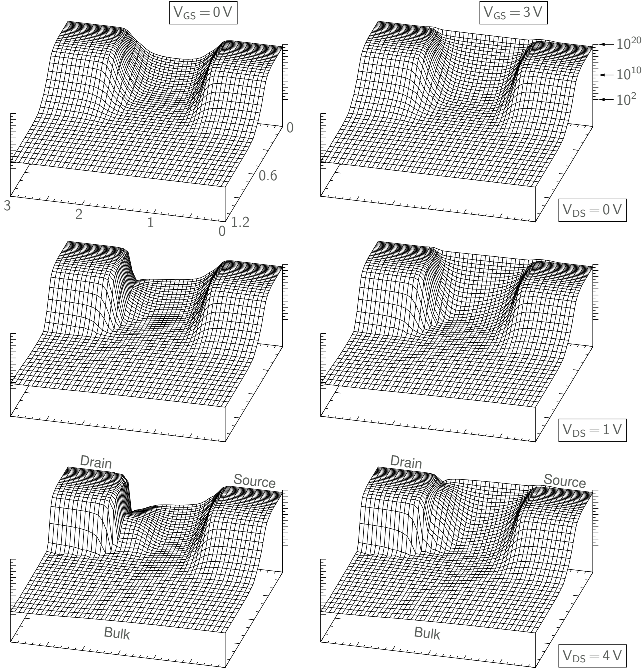
$V_{GS} = 0$ V
$V_{GS} = 3$ V
10^{20}
10^{10}
10^{2}
0
0.6
1.2
3
2
1
0
$V_{DS} = 0$ V
$V_{DS} = 1$ V
Drain
Source
Bulk
Drain
Source
Bulk
$V_{DS} = 4$ V





* $n(x, y)$ falls rapidly as we move from the Si-SiO_2 interface toward the bulk.





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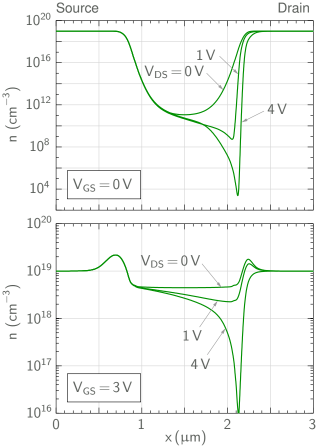
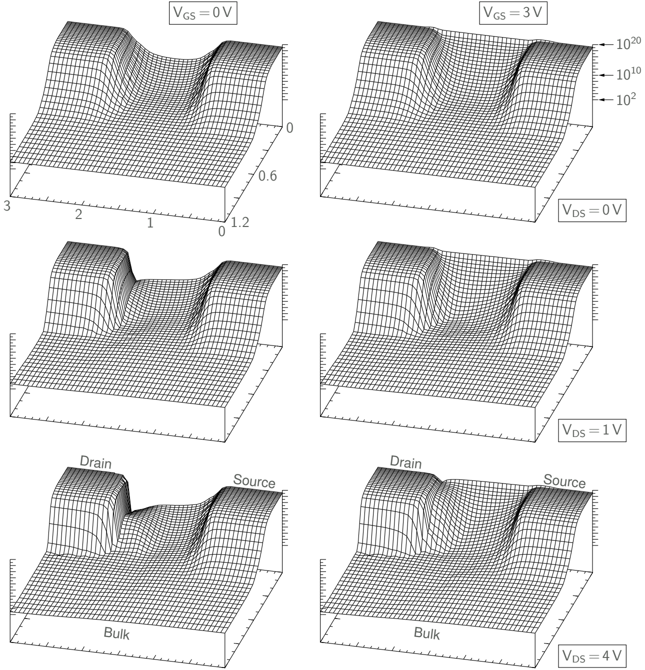
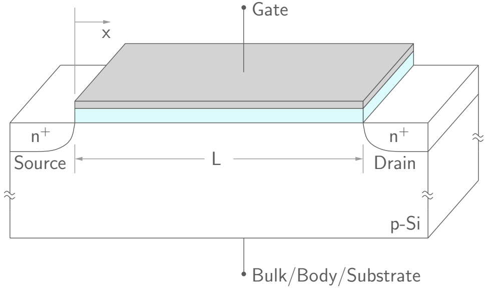
* The electron density in the channel (i.e., the inversion layer) is substantial only when $V_{GS} > V_{th}$.



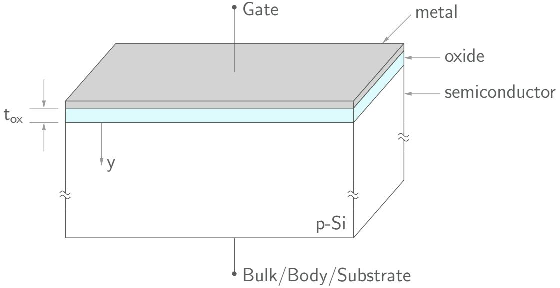


* $n(x, y)$ falls rapidly as we move from the Si-SiO_2 interface toward the bulk.
* The electron density in the channel (i.e., the inversion layer) is substantial only when $V_{GS} > V_{th}$.
* The electron density is larger near the source end of the channel than at the drain end.

MOS transistor and MOS capacitor



MOS transistor



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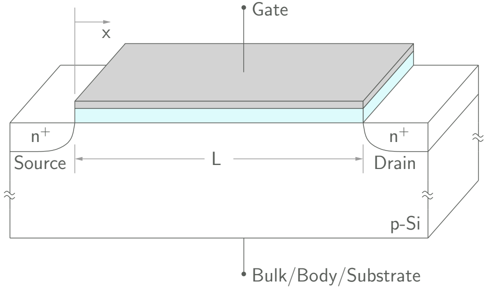

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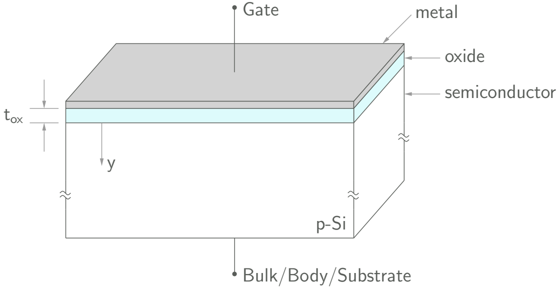

MOS capacitor

* In a MOS capacitor, DC current flow is blocked by the insulator, and therefore we could treat the Fermi level as constant.

  In a MOS transistor, a DC current can flow, which makes the situation very different.

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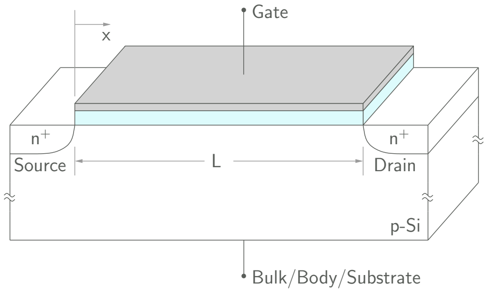

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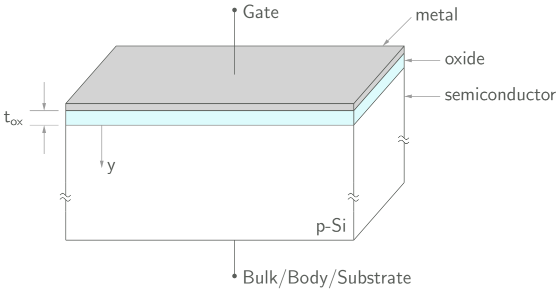

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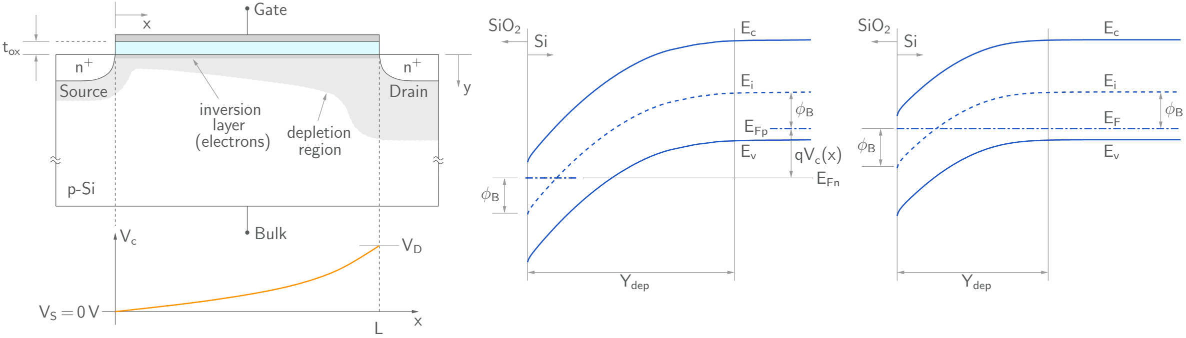
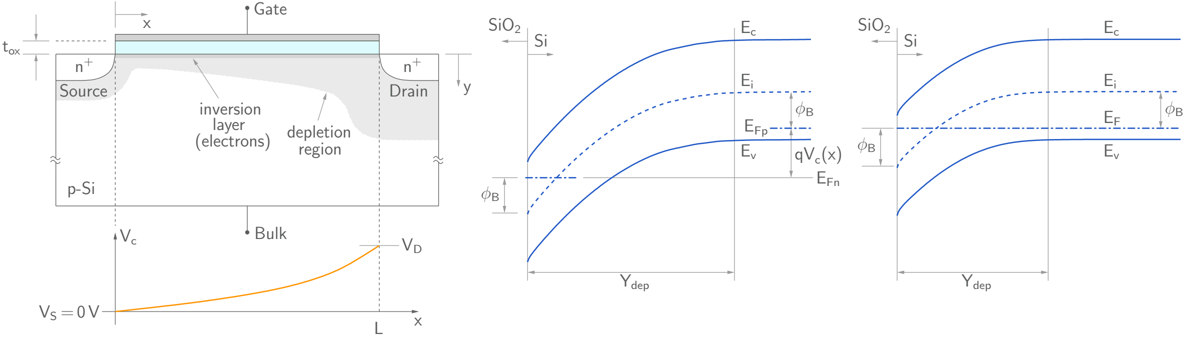
- In a MOS capacitor, the surface potential ψ_s depends only on V_G (with respect to the bulk contact).

  In a MOS transistor, ψ_s is affected by the the gate, source, and drain voltages.

MOS transistor and MOS capacitor

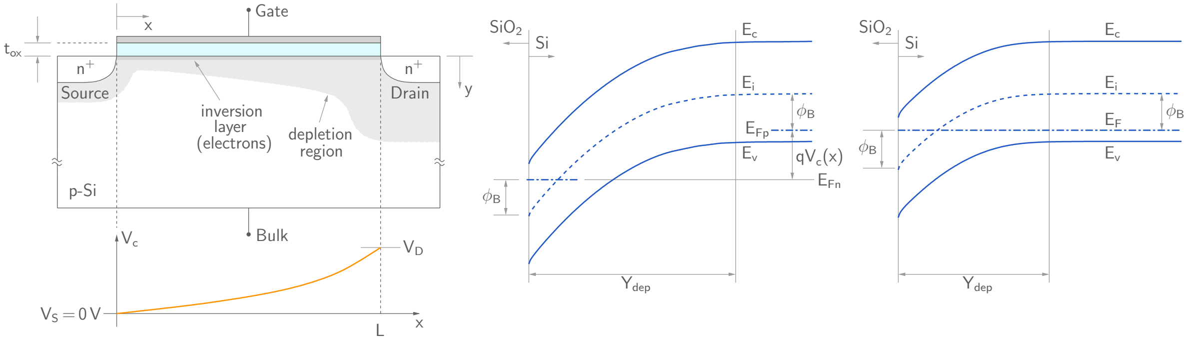


MOS transistor and MOS capacitor



* In a MOS transistor, the channel potential V_c (i.e., $\psi(y=0)$) varies from approximately V_s (0 V) at $x=0$ to V_D at $x=L$.

MOS transistor and MOS capacitor



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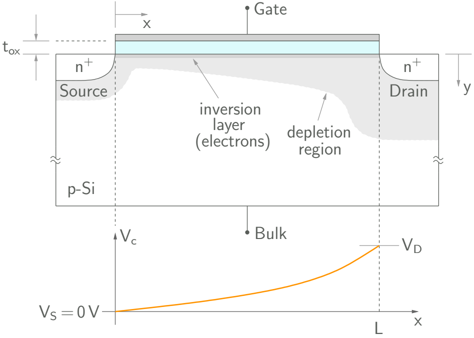

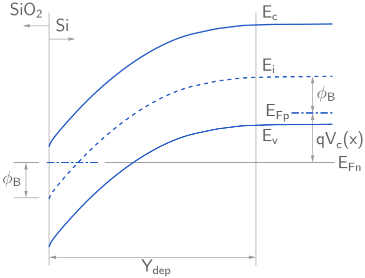

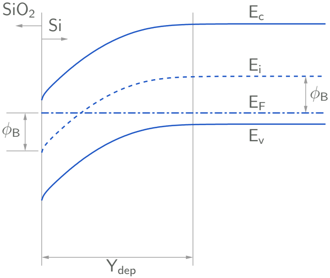

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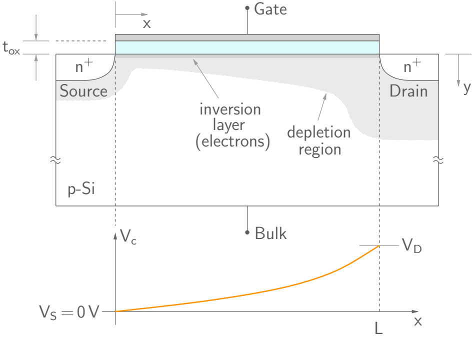
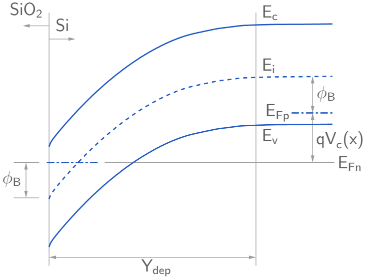
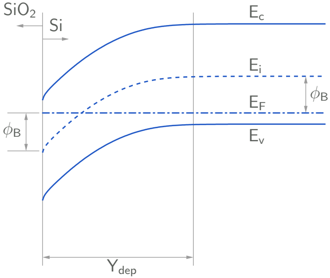
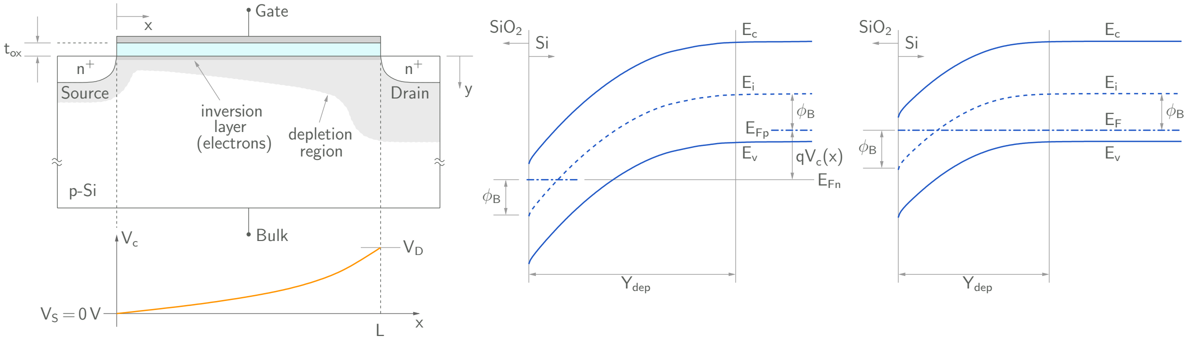
* At $y \to \infty$ (the bulk region), the quasi-Fermi level E_{Fp} is $q\phi_B$ below E_i, as in the MOS capacitor.
* At $y=0$ (the Si-SiO$_2$ interface), the the quasi-Fermi level E_{Fn} is about $q\phi_B$ above the intrinsic level E_i, as in the MOS capacitor.

MOS transistor and MOS capacitor









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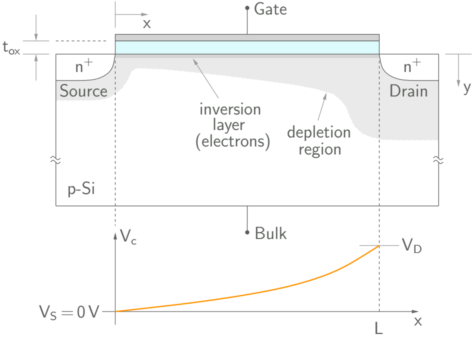
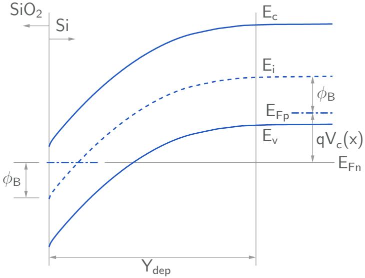
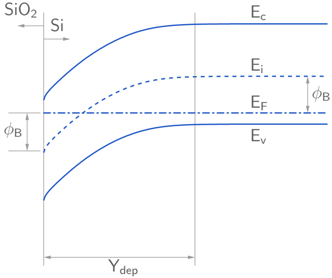
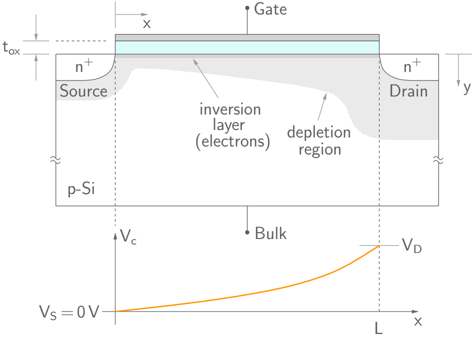


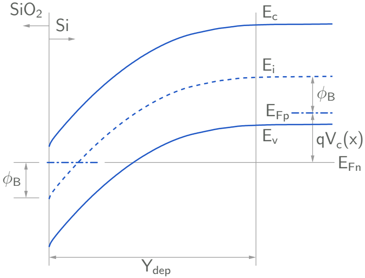


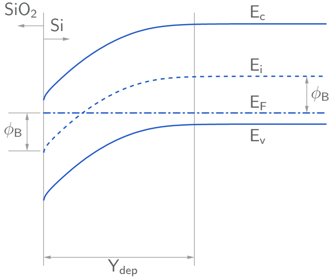


* In the capacitor, E_F is constant, so the total voltage drop in the semiconductor is simply $2\phi_B$.
* In the transistor, the two quasi-Fermi levels (i.e., $E_{Fn}(0)$ and $E_{Fp}(\infty)$) are separated by qV_c. The total voltage drop between the Si-SiO_2 interface ($y = 0$) and the bulk region ($y \rightarrow \infty$) is $V_c + 2\phi_B$.

MOS transistor and MOS capacitor







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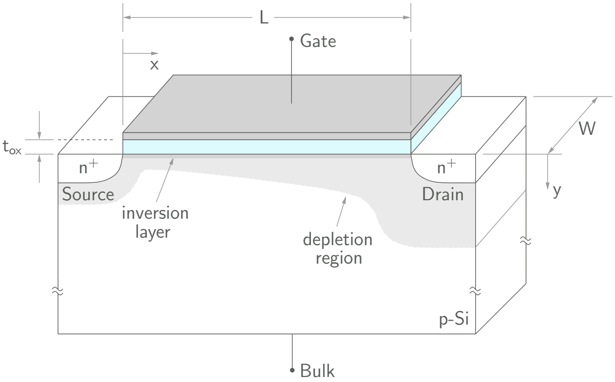
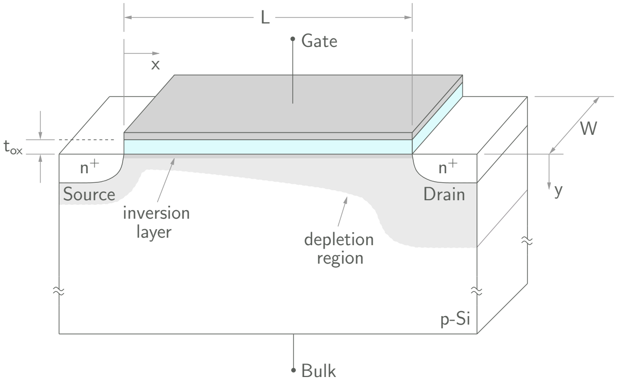
* The voltage drop ($V_c + 2\phi_B$) increases as we go from the source to the drain, and the depletion region becomes wider so as to accommodate the additional voltage difference.

MOS transistor: I-V relationship

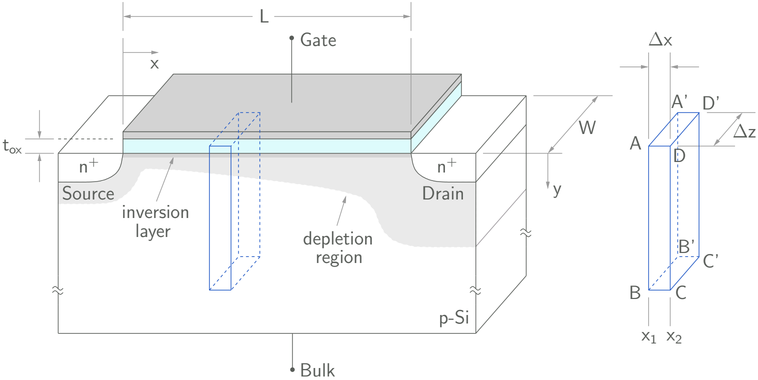


MOS transistor: I-V relationship

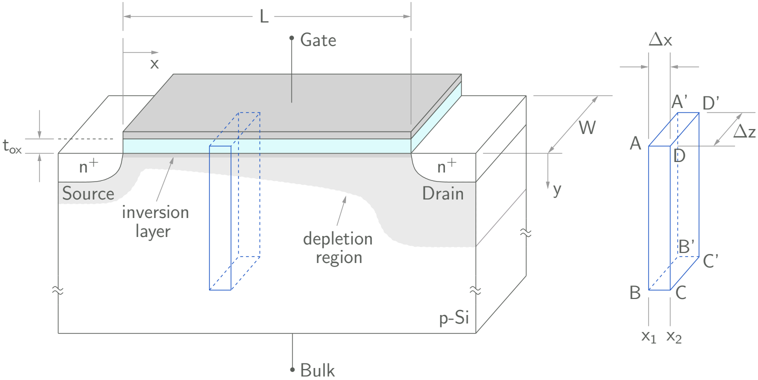


* Gradual channel approximation: We assume that the surface potential V_c in the x direction varies slowly from 0 V at the source end of the channel to V_D at the drain end.

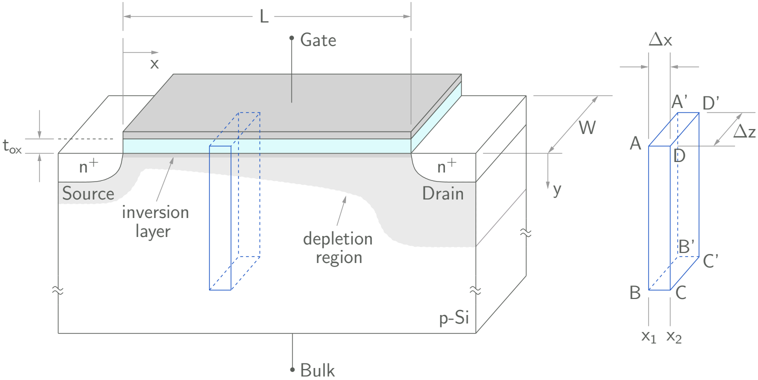
  In other words, the electric field in the x direction ($\mathcal{E}_x$) varies slowly with x.


L
Gate
x
t_{ox}
n^+
Source
inversion
layer
depletion
region
n^+
Drain
W
y
p-Si
Bulk
Δx
A'
D'
Δz
A
D
B'
C'
B
C
x_1
x_2

MOS transistor: I-V relationship



Gauss's law: $\displaystyle\int_V \rho\, dV = \oint_{ABCD} \mathbf{D}\cdot d\mathbf{A} + \oint_{A'B'C'D'} \mathbf{D}\cdot d\mathbf{A} + \oint_{AA'B'B} \mathbf{D}\cdot d\mathbf{A} + \oint_{DD'C'C} \mathbf{D}\cdot d\mathbf{A} + \oint_{AA'D'D} \mathbf{D}\cdot d\mathbf{A} + \oint_{BB'C'C} \mathbf{D}\cdot d\mathbf{A}.$



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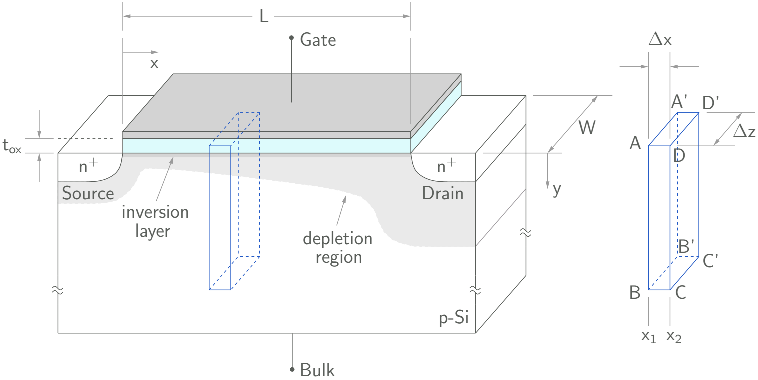
* The integrals over the rectangles $ABCD$ and $A'B'C'D'$ are both zero because we assume that the potential does not vary in the z direction.



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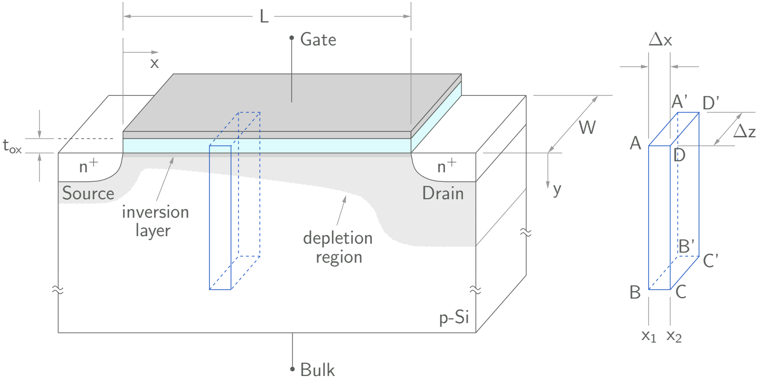
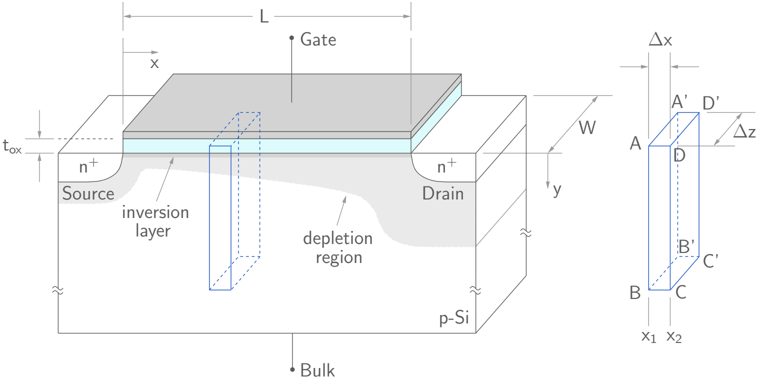
* The integrals over the rectangles $ABCD$ and $A'B'C'D'$ are both zero because we assume that the potential does not vary in the z direction.
* The integral over $BB'C'C$ is zero because the bands are flat in the bulk region.

MOS transistor: I-V relationship

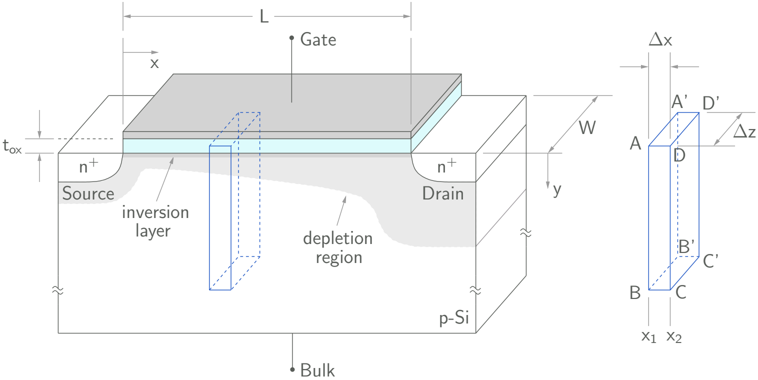


MOS transistor: I-V relationship



Gauss's law: $\displaystyle\int_V \rho\, dV = \oint_{AA'B'B} \mathbf{D} \cdot d\mathbf{A} + \oint_{DD'C'C} \mathbf{D} \cdot d\mathbf{A} + \oint_{AA'D'D} \mathbf{D} \cdot d\mathbf{A}.$

MOS transistor: I-V relationship



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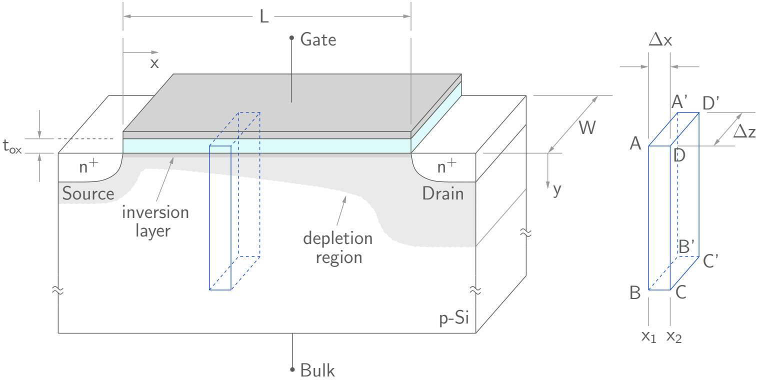
$$\oint_{AA'B'B} \mathbf{D} \cdot d\mathbf{A} = -\oint_{AA'B'B} \epsilon\, \mathcal{E}_x(x,y)\, dA,$$

MOS transistor: I-V relationship



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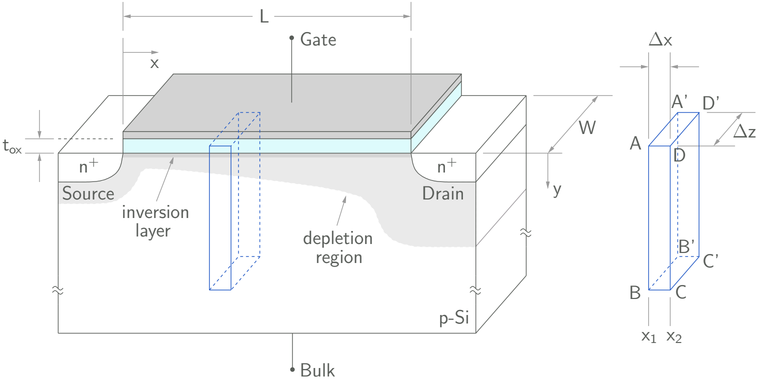

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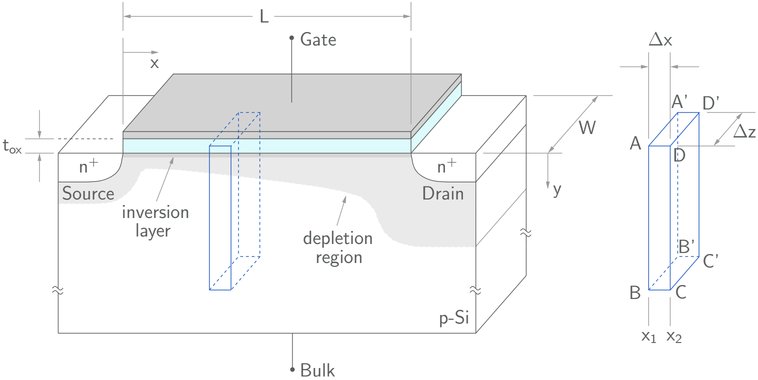
Gradual channel approximation $\rightarrow$ $\mathcal{E}_x$ varies slowly with x. $\rightarrow$ The two integrals add to zero.



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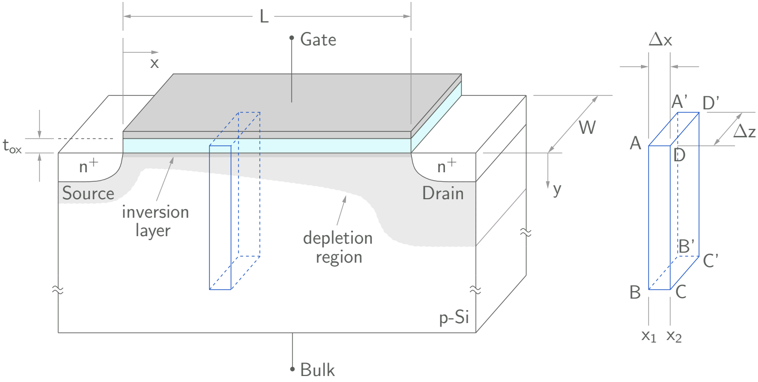
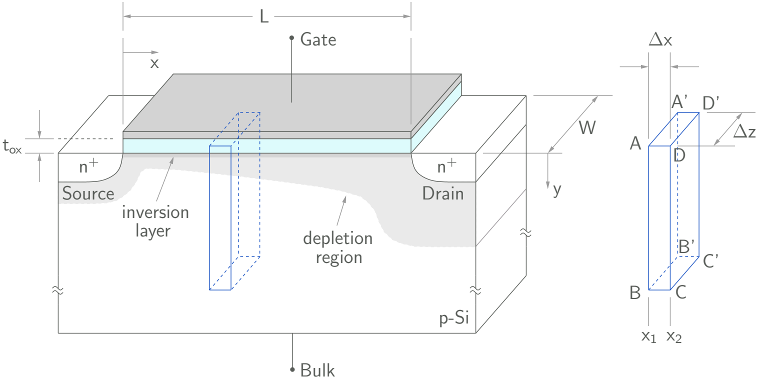
Gradual channel approximation $\rightarrow$ $\mathcal{E}_x$ varies slowly with x. $\rightarrow$ The two integrals add to zero.

$$\rightarrow \int_V \rho\, dV = \oint_{AA'D'D} \mathbf{D}\cdot \mathbf{dA}.$$

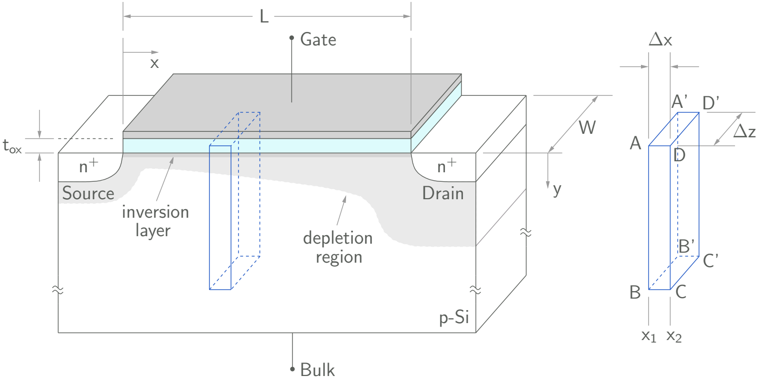
MOS transistor: I-V relationship





$$\int_V \rho\, dV = \oint_{AA'D'D} \mathbf{D}\cdot d\mathbf{A} = \Delta x \Delta z \int_0^{\infty} q\,(p - n - N_a^-)\, dy = -\,\Delta x \Delta z\, \epsilon_{\rm Si} \mathcal{E}^y_{\rm Si}(x) = -\,\Delta x \Delta z\, \epsilon_{\rm ox} \mathcal{E}^y_{\rm ox}(x).$$

MOS transistor: I-V relationship



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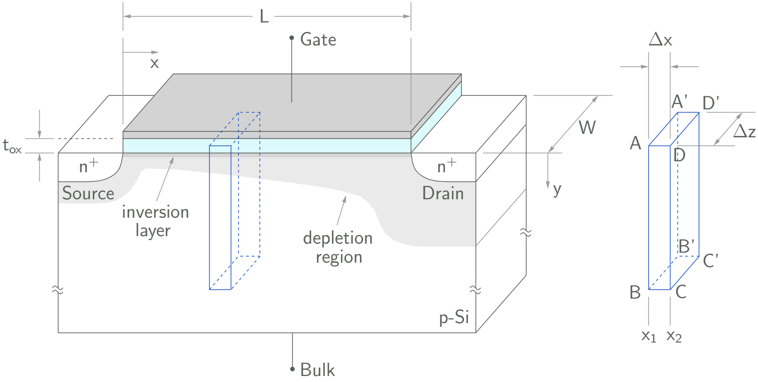
$$\rightarrow \quad -\, \epsilon_{\text{ox}} \mathcal{E}_{\text{ox}}^y(x) = -q \int_0^{\infty} \left[n(x,y) + (N_a^- - p) \right] dy \equiv Q_I(x) + Q_D(x).$$



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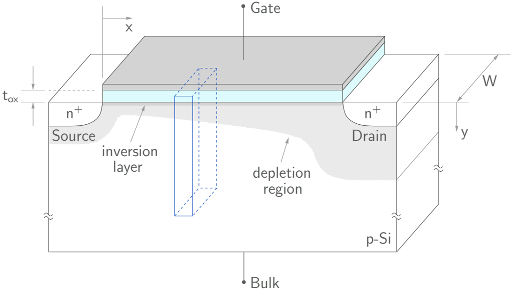
Note that the depletion charge Q_D varies with x since the depletion width varies with x.

M. B. Patil, IIT Bombay



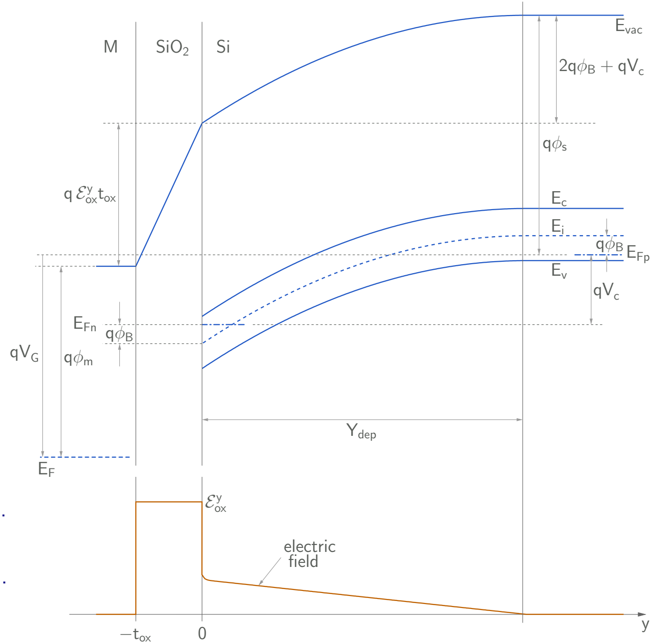
$$-\epsilon_{ox}\mathcal{E}^y_{ox}(x) = -q\int_0^\infty \left[n(x,y)+(N_a^- - p)\right] dy$$

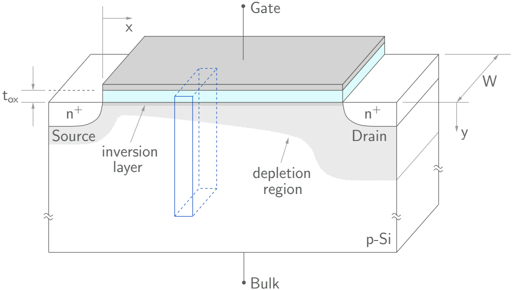
$$\rightarrow \quad \mathcal{E}^y_{ox}(x) = -\frac{Q_I(x)+Q_D(x)}{\epsilon_{ox}}.$$

$$q\phi_s = 2q\phi_B + qV_c + q\mathcal{E}_{ox}t_{ox} + q\phi_m - qV_G.$$

$$\rightarrow V_G - \phi_{ms} - 2\phi_B - V_c = \mathcal{E}^y_{ox}t_{ox} = -\frac{Q_I(x)+Q_D(x)}{C_{ox}}.$$

$$\rightarrow Q_I(x) = -C_{ox}\left[V_G - \phi_{ms} - 2\phi_B + \frac{Q_D(x)}{C_{ox}} - V_c(x)\right].$$





$$Q_I(x) = -C_{ox}\left[V_G - \phi_{ms} - 2\phi_B + \frac{Q_D(x)}{C_{ox}} - V_c(x)\right].$$

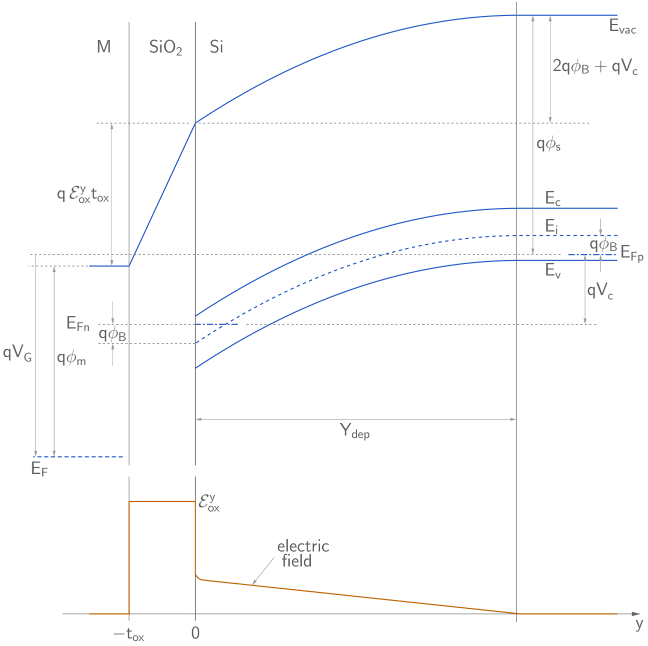
At $x = 0$, we have $V_c = 0\,\text{V}$, and

$Q_I(x=0) = -C_{ox}\,[V_G - V_{th}]$, where V_{th} is the same as the threshold voltage of the corresponding MOS capacitor.

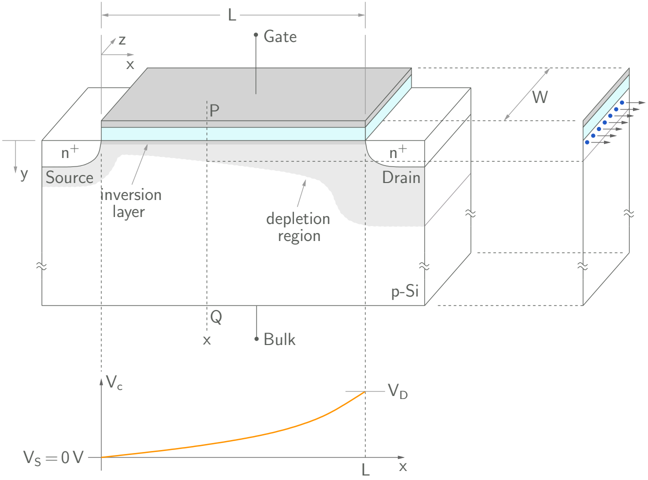
In general, we have

$Q_I(x) = -C_{ox}\,[V_G - V_{th}(x) - V_c(x)]$, with

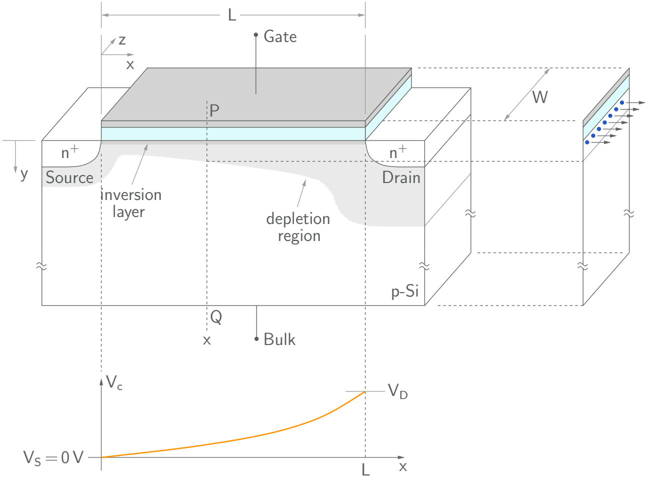
$$V_{th}(x) = \phi_{ms} + 2\phi_B - \frac{Q_D(x)}{C_{ox}}.$$



MOS transistor: I-V relationship



$$I_D = \iint q\, n(x,y,z)\, \mu_n \frac{dV_c}{dx}\, dydz$$



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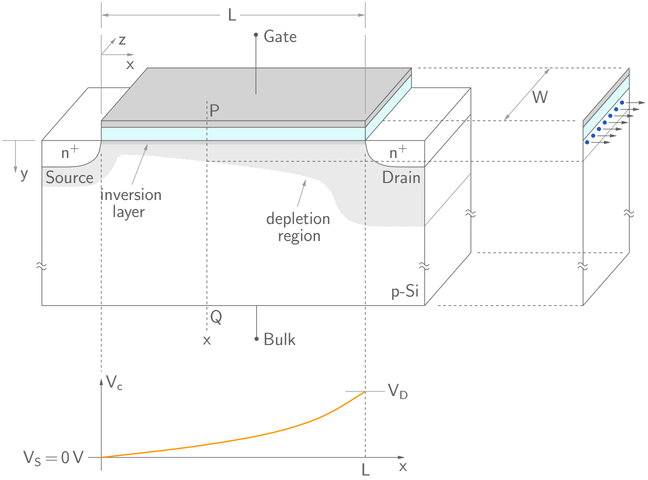
$$= \mu_n W \frac{dV_c}{dx} \int q\, n(x,y)\, dy = -\mu_n W \frac{dV_c}{dx}\, Q_I(x)$$



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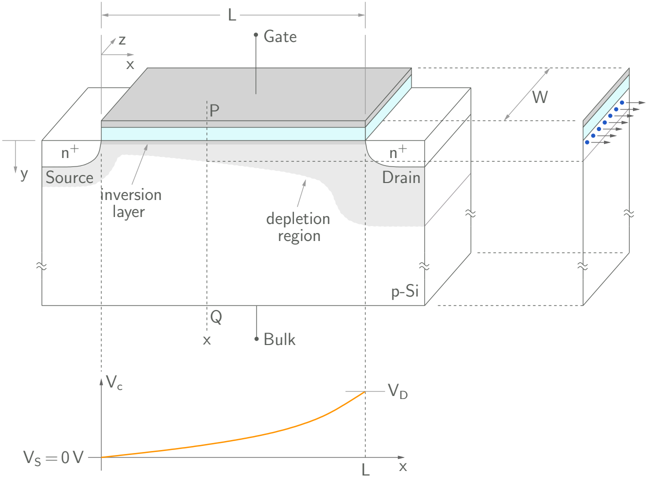
$$= -\mu_n W \frac{dV_c}{dx} \left[-C_{ox}(V_G - V_{th}(x) - V_c)\right]$$



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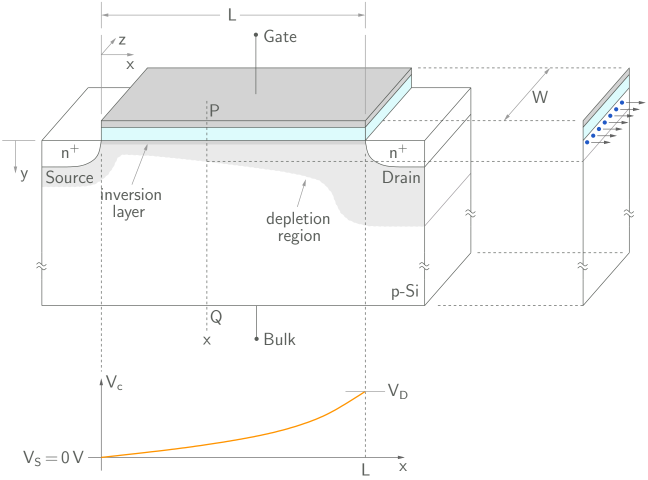

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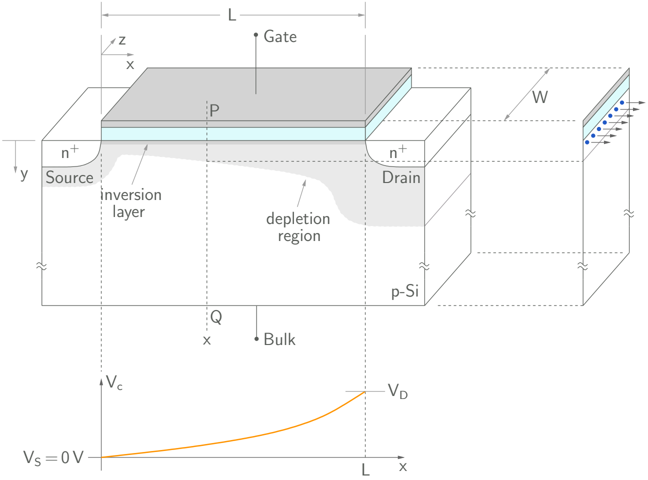
Remark: The mobility here is smaller than in bulk (typically by a factor of 2) because of additional scattering at the Si-SiO_2 interface.



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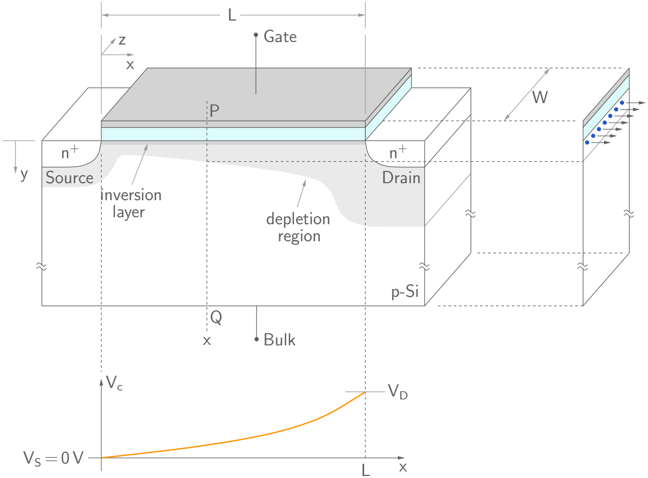
We now make a simplifying assumption, viz., $V_{th}(x) \approx V_{th}(x=0)$, which amounts to ingoring the x-dependence of Q_D.



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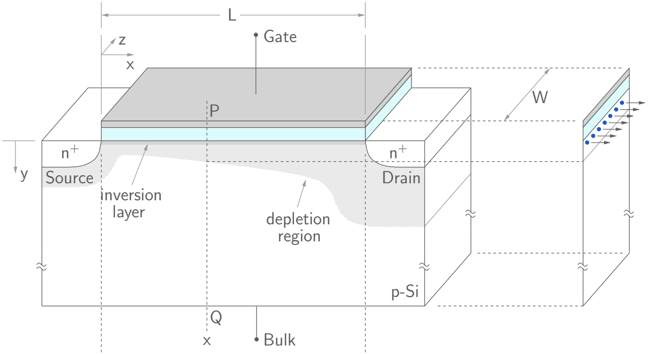
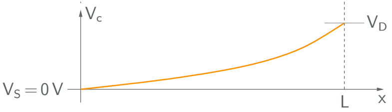
$$\int_0^L I_D dx = I_D L = \mu_n W C_{ox} \int_0^{V_D} (V_G - V_{th} - V_c)\, dV_c.$$





$$I_D = \iint q\, n(x,y,z)\, \mu_n \frac{dV_c}{dx}\, dydz$$
$$= \mu_n W \frac{dV_c}{dx} \int q\, n(x,y)\, dy = -\mu_n W \frac{dV_c}{dx}\, Q_I(x)$$
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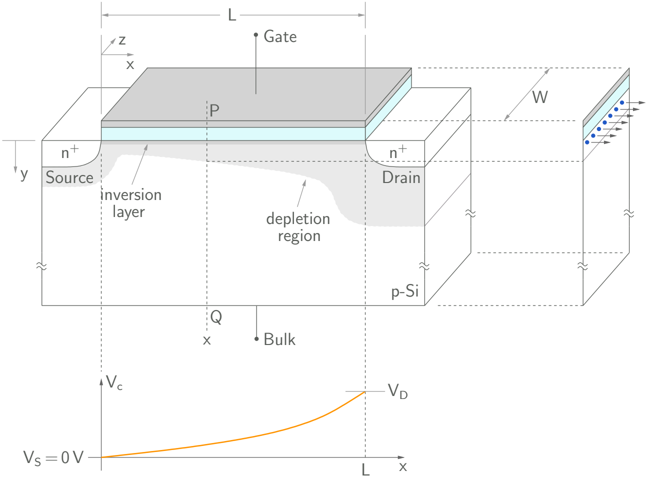
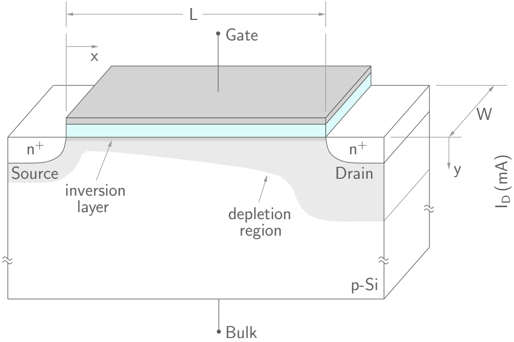
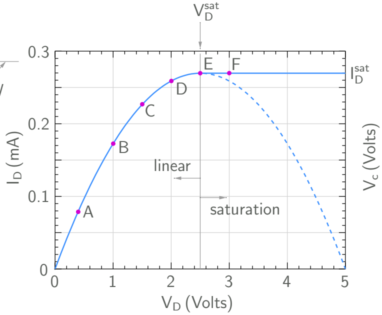
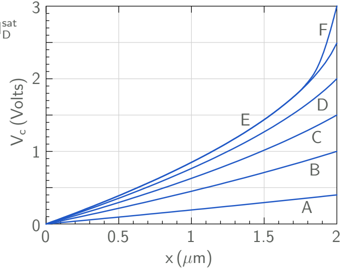
$$\int_0^L I_D\, dx = I_D\, L = \mu_n W C_{ox} \int_0^{V_D} (V_G - V_{th} - V_c)\, dV_c .$$

$$\rightarrow I_D = \mu_n \frac{W}{L} C_{ox} \left[(V_G - V_{th})V_D - \frac{1}{2} V_D^2\right].$$



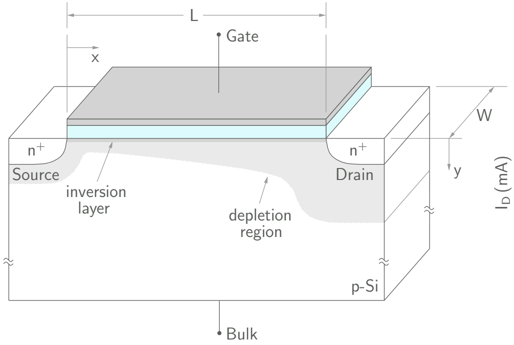


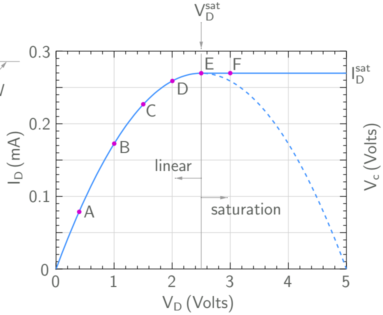


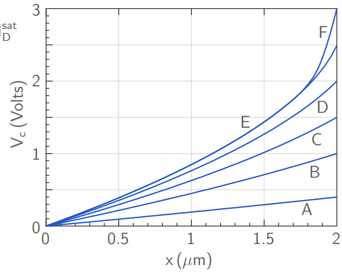


$$I_D = \mu_n \frac{W}{L} C_{ox} \left[(V_G - V_{th}) V_D - \frac{1}{2} V_D^2 \right].$$

$V_{th} = 0.5\,V$
$V_G = 3\,V$
$t_{ox} = 50\,nm$
$\mu_n = 500\,cm^2/V\text{-}s$
$L = 2\,\mu m$
$W = 5\,\mu m$







$$I_D = \mu_n \frac{W}{L} C_{ox} \left[(V_G - V_{th}) V_D - \frac{1}{2} V_D^2 \right].$$

* Consider a constant V_G ($> V_{th}$). The above equation predicts that, as V_D is increased, I_D will reach a maximum value and then decrease.

$V_{th} = 0.5\,\text{V}$
$V_G = 3\,\text{V}$
$t_{ox} = 50\,\text{nm}$
$\mu_n = 500\,\text{cm}^2/\text{V-s}$
$L = 2\,\mu\text{m}$
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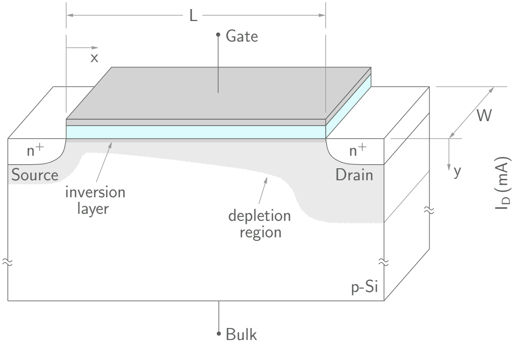

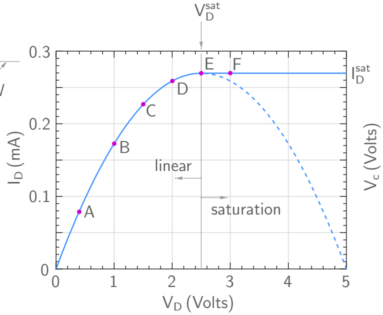

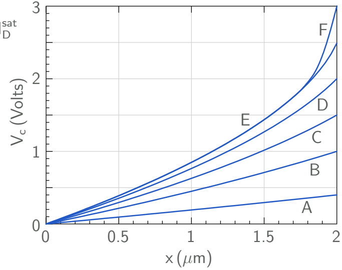

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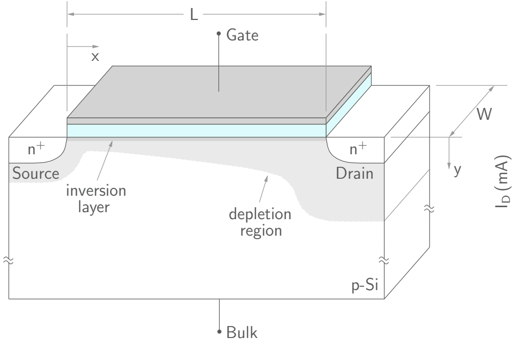
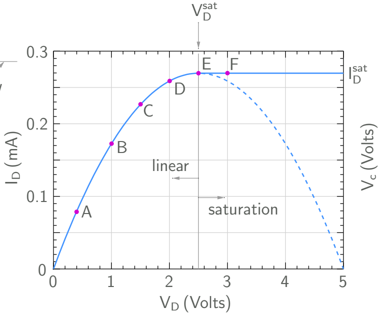
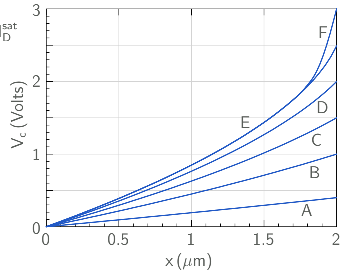
$V_G = 3\,V$
$t_{ox} = 50\,nm$
$\mu_n = 500\,cm^2/V\text{-}s$
$L = 2\,\mu m$
$W = 5\,\mu m$

* Consider a constant V_G ($> V_{th}$). The above equation predicts that, as V_D is increased, I_D will reach a maximum value and then decrease.
* In a real device, I_D saturates after reaching the maximum value.







Saturation:

$V_{th} = 0.5\,V$
$V_G = 3\,V$
$t_{ox} = 50\,nm$
$\mu_n = 500\,cm^2/V\text{-}s$
$L = 2\,\mu m$
$W = 5\,\mu m$

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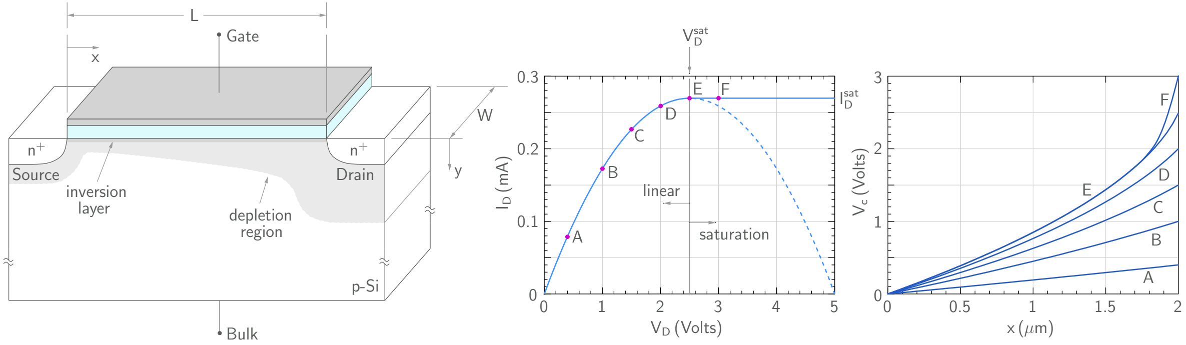
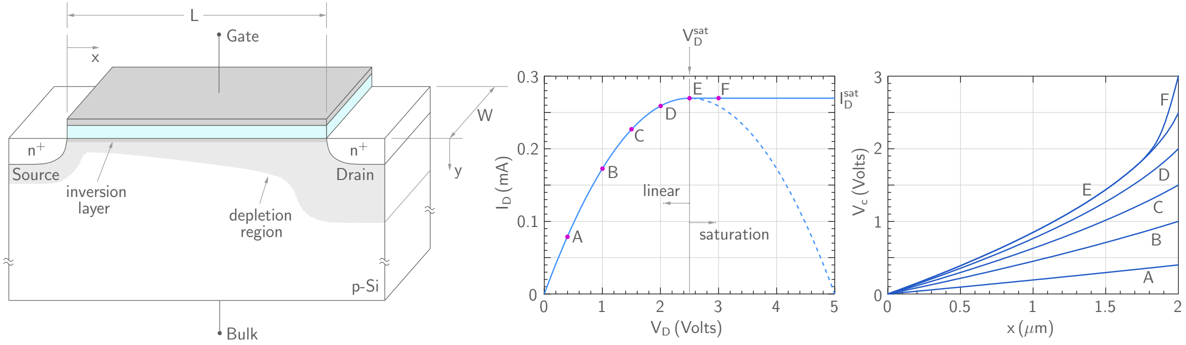


Saturation:

* The inversion charge, which is responsible for current conduction, decreases from S to D due to an increase in the channel potential: $Q_I(x) = -C_{ox}\,[V_G - V_{th}(x) - V_c(x)]$.

$V_{th} = 0.5\,\text{V}$
$V_G = 3\,\text{V}$
$t_{ox} = 50\,\text{nm}$
$\mu_n = 500\,\text{cm}^2/\text{V-s}$
$L = 2\,\mu\text{m}$
$W = 5\,\mu\text{m}$



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* The inversion charge, which is responsible for current conduction, decreases from S to D due to an increase in the channel potential: $Q_I(x) = -C_{ox}\,[V_G - V_{th}(x) - V_c(x)]$.
* When $V_c = V_G - V_{th}$, the inversion charge becomes nearly zero $\rightarrow$ The channel gets "pinched-off."

$V_{th} = 0.5\,V$
$V_G = 3\,V$
$t_{ox} = 50\,nm$
$\mu_n = 500\,cm^2/V\text{-}s$
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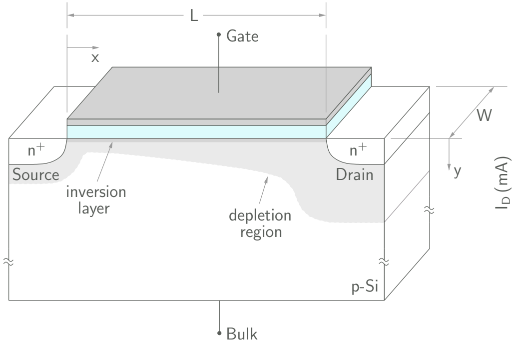

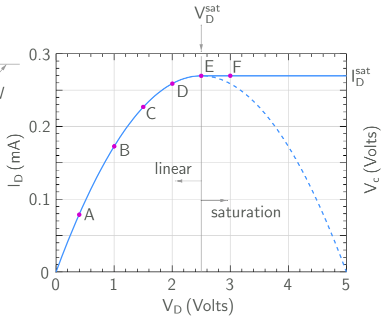

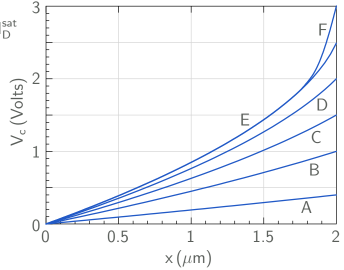

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* The inversion charge, which is responsible for current conduction, decreases from S to D due to an increase in the channel potential: $Q_I(x) = -C_{ox}\,[V_G - V_{th}(x) - V_c(x)]$.
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* Since V_c increases from S to D, pinch-off occurs at the drain end.

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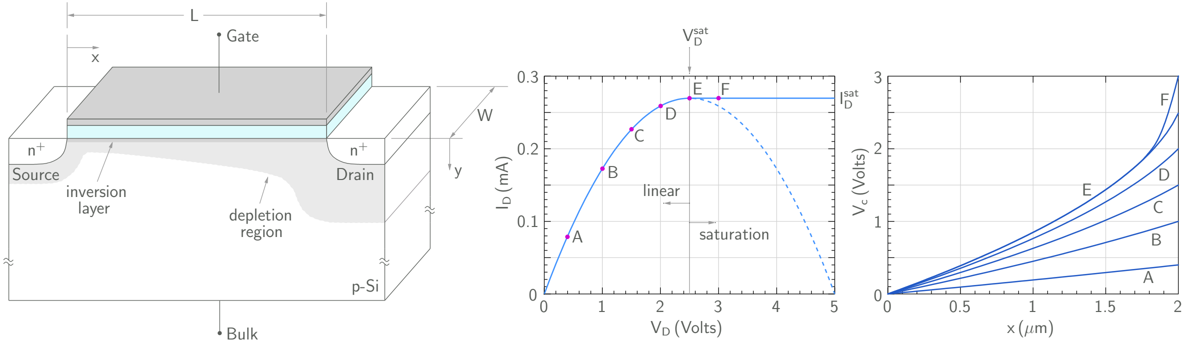

Saturation:

* The inversion charge, which is responsible for current conduction, decreases from S to D due to an increase in the channel potential: $Q_I(x) = -C_{ox}\,[V_G - V_{th}(x) - V_c(x)]$.
* When $V_c = V_G - V_{th}$, the inversion charge becomes nearly zero $\rightarrow$ The channel gets "pinched-off."
* Since V_c increases from S to D, pinch-off occurs at the drain end.
* Beyond pinch-off, the "excess" drain voltage $V_D - V_D^{sat}$ drops across a narrow high-field region, leaving the conditions in most of the device unchanged. $\rightarrow$ I_D remains equal to I_D^{sat}.

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$V_G = 3\,V$
$t_{ox} = 50\,nm$
$\mu_n = 500\,cm^2/V\text{-}s$
$L = 2\,\mu m$
$W = 5\,\mu m$

Example: For an NMOS transistor with $L = 2\,\mu\text{m}$, $W = 5\,\mu\text{m}$, $\mu_n = 500\,\text{cm}^2/\text{V-s}$, $t_{\text{ox}} = 500\,\text{Å}$, $V_{\text{th}} = 0.4\,\text{V}$,

Example: For an NMOS transistor with $L = 2\,\mu\text{m}$, $W = 5\,\mu\text{m}$, $\mu_n = 500\,\text{cm}^2/\text{V-s}$, $t_{\text{ox}} = 500\,\text{Å}$, $V_{\text{th}} = 0.4\,\text{V}$,

(a) Plot I_D versus V_{DS} for $V_{GS} = 1.5,\ 2,\ 2.5,\ 3,\ 3.5,\ 4\,\text{V}$.

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(b) Show the locus of V_{DS}^{sat} in the I_D-V_{DS} plane.

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(c) Plot I_D versus V_{GS} for $V_{DS} = 0.2\,\text{V}$ and $V_{DS} = 3\,\text{V}$.

$(V_{BS} = 0\,\text{V},\ T = 300\,\text{K})$.

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($V_{BS} = 0\,\text{V}$, $T = 300\,\text{K}$).

Solution:

(a) $I_D = \dfrac{W}{L}\,\mu_n C_{\text{ox}} \left[(V_{GS} - V_{\text{th}})V_{DS} - \dfrac{1}{2}\,V_{DS}^2 \right].$

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Solution:

(a) $$I_D = \frac{W}{L}\,\mu_n C_{\text{ox}}\left[(V_{GS} - V_{\text{th}})V_{DS} - \frac{1}{2}\,V_{DS}^2\right].$$

Saturation occurs when $V_{DS} = V_{GS} - V_{\text{th}}$.

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For each given value of V_{GS}, we first compute V_{DS}^{sat}.

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Saturation occurs when $V_{DS} = V_{GS} - V_{\text{th}}$.

For each given value of V_{GS}, we first compute V_{DS}^{sat}.

For $V_{DS} < V_{DS}^{\text{sat}}$, we use the expression for I_D above.

For $V_{DS} > V_{DS}^{\text{sat}}$, $I_D = I_D^{\text{sat}} = \dfrac{1}{2}\,\dfrac{W}{L}\,\mu_n C_{\text{ox}}\,(V_{GS} - V_{\text{th}})^2$.

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(c) Plot I_D versus V_{GS} for $V_{DS} = 0.2\,\text{V}$ and $V_{DS} = 3\,\text{V}$.

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(b) $I_D^{\text{sat}} = \dfrac{1}{2}\,\dfrac{W}{L}\,\mu_n C_{\text{ox}}\,(V_{GS} - V_{\text{th}})^2 = \dfrac{1}{2}\,\dfrac{W}{L}\,\mu_n C_{\text{ox}}\,(V_{DS}^{\text{sat}})^2$,

a parabola in the I_D–V_{DS} plane.

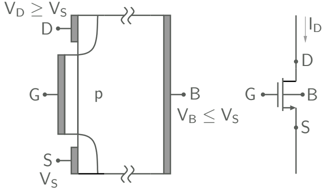
Example: For an NMOS transistor with $L = 2\,\mu$m, $W = 5\,\mu$m, $\mu_n = 500\,\text{cm}^2/\text{V-s}$, $t_{ox} = 500\,\text{Å}$, $V_{th} = 0.4\,$V,

(a) Plot I_D versus V_{DS} for $V_{GS} = 1.5, 2, 2.5, 3, 3.5, 4\,$V.

(b) Show the locus of V_{DS}^{sat} in the I_D-V_{DS} plane.

(c) Plot I_D versus V_{GS} for $V_{DS} = 0.2\,$V and $V_{DS} = 3\,$V.

($V_{BS} = 0\,$V, $T = 300\,$K).



Solution:

(a) $I_D = \dfrac{W}{L}\,\mu_n C_{ox}\left[(V_{GS} - V_{th})V_{DS} - \dfrac{1}{2}\,V_{DS}^2\right]$.

Saturation occurs when $V_{DS} = V_{GS} - V_{th}$.

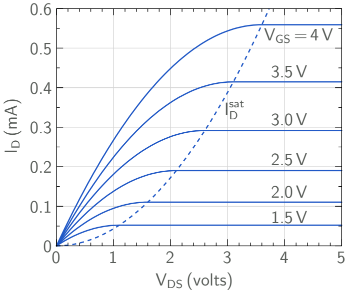
For each given value of V_{GS}, we first compute V_{DS}^{sat}.

For $V_{DS} < V_{DS}^{sat}$, we use the expression for I_D above.

For $V_{DS} > V_{DS}^{sat}$, $I_D = I_D^{sat} = \dfrac{1}{2}\,\dfrac{W}{L}\,\mu_n C_{ox}\,(V_{GS} - V_{th})^2$.

(b) $I_D^{sat} = \dfrac{1}{2}\,\dfrac{W}{L}\,\mu_n C_{ox}\,(V_{GS} - V_{th})^2 = \dfrac{1}{2}\,\dfrac{W}{L}\,\mu_n C_{ox}\,(V_{DS}^{sat})^2$,

a parabola in the I_D–V_{DS} plane.



Solution:

(c) $I_D = \dfrac{W}{L}\,\mu_n C_{\mathrm{ox}}\left[(V_{GS} - V_{\mathrm{th}})V_{DS} - \dfrac{1}{2}\,V_{DS}^2\right],\;\; V_{DS}^{\mathrm{sat}} = V_{GS} - V_{\mathrm{th}}\,.$

Solution:

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The condition required for saturation, viz., $V_{DS} > (V_{GS} - V_{\text{th}})$, can be re-written as $V_{GS} < (V_{DS} + V_{\text{th}})$.

Solution:

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The condition required for saturation, viz., $V_{DS} > (V_{GS}-V_{\mathrm{th}})$, can be re-written as $V_{GS} < (V_{DS}+V_{\mathrm{th}})$.

For a given V_{DS}, the boundary between the linear and saturation regions is given by

$V_{GS}^{\mathrm{sat}} = (V_{DS}+V_{\mathrm{th}})$.

Solution:

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$V_{GS}^{\text{sat}} = (V_{DS}+V_{\text{th}})$.

(i) $V_{DS} = 0.2\,\text{V}$: $V_{GS}^{\text{sat}} = 0.2+0.4 = 0.6\,\text{V}$.

Solution:

(c) $I_D = \frac{W}{L}\,\mu_n C_{\text{ox}}\left[(V_{GS}-V_{\text{th}})V_{DS} - \frac{1}{2}\,V_{DS}^2\right]$, $V_{DS}^{\text{sat}} = V_{GS} - V_{\text{th}}$.

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$V_{GS} < 0.6\,\text{V}$: saturation, $V_{GS} > 0.6\,\text{V}$: linear region.

Solution:

(c) $I_D = \dfrac{W}{L}\,\mu_n C_{\text{ox}}\left[(V_{GS}-V_{\text{th}})V_{DS}-\dfrac{1}{2}\,V_{DS}^2\right],\;\; V_{DS}^{\text{sat}} = V_{GS}-V_{\text{th}}.$

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$V_{GS}^{\text{sat}} = (V_{DS}+V_{\text{th}})$.

(i) $V_{DS} = 0.2\,\text{V}$: $V_{GS}^{\text{sat}} = 0.2+0.4 = 0.6\,\text{V}$.

$V_{GS} < 0.6\,\text{V}$: saturation, $\;V_{GS} > 0.6\,\text{V}$: linear region.

(ii) $V_{DS} = 3.0\,\text{V}$: $V_{GS}^{\text{sat}} = 3.0+0.4 = 3.4\,\text{V}$.

Solution:

(c) $I_D = \dfrac{W}{L}\,\mu_n C_{\mathrm{ox}}\left[(V_{GS}-V_{\mathrm{th}})V_{DS}-\dfrac{1}{2}\,V_{DS}^2\right],\ \ V_{DS}^{\mathrm{sat}} = V_{GS}-V_{\mathrm{th}}.$

The condition required for saturation, viz., $V_{DS} > (V_{GS}-V_{\mathrm{th}})$, can be re-written as $V_{GS} < (V_{DS}+V_{\mathrm{th}})$.

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$V_{GS} < 3.4\,\mathrm{V}$: saturation, $V_{GS} > 3.4\,\mathrm{V}$: linear region.

Solution:

(c) $I_D = \dfrac{W}{L}\,\mu_n C_{\text{ox}}\left[(V_{GS}-V_{\text{th}})V_{DS} - \dfrac{1}{2}\,V_{DS}^2\right]$, $V_{DS}^{\text{sat}} = V_{GS} - V_{\text{th}}$.

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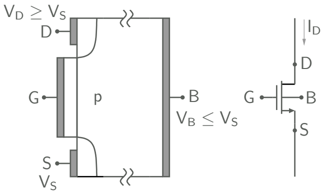
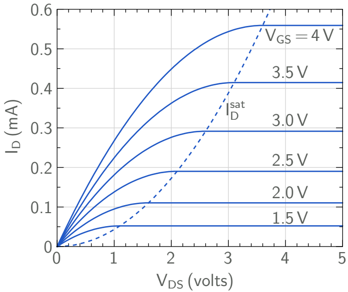
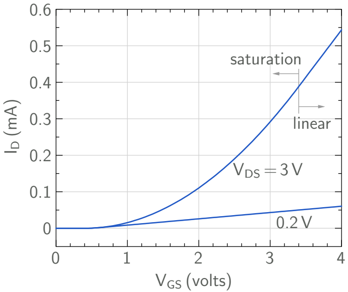
$V_{GS} < 0.6\,\text{V}$: saturation, $V_{GS} > 0.6\,\text{V}$: linear region.

(ii) $V_{DS} = 3.0\,\text{V}$: $V_{GS}^{\text{sat}} = 3.0 + 0.4 = 3.4\,\text{V}$.

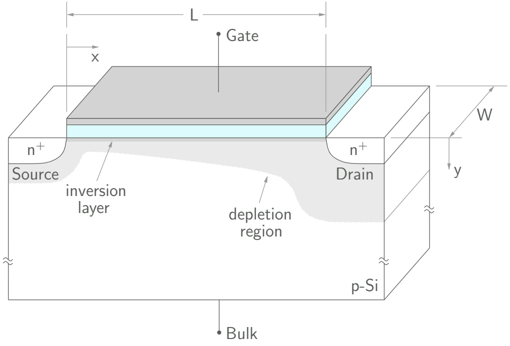
$V_{GS} < 3.4\,\text{V}$: saturation, $V_{GS} > 3.4\,\text{V}$: linear region.

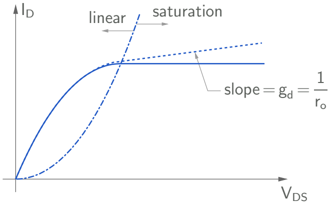






Channel length modulation





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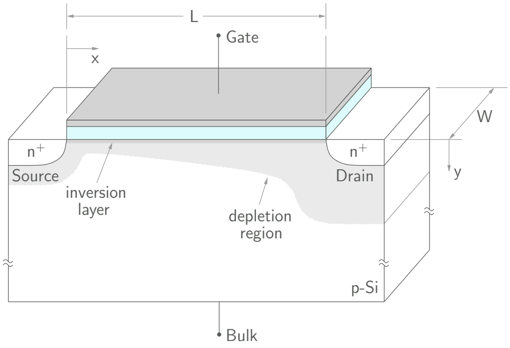
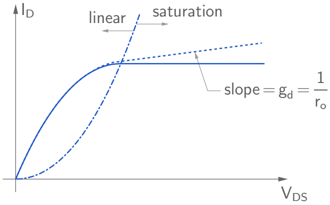
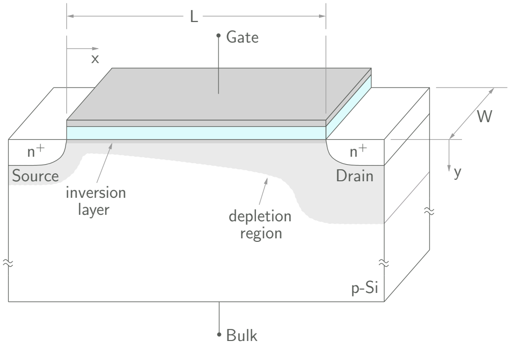
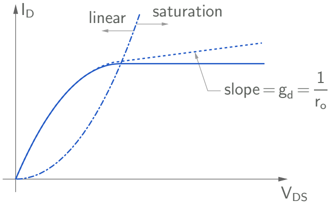




* In the saturation region, the Channel Length Modulation (CLM) effect gives rise to a non-zero slope in the I_D–V_{DS} characteristics of a MOSFET.

Channel length modulation





* In the saturation region, the Channel Length Modulation (CLM) effect gives rise to a non-zero slope in the I_D–V_{DS} characteristics of a MOSFET.
* The length of the high-field region ΔL makes the effective length of the transistor $L - \Delta L$, and since $I_D \sim 1/L$, the current increases with increasing ΔL, i.e., increasing V_D.

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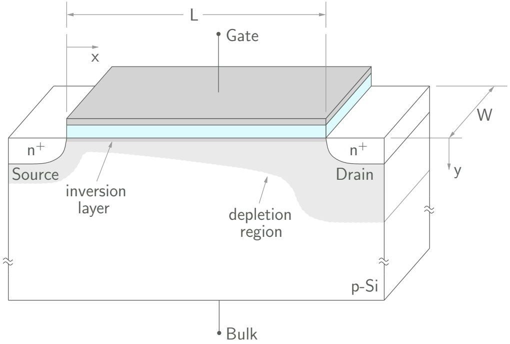

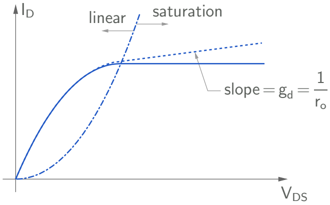

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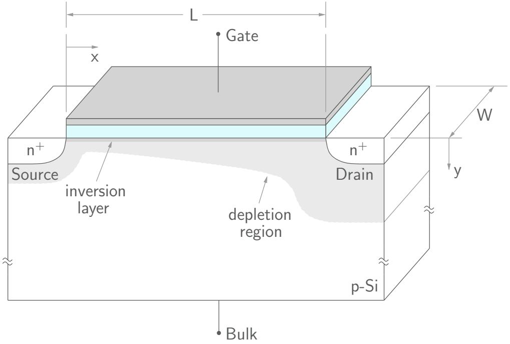

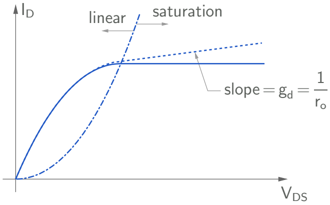

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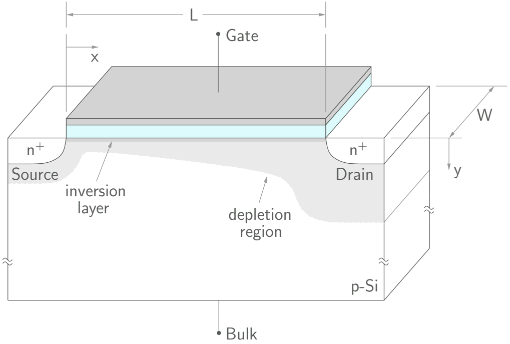

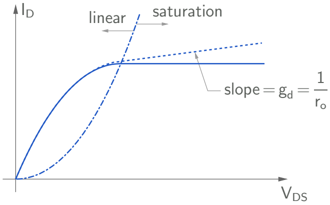

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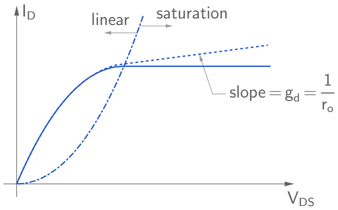
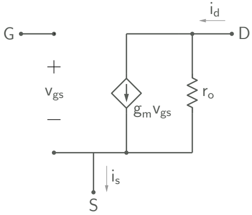
* The drain saturation current equation, modified to account for CLM, is given by
$$I_D^{sat} = \frac{1}{2}\,\frac{W}{L}\,\mu_n\,C_{ox}\,(V_{GS} - V_{th})^2\,(1 + \lambda V_{DS}).$$





In amplifier applications, a MOS transistor is biased in the saturation region. The drain current is given by

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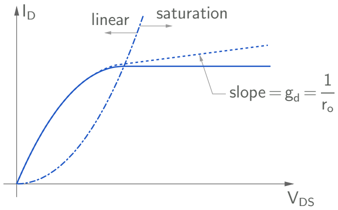

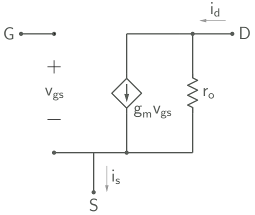

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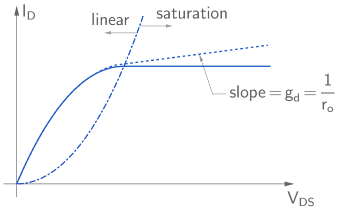
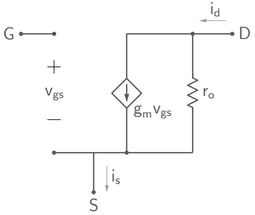
The parameters g_m (the transconductance) and r_o (the output resistance) are given by

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{\text{saturation}} = \frac{W}{L}\,\mu_n\,C_{ox}\,(V_{GS} - V_{th}), \quad (\text{assuming } \lambda V_{DS} \ll 1),$$





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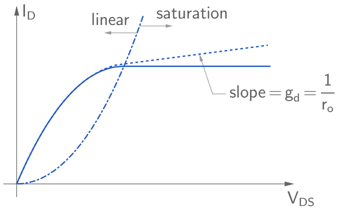
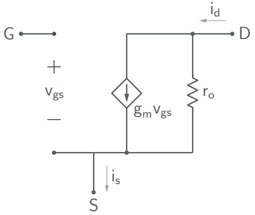
Small-signal model





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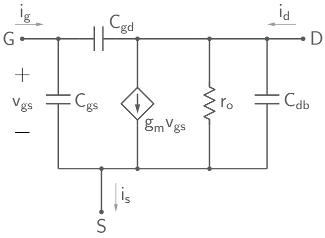
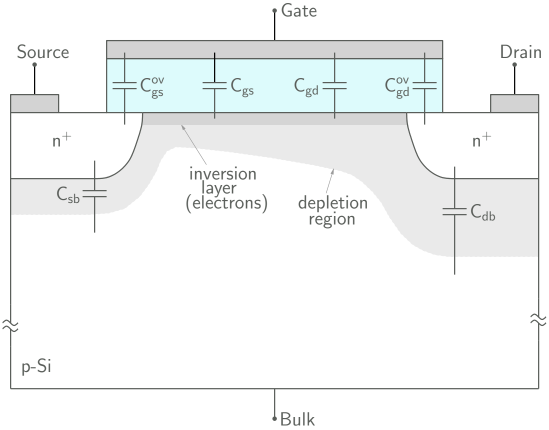
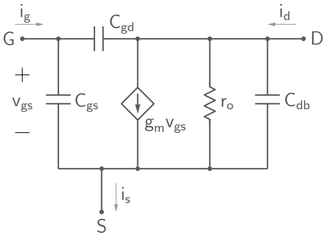
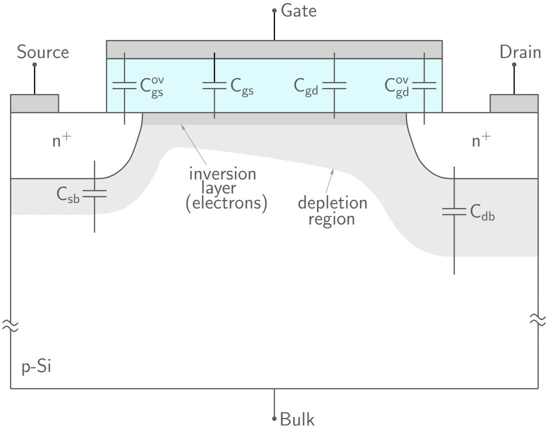




At high frequencies, the internal device capacitances must be included in the small-signal model.





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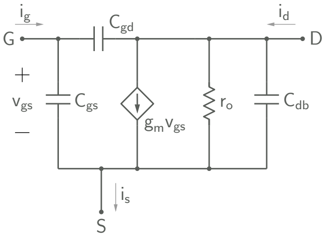
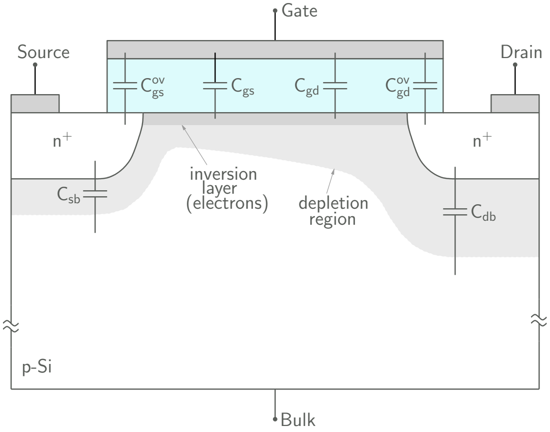
* The gate-to-channel capacitance is the largest capacitance, and it arises from the fact that the inversion charge Q_I varies with V_G.





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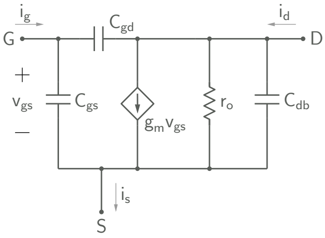
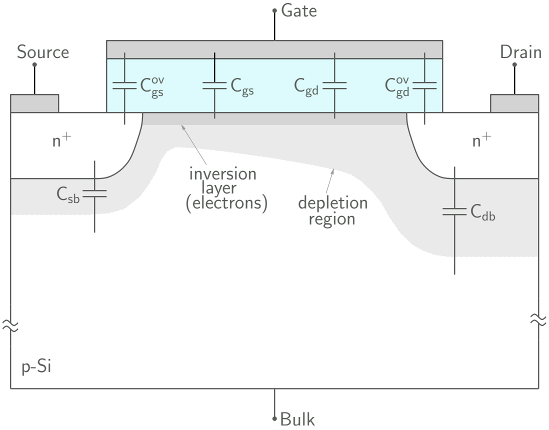
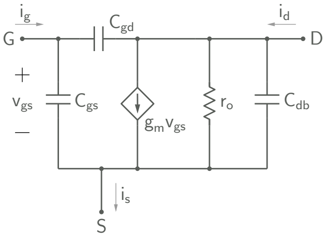
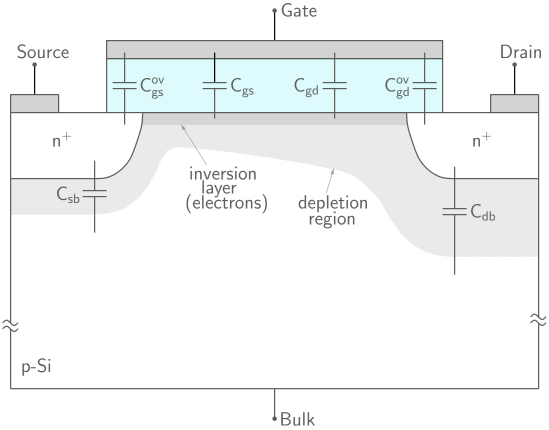
* The gate-to-channel capacitance is the largest capacitance, and it arises from the fact that the inversion charge Q_I varies with V_G.
* In saturation, $C_{gs} = \frac{2}{3} WLC_{ox}$, $C_{gd} = 0$ for an idealised transistor structure with no overlap between the gate electrode and the source or drain regions.

Small-signal model









* In a practical transistor, because of technological constraints, the gate electrode does overlap somewhat with the source and drain regions, leading to (small) overlap capacitances C_{gs}^{ov} and C_{gd}^{ov}, which must be added to C_{gs} and C_{gd}.

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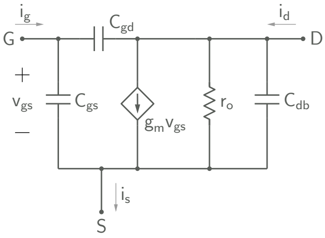

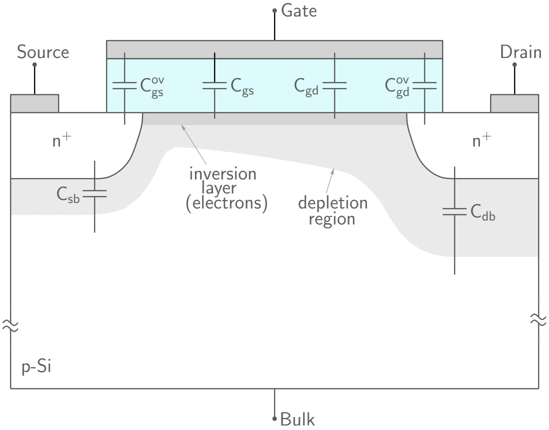

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* The capacitances C_{sb} and C_{db} represent the junction capacitance of the S-B and D-B junctions, respectively. The S and B terminals are typically connected together, so C_{sb} is bypassed.